

36V, Low Noise Zero-Drift Operational Amplifier

FEATURES

- **Supply Voltage Range: 4.75V to 36V**
- **Offset Voltage: 5 μ V (Maximum)**
- **Offset Voltage Drift: 0.025 μ V/ $^{\circ}$ C (Maximum, -40° C to 125° C)**
- **Input Noise Voltage**
 - **200nV_{P-P}, DC to 10Hz (Typ)**
 - **9nV/ $\sqrt{\text{Hz}}$, 1kHz (Typ)**
- **Input Common Mode Range: $V^- - 0.1\text{V}$ to $V^+ - 1.5\text{V}$**
- **Rail-to-Rail Output**
- **Unity Gain Stable**
- **Gain Bandwidth Product: 2.5MHz (Typ)**
- **Slew Rate: 1.6V/ μ s (Typ)**
- **A_{VOL} : 150dB (Typ)**
- **PSRR: 150dB (Typ)**
- **CMRR: 150dB (Typ)**
- **Shutdown Mode**

APPLICATIONS

- High Resolution Data Acquisition
- Reference Buffering
- Test and Measurement
- Electronic Scales
- Thermocouple Amplifiers
- Strain Gauges
- Low Side Current Sense
- Automotive Monitors and Control

DESCRIPTION

The **LTC[®]2058** is a dual, low noise, zero-drift operational amplifier that offers precision DC performance over a wide supply range of 4.75V to 36V. Offset voltage and 1/f noise are suppressed, allowing this amplifier to achieve a maximum offset voltage of 5 μ V and a DC to 10Hz input noise voltage of 200nV_{P-P} (Typ). The LTC2058's self-calibrating circuitry results in low offset voltage drift with temperature, 0.025 μ V/ $^{\circ}$ C (Max), and practically zero drift over time. The amplifier also features an excellent power supply rejection ratio (PSRR) of 150dB and a common mode rejection ratio (CMRR) of 150dB (Typ).

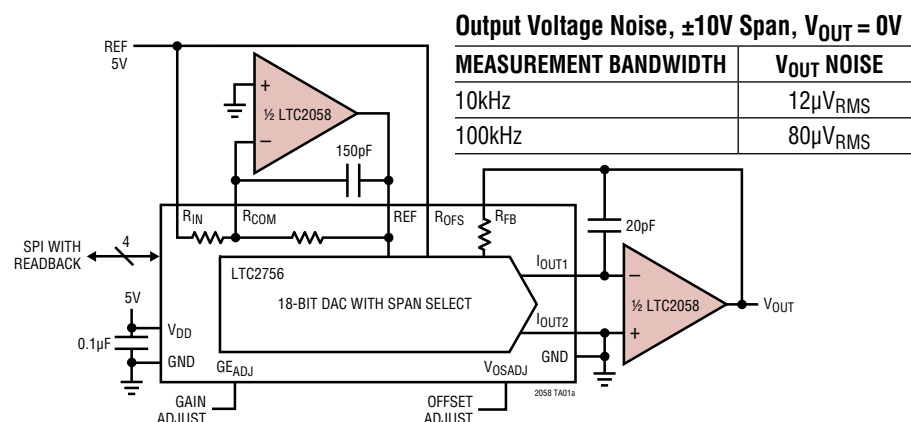
The LTC2058 provides rail-to-rail output swing and an input common mode range that includes the V^- rail. In addition to low offset and noise, this amplifier features a 2.5MHz (Typ) gain-bandwidth product and a 1.6V/ μ s (Typ) slew rate.

Wide supply range, combined with low noise, low offset, and excellent PSRR and CMRR make the LTC2058 well suited for high dynamic-range test, measurement, and instrumentation systems.

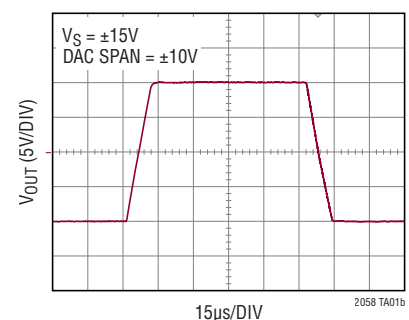
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TYPICAL APPLICATION

18-Bit Voltage Output DAC with Software-Selectable Ranges



20V Step Response of DAC I to V



LTC2058

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage

(V^+ to V^-)40V

Input Voltage

$-IN$, $+IN$ $V^- - 0.3V$ to $V^+ + 0.3V$

$\overline{SD}$, $SDCOM$ $V^- - 0.3V$ to $V^+ + 0.3V$

Input Current

$-IN$, $+IN$ $\pm 10mA$

$\overline{SD}$, $SDCOM$ $\pm 10mA$

Differential Input Voltage

$+IN$ to $-IN$ $\pm 6V$

$\overline{SD} - SDCOM$ $-0.3V$ to $5.3V$

Output Short-Circuit Duration Indefinite

Operating Temperature Range (Note 2)

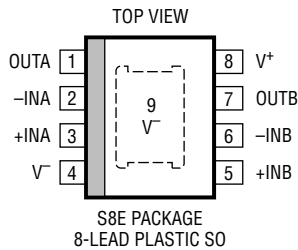
LTC2058I $-40^\circ C$ to $85^\circ C$

LTC2058H $-40^\circ C$ to $125^\circ C$

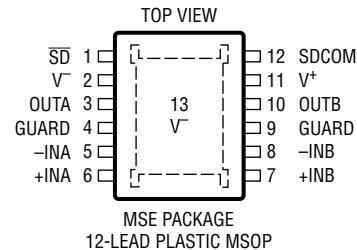
Storage Temperature Range $-65^\circ C$ to $150^\circ C$

Lead Temperature (Soldering, 10 sec) $300^\circ C$

PIN CONFIGURATION



$T_{JMAX} = 150^\circ C$, $\theta_{JC} = 5^\circ C/W$, $\theta_{JA} = 33^\circ C/W$
EXPOSED PAD (PIN 9) IS V^- , MUST BE SOLDERED TO PCB



$T_{JMAX} = 150^\circ C$, $\theta_{JC} = 10^\circ C/W$, $\theta_{JA} = 40^\circ C/W$
EXPOSED PAD (PIN 13) IS V^- , MUST BE SOLDERED TO PCB

ORDER INFORMATION

TUBES	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC2058IMSE#PBF	LTC2058IMSE#TRPBF	2058	12-Lead Plastic MSOP	$-40^\circ C$ to $85^\circ C$
LTC2058HMSE#PBF	LTC2058HMSE#TRPBF	2058	12-Lead Plastic MSOP	$-40^\circ C$ to $125^\circ C$
LTC2058IS8E#PBF	LTC2058IS8E#TRPBF	2058	8-Lead Plastic Small Outline	$-40^\circ C$ to $85^\circ C$
LTC2058HS8E#PBF	LTC2058HS8E#TRPBF	2058	8-Lead Plastic Small Outline	$-40^\circ C$ to $125^\circ C$

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Parts ending with PBF are ROHS and WEEE compliant.

For more information on tape and reel specifications, go to: [Tape and reel specifications](#) Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Unless otherwise noted, $V_S = \pm 2.5\text{V}$; $V_{CM} = V_{OUT} = 0\text{V}$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 3)			0.5	5	μV
$\frac{\Delta V_{OS}}{\Delta T}$	Average Input Offset Voltage Drift (Note 3)	-40°C to 125°C	●		0.025	$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current (Notes 4, 5)	-40°C to 85°C -40°C to 125°C	● ●	30	100 200 4.5	pA pA nA
I_{OS}	Input Offset Current (Notes 4, 5)	-40°C to 85°C -40°C to 125°C	● ●	60	200 200 300	pA pA pA
i_n	Input Noise Current Spectral Density (Note 8)	1kHz, $C_{EXT} = 0\text{pF}$		0.5		$\text{pA}/\sqrt{\text{Hz}}$
e_n	Input Noise Voltage Spectral Density	1kHz		9		$\text{nV}/\sqrt{\text{Hz}}$
$e_{n\text{P-P}}$	Input Noise Voltage	DC to 10Hz		200		$\text{nV}_{\text{P-P}}$
Z_{IN}	Differential Input Impedance Common Mode Input Impedance			225k 8 10 ¹² 20		ΩpF ΩpF
CMRR	Common Mode Rejection Ratio (Note 6)	$V_{CM} = V^- - 0.1\text{V}$ to $V^+ - 1.5\text{V}$ -40°C to 85°C -40°C to 125°C	● ●	123 121 118	150	dB dB dB
PSRR	Power Supply Rejection Ratio (Note 6)	$V_S = 4.75\text{V}$ to 36V -40°C to 125°C	●	140 140	150	dB dB
A_{VOL}	Open Loop Voltage Gain (Note 6)	$V_{OUT} = V^- + 0.5\text{V}$ to $V^+ - 0.3\text{V}$, $R_L = 1\text{k}\Omega$ -40°C to 125°C	●	124 120	150	dB dB
$V_{OL} - V^-$	Output Voltage Swing Low	No Load -40°C to 125°C $I_{SINK} = 1\text{mA}$ -40°C to 125°C $I_{SINK} = 5\text{mA}$ -40°C to 85°C -40°C to 125°C	● ● ● ● ●	5 55 260	15 20 150 200 470 750 750	mV mV mV mV mV mV mV
$V^+ - V_{OH}$	Output Voltage Swing High	No Load -40°C to 125°C $I_{SOURCE} = 1\text{mA}$ -40°C to 125°C $I_{SOURCE} = 5\text{mA}$ -40°C to 85°C -40°C to 125°C	● ● ● ● ●	5.5 50 235	16 20 75 95 315 365 400	mV mV mV mV mV mV mV
I_{SC}	Short-Circuit Current	Sourcing/Sinking		20/19	31/30	mA
SR_{RISE}	Rising Slew Rate	$A_V = -1$, $R_L = 10\text{k}\Omega$		1.6		$\text{V}/\mu\text{s}$
SR_{FALL}	Falling Slew Rate	$A_V = -1$, $R_L = 10\text{k}\Omega$		1.7		$\text{V}/\mu\text{s}$
GBW	Gain Bandwidth Product			2.5		MHz
f_C	Internal Chopping Frequency			100		kHz
I_S	Supply Current Per Amplifier	No Load -40°C to 85°C -40°C to 125°C In Shutdown Mode -40°C to 85°C -40°C to 125°C	● ● ● ● ●	0.95 3	1.15 1.4 1.55 4.25 5	mA mA mA μA μA μA
V_{SDL}	Shutdown Threshold ($\overline{SD}$ – SDCOM) Low (Note 7)	-40°C to 125°C	●		0.8	V
V_{SDH}	Shutdown Threshold ($\overline{SD}$ – SDCOM) High (Note 7)	-40°C to 125°C	●	2		V
	SDCOM Voltage Range (Note 7)	-40°C to 125°C	●	V^-	$V^+ - 2\text{V}$	V
$I_{\overline{SD}}$	$\overline{SD}$ Pin Current (Note 7)	-40°C to 125°C , $V_{\overline{SD}} - V_{SDCOM} = 0$	●	-1	-0.5	μA
I_{SDCOM}	SDCOM Pin Current (Note 7)	-40°C to 125°C , $V_{\overline{SD}} - V_{SDCOM} = 0$	●	0.75	1.5	μA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Unless otherwise noted, $V_S = \pm 15\text{V}$; $V_{CM} = V_{OUT} = 0\text{V}$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 3)			0.5	5	μV
$\frac{\Delta V_{OS}}{\Delta T}$	Average Input Offset Voltage Drift (Note 3)	-40°C to 125°C	●		0.025	$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current (Note 4, 5)	-40°C to 85°C -40°C to 125°C	● ●	30	100 200 4.5	pA pA nA
I_{OS}	Input Offset Current (Note 4, 5)	-40°C to 85°C -40°C to 125°C	● ●	60	200 200 300	pA pA pA
i_n	Input Noise Current Spectral Density (Note 8)	1kHz, $C_{EXT} = 0\text{pF}$ 1kHz, $C_{EXT} = 22\text{pF}$		1 0.5		$\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$
e_n	Input Noise Voltage Spectral Density	1kHz		9		$\text{nV}/\sqrt{\text{Hz}}$
$e_{n\text{P-P}}$	Input Noise Voltage	DC to 10Hz		200		$\text{nV}_{\text{P-P}}$
Z_{IN}	Differential Input Impedance Common Mode Input Impedance			$225\text{k}\Omega$ 13 $10^{12}\Omega$ 6		Ω pF Ω pF
CMRR	Common Mode Rejection Ratio (Note 6)	$V_{CM} = V^- - 0.1\text{V}$ to $V^+ - 1.5\text{V}$ -40°C to 85°C -40°C to 125°C	● ●	138 137 135	150	dB dB dB
PSRR	Power Supply Rejection Ratio (Note 6)	$V_S = 4.75\text{V}$ to 36V -40°C to 125°C	●	140 140	150	dB dB
A_{VOL}	Open Loop Voltage Gain (Note 6)	$V_{OUT} = V^- + 0.4\text{V}$ to $V^+ - 0.25\text{V}$, $R_L = 10\text{k}\Omega$ -40°C to 125°C	●	137 133	150	dB dB
$V_{OL} - V^-$	Output Voltage Swing Low	No Load -40°C to 125°C $I_{SINK} = 1\text{mA}$ -40°C to 125°C $I_{SINK} = 5\text{mA}$ -40°C to 85°C -40°C to 125°C	● ● ● ● ●	5 55 270	15 20 150 200 470 750 750	mV mV mV mV mV mV mV
$V^+ - V_{OH}$	Output Voltage Swing High	No Load -40°C to 125°C $I_{SOURCE} = 1\text{mA}$ -40°C to 125°C $I_{SOURCE} = 5\text{mA}$ -40°C to 85°C -40°C to 125°C	● ● ● ● ●	7 50 235	18 22 75 90 315 365 400	mV mV mV mV mV mV mV
I_{SC}	Short-Circuit Current	Sourcing/Sinking		20/25	31/36	mA
SR_{RISE}	Rising Slew Rate	$A_V = -1$, $R_L = 10\text{k}\Omega$		1.6		$\text{V}/\mu\text{s}$
SR_{FALL}	Falling Slew Rate	$A_V = -1$, $R_L = 10\text{k}\Omega$		1.7		$\text{V}/\mu\text{s}$
GBW	Gain Bandwidth Product			2.5		MHz
f_C	Internal Chopping Frequency			100		kHz
I_S	Supply Current Per Amplifier	No Load -40°C to 85°C -40°C to 125°C In Shutdown Mode -40°C to 85°C -40°C to 125°C	● ● ● ● ●	1 5	1.2 1.45 1.6 7.5 9	mA mA mA μA μA μA
V_{SDL}	Shutdown Threshold ($\overline{\text{SD}}$ – SDCOM) Low (Note 7)	-40°C to 125°C	●		0.8	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Unless otherwise noted, $V_S = \pm 15\text{V}$; $V_{CM} = V_{OUT} = 0\text{V}$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{SDH}	Shutdown Threshold ($\overline{SD}$ – SDCOM) High (Note 7)	-40°C to 125°C ●	2			V
	SDCOM Voltage Range (Note 7)	-40°C to 125°C ●	V^-		$V^+ - 2\text{V}$	V
$I_{\overline{SD}}$	$\overline{SD}$ Pin Current (Note 7)	-40°C to 125°C , $V_{\overline{SD}} - V_{SDCOM} = 0$ ●	-1	-0.5		μA
I_{SDCOM}	SDCOM Pin Current (Note 7)	-40°C to 125°C , $V_{\overline{SD}} - V_{SDCOM} = 0$ ●		0.75	1.5	μA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC2058I is guaranteed to meet specified performance from -40°C to 85°C . The LTC2058H is guaranteed to meet specified performance from -40°C to 125°C .

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurements of these voltage levels during automated testing. V_{OS} is measured to a limit determined by test equipment capability.

Note 4: These specifications are limited by automated test system capability. Leakage currents and thermocouple effects reduce test accuracy. For tighter guaranteed specifications, please contact LTC Marketing.

Note 5: Input BIAS current is measured using an equivalent source impedance of $100\text{M}\Omega \parallel 51\text{pF}$.

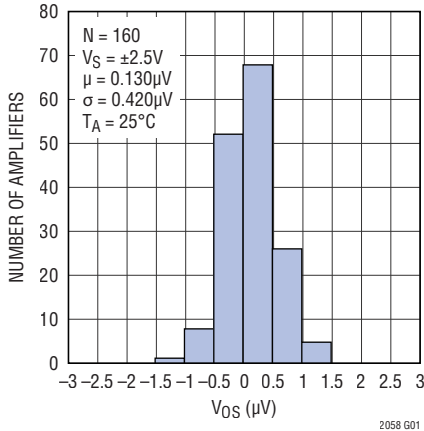
Note 6: Minimum specifications for these parameters are limited by the capabilities of the automated test system, which has an accuracy of approximately $10\mu\text{V}$ for V_{OS} measurements. For reference, $30\text{V}/1\mu\text{V}$ is 150dB of voltage ratio.

Note 7: MSE package only.

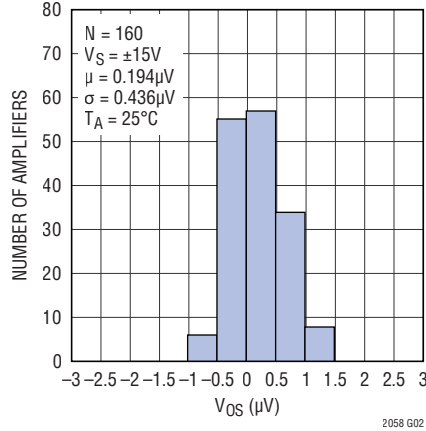
Note 8: Refer to the Application Information section for more details.

TYPICAL PERFORMANCE CHARACTERISTICS

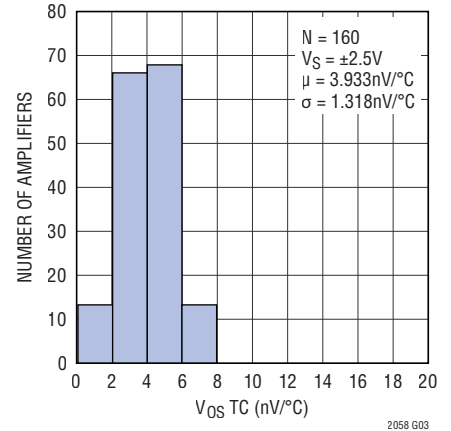
Input Offset Voltage Distribution



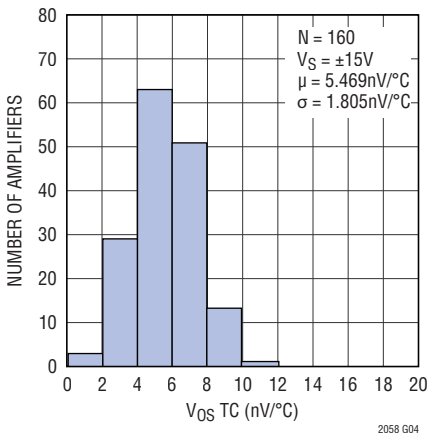
Input Offset Voltage Distribution



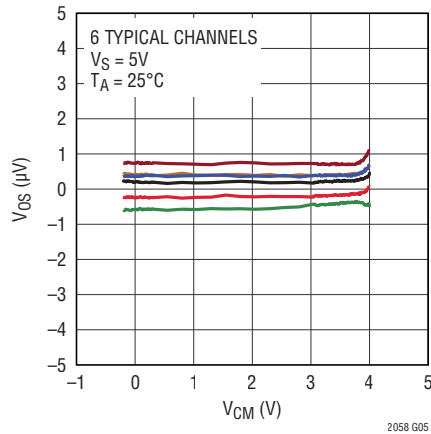
Input Offset Voltage Drift Distribution



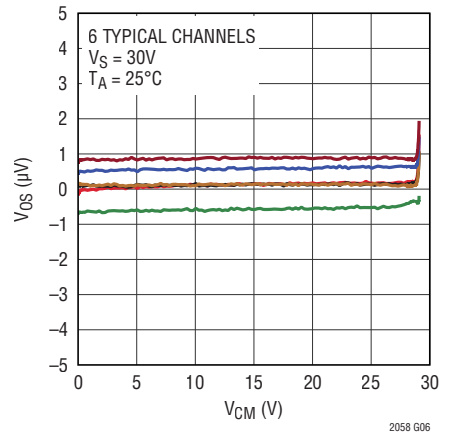
Input Offset Voltage Drift Distribution



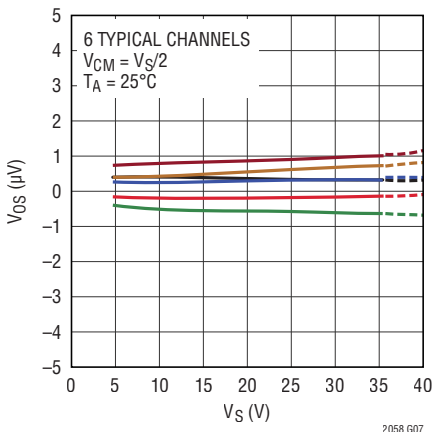
Input Offset Voltage vs Input Common Mode Voltage



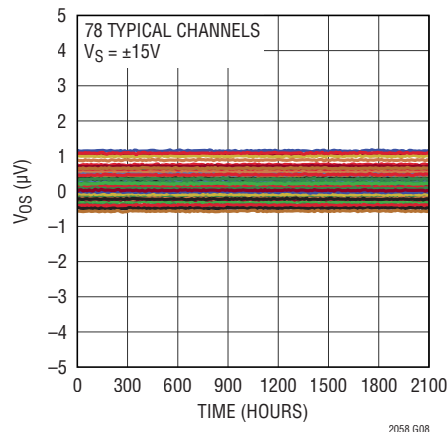
Input Offset Voltage vs Input Common Mode Voltage



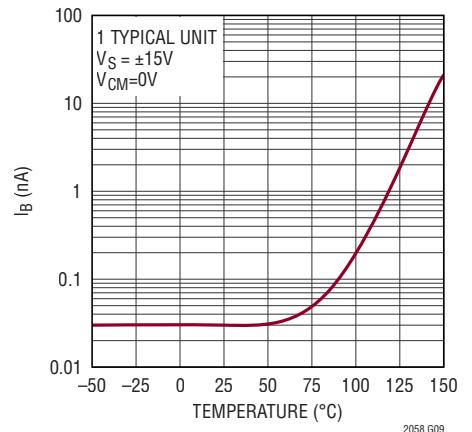
Input Offset Voltage vs Supply Voltage



Long-Term Input Offset Voltage Drift

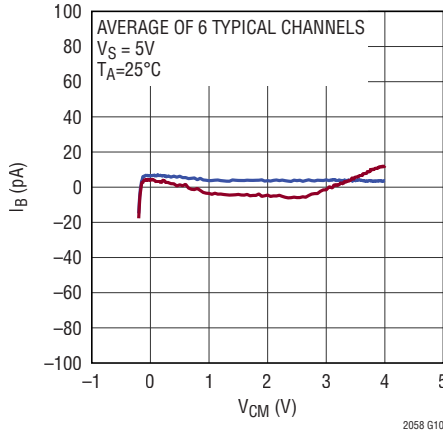


Input Bias Current vs Temperature

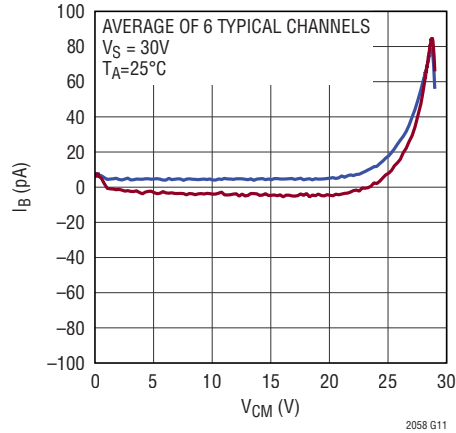


TYPICAL PERFORMANCE CHARACTERISTICS

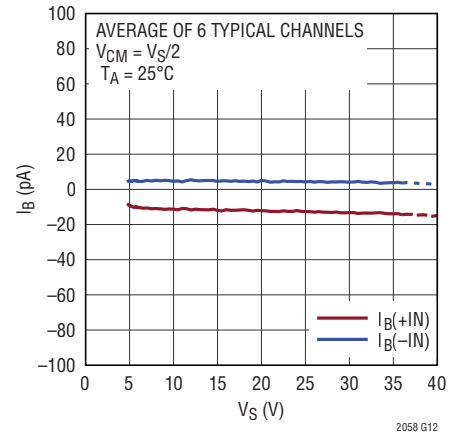
Input Bias Current vs Input Common Mode Voltage



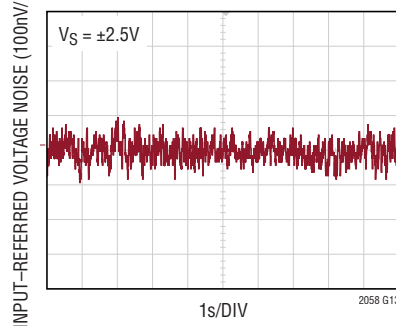
Input Bias Current vs Input Common Mode Voltage



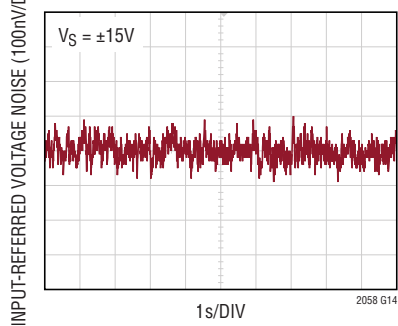
Input Bias Current vs Supply Voltage



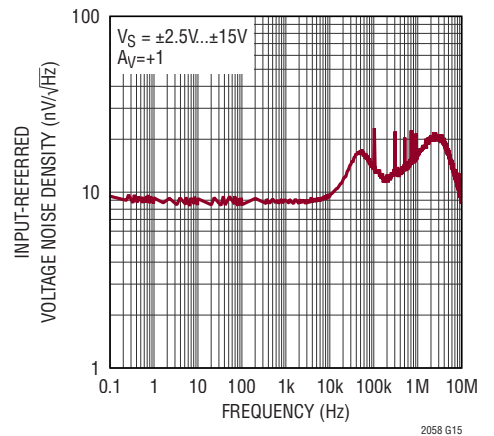
DC to 10Hz Voltage Noise



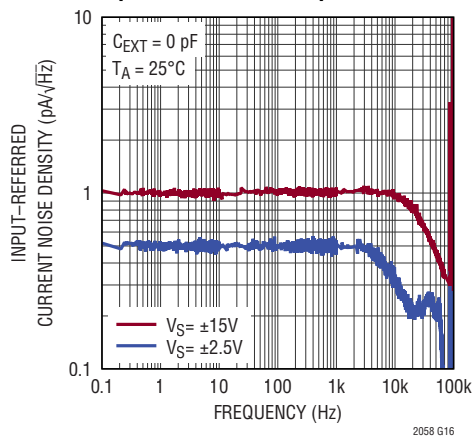
DC to 10Hz Voltage Noise



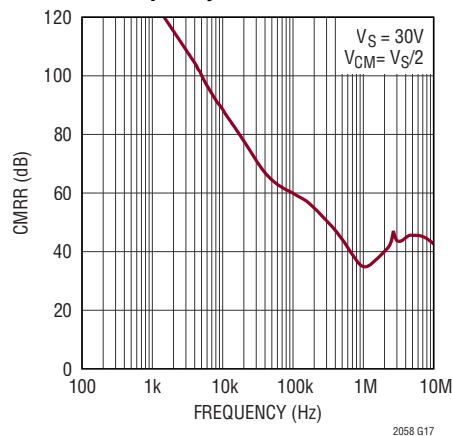
Input Voltage Noise Spectrum



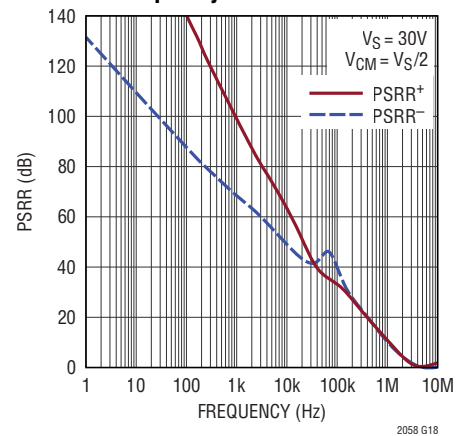
Input Current Noise Spectrum



Common Mode Rejection Ratio vs Frequency

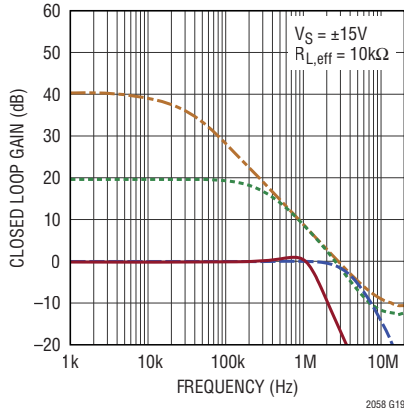


Power Supply Rejection Ratio vs Frequency

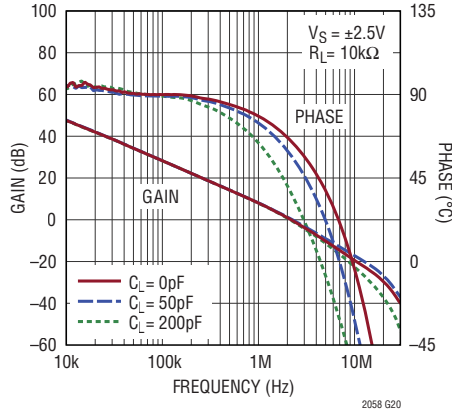


TYPICAL PERFORMANCE CHARACTERISTICS

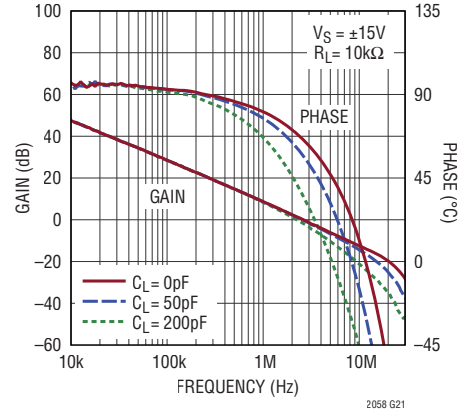
Closed Loop Gain vs Frequency



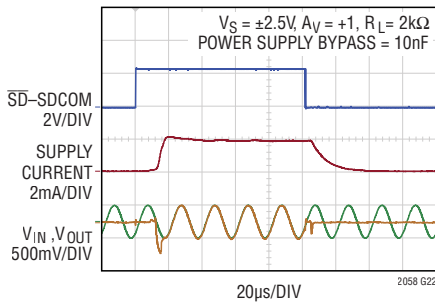
Open Loop Gain vs Frequency



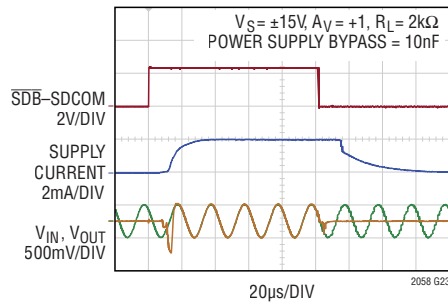
Open Loop Gain vs Frequency



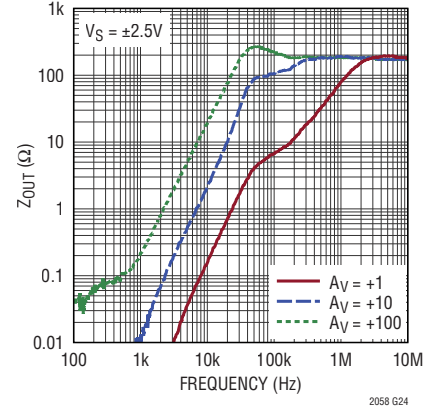
Shutdown Transient with Sinusoid Input



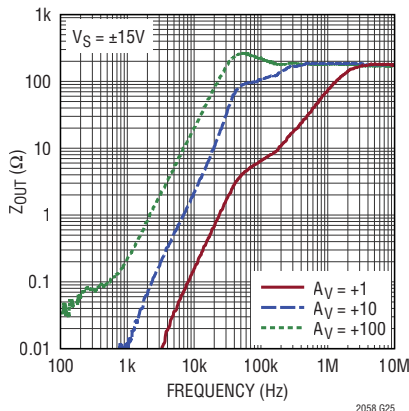
Shutdown Transient with Sinusoid Input



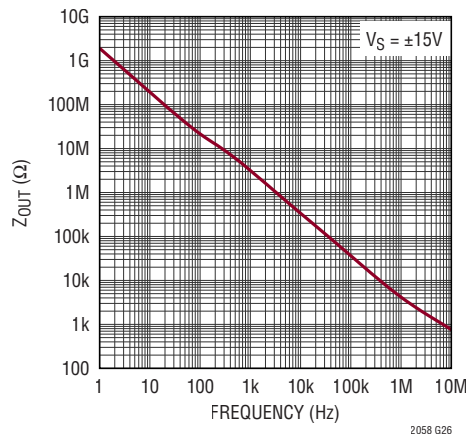
Closed Loop Output Impedance vs Frequency



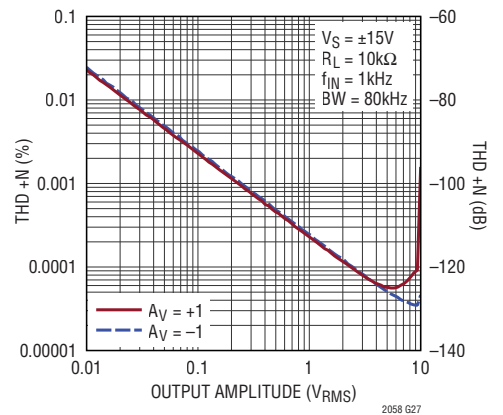
Closed Loop Output Impedance vs Frequency



Output Impedance in Shutdown vs Frequency

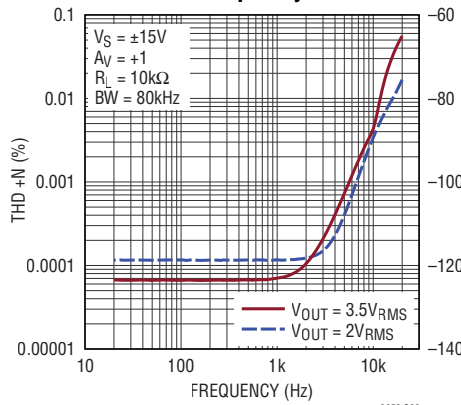


THD +N vs Amplitude



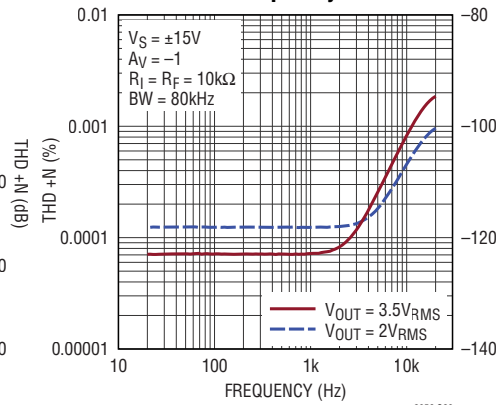
TYPICAL PERFORMANCE CHARACTERISTICS

THD +N vs Frequency



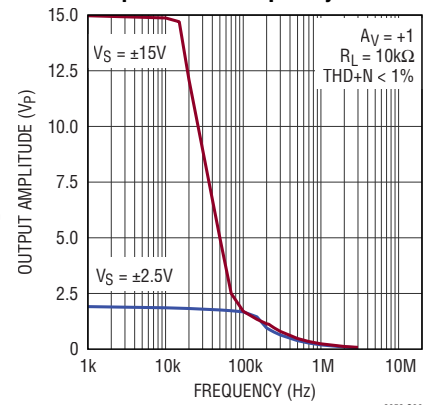
2058 G28

THD +N vs Frequency



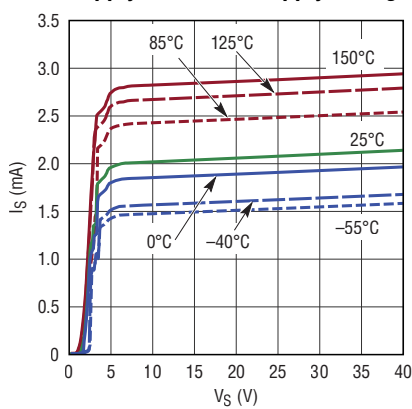
2058 G29

Maximum Undistorted Output Amplitude vs Frequency



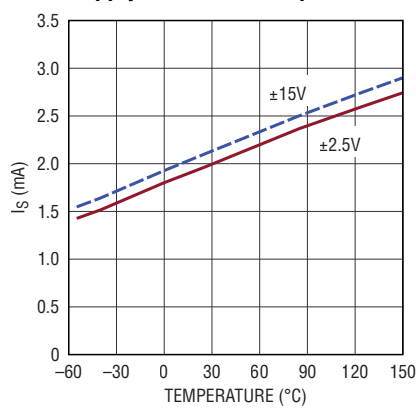
2058 G30

Supply Current vs Supply Voltage



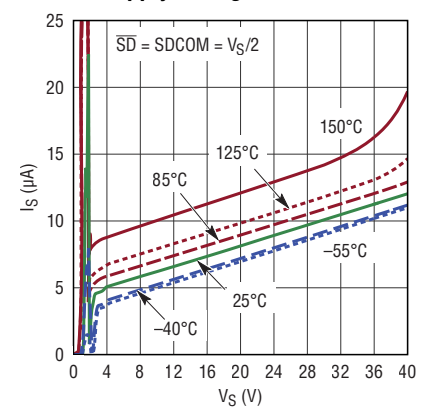
2058 G31

Supply Current vs Temperature



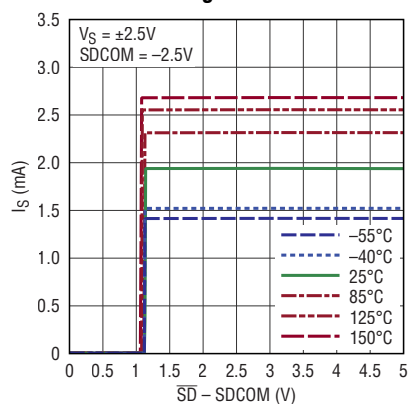
2058 G32

Shutdown Supply Current vs Supply Voltage



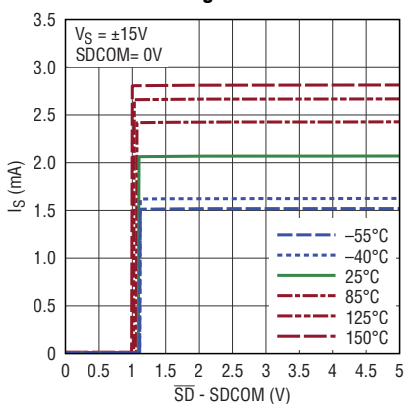
2058 G33

Supply Current vs Shutdown Control Voltage



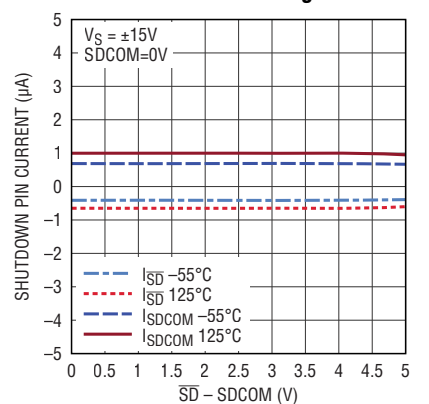
2058 G34

Supply Current vs Shutdown Control Voltage



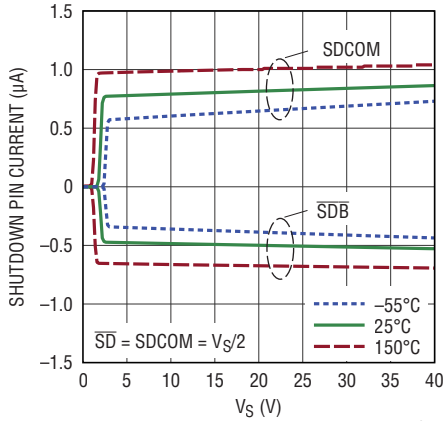
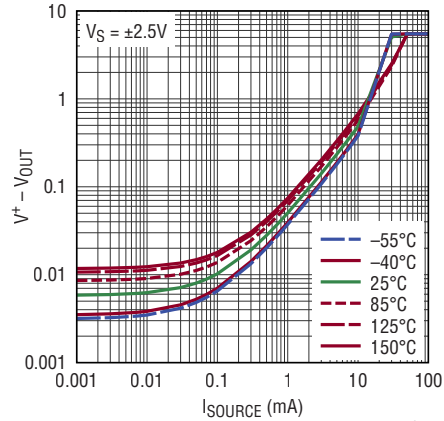
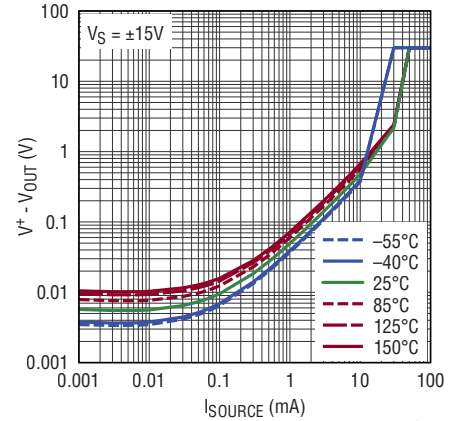
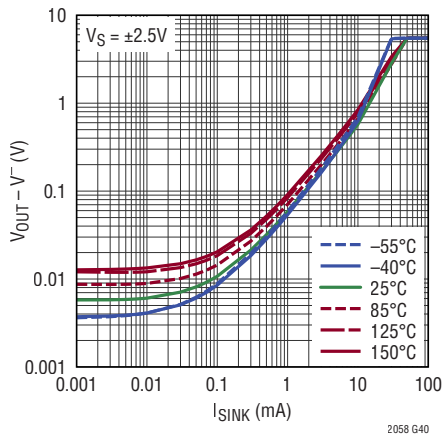
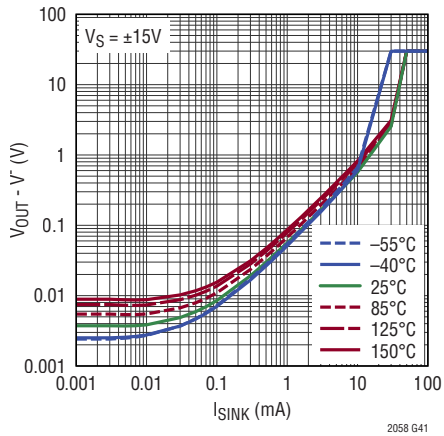
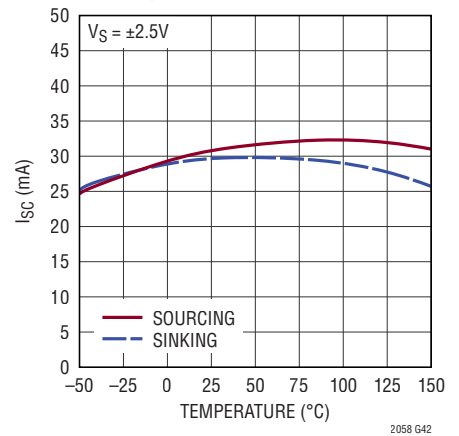
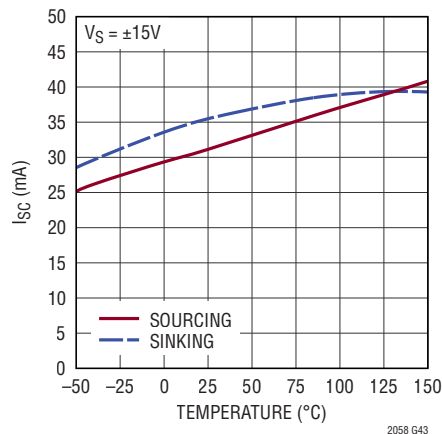
2058 G35

Shutdown Pin Current vs Shutdown Pin Voltage

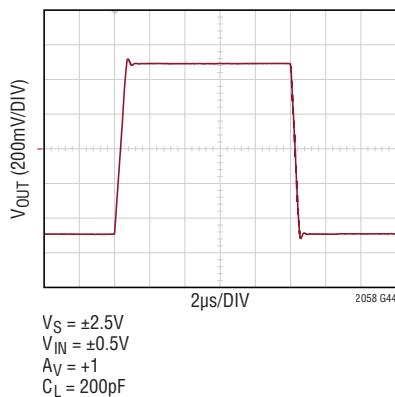


2058 G36

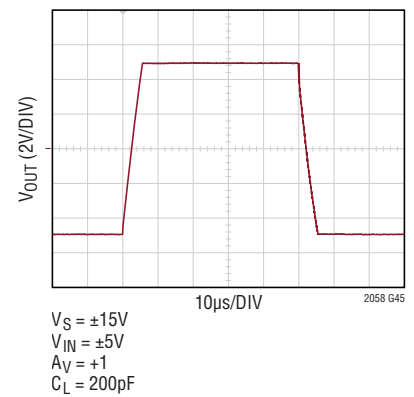
TYPICAL PERFORMANCE CHARACTERISTICS

Shutdown Pin Current
vs Supply VoltageOutput Voltage Swing High
vs Load CurrentOutput Voltage Swing High
vs Load CurrentOutput Voltage Swing Low
vs Load CurrentOutput Voltage Swing Low
vs Load CurrentShort-Circuit Current
vs TemperatureShort-Circuit Current
vs Temperature

Large Signal Response

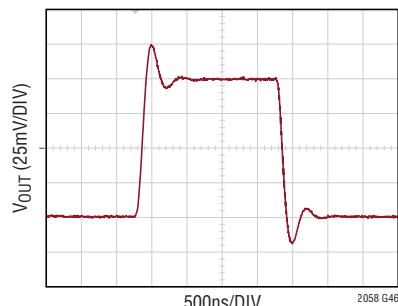


Large Signal Response



TYPICAL PERFORMANCE CHARACTERISTICS

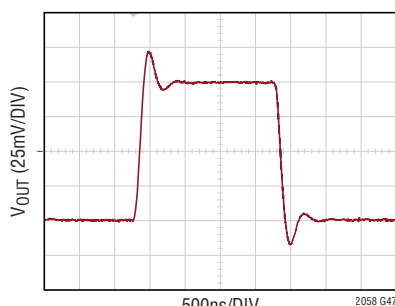
Small Signal Response



$V_S = \pm 2.5V$
 $V_{IN} = \pm 50mV$
 $A_V = +1$
 $C_L = 200pF$

2058 G46

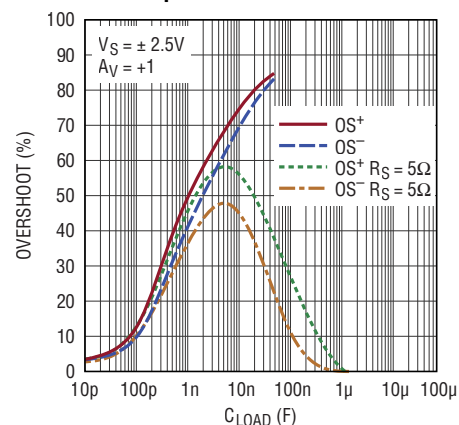
Small Signal Response



$V_S = \pm 15V$
 $V_{IN} = \pm 50mV$
 $A_V = +1$
 $C_L = 200pF$

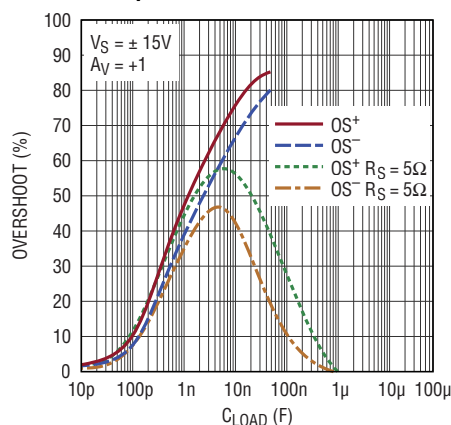
2058 G47

Small Signal Overshoot vs Capacitive Load



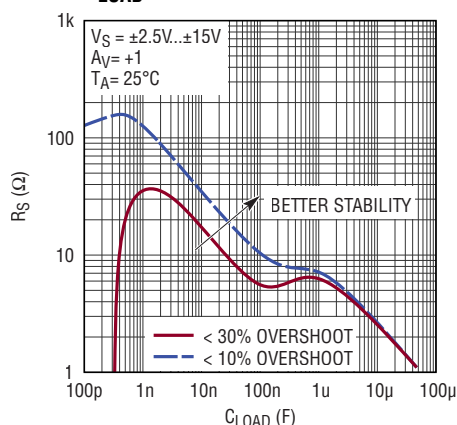
2058 G48

Small Signal Overshoot vs Capacitive Load



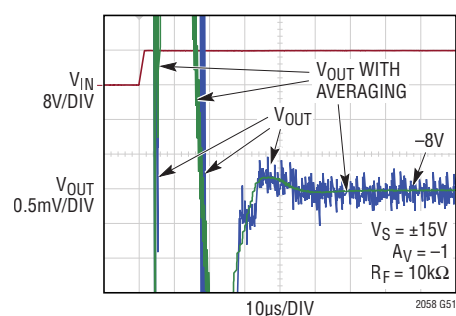
2058 G49

Output Series Resistance vs CLoad and Overshoot



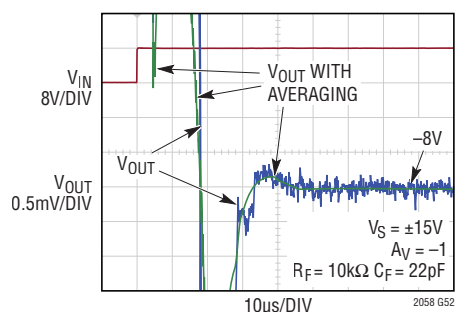
2058 G50

Large Signal Settling Transient



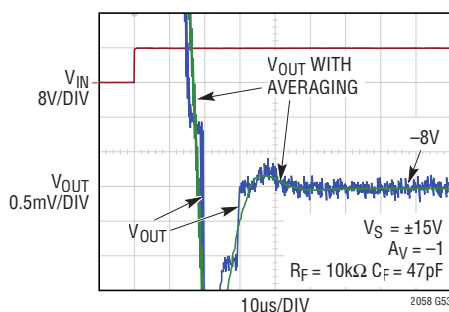
2058 G51

Large Signal Settling Transient



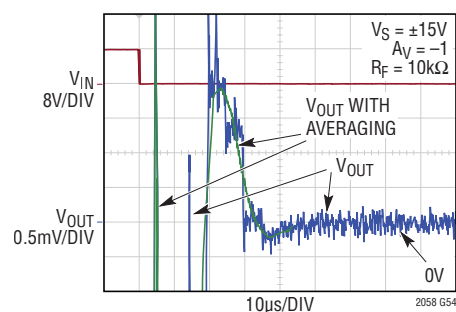
2058 G52

Large Signal Settling Transient



2058 G53

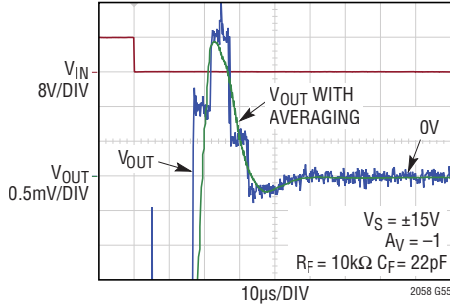
Large Signal Settling Transient



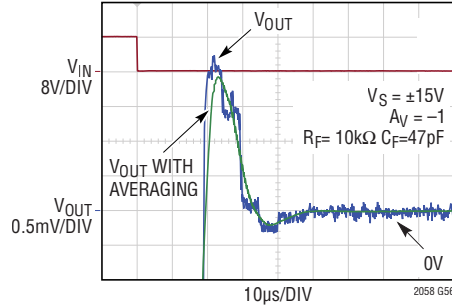
2058 G54

TYPICAL PERFORMANCE CHARACTERISTICS

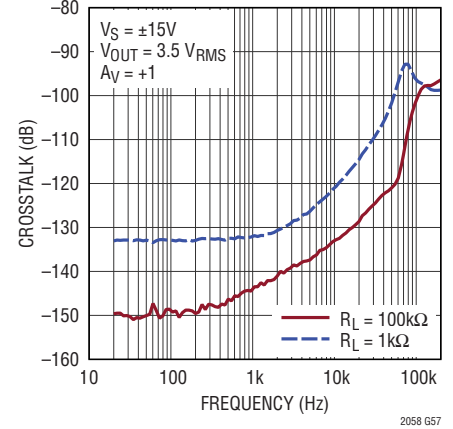
Large Signal Settling Transient



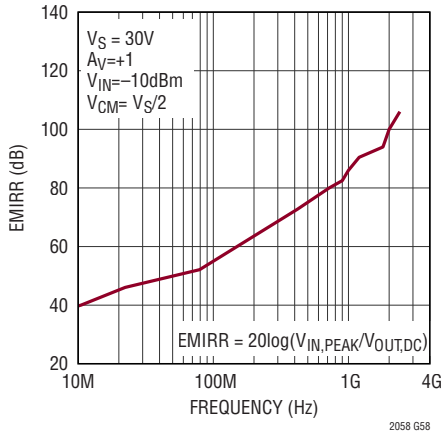
Large Signal Settling Transient



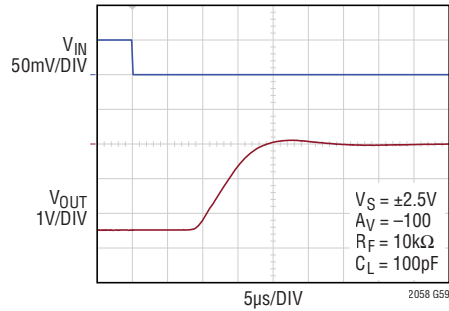
Crosstalk



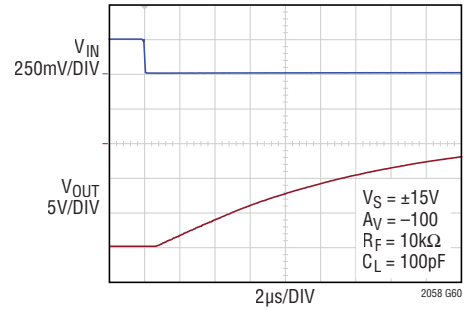
EMIRR IN+ vs Frequency



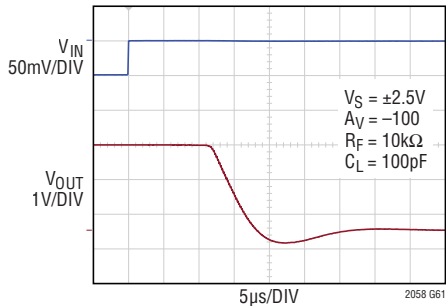
Output Overload Recovery



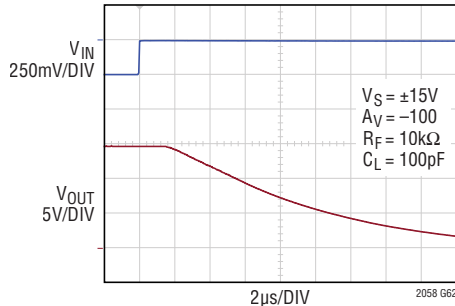
Output Overload Recovery



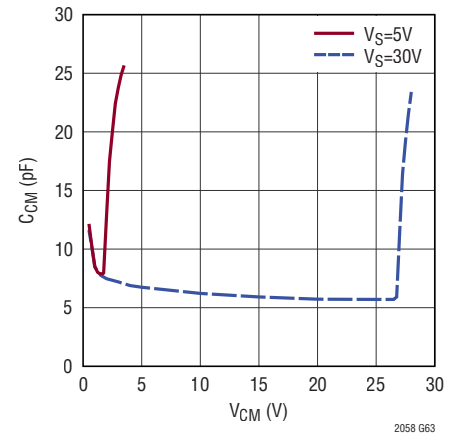
Output Overload Recovery



Output Overload Recovery



Input Common Mode Capacitance vs Input Common Mode Voltage



PIN FUNCTIONS

S8E

OUTA (Pin 1): Amplifier A Output.

–INA (Pin 2): Amplifier A Inverting Input.

+INA (Pin 3): Amplifier A Noninverting Input.

V[–] (Pin 4): Negative Power Supply.

+INB (Pin 5): Amplifier B Noninverting Input.

–INB (Pin 6): Amplifier B Inverting Input.

OUTB (Pin 7): Amplifier B Output.

V⁺ (Pin 8): Positive Power Supply.

Exposed Pad (Pin 9): Must Be Connected to V[–].

MSE12

$\overline{\text{SD}}$ (Pin 1): Shutdown Control Pin.

V[–] (Pin 2): Negative Power Supply.

OUTA (Pin 3): Amplifier A Output.

GUARD (Pin 4): Guard Ring. No internal connection. (See Applications Information)

–INA (Pin 5): Amplifier A Inverting Input.

+INA (Pin 6): Amplifier A Noninverting Input.

+INB (Pin 7): Amplifier B Noninverting Input.

–INB (Pin 8): Amplifier B Inverting Input.

GUARD/NC (Pin 9): Guard Ring. No internal connection. (See Application Information)

OUTB (Pin 10): Amplifier B Output.

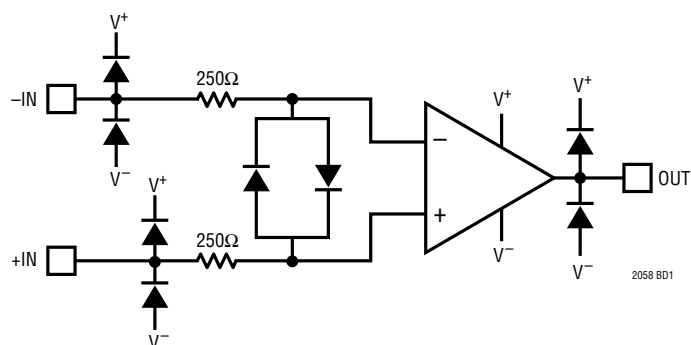
V⁺ (Pin 11): Positive Power Supply.

SDCOM (Pin 12): Reference Voltage for $\overline{\text{SD}}$.

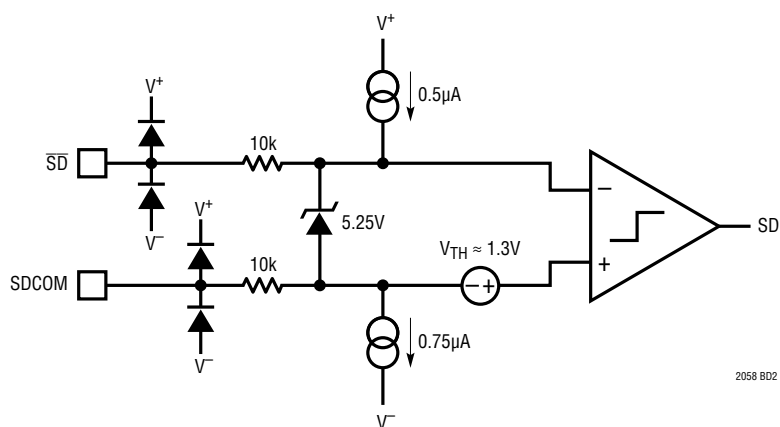
Exposed Pad (Pin 13): Must Be Connected to V[–].

BLOCK DIAGRAMS

Amplifier (Each Channel)



Shutdown Circuit (MSE12 Package Only)



APPLICATIONS INFORMATION

Input Voltage Noise

Chopper stabilized amplifiers like the LTC2058 achieve low offset and $1/f$ noise by heterodyning DC and flicker noise to higher frequencies. In a classical chopper stabilized amplifier, this process results in idle tones at the chopping frequency and its odd harmonics.

The LTC2058 utilizes circuitry to suppress these spurious artifacts to well below the offset voltage. The typical ripple magnitude at 100kHz is much less than $1\mu\text{V}_{\text{RMS}}$.

The voltage noise spectrum of the LTC2058 is shown in Figure 1. If lower noise is required, consider the following circuit from the Typical Applications section: Paralleling Choppers to Improve Noise.

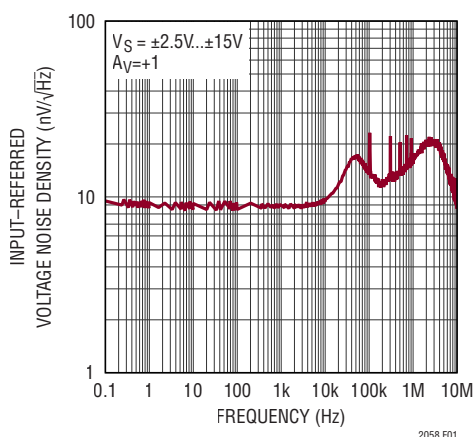


Figure 1. Input Voltage Noise Spectrum

Input Current Noise

For applications with high source impedances, input current noise can be a significant contributor to total output noise. For this reason, it is important to consider noise current interaction with circuit elements placed at the amplifier's inputs.

The current noise spectrum of the LTC2058 is shown in Figure 2. The characteristic curve shows no $1/f$ behavior. As with all zero-drift amplifiers, there is a significant current noise component at the offset-nulling frequency. This phenomenon is discussed in the Input Bias Current section.

It is important to note that the current noise is not equal to $\sqrt{2qI_B} \text{ A}/\sqrt{\text{Hz}}$. This formula is relevant for base current in bipolar transistors and diode currents; but for most

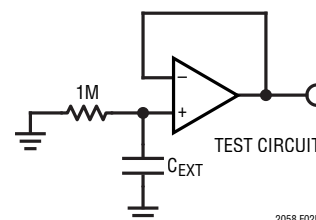
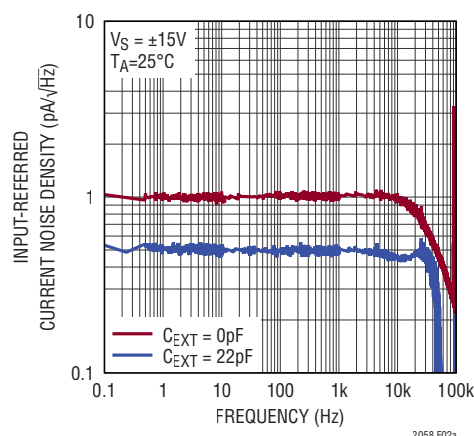


Figure 2. Input Current Noise Spectrum

chopper and auto-zero amplifiers with switched inputs, the dominant current noise mechanism is not shot noise.

Input Bias Current

The LTC2058's input bias currents are comprised of two very different constituents, diode leakage and charge injection. Leakage currents increase with temperature, while the charge injection from the switching inputs remains relatively constant with temperature. The composite of these two currents over temperature is illustrated in Figure 3.

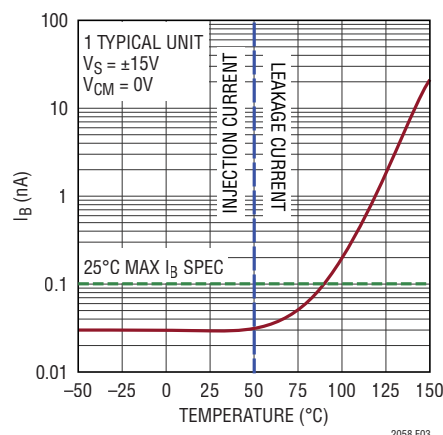


Figure 3. Input Bias Current vs Temperature

APPLICATIONS INFORMATION

How the various input bias currents behave and contribute to error depends on the nature of the source impedance. For the input bias currents specified in the electrical tables, the source impedances are high value resistors bypassed with shunt filter capacitance. Figure 4 shows the effective DC error as an input referred current error (output DC voltage error divided by gain and then by the source resistance) as a function of the filter capacitance. Note that the effective DC error decreases as the capacitance increases. The added external capacitance (C_{EXT}) also reduces the input current noise as shown in Figure 2.

Another function of the input capacitance is to reduce the effects of charge injection. The charge injection based current has a frequency component at the chopping frequency and its harmonics. In time domain these frequency components appear as current pulses (appearing at regular intervals related to the chopping frequency). When these small current pulses interact with source impedances or gain setting resistors, the resulting voltage spikes are amplified by the closed loop gain. For higher source impedances, this may cause the 100kHz chopping frequency to be visible in the output spectrum, which is a phenomenon known as clock feedthrough. To prevent excessive clock

feedthrough, keep gain-setting resistors and source impedances as low as possible. When DC highly resistive source impedance is required, the capacitor across the source impedance reduces the AC impedance, reducing the amplitude of the input voltage spikes. Another way to reduce clock injection effects is to bandwidth limit after the op amp output.

Injection currents from the two inputs are of equal magnitude but opposite direction. Therefore, input bias current effects on offset voltage due to injection currents will not be canceled by placing matched impedances at both inputs.

Above 50°C, leakage of the ESD protection diodes begins to dominate the input bias current and continues to increase exponentially at elevated temperatures. Unlike injection current, leakage currents are in the same direction for both inputs. Therefore, the output error due to leakage currents can be mitigated by matching the source impedances seen by the two inputs. Keep in mind that if the source-impedance-matching technique is employed to cancel the effect of the leakage currents, below 50°C there is an offset voltage error of $2I_B \times R$ due to the charge-injection currents. If $I_B = 100\text{pA}$ and $R = 10\text{k}$, the error is $2\mu\text{V}$.

Thermocouple Effects

In order to achieve accuracy on the microvolt level, thermocouple effects must be considered. Any connection of dissimilar metals forms a thermoelectric junction and generates a small temperature-dependent voltage. Also known as the Seebeck Effect, these thermal EMFs can be the dominant error source in low drift circuits.

Connectors, switches, relay contacts, sockets, resistors, and solder are all candidates for significant thermal EMF generation. Even junctions of copper wire from different manufacturers can generate thermal EMFs of $200\text{nV}/^\circ\text{C}$, which is 8 times the maximum drift specification of the LTC2058. Figure 5 and Figure 6 illustrate the potential magnitude of these voltages and their sensitivity to temperature.

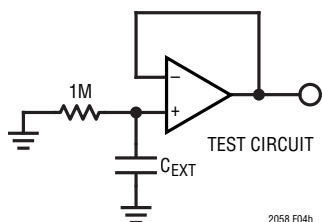
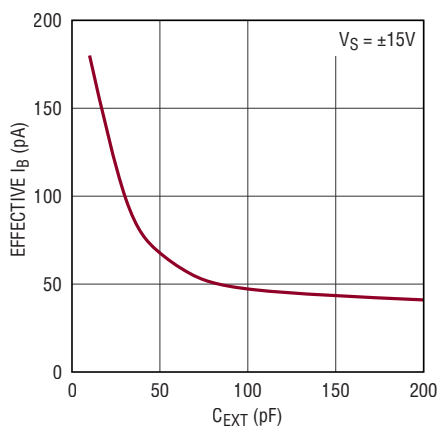


Figure 4. Input Bias Current vs Input Capacitance

APPLICATIONS INFORMATION

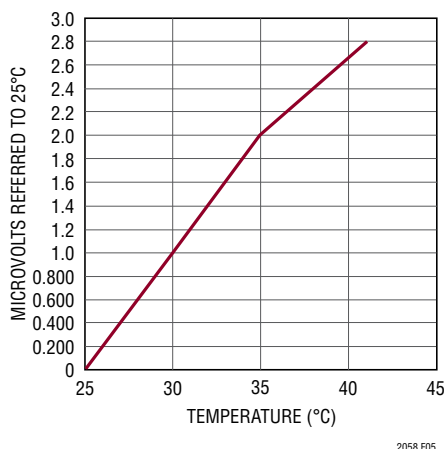


Figure 5. Thermal EMF Generated by Two Copper Wires from Different Manufacturers

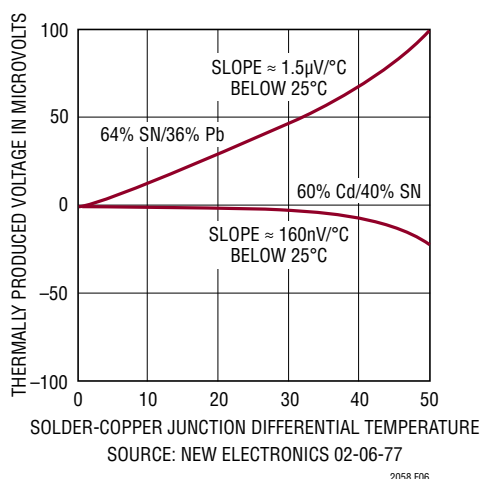


Figure 6. Solder-Copper Thermal EMFs

In order to minimize thermocouple-induced errors, attention must be given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input signal path and avoid connectors, sockets, switches, and relays whenever possible. If such components are required, they should be selected for low thermal EMF characteristics. Furthermore, the number, type, and layout of junctions should be matched for both inputs with respect to thermal gradients on the circuit board. Doing so may involve deliberately introducing dummy junctions to offset unavoidable junctions.

Air currents can also lead to thermal gradients and cause significant noise in measurement systems. It is important to prevent airflow across sensitive circuits. Doing so will often reduce thermocouple noise substantially.

A summary of techniques can be found in Figure 7.

Leakage Effects

Leakage currents into high impedance signal nodes can easily degrade measurement accuracy of sub-nanoamp signals. High voltage and high temperature applications are especially susceptible to these issues. Quality insulation materials should be used, and insulating surfaces should be cleaned to remove fluxes and other residues. For humid environments, surface coating may be necessary to provide a moisture barrier.

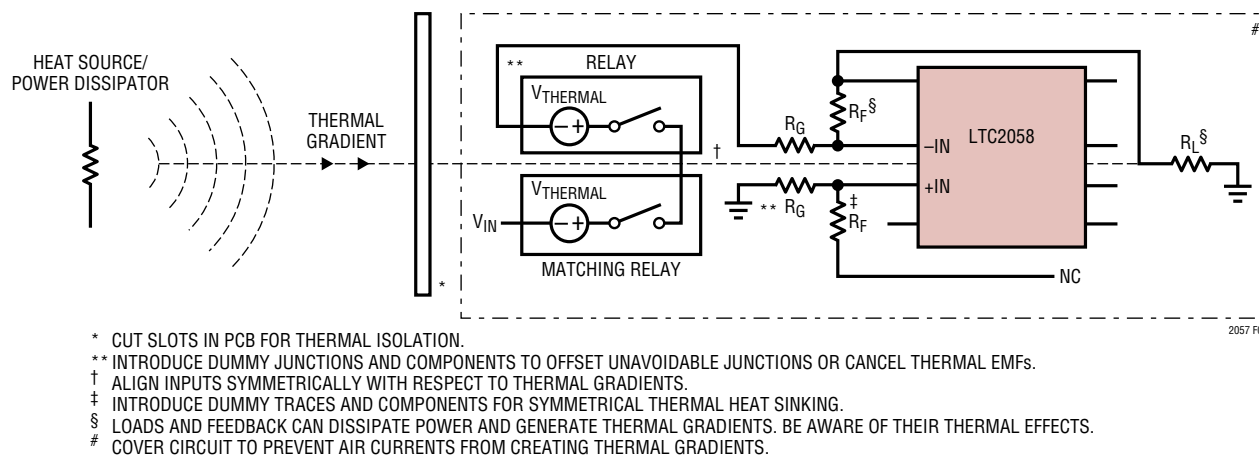
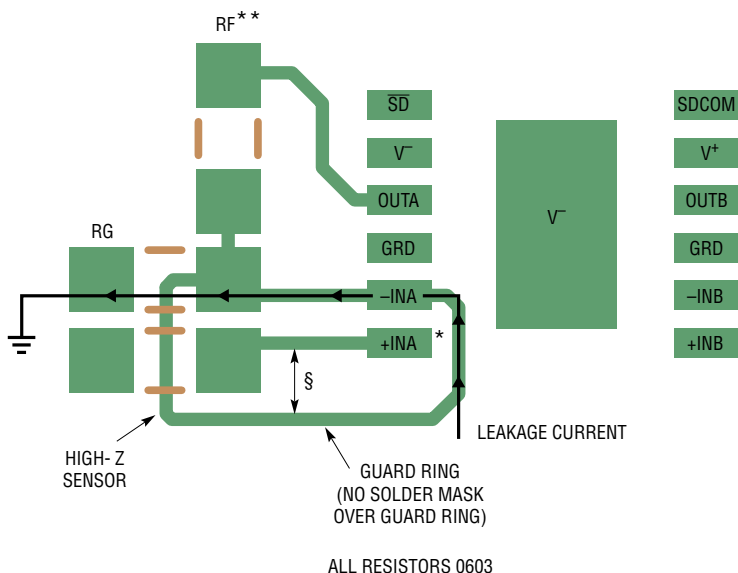


Figure 7. Techniques for Minimizing Thermocouple-Induced Errors

APPLICATIONS INFORMATION

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential very close to that of the inputs. The ring must be tied to a low impedance node. For inverting configurations, the guard ring should be tied to the potential of the positive input (+IN). For noninverting configurations, the guard ring

should be tied to the potential of the negative input (–IN). In order for this technique to be effective, the guard ring must not be covered by solder mask. Ringing both sides of the printed circuit board may be required. See Figure 8a and Figure 8b for examples of proper layout.



* MINIMIZE SPACING TO MAXIMIZE THE CLEARANCE BETWEEN THE EXPOSED GUARD RING AND THE EXPOSED PAD

** V_{ERROR} = I_{LEAK} R_G; R_G << Z_{SENSOR}

§ NO LEAKAGE CURRENT, V_{+IN} = V_{GRD}

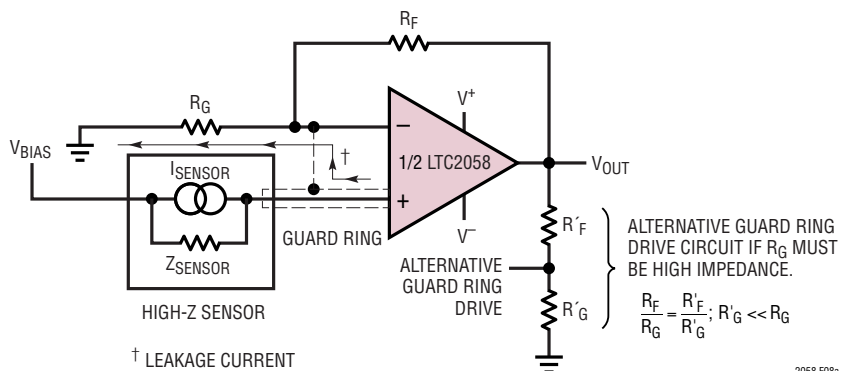


Figure 8a. Example Layout of Noninverting Amplifier with Leakage Guard Ring (Channel A Shown)

APPLICATIONS INFORMATION

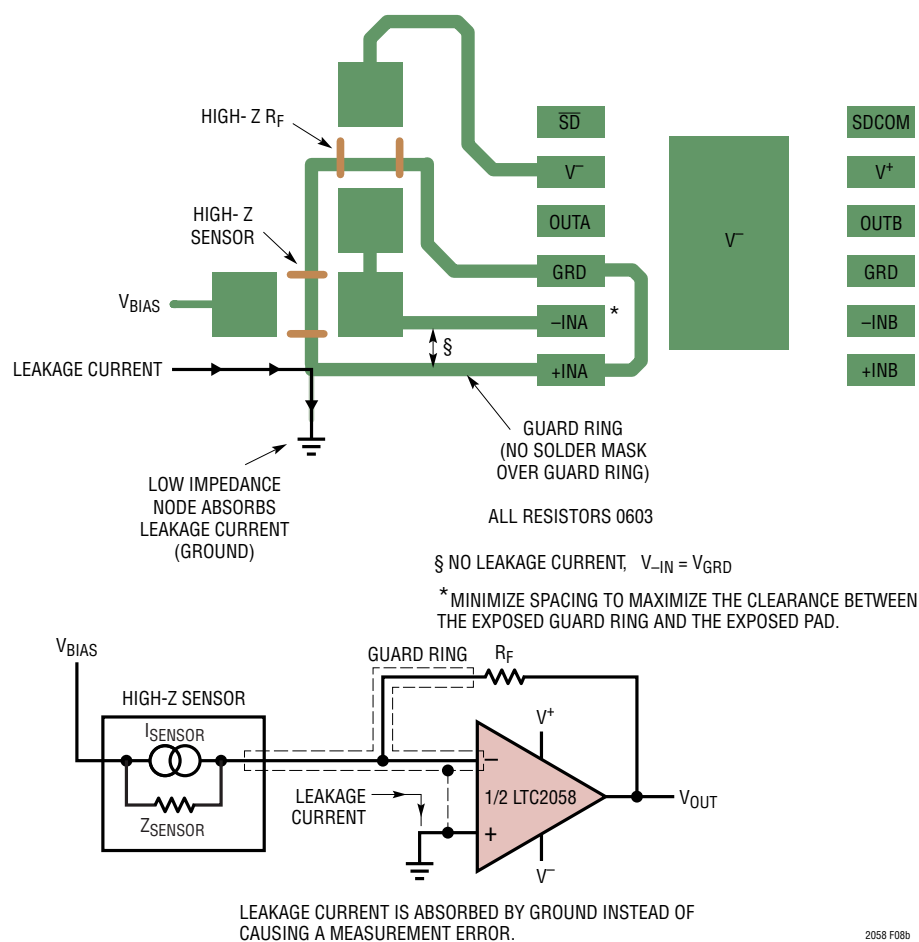


Figure 8b. Example Layout of Inverting Amplifier with Leakage Guard Ring (Channel A Shown)

APPLICATIONS INFORMATION

For low leakage applications, the LTC2058 is available in an MSE12 package with a special pinout that facilitates the layout of guard ring structures. The pins adjacent to the inputs have no internal connection, allowing a guard ring to be routed through them.

Power Dissipation

Since the LTC2058 is capable of operating at 36V total supply, care should be taken with respect to power dissipation in the amplifier. When driving heavy loads at high voltages, use the θ_{JA} of the package to estimate the resulting die-temperature rise and take measures to ensure that the resulting junction temperature does not exceed specified limits. PCB metallization and heat sinking should also be considered when high power dissipation is expected. The LTC2058 is packaged in thermally-enhanced S8E and MSE12 packages. These packages feature lower package thermal resistances compared to their standard counterparts and exposed pads to facilitate heat sinking. The exposed bottom pad must be soldered to the PCB and due to its internal connection to V^- it is required to connect the exposed pad to V^- . For more efficient heat sinking, it is recommended that the exposed pad have as much PCB metal connected to it as reasonably available. Thermal information for all packages can be found in the Pin Configuration section.

Electrical Overstress and Input Protection

Absolute maximum ratings should not be exceeded. Avoid driving the input and output pins beyond the rails, especially at supply voltages approaching 40V. The inputs of LTC2058 are internally protected by ESD diodes (see Block Diagrams section). The Anode of the bottom side diode is the substrate, so driving an input below the rail can induce undesired parasitic behavior. If overvoltage conditions cannot be prevented, a resistor in series with the threatened pin can be used to limit fault current to below the absolute maximum rating and reduce the possibility of device damage. This technique is shown in Figure 9.

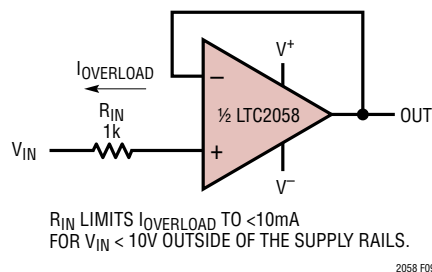


Figure 9. Using a Resistor to Limit Input Current

The current limiting resistance should not be so high as to add noise and error voltages from interaction with input bias currents. Resistances up to 2k will not significantly impact noise or precision. Use the Figure 10 and Figure 11 (I-V Characteristics of the internal ESD diodes) to help determine the appropriate value of the resistor.

In harsh environments, reliability can be enhanced further with protection circuitry as illustrated in Figure 12. This circuit utilizes low-leakage diodes (Nexperia BAV199) to protect the input. R2 protects the external diodes, and R1 is added to limit the current which would get to the internal diodes. In this circuit R1 can be small as the applied voltage is already reduced by the external protection diodes.

In high temperature applications where the leakage currents of the internal ESD diodes dominate the input bias current, the circuit may benefit from adding an input bias cancellation resistor in the feedback path (see Typical Application Section: Input Bias Current).

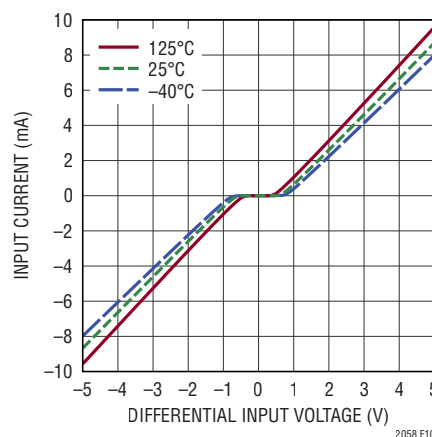


Figure 10. Differential Input Voltage VS Current

APPLICATIONS INFORMATION

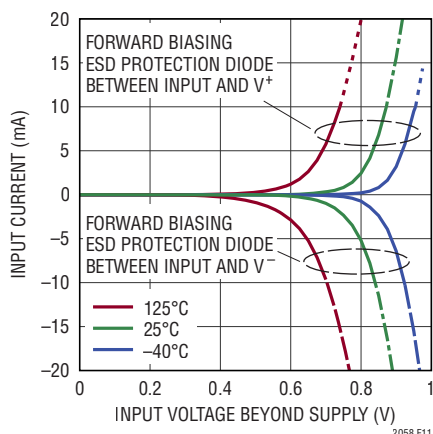


Figure 11. ESD Protection Diode Forward Bias Voltage vs Current

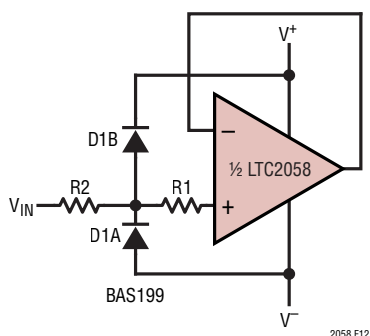


Figure 12. Input Protection Circuit Using External Diodes

Shutdown Mode

The LTC2058 in the MSE12 package features a shutdown mode for low power applications. In the OFF state, both amplifiers are shut off and draw less than 9 μ A of supply current per amplifier. Also in the OFF stage, both outputs present high impedances to external circuitry.

Keep in mind that during the OFF state, even with the amplifier output being high impedance, the output may still be modulated by the input signal through the input differential clamp and the feedback resistor. (Refer to the block diagram for the location of the differential clamp). Also depending on the resistor values, significant current may still be drawn from the input source.

Shutdown control is accomplished using a separate logic reference input (SDCOM) and a shutdown pin ($\overline{\text{SD}}$). This method allows for low voltage digital control logic to operate independently of the amplifier's high voltage supply rails. A summary of control logic and operating ranges is shown in Table 1 and Table 2.

Table 1. Shutdown Control Logic

SHUTDOWN PIN CONDITION	AMPLIFIER STATE
$\overline{\text{SD}}$ = Float, SDCOM = Float	ON
$\overline{\text{SD}} - \text{SDCOM} \geq 2\text{V}$	ON
$\overline{\text{SD}} - \text{SDCOM} \leq 0.8\text{V}$	OFF

Table 2. Operating Voltage Range for Shutdown Pins

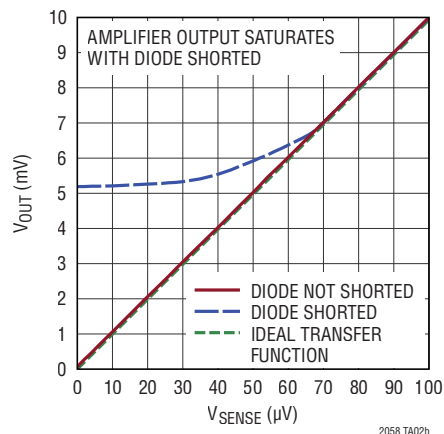
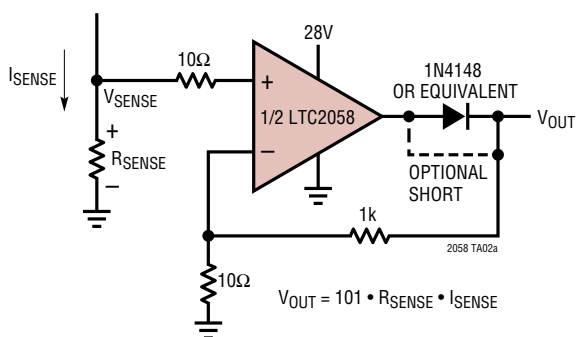
	MIN	MAX
$\overline{\text{SD}} - \text{SDCOM}$	-0.2V	5.2V
SDCOM	V ⁻	V ⁺ - 2V
$\overline{\text{SD}}$	V ⁻	V ⁺

If the shutdown feature is not required, $\overline{\text{SD}}$ and SDCOM may be left floating. Internal circuitry will automatically keep the amplifier in the ON state.

For operation in noisy environments, a capacitor between $\overline{\text{SD}}$ and SDCOM is recommended to prevent noise from changing the shutdown state.

When there is a danger of $\overline{\text{SD}}$ and SDCOM being pulled beyond the supply rails, resistance in series with the shutdown pins is recommended to limit current.

Low Side Current Sense Amplifier Transfer Function



4CM CARBON MONOXIDE SENSOR
CITY TECHNOLOGY
70nA/ppm CO TYPICAL

The circuit diagram shows two LTC2058 op-amps. The first op-amp is configured as a voltage follower with its non-inverting input (+) connected to a 5V supply and its inverting input (-) connected to a -5V supply via a 15k resistor (R1). The output of the first op-amp is connected to the CE pin of the 4CM CO sensor. The sensor's RE pin is connected to a -5V supply via a 15k resistor (R2). The sensor's WE pin is connected to a P-channel JFET (PJFET J177) whose gate is connected to a -5V supply and its source is connected to a 1M resistor (R4) leading to a V+ supply. The sensor's output is connected to the non-inverting input (+) of the second op-amp via a 5Ω load resistor (R_LOAD). The second op-amp is configured as a voltage follower with its non-inverting input (+) connected to a 5V supply and its inverting input (-) connected to a -5V supply via a 35.7k resistor (R3). The output of the second op-amp is V_OUT. A 10nF capacitor (C2) is connected between the input and output of the second op-amp. A 100nF capacitor (C1) is connected between the CE and RE pins of the sensor. The text '2058 TA03' is located at the bottom right of the second op-amp.

5V
1/2 LTC2058
-5V
R1, 15k
C1, 100nF
R2, 15k
CE
WE
R_LOAD, 5Ω
PJFET J177
R4, 1M
V+
5V
1/2 LTC2058
-5V
C2, 10nF
R3, 35.7k
V_OUT
2058 TA03

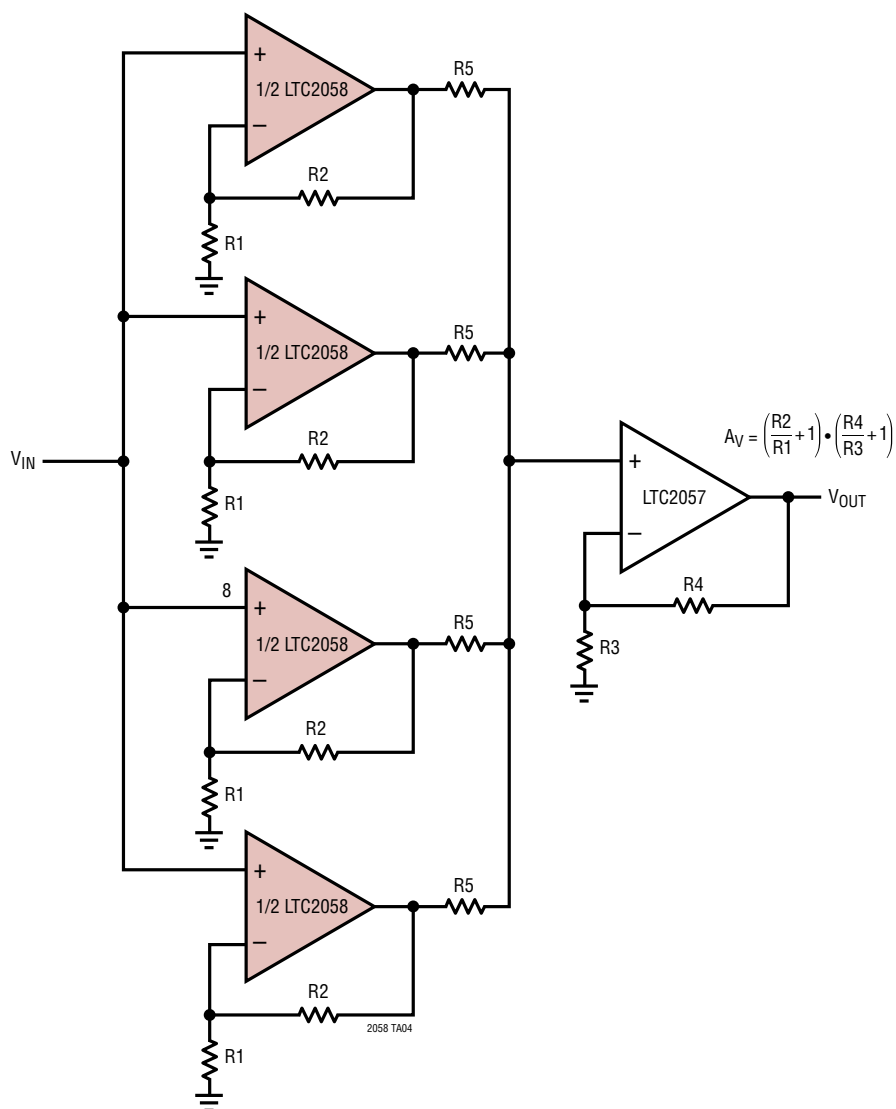
SPLIT RAIL SUPPLY REQUIRED

4CM COUNTER ELECTRODE (CE)
SELF-BIASES BELOW WE POTENTIAL
 $V_{WE} - V_{CE} = -0.3V \text{ TO } -0.4V \text{ TYPICAL}$

TYPICAL GAIN:
2.5mV/ppm CO
MAX OUTPUT:
5V AT 2000ppmCO

TYPICAL APPLICATIONS

Paralleling Choppers to Improve Noise



$$\text{DC TO 10Hz NOISE} = \frac{200\text{nV}_{\text{P-P}}}{\sqrt{N}}, e_n = \frac{9\text{nV}/\sqrt{\text{Hz}}}{\sqrt{N}}, i_n = \sqrt{N} \cdot 1\text{pA}/\sqrt{\text{Hz}}, I_B < N \cdot 100\text{pA (MAX)}$$

WHERE N IS THE NUMBER OF PARALLELED INPUT AMPLIFIERS.

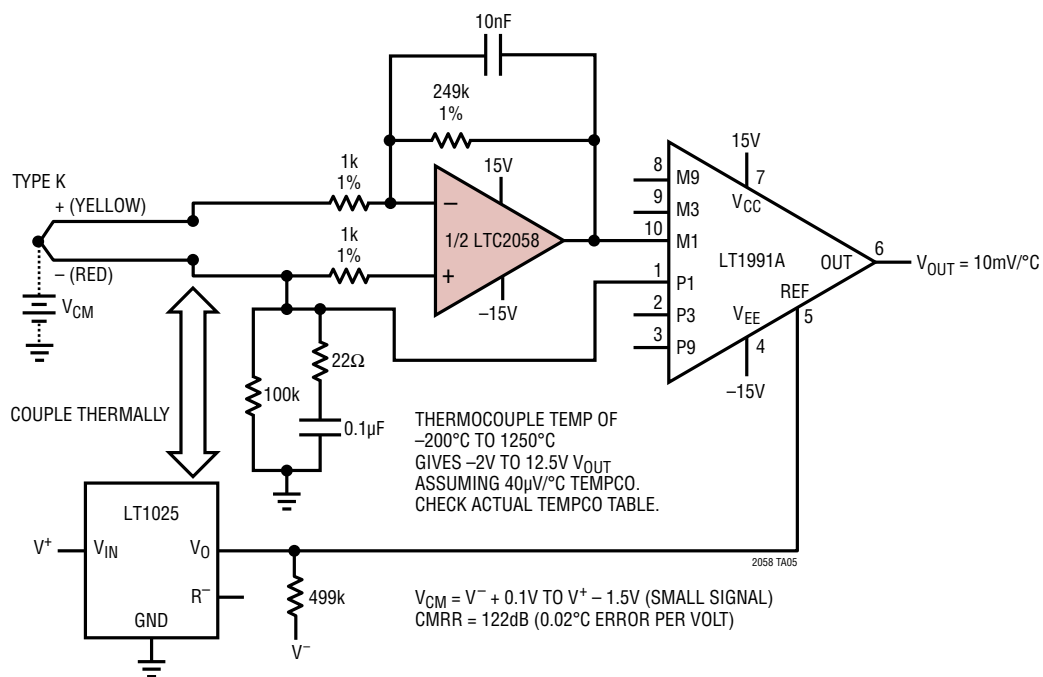
FOR N = 4, DC TO 10Hz NOISE = 100nV_{P-P}, $e_n = 4.5\text{nV}/\sqrt{\text{Hz}}$, $i_n = 2\text{pA}/\sqrt{\text{Hz}}$, $I_B < 100\text{pA (MAX)}$.

R₅ SHOULD BE A FEW HUNDRED OHMS TO ISOLATE AMPLIFIER OUTPUTS WITHOUT CONTRIBUTING SIGNIFICANTLY TO NOISE OR I_B-INDUCED ERROR.

$$\left(\frac{R_2}{R_1} + 1\right) \gg \sqrt{N} \text{ FOR OUTPUT AMPLIFIER NOISE TO BE INSIGNIFICANT.}$$

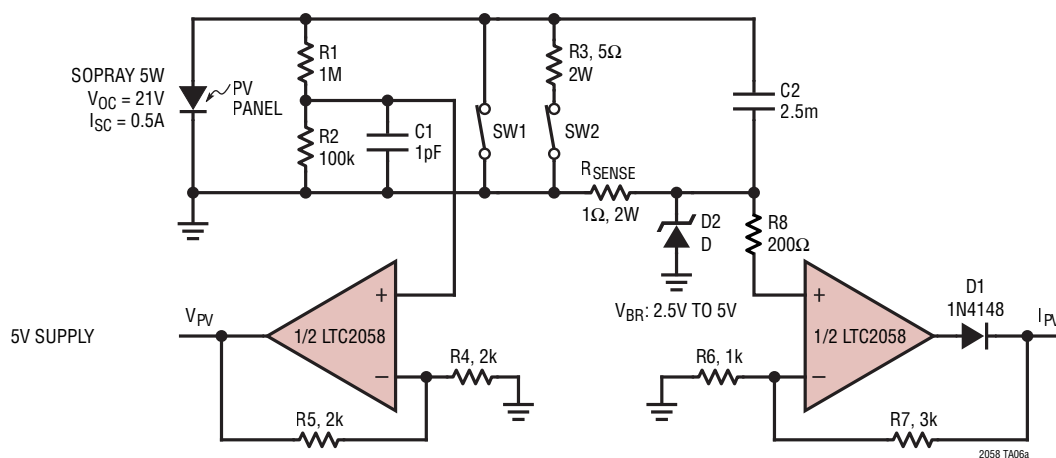
TYPICAL APPLICATIONS

Differential Thermocouple Amplifier

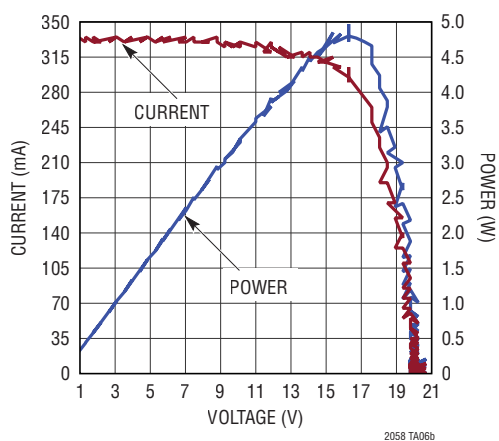


TYPICAL APPLICATIONS

Photovoltaic Module Sweep Measurement

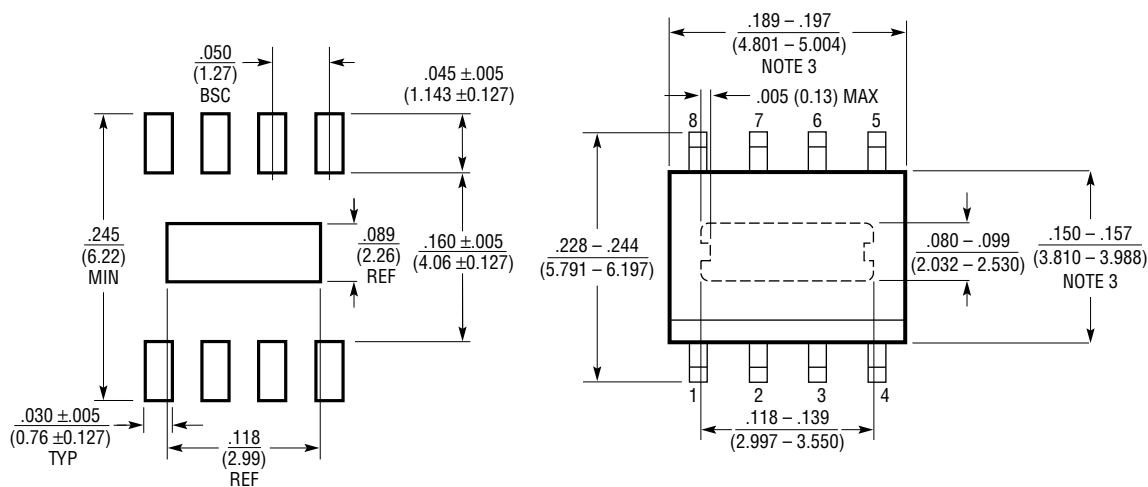


I-V and P-V Curves

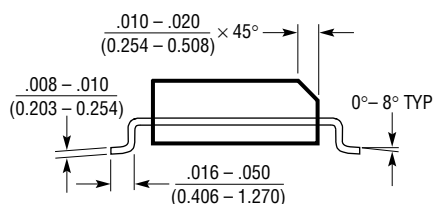


PACKAGE DESCRIPTION

S8E Package 8-Lead Plastic SOIC (Narrow .150 Inch) Exposed Pad (Reference LTC DWG # 05-08-1857 Rev C)



RECOMMENDED SOLDER PAD LAYOUT



NOTE:

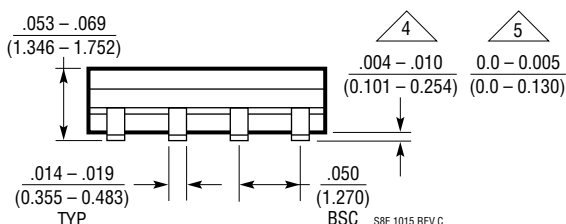
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

2. DRAWING NOT TO SCALE

3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED $.010"$ (0.254mm)

4. STANDARD LEAD STANDOFF IS 4mils TO 10mils (DATE CODE BEFORE 542)

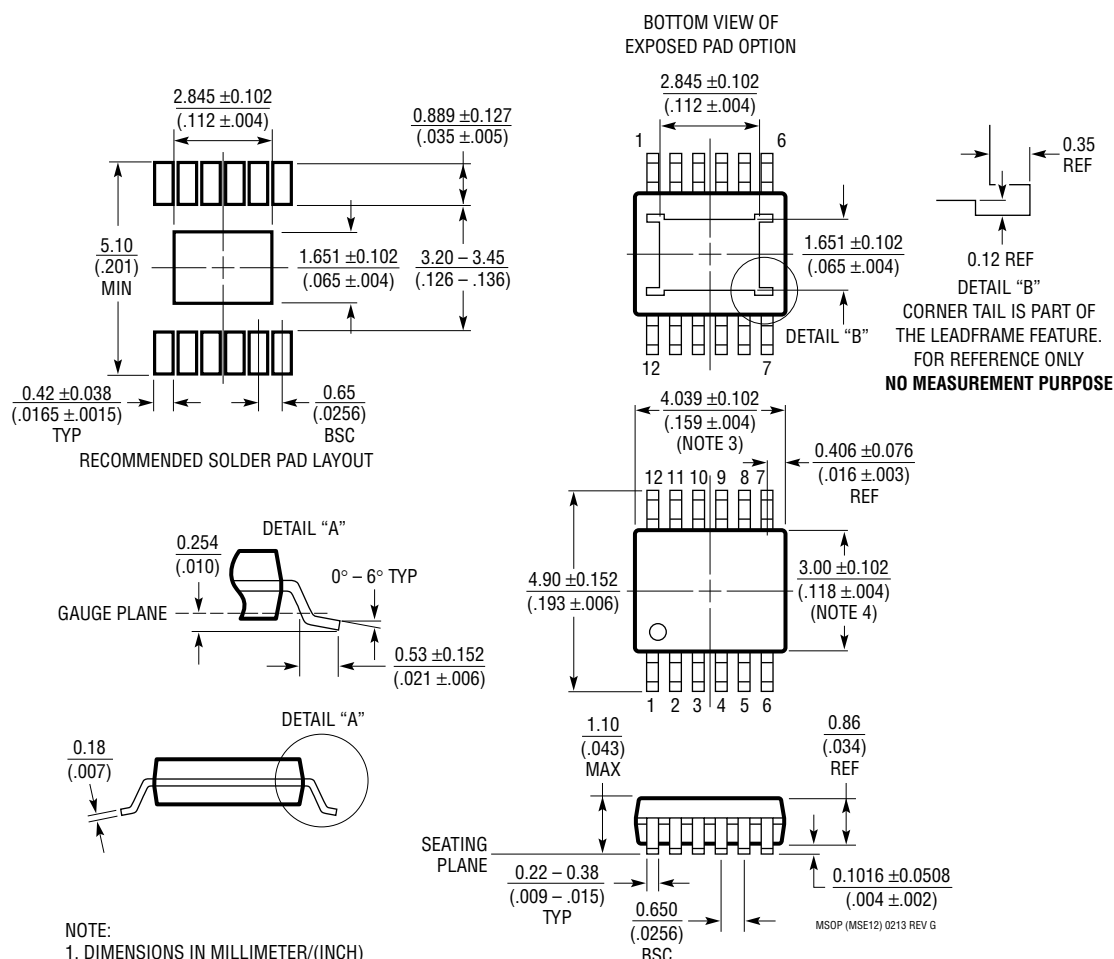
5. LOWER LEAD STANDOFF IS 0mils TO 5mils (DATE CODE AFTER 542)



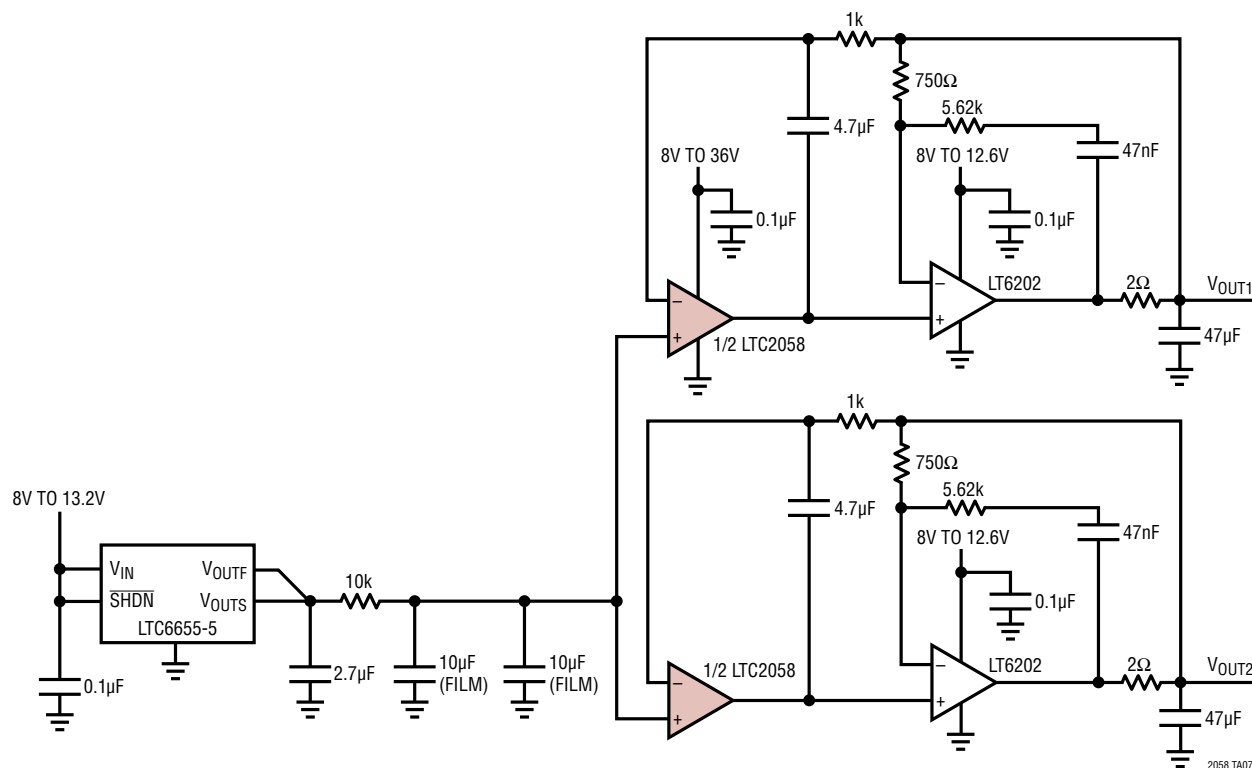
S8E 1015 REV C

PACKAGE DESCRIPTION

MSE Package 12-Lead Plastic MSOP, Exposed Die Pad (Reference LTC DWG # 05-08-1666 Rev G)



Precision Filtering Voltage Reference Distribution Buffers



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2057/ LTC2057HV	High Voltage, Low Noise, Zero Drift Amplifier	4μV V _{OS} , 4.75V to 60V V _S , 1mA I _S , RR Output
LTC2050HV	Zero-Drift Operational Amplifier	3μV V _{OS} , 2.7V to 12V V _S , 1.5mA I _S , RR Output
LTC2051/LTC2052	Dual/Quad, Zero-Drift Operational Amplifier	3μV V _{OS} , 2.7V to 12V V _S , 1.5mA I _S , RR Output
LTC2053	Precision, Rail-to-Rail, Zero-Drift, Resistor-Programmable Instrumentation Amplifier	10μV V _{OS} , 2.7V to 11V V _S , 1.3mA I _S , RRIO
LTC2054/LTC2055	Micropower, Single/Dual, Zero-Drift Operational Amplifier	5μV V _{OS} , 2.7V to 12V V _S , 0.2mA I _S , RRIO
LTC6652	Precision, Low Drift, Low Noise, Buffered Reference	5ppm/°C, 0.05% Initial Accuracy, 2.1ppm _{P-P} Noise
LT6654	Precision, Wide Supply, High Output Drive, Low Noise Reference	10ppm/°C, 0.05% Initial Accuracy, 1.6ppm _{P-P} Noise
LTC6655	0.25ppm Noise, Low Drift, Precision, Buffered Reference Family	2ppm/°C, 0.025% Initial Accuracy, 0.25ppm _{P-P} Noise
LT6016/LT6017	Dual/Quad, 76V Over-The-Top® Input Operational Amplifier	50μV V _{OS} , 3V to 50V V _S , 0.335mA I _S , RRIO
LTC6090	140V Operational Amplifier	50pA I _B , 1.6mV V _{OS} , 9.5V to 140V V _S , 4.5mA I _S , RR Output
LT5400	Quad Matched Resistor Network	±0.01%, ±0.2ppm/°C Matching