EN27LV020 / EN27LV020B 2Megabit Low Voltage EPROM (256K x 8)

FEATURES

- Read Access Time:
  -90ns, -120ns, -150ns, -200ns
- Single +3.3V Power Supply
  -Regulated power supply 3.0V - 3.6V (EN27LV020)
  -Unregulated power supply 2.7V - 3.6V (EN27LV020B for battery operated systems)
- Programming Voltage +12.75V
- QuikRite™ Programming Algorithm
- Typical programming time 20µs
- Low Power CMOS Operation
- 1µA Standby (Typical)
- 15mA Operation (Max.)
- CMOS- and TTL-Compatible I/O
- High-Reliability CMOS Technology
- Latch-Up Immunity to 100mA
  from -1V to V_{CC} + 1V
- Two-Line Control ($\overline{OE}$ & $\overline{CE}$)
- Standard Product Identification Code
- JEDEC Standard Pinout
  - 32-pin PDIP
  - 32-pin PLCC
  - 32-pin TSOP (Type 1)
- Commercial and Industrial Temperature Ranges

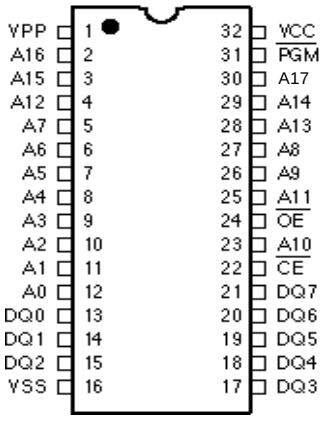
GENERAL DESCRIPTION

The EN27LV020 / EN27LV020B is a low-voltage, low-power 2-Megabit, 3.3V one-time-programmable (OTP) read-only memory (EPROM). Organized into 256K words with 8 bits per word, it features QuikRite™ single-address location programming, typically at 20µs per byte. Any byte can be accessed in less than 90ns. The EN27LV020 / EN27LV020B has separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls which eliminate bus contention issues. The EN27LV020 has a Vcc tolerance range of 3.0V to 3.6 V, making it suitable for use in systems that have regulated power supplies. The EN27LV020B has a Vcc tolerance range of 2.7 V to 3.6V, making it an ideal device for battery operated systems.

FIGURE 1. PDIP

Pin Name	Function
A0-A17	Addresses
DQ0-DQ7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe

PDIP Top View



Preliminary

FIGURE 2. TSOP

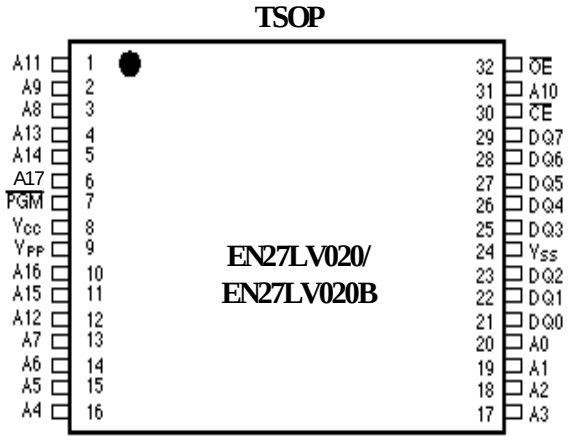


FIGURE 3. PLCC

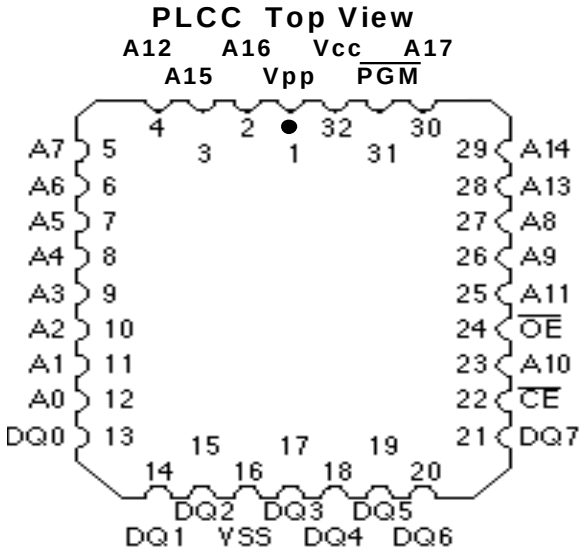
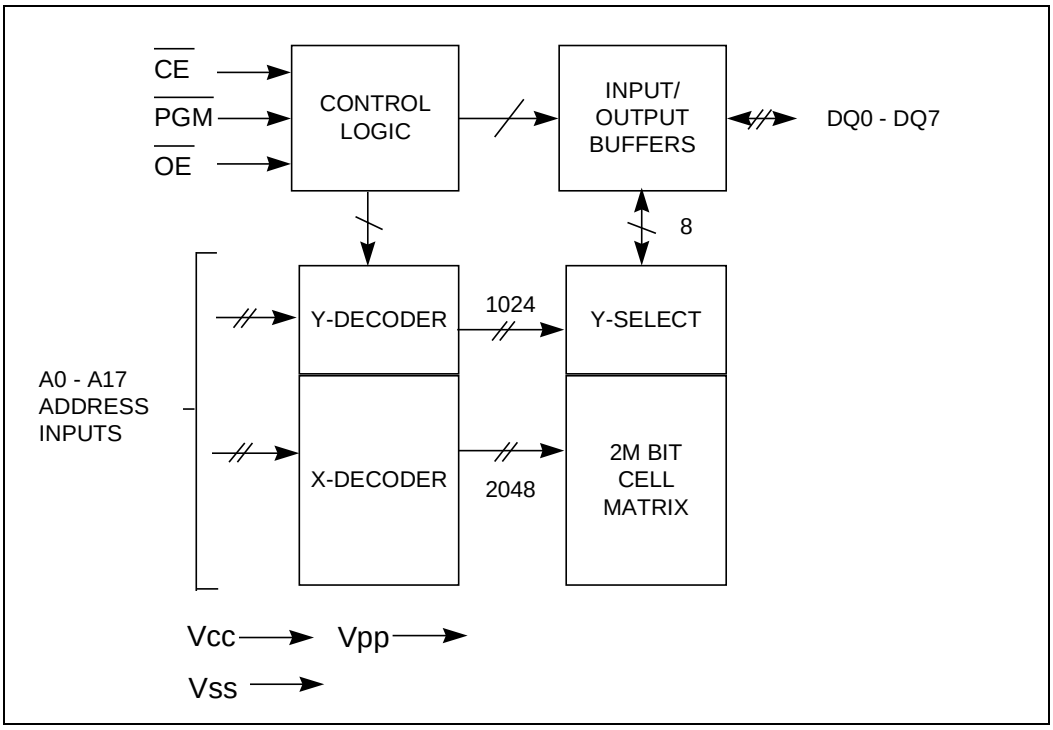


FIGURE 4. BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

THE QUIKRITE™ PROGRAMMING OF THE EN27LV020 / EN27LV020B

When the EN27LV020 / EN27LV020B is delivered, the chip has all 2M bits in the "ONE", or HIGH state. "ZEROs" are loaded into the EN27LV020 / EN27LV020B through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25V is applied to the V_{PP} pin, $\overline{OE}$ is at V_{IH}, and $\overline{CE}$ and $\overline{PGM}$ are at V_{IL}. For programming, the data to be programmed is applied with 8 bits in parallel to the data pins.

The QUIKRITE™ programming flowchart in Figure 5 shows Eon's interactive programming algorithm. The interactive algorithm reduces programming time by using 20 µs to 100 µs programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data is not verified, additional pulses are given until it is verified or until the maximum number of pulses is reached. This process is repeated while sequencing through each address of the EN27LV020 / EN27LV020B. This part of the programming algorithm is done at V_{CC} = 6.25V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. This ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is read at $V_{CC} = V_{PP} = 5.25 \pm 0.25$V to verify the entire memory. EN27LV020 / EN27LV020B can be programmed using the same programming algorithm as the 5V Read EPROM EN27C020.

PROGRAM INHIBIT MODE

Programming of multiple EN27LV020 / EN27LV020B in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$, all like inputs of the parallel EN27LV020 / EN27LV020B may be common. A TTL low-level program pulse applied to an EN27LV020 / EN27LV020B $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25V, $\overline{PGM}$ LOW, and $\overline{OE}$ HIGH will program that EN27LV020 / EN27LV020B. A high-level $\overline{CE}$ input inhibits the other EN27LV020 / EN27LV020B from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determining that they were correctly programmed. The verification should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} at its programming voltage.

AUTO PRODUCT IDENTIFICATION

The Auto Product Identification mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the EN27LV020 / EN27LV020B.

To activate this mode, the programming equipment must force 12.0 V ± 0.5V on address line A9 of the EN27LV020 / EN27LV020B. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}, when A1 = V_{IH}. All other address lines must be held at V_{IL} during Auto Product Identification mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and byte 1 (A0 = V_{IH}), the device code. For the EN27LV020 / EN27LV020B these two identifiers bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit. When A1 = V_{IL}, the EN27LV020 / EN27LV020B will read out the binary code of 7F, continuation code, to signify the unavailability of manufacturer ID codes.

READ MODE

The EN27LV020 / EN27LV020B has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs (t_{OE}) after the falling edge of $\overline{OE}$, assuming the $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The EN27LV020 / EN27LV020B has CMOS standby mode which reduces the maximum V_{CC} current to 10μA. It is placed in CMOS standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The EN27LV020 / EN27LV020B also has a TTL-standby mode which reduces the maximum V_{CC} current to 0.6 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selection function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and VSS to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7μF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A1	A9	V_{PP}	Output
Read	V_{IL}	V_{IL}	X [2]	X	X	X	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	X	X	V_{CC}	High Z
Standby (TTL)	V_{IH}	X	X	X	X	X	V_{CC}	High Z
Standby (CMOS)	$V_{CC} \pm 0.3V$	X	X	X	X	X	V_{CC}	High Z
Program [4]	V_{IL}	V_{IH}	V_{IL}	X	X	X	V_{PP}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	X	V_{PP}	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	X	X	V_{PP}	High Z
Manufacturer Code [3]	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	VH[1]	V_{CC}	1C
Device Code [3]	V_{IL}	V_{IL}	X	V_{IH}	V_{IH}	VH[1]	V_{CC}	02

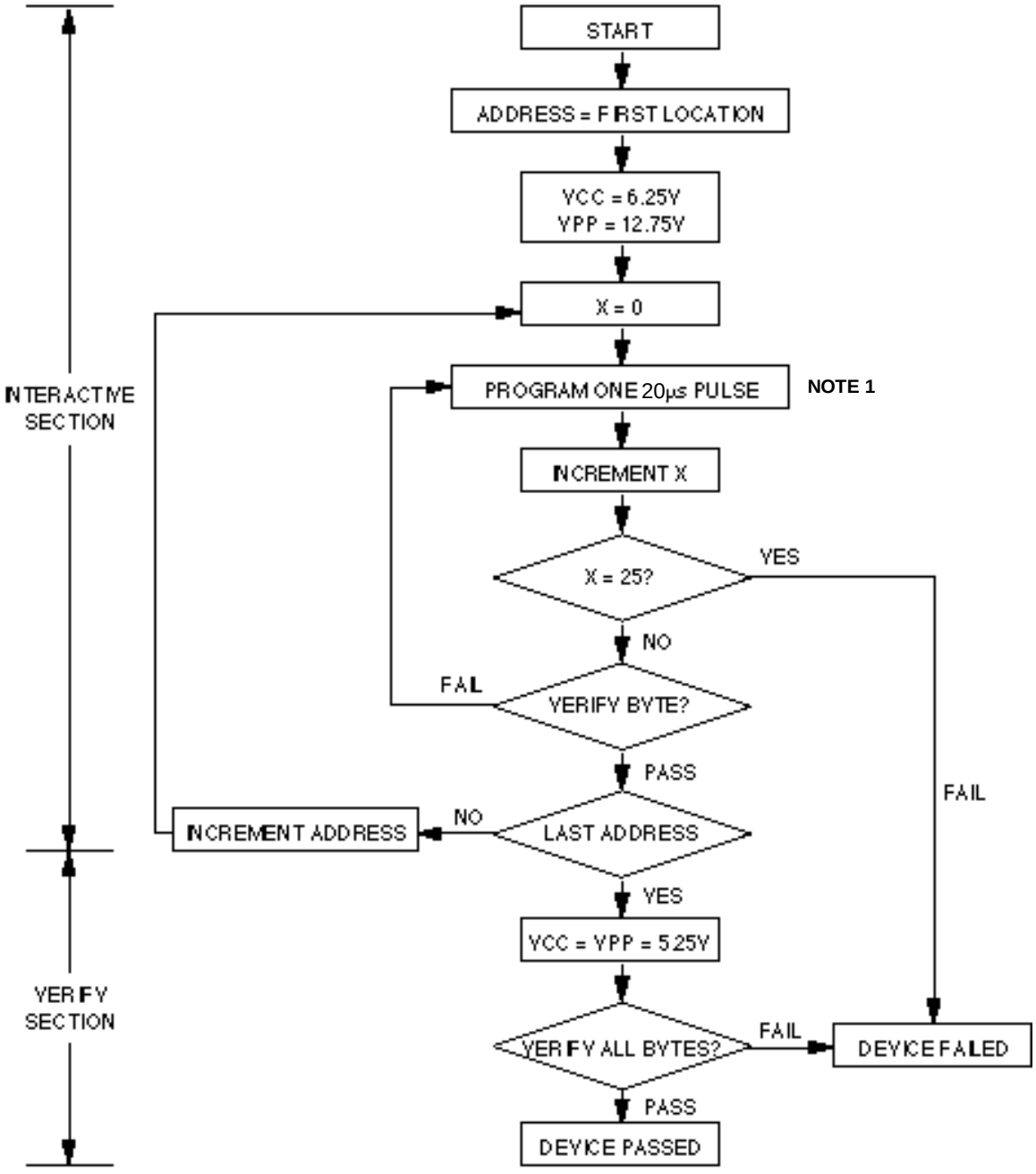
NOTES:

1) VH = 12.0V ± 0.5V
2) X = Either V_{IH} or V_{IL}
3) For Manufacturer Code and Device Code, A1 = V_{IH}
   When A1 = V_{IL}, both codes will read 7F
4) See DC Programming Characteristics for V_{PP} voltage during programming

EON'S STANDARD PRODUCT IDENTIFICATION CODE

	Pins										Hex Data
Code	A0	A1	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	
Manufacturer	0	1	0	0	0	1	1	1	0	0	1C
Device Type	1	1	0	0	0	0	0	0	1	0	02
Continuation	0	0	0	1	1	1	1	1	1	1	7F
	1	0	0	1	1	1	1	1	1	1	7F

FIGURE 5. QUIKRITE™ PROGRAMMING FLOW CHART



NOTE 1: Either 100µs or 20µs pulse.

Preliminary

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 ° C to +125 ° C
Ambient Temperature with Power Applied	-40 ° C to +85 ° C
Voltage with Respect to V_{SS}	
All pins except A9, V_{PP}, V_{CC}	-0.6V to V_{CC} + 0.5V
A9, V_{PP}	-0.6V to +13.5V
V_{CC}	-0.6V to +7.0V

OPERATING RANGES

Commercial (C) Case Temperature(Tc)	0 ° C to +70 ° C
Industrial (I) Case Temperature(Tc)	-40 ° C to +85 ° C
Supply READ Voltages	+3.0V to +3.6V
(for battery operated systems)	+2.7V to +3.6V

(Functionality is guaranteed between these limits)

*Stresses above those shown above may cause permanent damage to the device. This is a stress rating only and operation above these specifications for extended periods may affect device reliability. Operation outside the **"OPERATING RANGES"** shown above voids any and all warranty provisions.*

DC CHARACTERISTICS FOR READ OPERATION

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -2.0mA
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0mA
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
I_{LI}	Input Leakage Current	-5	5	µA	V_{IN} = 0 to 3.6V
I_{LO}	Output Leakage Current	-10	10	µA	V_{OUT} = 0 to 3.6V
I_{CC3}	V_{CC} Power -Down Current		10	µA	$\overline{CE}$ = V_{CC} ± 0.3V
I_{CC2}	V_{CC} Standby Current		0.6	mA	$\overline{CE}$ = V_{IH}
I_{CC1}	V_{CC} Active Current		15	mA	$\overline{CE}$ = V_{IL}, f=5MHz, I_{OUT} = 0mA
I_{PP1}	V_{PP} Supply Current Read		100	µA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = 3.6V

CAPACITANCE

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	8	12	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
C_{VPP}	V_{PP} Capacitance	18	25	pF	V_{PP} = 0V

AC CHARACTERISTICS FOR READ OPERATION

Symbol	Parameter	EN27LV020 / EN27LV020B Condition	-90 Min	-90 Max	-120 -120 Min	-120 -120 Max	-150 -150 Min	-150 -150 Max	-200 -200 Min	-200 -200 Max	Unit
tACC (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		90		120		150		200	ns
tCE (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		90		120		150		200	ns
tOE (2, 3)	$\overline{OE}$ to Output Delay	$\overline{OE}$ = V_{IL}		45		45		50		50	ns
tDF (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			40		40		40		40	ns
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		0		0		ns

Note: Please contact Marketing Department for other speed requirements.

FIGURE 6. AC WAVEFORMS FOR READ OPERATION

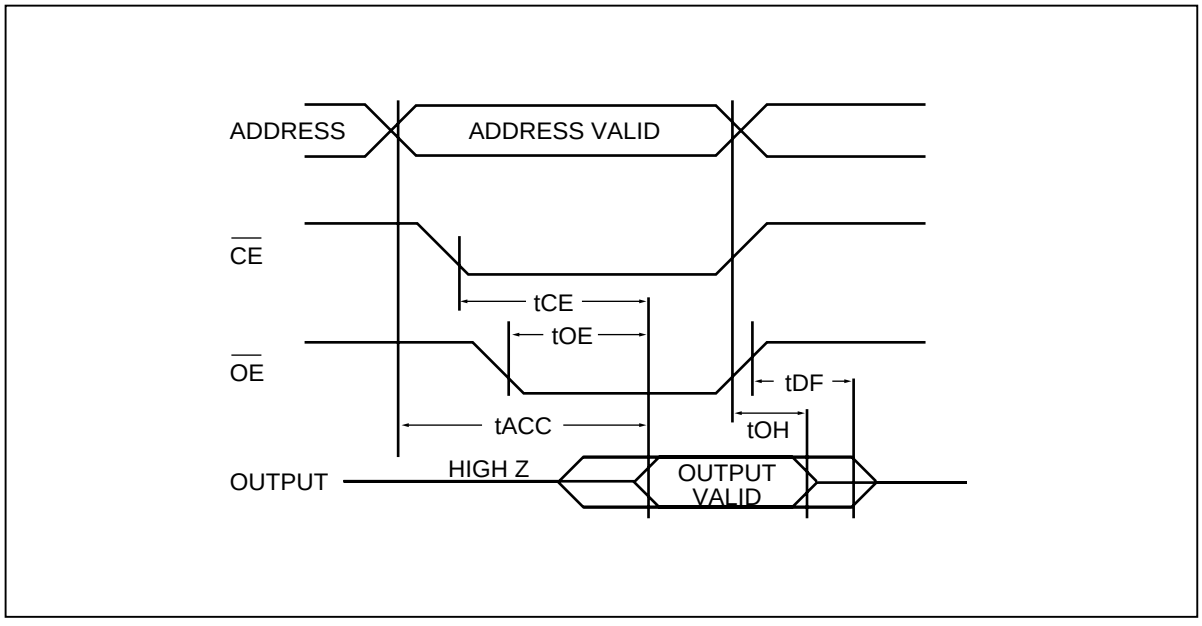
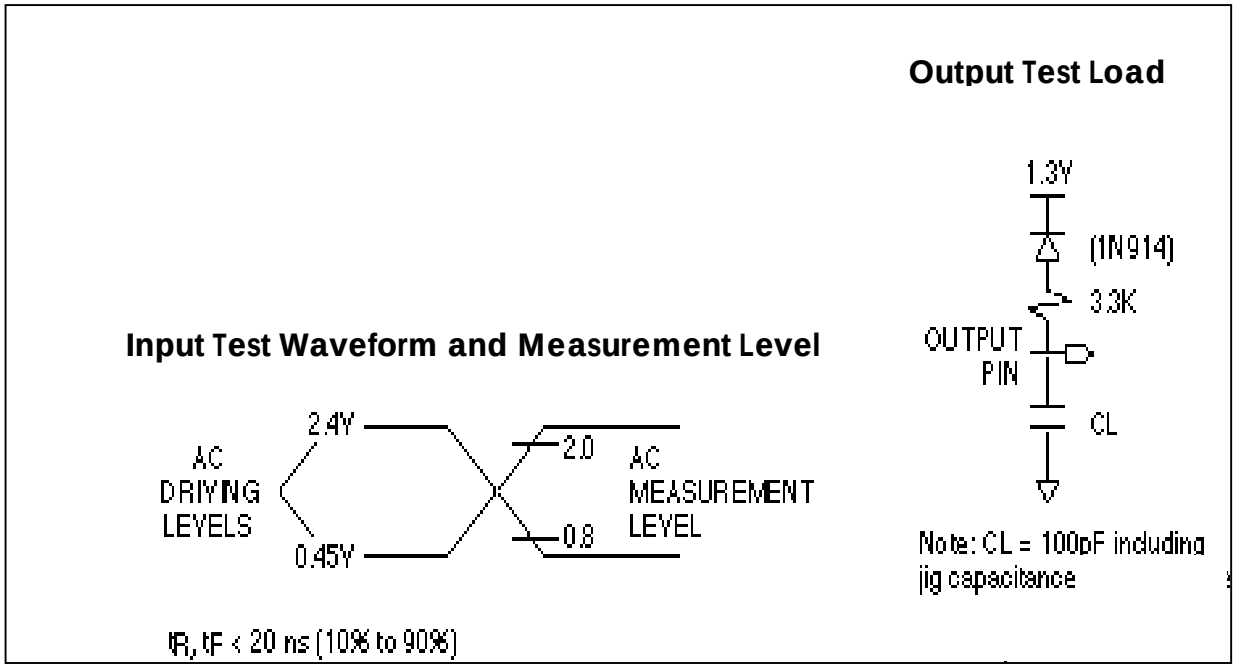


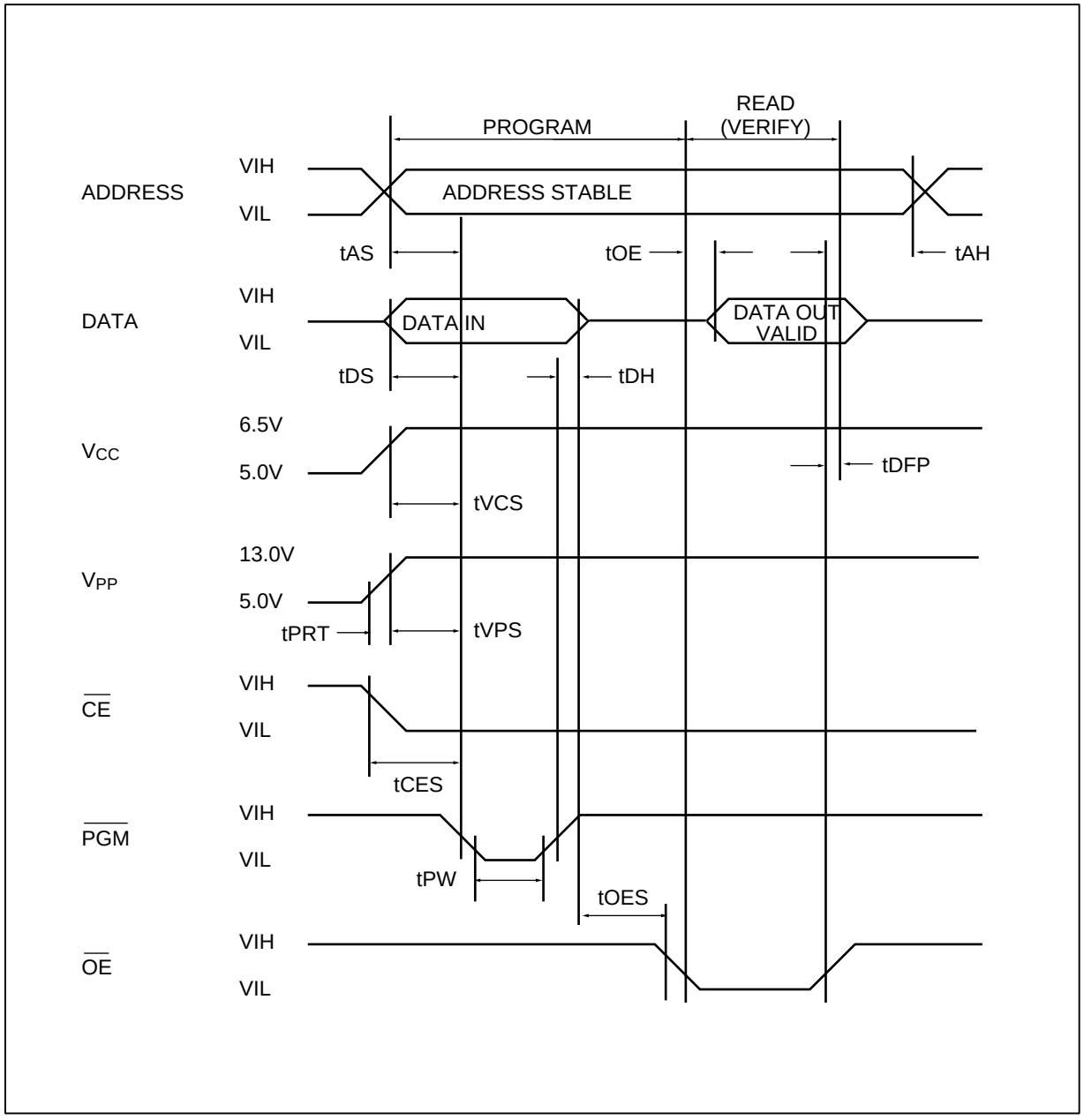
FIGURE 7: TEST WAVEFORMS AND MEASUREMENTS



DC PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Limits Min.	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		5.0	µA
V_{IL}	Input Low Level		-0.5	0.8	V
V_{IH}	Input High Level		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = - 400 µA	2.4		V
I_{ccp}	V_{CC} Supply Current			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}$ = $\overline{PGM}$ = V_{IL},		10	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V
V_{cc}	Quikrite Supply Voltage		6.0	6.5	V
V_{pp}	Quikrite Programming Voltage		12.5	13.0	V

FIGURE 8. PROGRAMMING WAVEFORMS



SWITCHING PROGRAMMING CHARACTERISTICS

(T_A = + 25 ° C ± 5 ° C)

PARAMETER SYMBOL				
STANDARD	**PARAMETER DESCRIPTION**	**Min.**	**Max**	**Units**
t_{AS}	Address Setup Time	2		µs
t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DS}	Data Setup Time	2		µs
t_{AH}	Address Hold Time	0		µs
t_{DH}	Data Hold Time	2		µs
t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	V_{PP} Setup Time	2		µs
t_{PW}	PGM Program Pulse Width	20	105	µs
t_{VCS}	V_{cc} Setup Time	2		µs
t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{OE}	Data Valid from $\overline{OE}$		150	ns

ORDERING INFORMATION

EN27LV020 / EN27LV020B 90 P I

TEMPERATURE RANGE
(Blank) = Commercial (0 ° C to +70 ° C)
I = Industrial (-40 ° C to +85 ° C)

PACKAGE
P = 32 Plastic DIP
J = 32 Plastic PLCC
T = 32 Plastic TSOP

SPEED
90 = 90ns
120 = 120ns
150 = 150ns
200 = 200ns

BASE PART NUMBER
EN = EON Silicon Devices
27 = EPROM
LV = Low Voltage CMOS
020 = 256K x 8 3.0V to 3.6V Vcc

Tolerance

Preliminary

020B = 256K x 8 2.7V to 3.6V Vcc

Tolerance