CLC414 Quad, Low Power Monolithic Op Amp

Check for Samples: CLC414

FEATURES

- **90MHz Small Signal Bandwidth**
- **2mA Quiescent Current Per Amplifier**
- **70dB Channel Isolation @ 5MHz**
- **0.1%/0.12° Differential Gain/Phase**
- **16ns Settling to 0.1%**
- **100V/µs Slew Rate**
- **3.3ns Rise and Fall Time ($2V_{PP}$)**
- **70mA Output Current**

APPLICATIONS

- **Composite Video Distribution Amps**
- **HDTV Amplifiers**
- **RGB Video Amplifiers**
- **CCD Signal Processing**
- **Active Filters**
- **Instrumentation Diff. Amps**
- **General Purpose High Density Requirements**

DESCRIPTION

The CLC414 is a low power, quad, monolithic operational amplifier designed for intermediate gain applications where power and cost per channel are of primary concern. Benefitting from TI's current feedback architecture, the CLC414 offers a gain range of ±1 to ±10 while providing stable, oscillation free operation without external compensation, even at unity gain.

Operating from ±5V supplies, the CLC414 consumes only 25mW of power per channel, yet maintains a 90MHz small signal bandwidth and a 1000V/µs slew rate. The CLC414 also provides wide channel isolation with its 70dB crosstalk (input referred at 5MHz). Applications requiring a high density solution to high speed amplification such as active filters and instrumentation diff amps will benefit from the CLC414's four integrated, wideband op amps in one 14-pin package.

Commercial remote sensing applications and battery powered radio transceivers requiring high performance, low power will find the CLC414 to be an attractive, cost effective solution. In composite video switching and distribution applications, the CLC414 offers differential gain and phase performance of 0.1%, 0.12° at 3.58MHz.

The lower power CLC414 and the wideband CLC415 are quad versions of the CLC406. Both of these quads afford the designer lower power consumption and lower cost per channel with the additional benefit of requiring less board space per amplifier.

Construction using an advanced, complementary bipolar process and TI's proven current feedback architecture, the CLC414 is available in several versions to meet a variety of requirements.

Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-91693

Space level versions also available.

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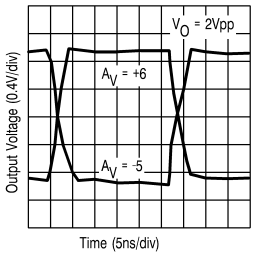


Figure 1. Small Signal Pulse Response

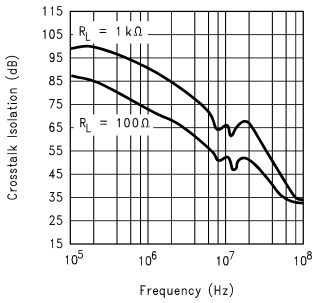


Figure 2. All-Hostile Crosstalk Isolation

CONNECTION DIAGRAM

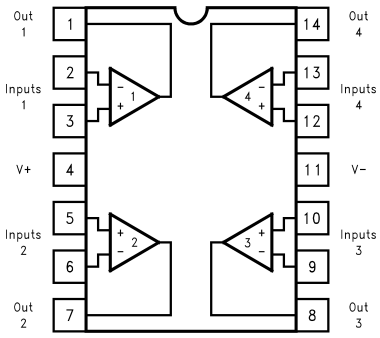


Figure 3. Pinout PDIP & SOIC
See Package Numbers NFF and D

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage (V_{CC})		±7V
I_{OUT}	Output is Short Circuit protected to ground, but maximum reliability will be maintained if I_{OUT} does not exceed...	70mA
Common Mode Input Voltage		±V_{CC}
Differential Input Voltage		±10V
Junction Temperature		+150°C
Operating Temperature Range		−40°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature Range (Soldering 10 sec)		+300°C
ESD Rating (Human Body Model)		<1000V

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of ELECTRICAL CHARACTERISTICS specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

OPERATING RATINGS

Thermal Resistance		
Package	(θ_{JC})	(θ_{JA})
PDIP	60°C/W	110°C/W
SOIC	45°C/W	115°C/W

ELECTRICAL CHARACTERISTICS

(A_V = +6, V_{CC} = ±5V, R_L = 100Ω, R_f = 500Ω; Unless Specified)

Symbol	Parameter	Conditions	Typ	Max/Min(1)			Units
Ambient Temperature		CLC414AJ	+25°C	−40°C	+25°C	+85°C	
Frequency Domain Response							
SSBW	-3dB Bandwidth	V_{OUT} < $2V_{PP}$	90	>60	>60	>45	MHz
LSBW		V_{OUT} < $5V_{PP}$	55	>35	>40	>35	MHz
	Gain Flatness	V_{OUT} < $2V_{PP}$					
GFPL	Peaking	DC to 15MHz	0	<0.15	<0.15	<0.15	dB
GFPH	Peaking	>15MHz	0	<0.3	<0.3	<0.3	dB
GFR	Rolloff	DC to 30MHz	0.3	<1.0	<1.0	<1.5	dB
LPD	Linear Phase Deviation	DC to 30MHz	0.8	<1.2	<1.2	<1.5	deg
DG1	Differential Gain, A_V = +2	R_L = 150Ω, 3.58MHz	0.10	<0.15	<0.20	<0.25	%
DG2		R_L = 150Ω, 4.43MHz	0.12	<0.20	<0.25	<0.30	%
DP1	Differential Phase, A_V = +2	R_L = 150Ω, 3.58MHz	0.12	<0.15	<0.20	<0.50	deg
DP2		R_L = 150Ω, 4.43MHz	0.15	<0.20	<0.25	<0.60	deg
XT	Crosstalk Input Referred	5MHz (All Hostile)	60	<58	<58	<56	dB
CXT		5MHz (Chan. to Chan.)	70	<63	<63	<61	dB

(1) Max/min ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

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ELECTRICAL CHARACTERISTICS (continued)

(A_V = +6, V_{CC} = ±5V, R_L = 100Ω, R_f = 500Ω; Unless Specified)

Symbol	Parameter		Conditions	Typ	Max/Min (1)			Units
Time Domain Response								
TRS	Rise and Fall Time		2V Step	3.3	<5.0	<5.0	<6.5	ns
TRL			5V Step	4.0	<7.0	<6.0	<7.0	ns
TS1	Settling Time	to ±0.1%	2V Step	16	<24	<24	<30	ns
TS2		to 0.02%	2V Step	60	<80	<80	<100	ns
OS	Overshoot		2V Step	5	<10	<10	<10	%
SR	Slew Rate			1000	>600	>600	>480	V/µs
Distortion And Noise Response								
HD2	2nd Harmonic Distortion		$2V_{PP}$, 5MHz	−47	<−41	<−41	<−37	dBc
HD3	3rd Harmonic Distortion		$2V_{PP}$, 5MHz	−55	<−47	<−47	<−45	dBc
	Equivalent Noise Input							
VN	Non-Inverting Voltage		>1MHz	4.2	<5.0	<5.0	<5.5	nV/√Hz
ICN	Inverting Current		>1MHz	9.8	<11.8	<11.8	<13.0	pA/√Hz
NCN	Non-Inverting Current		>1MHz	1.3	<1.6	<1.6	<1.8	pA/√Hz
SNF	Total Noise Floor		>1MHz	−154	<−153	<−153	<−152	dBm_{1Hz}
INV	Total Integrated Noise		>1MHz to 75MHz	37	<44	<44	<48	µV
Static, DC Performance								
VIO	Input Offset Voltage (2)			2	<10.5	<6	<14	mV
DVIO	Average Temperature Coefficient			30	<80	-	<80	µV/C°
IBN	Input Bias Current (2)		Non-Inverting	1	<10	<5	<5	µA
DIBN	Average Temperature Coefficient			20	<75	–	<30	nA/°C
IBI	Input Bias Current (2)		Inverting	2	<20	<6	<10	µA
DIBI	Average Temperature Coefficient			20	<140	–	<75	nA/°C
PSRR	Power Supply Rejection Ratio			50	>46	>46	>44	dB
CMRR	Common Mode Rejection Ratio			50	>45	>45	>43	dB
ICC	Supply Current (2)		No Load	10	<11.5	<11.5	<11.5	mA
Miscellaneous Performance								
RIN	Non Inverting Input Resistance			2000	>500	>1000	>1000	kΩ
CIN	Non-Inverting Input Capacitance			1.0	<2.0	<2.0	<2.0	pF
RO	Output Impedance		DC	0.2	<0.6	<0.3	<0.2	Ω
VO	Output Voltage Range		R_L = 100Ω	±2.8	±2.5	±2.6	±2.7	V
CMIR	Common Mode Input Range			±2.2	±1.4	±2.0	±2.0	V
IO	Output Current			70	30	50	50	mA

(2) AJ-level: spec. is 100% tested at +25°C.

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TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°, A_V = +6, V_{CC} = ±5V, R_L = 100Ω, R_f = 500Ω; Unless Specified).

Non-Inverting Frequency Response

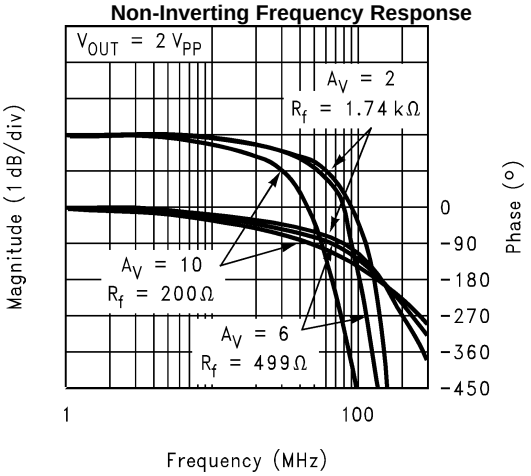


Figure 4.

Inverting Frequency Response

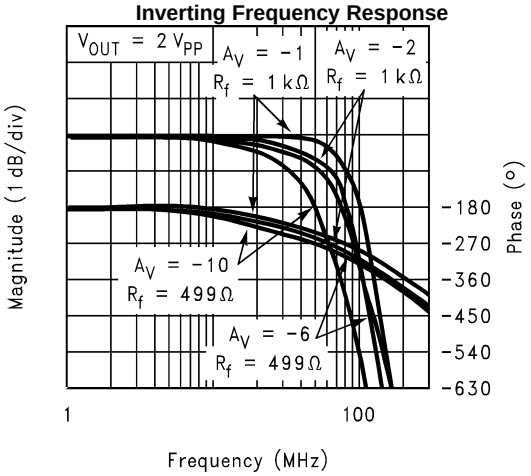


Figure 5.

Frequency Response for Various R_LS

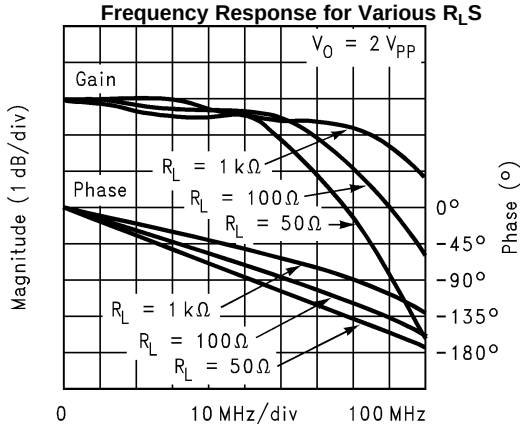


Figure 6.

Small Signal Pulse Response

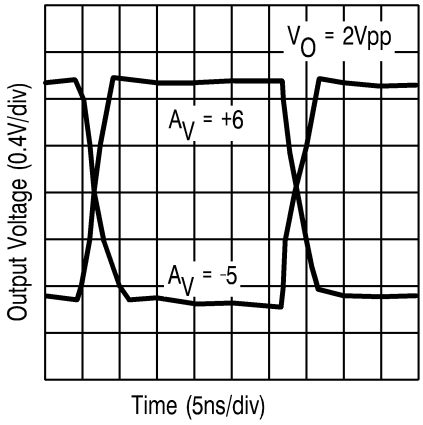


Figure 7.

Short-Term Settling Time

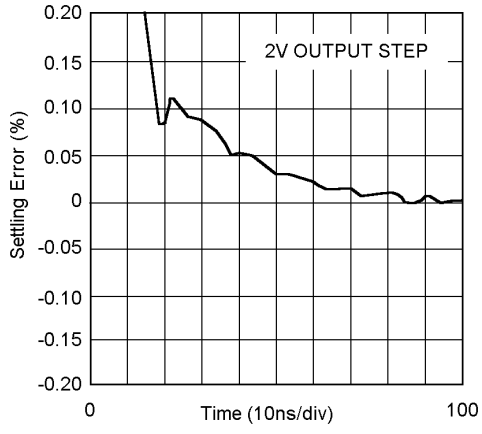


Figure 8.

Long-Term Settling Time

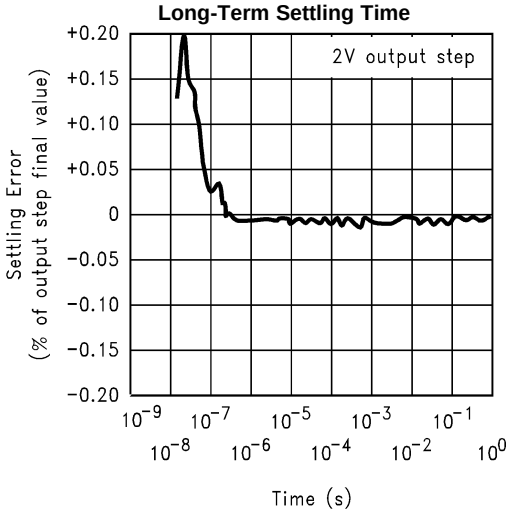


Figure 9.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = 25°, A_V = +6, V_{CC} = ±5V, R_L = 100Ω, R_f = 500Ω; Unless Specified).

2nd and 3rd Harmonic Distortion

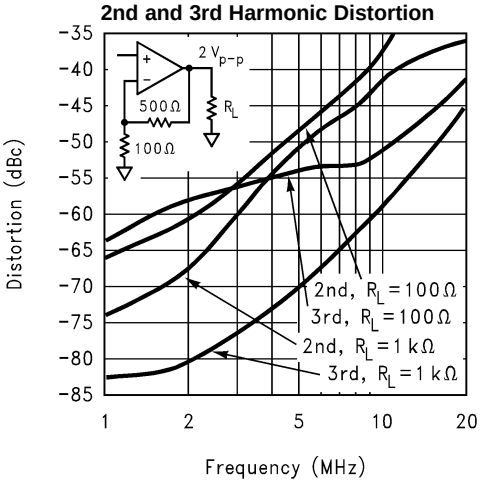


Figure 10.

2-Tone, 3rd Order, Spurious Levels

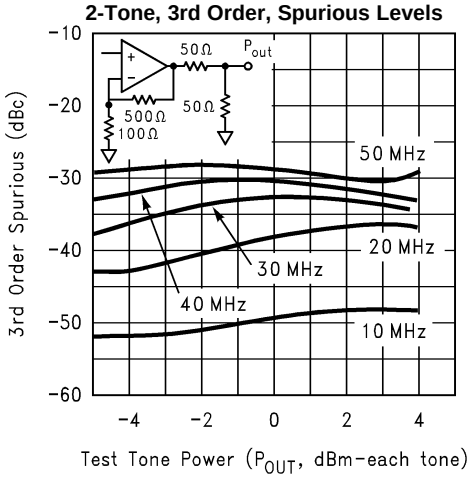


Figure 11.

Settling Time vs. Capacitive Load

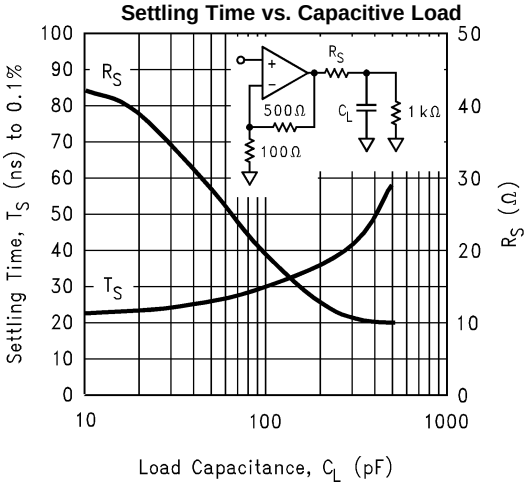


Figure 12.

All-Hostile Crosstalk Isolation

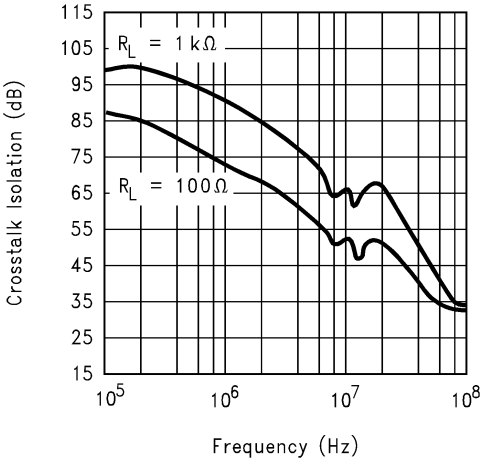


Figure 13.

Most Susceptible Channel-Channel Pulse Coupling

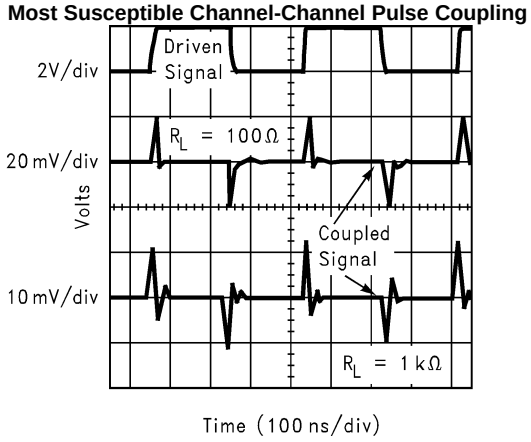


Figure 14.

Differential Gain and Phase (4.43 MHz, A_V=+2)

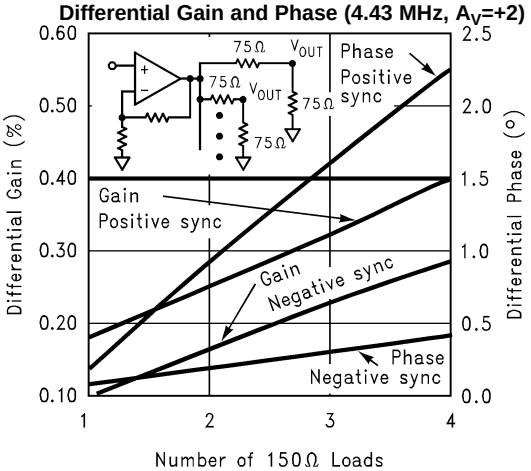


Figure 15.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = 25°, A_V = +6, V_{CC} = ±5V, R_L = 100Ω, R_f = 500Ω; Unless Specified).

Equivalent Input Noise

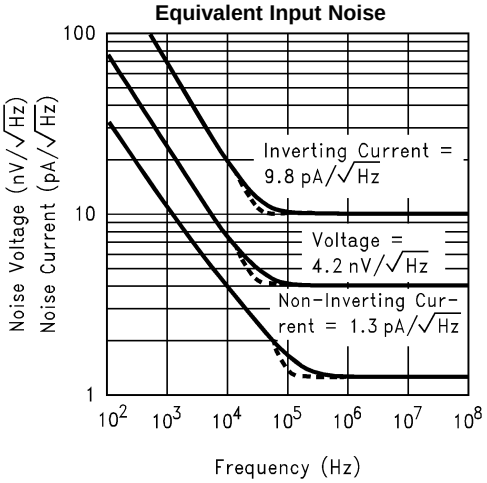


Figure 16.

Open-Loop Transimpedance Gain, Z(s)

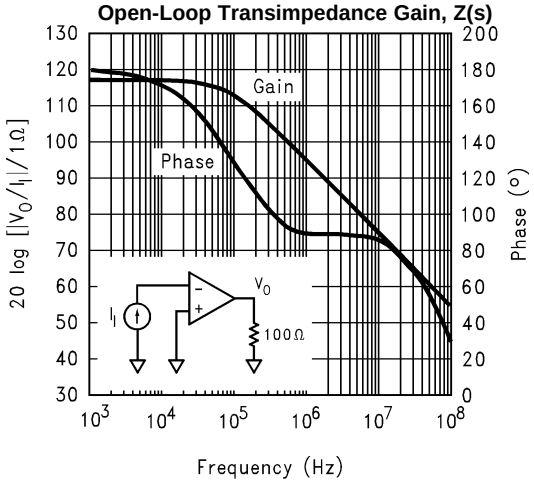


Figure 17.

PSRR, CMRR, and Closed Loop R_O

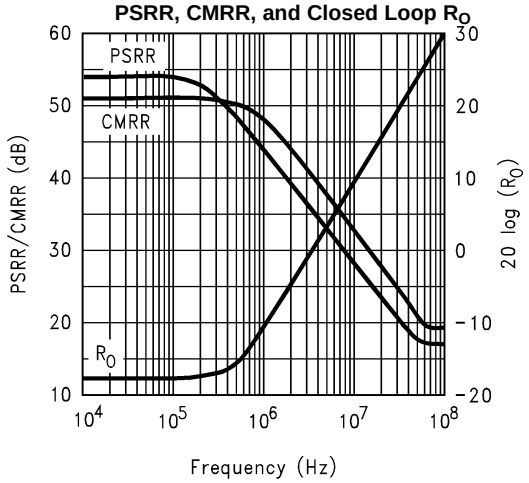


Figure 18.

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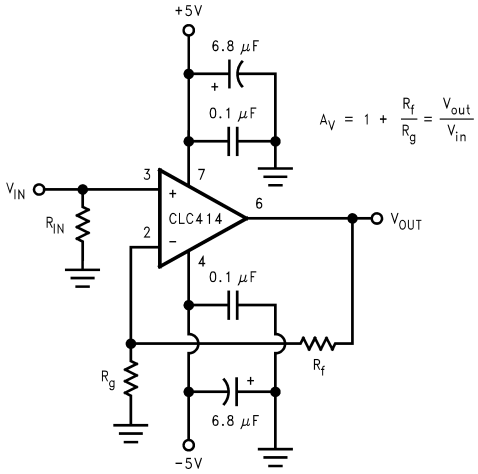


Figure 19. Recommended Non-Inverting Gain Circuit

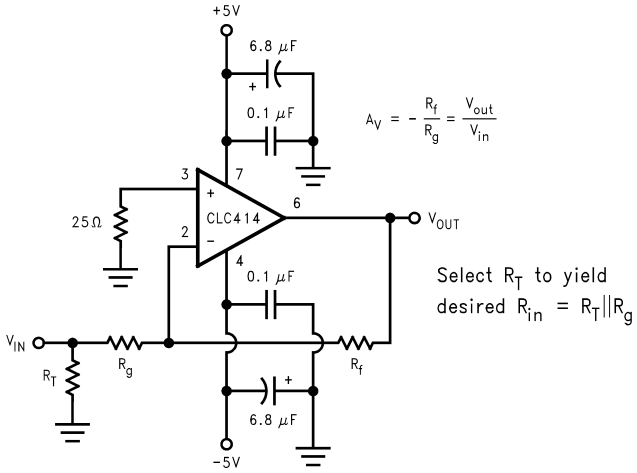


Figure 20. Recommended Inverting Gain Circuit

Feedback Resistor

The CLC414 achieves its exceptional AC performance while requiring very low quiescent power by using the current feedback topology and an internal slew rate enhancement circuit. The loop gain and frequency response for a current feedback op amp is predominantly set by the feedback resistor value. The CLC414 is optimized for a gain of +6 to use a 500Ω feedback resistor **(use a 1kΩ R_f for maximally flat response at a gain of +2).** Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 provides a more detailed discussion of choosing a feedback resistor. The equations found in this application note are to be considered a starting point for the determination of R_f at any gain. The value of input impedance of the CLC414 is approximately 250Ω. These equations do not account for parasitic capacitance at the inverting input nor across R_f. The plot found below entitled Figure 21 offers values of R_f which will optimize the frequency response of the CLC414 over its ±1 to ±10 gain range. Unlike voltage feedback, current feedback op amps require a non-zero R_f for unity gain followers.

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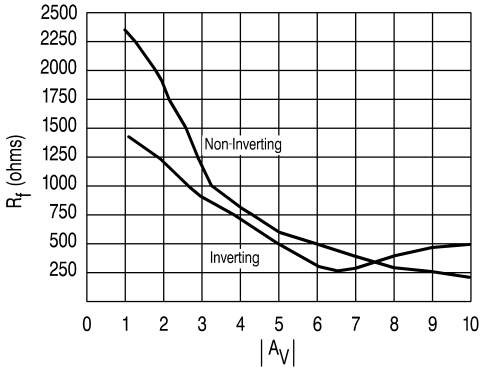


Figure 21. Recommended R_f vs. Gain

Unused Amplifiers

It is recommended that any unused amplifiers in the quad package be connected as unity gain followers (R_f = 500Ω) with the non-inverting input tied to ground through a 50Ω resistor.

Slew Rate and Harmonic Distortion

Please see the application information for the CLC406.

Differential Gain and Phase

Differential gain and phase performance specifications are common to composite video distribution applications. These specifications refer to the change in small signal gain and phase of the color subcarrier frequency (4.43MHz for PAL composite video) as the amplifier output is swept over a range of DC voltages. Application Note OA-08 provides an additional discussion of differential gain and phase measurements.

Non-inverting Source Impedance

For best operation, the DC source impedance looking out of the non-inverting input should be less than 3kΩ but greater than 20Ω. Parasitic self oscillations may occur in the input transistors if the DC source impedance is out of this range. This impedance also acts as the gain for the non-inverting input bias and noise currents and therefore can become troublesome for high values of DC source impedance. The inverting configuration of Figure 20 shows a 25Ω resistor to ground on the non-inverting input which insures stability but does not provide bias current cancellation. The input bias currents are unrelated for a current feedback amplifier which eliminates the need for source impedance matching to achieve bias current cancellation.

DC Accuracy and Noise Calculation

Please refer to the application information for the CLC406.

Crosstalk

In any multi-channel integrated circuit there is an undesirable tendency for the signal in one channel to couple with and reproduce itself in the output of another channel. This effect is referred to as crosstalk. Crosstalk is expressed as channel separation or channel isolation which indicates the magnitude of this undesirable effect. This effect is measured by driving one or more channels and observing the output of the other undriven channel(s). The CLC414 plot page offers two different graphs detailing the effect of crosstalk over frequency. One plot entitled " All-Hostile Crosstalk Isolation" graphs all-hostile input-referred crosstalk. All-hostile crosstalk refers to the condition where three channels are driven simultaneously while observing the output of the undriven fourth channel. Input-referred implies that crosstalk is directly affected by gain and therefore a higher gain increases the crosstalk effect by a factor equal to that gain setting. The plot entitled " Most Susceptible Channel-to-Channel Pulse Coupling" describes the effect of crosstalk when one channel is driven with a $2V_{PP}$ pulse while the output of the most effected channel is observed.

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Printed Circuit Layout

As with any high speed component, a careful attention to the board layout is necessary for optimum performance. Of particular importance is the careful control of parasitic capacitances on the output pin. As the output impedance plot shows, the closed loop output for the CLC414 eventually becomes inductive as the loop gain rolls off with increasing frequency. Direct capacitive loading on the output pin can quickly lead to peaking in the frequency response, overshoot in the pulse response, ringing or even sustained oscillations. The " Settling Time vs. Capacitive Load" plot should be used as a starting point for the selection of a series output resistor when a capacitive load must be driven. A quad amplifier will require careful attention to signal routing in order to minimize the effects of crosstalk. Signal coupling through the power supplies can be reduced with bypass capacitors placed close to the device supply pins.

Evaluation Board

Evaluation PC boards (part number 730024 for through-hole and 730031 for SOIC) for the CLC414 are available.

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REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	10

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