4-Channel Low-Power PAL/NTSC/SECAM Video Decoder With Independent Scalers and Fast Lock

Check for Samples: TVP5154A

1 Introduction

1.1 Features

- Four Separate Video Decoder Channels With Features for Each Channel:
  - Accept NTSC (J, M, 4.43), PAL (B, D, G, H, I, M, N, Nc), and SECAM (B, D, G, K, K1, L) Video
  - Support ITU-R BT.601 Standard Sampling
  - High-Speed 9-Bit Analog-to-Digital Converter (ADC)
  - Two Composite Inputs or One S-Video Input (for Each Channel)
  - Fully Differential CMOS Analog Preprocessing Channels With Clamping and Automatic Gain Control (AGC) for Best Signal to Noise (SNR) Performance
  - Brightness, Contrast, Saturation, Hue, and Sharpness Control Through Inter-Integrated Circuit (I^2C)
  - Complementary 4-Line (3-H Delay) Adaptive Comb Filters for Both Cross-Luminance and Cross-Chrominance Noise Reduction
  - Patented Architecture for Locking to Weak, Noisy, or Unstable Signals
- Four Independent Polymorphic Scalers
- Single or Concurrent Scaled and Unscaled Outputs Via Dual Clocking Data, Interleaved 54-MHz Data or Single 27-MHz Clock
- Scaled/Unscaled Image Toggle Mode Gives Variable Field Rate for Both Scaled and Unscaled Video
- Low Power Consumption: 700 mW Typical
- 128-Pin Thin Quad Flat Pack (TQFP) Package
- Single 14.31818-MHz Crystal for All Standards and All Channels
- Internal Phase-Locked Loop (PLL) for Line-Locked Clock (Separate for Each Channel) and Sampling
- Sub-Carrier Genlock Output for Synchronizing Color Sub-Carrier of External Encoder
- Standard Programmable Video Output Format
  - ITU-R BT.656, 8-Bit 4:2:2 With Embedded Syncs
  - 8-Bit 4:2:2 With Discrete Syncs
- Advanced Programmable Video Output Formats
  - 2× Over-Sampled Raw Vertical Blanking Interval (VBI) Data During Active Video
  - Sliced VBI Data During Horizontal Blanking or Active Video
- VBI Modes Supported:
  - Teletext (NABTS, WST)
  - Closed-Caption Decode With FIFO, and Extended Data Services (EDS)
  - Wide Screen Signaling (WSS), Video Program System (VPS), Copy Generation Management System (CGMS), Vertical Interval Time Code (VITC)
  - Gemstar 1×/2× Electronic Program Guide Compatible Mode
  - Custom Configuration Mode Allows User to Program the Slice Engine for Unique VBI Data Signals
- Improved Fast Lock Mode Can Be Used When Input Video Standard Is Known and Signals on Switching Channels Are Clean
- Four Possible I^2C Addresses Allowing 16 Decoder Channels on a Single I^2C Bus
- Available in Commercial (0°C to 70°C) and Industrial (–40°C to 85°C) Temperature Ranges

1.2 Description

The TVP5154A device is a 4-channel, low-power, NTSC/PAL/SECAM video decoder. Available in a space-saving 128-pin thin quad flat pack (TQFP) package, each channel of the TVP5154A decoder converts NTSC, PAL, or SECAM video signals to 8-bit ITU-R BT.656 format. Discrete syncs are also

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available. All four channels of the TVP5154A are independently controllable. The decoders share one crystal for all channels and for all supported standards. The TVP5154A can be programmed using a single inter-integrated circuit (I^2C) serial interface. The decoder uses a 1.8-V supply for its analog and digital supplies, and a 3.3-V supply for its I/O. The optimized architecture of the TVP5154A decoder allows for low power consumption. The decoder consumes less than 720 mW of power in typical operation.

Each channel of the TVP5154A is an independent video decoder with a programmable polymorphic scaler. Each channel converts baseband analog video into digital YCbCr 4:2:2 component video, which can then be scaled down to any resolution to 1/256 vertical and 15-bit horizontal in 2-pixel decrements. Composite and S-video inputs are supported. Each channel includes one 9-bit analog-to-digital converter (ADC) with 2× sampling. Sampling is ITU-R BT.601 (27.0) MHz, generated from a single 14.31818-MHz crystal or oscillator input) and is line locked. The output formats can be 8-bit 4:2:2 with discrete syncs or 8-bit ITU-R BT.656 with embedded synchronization.

The TVP5154A utilizes Texas Instruments patented technology for locking to weak, noisy, or unstable signals. A real-time control (RTC) output is generated for each channel for synchronizing downstream video encoders.

Complementary 4-line adaptive comb filtering is available per channel for both the luma and chroma data paths to reduce both cross-luma and cross-chroma artifacts. A chroma trap filter also is available.

An improved fast lock mode can be used when the input video standard is known and the signals on the switching channels are clean. Note, switching from snow and/or noisy channels to good channels takes longer. In fast lock mode, video lock is achieved in three fields or less.

Video characteristics, including hue, contrast, brightness, saturation, and sharpness, may be independently programmed for each channel using the industry standard I^2C serial interface. The TVP5154A generates synchronization, blanking, lock, and clock signals in addition to digital video outputs for each channel. The TVP5154A includes methods for advanced vertical blanking interval (VBI) data retrieval. The VBI data processor slices, parses, and performs error checking on teletext, closed caption, and other data in several formats.

I^2C commands can be sent to one or more decoder cores simultaneously, reducing the amount of I^2C activity necessary to configure each core. A register controls which decoder core receives I^2C commands, and can be configured such that all four decoders receive commands at the same time.

The main blocks for each of the channels of the TVP5154A decoder include:

- Robust sync detector
- ADC with analog processor
- Y/C separation using 4-line adaptive comb filter
- Independent, concurrent scaler outputs
- Chrominance processor
- Luminance processor
- Video clock/timing processor and power-down control
- I^2C interface
- VBI data processor

1.3 Applications

- **Security/Surveillance Digital Video Recorders/Servers and PCI Products**
- **Automotive Infotainment Video Hub**
- **Large-Format Video Wall Displays**
- **Games Systems**

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1.4 Related Products

- TVP5150AM1
- TVP5151
- TVP5146M2
- TVP5147M1
- TVP5158

1.5 Trademarks

PowerPAD is a trademark of Texas Instruments.

Macrovision is a trademark of Macrovision Corporation.

Gemstar is a trademark of Gemstar-TV Guide International.

Other trademarks are the property of their respective owners.

1.6 Document Conventions

Throughout this data manual, several conventions are used to convey information. These conventions are:

- To identify a binary number or field, a lower case b follows the numbers. For example: 000b is a 3-bit binary field.
- To identify a hexadecimal number or field, a lower case h follows the numbers. For example: 8AFh is a 12-bit hexadecimal field.
- All other numbers that appear in this document that do not have either a b or h following the number are assumed to be decimal format.
- If the signal or terminal name has a bar above the name (for example, RESETB), then this indicates the logical NOT function. When asserted, this signal is a logic low, 0, or 0b.
- RSVD indicates that the referenced item is reserved.

1.7 Ordering Information

T_A	PACKAGED DEVICES(1)	PACKAGE OPTION
	128-PIN TQFP PowerPAD™	
0°C to 70°C	TVP5154APNP	Tray
	TVP5154APNPR	Tape and reel
–40°C to 85°C	TVP5154AIPNP	Tray
	TVP5154AIPNPR	Tape and reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

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2 Device Details

2.1 Functional Block Diagram

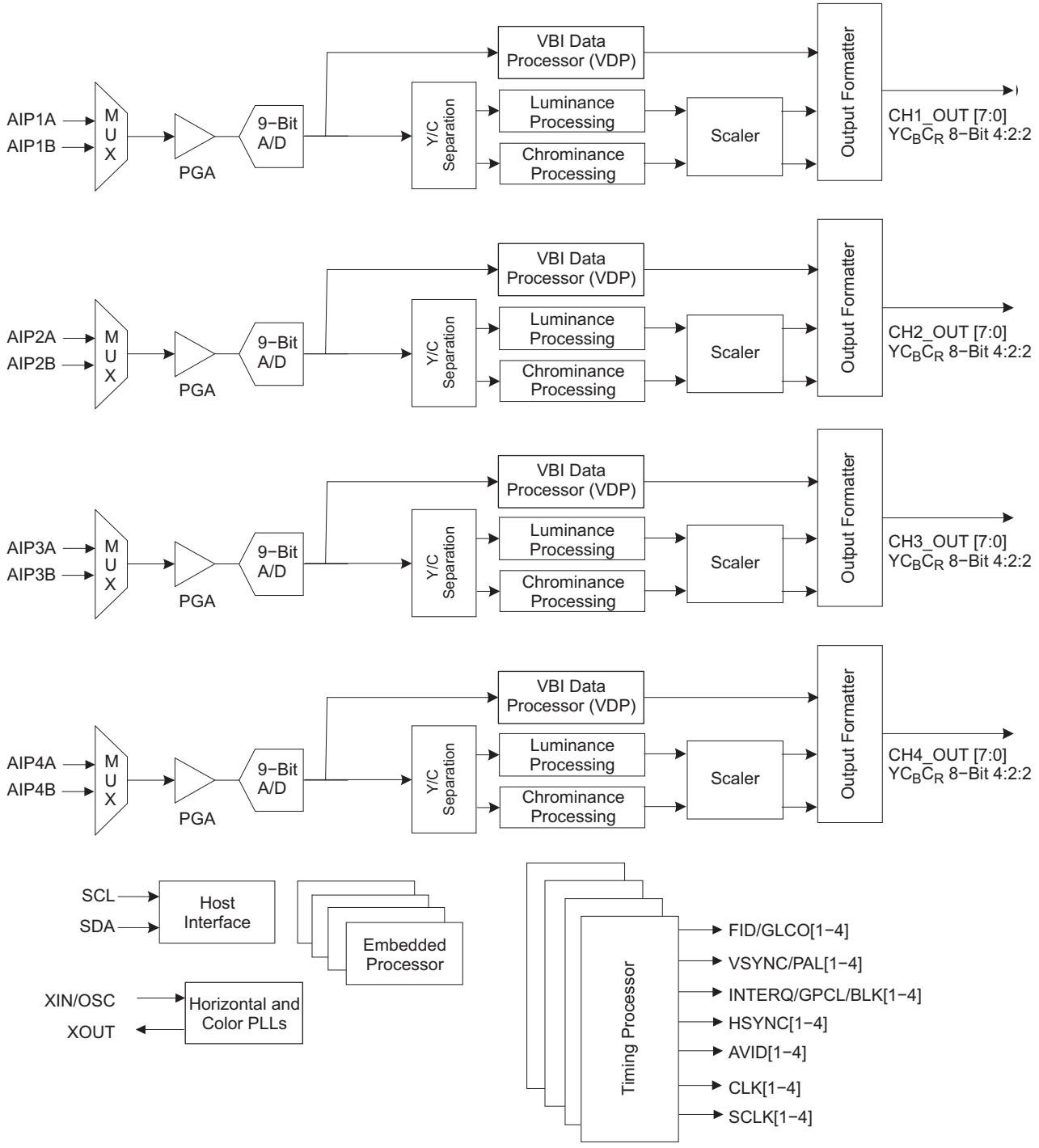

Figure 2-1. Functional Block Diagram

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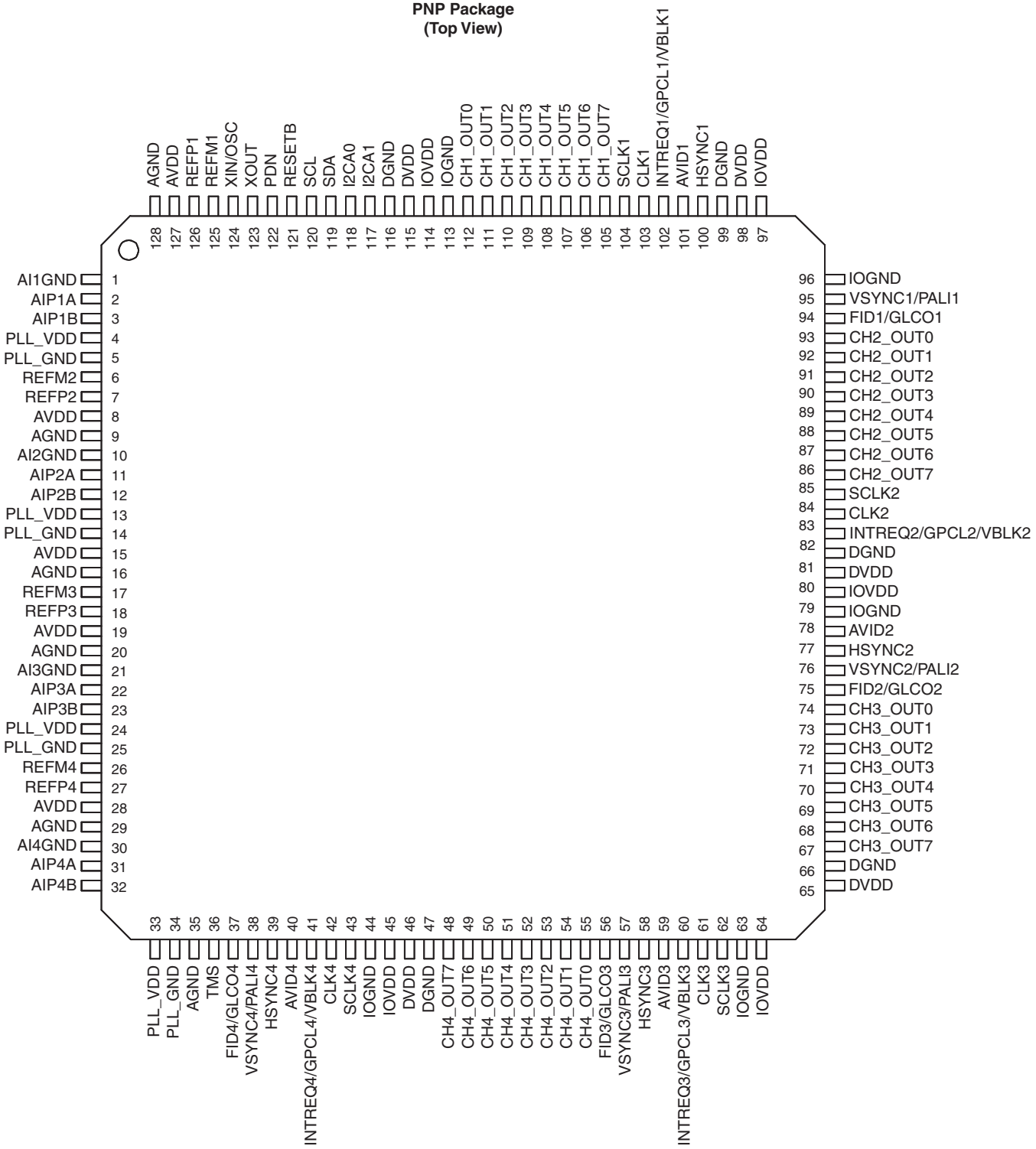
2.2 Terminal Diagram

PNP Package
(Top View)



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2.3 Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
Analog Section			
AIP1A AIP1B	2 3	I	Analog inputs for Channel 1. Connect to the video analog input via a 0.1-µF capacitor. The maximum input range is 0–0.75 V_{PP}, and may require an attenuator to reduce the input amplitude to the desired level. If not used, connect to AGND via a 0.1-µF capacitor. See the schematic in Section 10.
AIP2A AIP2B	11 12	I	Analog inputs for Channel 2. Connect to the video analog input via a 0.1-µF capacitor. The maximum input range is 0-0.75 V_{PP}, and may require an attenuator to reduce the input amplitude to the desired level. If not used, connect to AGND via a 0.1-µF capacitor. See the schematic in Section 10.
AIP3A AIP3B	22 23	I	Analog inputs for Channel 3. Connect to the video analog input via a 0.1-µF capacitor. The maximum input range is 0-0.75 V_{PP}, and may require an attenuator to reduce the input amplitude to the desired level. If not used, connect to AGND via a 0.1-µF capacitor. See the schematic in Section 10.
AIP4A AIP4B	31 32	I	Analog inputs for Channel 4. Connect to the video analog input via a 0.1-µF capacitor. The maximum input range is 0-0.75 V_{PP}, and may require an attenuator to reduce the input amplitude to the desired level. If not used, connect to AGND via a 0.1-µF capacitor. See the schematic in Section 10.
AVDD	8, 15, 19, 28, 127	P	Analog power supply. Connect to 1.8-V analog supply.
AGND	9, 16, 20, 29, 35, 128	G	Analog power supply return. Connect to analog ground.
AIxGND	1, 10, 21, 30	G	Analog input signal return. Connect to analog ground.
PLL_GND	5, 14, 25, 34	G	PLL power supply return. Connect to analog ground.
PLL_VDD	4, 13, 24, 33	P	PLL power supply. Connect to 1.8-V analog supply.
REFMx	6, 17, 26, 125	I	Reference supply decoupling . Connect to analog ground through a 1-µF capacitor. Connect to REFPx through a 1-µF capacitor.
REFPx	7, 18, 27, 126	I	Reference supply decoupling . Connect to analog ground through a 1-µF capacitor. Connect to REFMx through a 1-µF capacitor.
Digital Section			
DGND	47, 66, 82, 99, 116	G	Digital power supply return. Connect to digital ground
DVDD	46, 65, 81, 98, 115	P	Digital power supply. Connect to 1.8-V digital supply.
IOGND	44, 63, 79, 96, 113	G	I/O power supply return. Connect to digital ground.
IOVDD	45, 64, 80, 97, 114	P	I/O power supply. Connect to 3.3-V digital supply
FID1/GLCO1 FID2/GLCO2 FID3/GLCO3 FID4/GLCO4	94 75 56 37	O	1. FID: Odd/even field indicator or vertical lock indicator. For the odd/even indicator, a 1 indicates the odd field. 2. GLCO: This serial output carries color PLL information. A slave device can decode the information to allow chroma frequency control from the TVP5154A decoder. Data is transmitted at the CLK rate in Genlock mode.
AVID1 AVID2 AVID3 AVID4	101 78 59 40	O	Active video indicator. This signal is high during the horizontal active time of the video output.
INTREQ1/GPCL1/VBLK1 INTREQ2/GPCL2/VBLK2 INTREQ3/GPCL3/VBLK3 INTREQ4/GPCL4/VBLK4	102 83 60 41	I/O	1. Interrupt request : Open drain when active low. 2. GPCL: General-purpose output. In this mode, the state of GPCL is directly programmed via I^2C. 3. VBLK: Vertical blank output. In this mode, the GPCL terminal is used to indicate the VBI of the output video. The beginning and end times of this signal are programmable via I^2C.

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TERMINAL		I/O	DESCRIPTION
NAME	NO.		
HSYNC1 HSYNC2 HSYNC3 HSYNC4	100 77 58 39	O	Horizontal synchronization
VSYNC1/PALI1 VSYNC2/PALI2 VSYNC3/PALI3 VSYNC4/PALI4	95 76 57 38	O	1. VSYNC: Vertical synchronization 2. PALI: PAL line indicator or horizontal lock indicator. For the PAL line indicator, a 1 indicates a noninverted line, and a 0 indicates an inverted line.
PDN	122	I	Power down (active low). A 0 on this pin puts the decoder in standby mode. PDN preserves the value of the registers.
RESETB	121	I	Active-low reset. RESETB can be used only when PDN = 1. When RESETB is pulled low, it resets all the registers and restarts the internal microprocessor.
SCL	120	I/O	I^2C serial clock (open drain)
SDA	119	I/O	I^2C serial data (open drain)
I2CA0	118	I	During power-on reset, this pin is sampled along with pin 117 (I2CA1) to determine the I^2C address the device is configured to. A 10-kΩ resistor should pull this either high (to IOVDD) or low to select different I^2C device addresses.
I2CA1	117	I	During power-on reset, this pin is sampled along with pin 118 (I2CA0) to determine the I^2C address the device is configured to. A 10-kΩ resistor should pull this either high (to IOVDD) or low to select different I^2C device addresses.
CLK1 CLK2 CLK3 CLK4	103 84 61 42	O	Unscaled system data clock at either 27 MHz or 54 MHz
SCLK1 SCLK2 SCLK3 SCLK4	104 85 62 43	O	Scaled system data clock at 27 MHz. This signal can be used to qualify scaled/unscaled data when the unscaled system data clock is set to 54 MHz.
XIN/OSC XOUT	124 123	I O	External clock reference. The user may connect XIN to an oscillator or to one terminal of a crystal oscillator. The user may connect XOUT to the other terminal of the crystal oscillator or not connect XOUT at all. One single 14.31818-MHz crystal or oscillator is needed for ITU-R BT.601 sampling, for all supported standards.
CH1_OUT[7:0]	105–112	O	Decoded ITU-R BT.656 output/YCbCr 4:2:2 output with discrete sync for channel 1
CH2_OUT[7:0]	86–93	O	Decoded ITU-R BT.656 output/YCbCr 4:2:2 output with discrete sync for channel 2
CH3_OUT[7:0]	67–74	O	Decoded ITU-R BT.656 output/YCbCr 4:2:2 output with discrete sync for channel 3
CH4_OUT[7:0]	48–55	O	Decoded ITU-R BT.656 output/YCbCr 4:2:2 output with discrete sync for channel 4
TMS	36	I	Test-mode select. This pin should be connected to digital ground for correct device operation.

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3 Functional Description

3.1 Analog Front End

Each channel of the TVP5154A decoder has an analog input channel that accepts two video inputs, which should be ac coupled through 0.1-µF capacitors. The decoder supports a maximum input voltage range of 0.75 V; therefore, an attenuation of one-half is needed for standard input signals with a peak-to-peak variation of 1.5 V. The maximum parallel termination before the input to the device is 75 Ω. See the schematic in Section 10 for recommended configuration. The two analog input ports can be connected as follows:

- Two selectable composite video inputs or
- One S-video input

An internal clamping circuit restores the ac-coupled video signal to a fixed dc level.

The programmable gain amplifier (PGA) and the automatic gain control (AGC) circuit work together to ensure that the input signal is amplified or attenuated correctly, ensuring the proper input range for the ADC.

When switching CVBS inputs from one input to the other, the AGC settings are internally stored and the previous settings for the new input are restored. This eliminates flashes and dark frames associated with switching between inputs that have different signal amplitudes.

The ADC has nine bits of resolution and runs at a maximum speed of 27 MHz. The clock input for the ADC comes from the PLL.

3.2 Composite Processing Block Diagram

The composite processing block processes NTSC/PAL/SECAM signals into the YCbCr color space. Figure 2-1 shows the basic architecture of this processing block.

Figure 2-1 shows the luminance/chrominance (Y/C) separation process in the TVP5154A decoders. The composite video is multiplied by sub-carrier signals in the quadrature modulator to generate the color difference signals Cb and Cr. Cb and Cr are then low pass (LP) filtered to achieve the desired bandwidth and to reduce crosstalk.

An adaptive 4-line comb filter separates CbCr from Y. Chroma is remodulated through another quadrature modulator and subtracted from the line-delayed composite video to generate luma. Contrast, brightness, hue, saturation, and sharpness (using the peaking filter) are programmable via I^2C.

The Y/C separation is bypassed for S-video input. For S-video, the remodulation path is disabled.

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3.3 Adaptive Comb Filtering

The 4-line comb filter can be selectively bypassed in the luma or chroma path. If the comb filter is bypassed in the luma path, then chroma trap filters are used which are shown in Figure 3-1 and Figure 3-2. TI's patented adaptive 4-line comb filter algorithm reduces artifacts, such as hanging dots at color boundaries, and detects and properly handles false colors in high-frequency luminance images, such as a multiburst pattern or circle pattern.

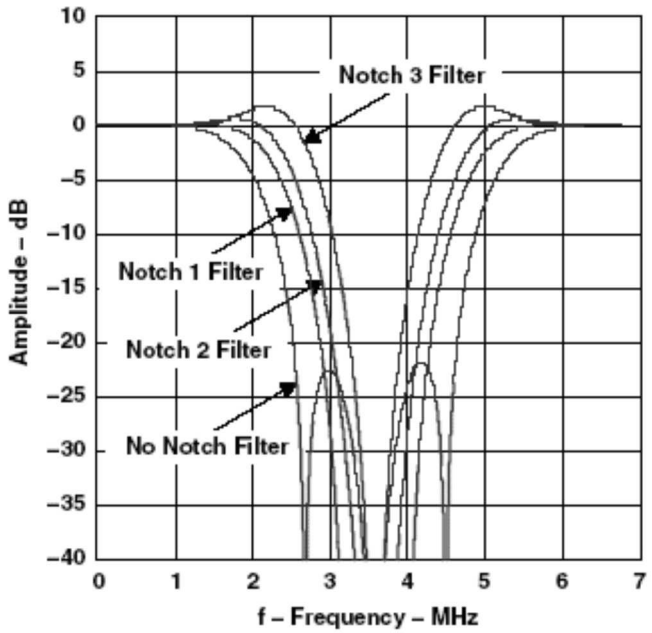

Figure 3-1. Chroma Trap Filter Frequency Response, NTSC ITU-R BT.601 Sampling

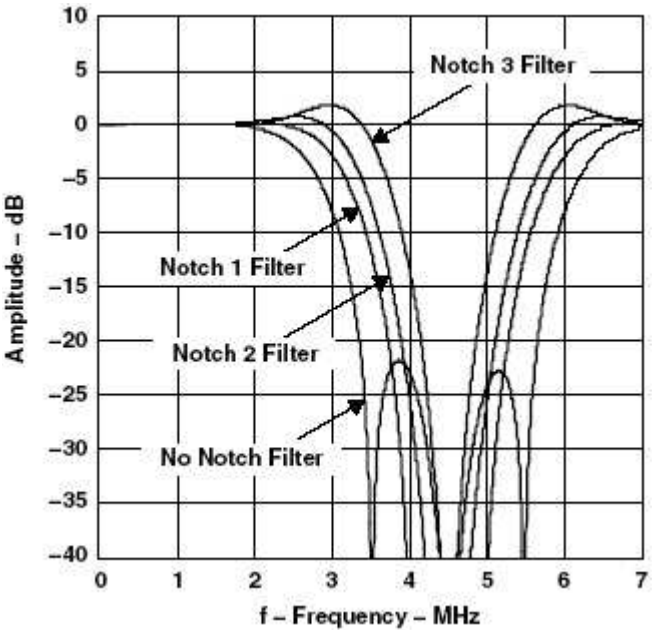

Figure 3-2. Chroma Trap Filter Frequency Response, PAL ITU-R BT.601 Sampling

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3.4 Color Low-Pass Filter

In some applications, it is desirable to limit the Cb/Cr bandwidth to avoid crosstalk. This is especially true in the case of video signals that have asymmetrical Cb/Cr sidebands. The provided color LP filters limit the bandwidth of the Cb/Cr signals. Color LP filters are needed when the comb filtering turns off, due to extreme color transitions in the input image. See Chrominance Control #2 Register (Section 7.2.27), for the response of these filters. The filters have three options that allow three different frequency responses based on the color frequency characteristics of the input video as shown in Figure 3-3.

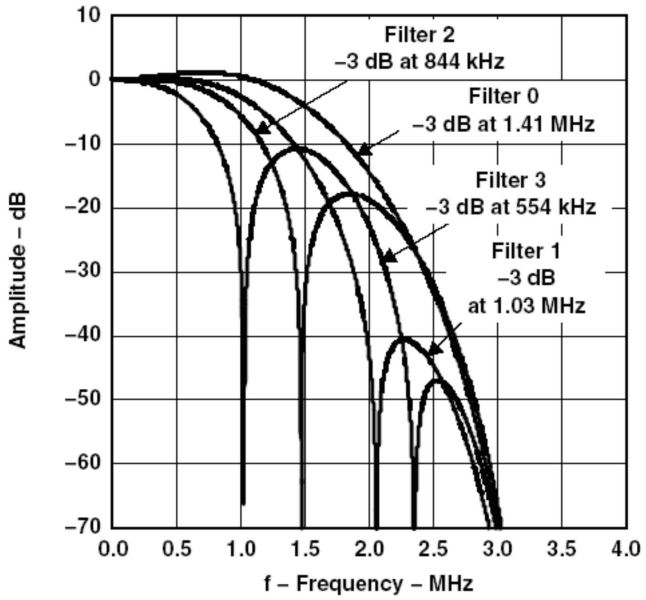

Figure 3-3. Color Low-Pass Filter with Filter Characteristics, NTSC/PAL ITU-R BT.601 Sampling

3.5 Luminance Processing

The luma component is derived from the composite signal by subtracting the remodulated chroma information. A line delay exists in this path to compensate for the line delay in the adaptive comb filter in the color processing chain. The luma information is then fed into the peaking circuit, which enhances the high-frequency components of the signal, thus, improving sharpness.

3.6 Chrominance Processing

For NTSC/PAL formats, the color processing begins with a quadrature demodulator. The Cb/Cr signals then pass through the gain control stage for chroma saturation adjustment. An adaptive comb filter is applied to the demodulated signals to separate chrominance and eliminate cross-chrominance artifacts. An automatic color-killer circuit is also included in this block. The color killer suppresses the chrominance processing when the burst amplitude falls below a programmable threshold (see I^2C subaddress 06h, Section 7.2.7). The SECAM standard is similar to PAL except for the modulation of color, which is FM instead of QAM.

3.7 Timing Processor

The timing processor is a combination of hardware and software running in the internal microprocessor that serves to control horizontal lock to the input sync pulse edge, AGC and offset adjustment in the analog front end, and vertical sync detection.

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3.8 VBI Data Processor

The TVP5154A VBI data processor (VDP) slices various data services, such as teletext (WST, NABTS), closed caption (CC), wide screen signaling (WSS), etc. These services are acquired by programming the VDP to enable standards in the VBI. The results are stored in a FIFO and/or registers. The teletext results are stored in a FIFO only. Table 3-1 lists a summary of the types of VBI data supported according to the video standard. It supports ITU-R BT.601 sampling for each.

Table 3-1. Data Types Supported by the VDP

LINE MODE REGISTER (D0h–FCh) BITS [3:0]	NAME	DESCRIPTION
0000b	WST SECAM	Teletext, SECAM
0001b	WST PAL B	Teletext, PAL, System B
0010b	WST PAL C	Teletext, PAL, System C
0011b	WST, NTSC B	Teletext, NTSC, System B
0100b	NABTS, NTSC C	Teletext, NTSC, System C
0101b	NABTS, NTSC D	Teletext, NTSC, System D (Japan)
0110b	CC, PAL	Closed caption PAL
0111b	CC, NTSC	Closed caption NTSC
1000b	WSS/CGMS-A, PAL	Wide-screen signaling/Copy Generation Management System-Analog, PAL
1001b	WSS/CGMS-A, NTSC	Wide-screen signaling/Copy Generation Management System-Analog, NTSC
1010b	VITC, PAL	Vertical interval timecode, PAL
1011b	VITC, NTSC	Vertical interval timecode, NTSC
1100b	VPS, PAL	Video program system, PAL
1101b	Gemstar 2x Custom 1	Electronic program guide
1110b	Reserved	Reserved
1111b	Active Video	Active video/full field

At power up, the host interface is required to program the VDP-configuration RAM (VDP-CRAM) contents with the lookup table (see Section 7.2.69). This is done through port address C3h. Each read from or write to this address auto increments an internal counter to the next RAM location. To access the VDP-CRAM, the line mode registers (D0h–FCh) must be programmed with FFh to avoid a conflict with the internal microprocessor and the VDP in both writing and reading. Full field mode must also be disabled.

Available VBI lines are from line 6 to line 27 of both field 1 and field 2. Each line can be any VBI mode.

Output data is available either through the VBI-FIFO (B0h) or through dedicated registers at 90h–AFh, both of which are available through the I^2C port.

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3.9 VBI FIFO and Ancillary Data in Video Stream

Sliced VBI data can be output as ancillary data in the video stream in the ITU-R BT.656 mode. VBI data is output during the horizontal blanking period following the line from which the data was retrieved. Table 3-2 shows the header format and sequence of the ancillary data inserted into the video stream. This format is also used to store any VBI data into the FIFO. The size of FIFO is 512 bytes. Therefore, the FIFO can store up to 11 lines of teletext data with the NTSC NABTS standard.

Table 3-2. Ancillary Data Format and Sequence

BYTE NO.	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	DESCRIPTION	
0	0	0	0	0	0	0	0	0	Ancillary data preamble	
1	1	1	1	1	1	1	1	1		
2	1	1	1	1	1	1	1	1		
3	NEP	EP	0	1	0	DID2	DID1	DID0	Data ID (DID)	
4	NEP	EP	F5	F4	F3	F2	F1	F0	Secondary data ID (SDID)	
5	NEP	EP	N5	N4	N3	N2	N1	N0	Number of 32 bit data (NN)	
6	Video line # [7:0]								Internal data ID0 (IDID0)	
7	0	0	0	Data error	Match #1	Match #2	Video line # [9:8]		Internal data ID1 (IDID1)	
8	1. Data								Data byte	1st word
9	2. Data								Data byte	
10	3. Data								Data byte	
11	4. Data								Data byte	
⋮	⋮								⋮	
	—1. Data								Data byte	Nth word
	m. Data								Data byte	
	NEP	EP	CS[5:0]						Check sum	
4(N+2)-1	0	0	0	0	0	0	0	0	Fill byte	

EP: Even parity for D0–D5

NEP: Negated even parity

DID: 91h: Sliced data of VBI lines of first field
53h: Sliced data of line 24 to end of first field
55h: Sliced data of VBI lines of second field
97h: Sliced data of line 24 to end of second field

SDID: This field holds the data format taken from the line mode register of the corresponding line.

NN: Number of Dwords beginning with byte 8 through 4(N+2). This value is the number of Dwords where each Dword is 4 bytes.

IDID0: Transaction video line number [7:0]

IDID1: Bit 0/1 = Transaction video line number [9:8]
Bit 2 = Match 2 flag
Bit 3 = Match 1 flag
Bit 4 = 1 if an error was detected in the EDC block. 0 if not.

CS: Sum of D0–D7 of DID through last data byte

Fill byte: Fill bytes make a multiple of four bytes from byte 0 to last fill byte. For teletext modes, byte 8 is the sync pattern byte. Byte 9 is 1. Data (the first data byte).

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3.10 Raw Video Data Output

The TVP5154A decoder can output raw A/D video data at 2× sampling rate for external VBI slicing. This is transmitted as an ancillary data block during the active horizontal portion of the line and during vertical blanking.

3.11 Output Formatter

The output formatter is responsible for generating the output digital video stream. The YCbCr digital output can be programmed as 8-bit 4:2:2 or 8-bit ITU-R BT.656 parallel interface standard. Depending on which output mode is selected, the output for each channel can be unscaled data, scaled data, or both scaled and unscaled data interleaved in various ways.

Table 3-3. Summary of Line Frequencies, Data Rates and Pixel Counts for Different Standards

STANDARDS (ITU-R BT.601)	PIXELS PER LINE	ACTIVE PIXELS PER LINE	LINES PER FRAME	PIXEL FREQUENCY (MHz)	COLOR SUB-CARRIER FREQUENCY (MHz)	HORIZONTAL LINE RATE (kHz)
NTSC-J, M	858	720	525	13.5	3.579545	15.73426
NTSC-4.43	858	720	525	13.5	4.43361875	15.73426
PAL-M	858	720	525	13.5	3.57561149	15.73426
PAL-B, D, G, H, I	864	720	625	13.5	4.43361875	15.625
PAL-N	864	720	625	13.5	4.43361875	15.625
PAL-Nc	864	720	625	13.5	3.58205625	15.625
SECAM	864	720	625	13.5	4.40625/4.25	15.625

3.12 Synchronization Signals

External (discrete) syncs are provided via the following signals:

- VSYNC (vertical sync)
- FID/VLK (field indicator or vertical lock indicator)
- GPCL/VBLK (general-purpose I/O or vertical blanking indicator)
- PALI/HLK (PAL switch indicator or horizontal lock indicator)
- HSYNC (horizontal sync)
- AVID (active video indicator)

VSYNC, FID, PALI, and VBLK are software set and programmable to the CLK pixel count. This allows any possible alignment to the internal pixel count and line count. The default settings for a 525-/625-line video output are shown in Figure 3-4.

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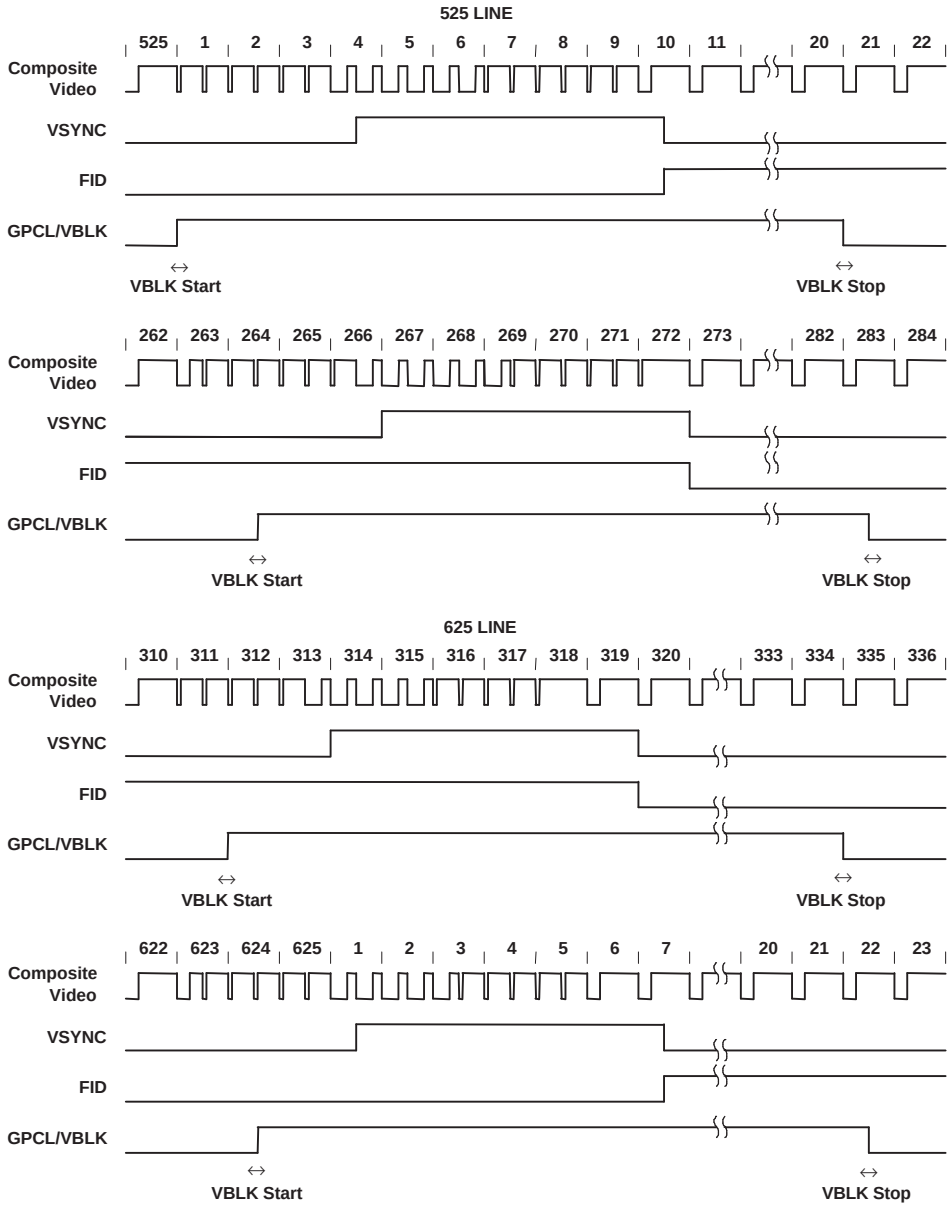
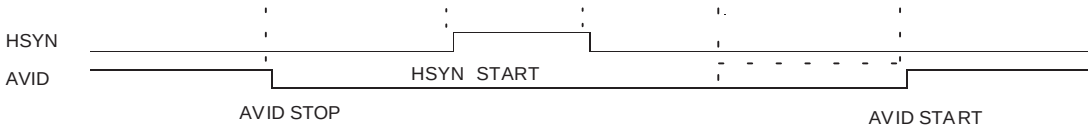


Line numbering conforms to ITU-R BT.470.

Figure 3-4. 8-Bit 4:2:2, Timing With 2× Pixel Clock (CLK) Reference



NOTE: AVID rising edge occurs four CLK cycles early when in ITU-R BT.656 output mode.

Figure 3-5. Horizontal Synchronization Signals

3.13 Active Video (AVID) Cropping

AVID cropping provides a means to decrease the amount of video data output. This is accomplished by horizontally blanking a number of AVID pulses and by vertically blanking a number of lines per frame. The horizontal AVID cropping is controlled using registers 11h and 12h for start pixels MSB and LSB, respectively.

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Registers 13h and 14h provide access to stop pixels MSB and LSB, respectively. The vertical AVID cropping is controlled using the vertical blanking (VBLK) start and stop registers at addresses 18h and 19h. Figure 3-6 shows an AVID application.

AVID cropping can be independently controlled for scaled (registers 25h, 26h, 29h, and 2Ah) and unscaled (registers 11h thru 14h) data streams. AVID start and stop must be changed in multiples of two pixels to ensure correct UV alignment.

Additionally, AVID start and stop can be configured to include the SAV- and EAV-embedded sync signals or to exclude them, and to either include or exclude ITU656 ancillary data.

NOTE

The above settings alter AVID output timing, but the video output data is not forced to black level outside of the AVID interval.

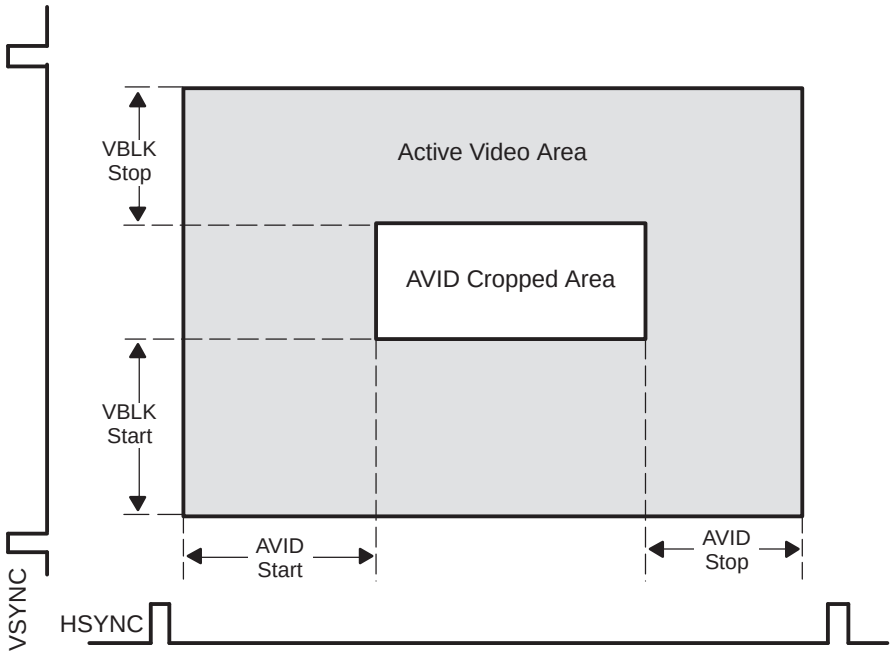

Figure 3-6. AVID Application

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3.14 Embedded Syncs

Standards with embedded syncs insert SAV and EAV codes into the data stream at the beginning and end of horizontal blanking. These codes contain the V and F bits that also define vertical timing. F and V change on EAV. Table 3-4 gives the format of the SAV and EAV codes.

H equals 1 always indicates EAV. H equals 0 always indicates SAV. The alignment of V and F to the line and field counter varies depending on the standard. See ITU-R BT.656 for more information on embedded syncs.

The P bits are protection bits:

P3 = V x or
H P2 = F x or
H P1 = F x or
V P0 = F x or
V x or H

Table 3-4. EAV and SAV Sequence

	8-BIT DATA							
	D7 (MSB)	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Preamble	1	1	1	1	1	1	1	1
Preamble	0	0	0	0	0	0	0	0
Preamble	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0

The status word may be modified to pass information about whether the current data corresponds to scaled or unscaled data. See register 1Fh for more information.

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3.15 Clock and Data Control

Figure 3-7 shows a logical schematic of the data and clock control signals.

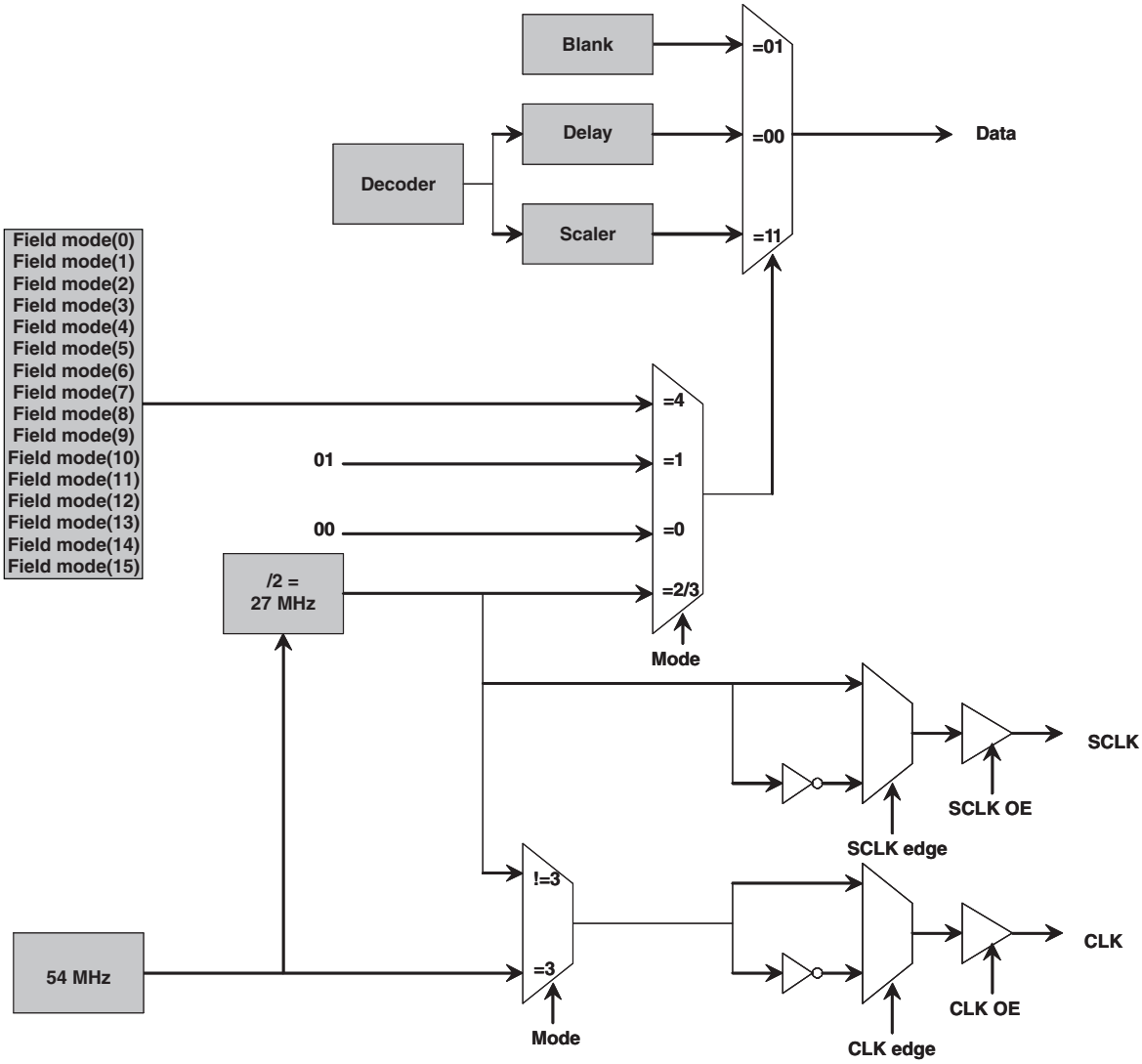

Figure 3-7. Clock and Data Control

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4 I²C Host Interface

The I²C standard consists of two signals, serial input/output data line (SDA) and input/output clock line (SCL), which carry information between the devices connected to the bus. The input pins I2CA0 and I2CA1 are used to select the slave address to which the device responds. Although the I²C system can be multimastered, the TVP5154A decoder functions as a slave device only.

Both SDA and SCL must be connected to IOVDD via pullup resistors. When the bus is free, both lines are high. The slave address select terminals (I2CA0 and I2CA1) enable the use of four TVP5154A decoders on the same I²C bus. At the trailing edge of reset, the status of the I2CA0 and I2CA1 lines are sampled to determine the device address used. Table 4-1 summarizes the terminal functions of the I²C-mode host interface. Table 4-2 shows the device address selection options.

Table 4-1. I²C Terminal Description

SIGNAL	TYPE	DESCRIPTION
I2CA0	I	Slave address selection
I2CA1	I	Slave address selection
SCL	I/O (open drain)	Input/output clock line
SDA	I/O (open drain)	Input/output data line

Table 4-2. I²C Host Interface Device Addresses

A6	A5	A4	A3	A2	A1 (I2CA1)	A0 (I2CA0)	R/W	HEX
1	0	1	1	1	0	0	1/0	B9/B8
1	0	1	1	1	0	1	1/0	BB/BA
1	0	1	1	1	1	0	1/0	BD/BC
1	0	1	1	1	1	1	1/0	BF/BE

Data transfer rate on the bus is up to 400 kbit/s. The number of interfaces connected to the bus is dependent on the bus capacitance limit of 400 pF. The data on the SDA line must be stable during the high period of the SCL, except for start and stop conditions. The high or low state of the data line can only change with the clock signal on the SCL line being low. A high-to-low transition on the SDA line while the SCL is high indicates an I²C start condition. A low-to-high transition on the SDA line while the SCL is high indicates an I²C stop condition.

Every byte placed on the SDA must be eight bits long. The number of bytes that can be transferred is unrestricted. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the I²C master.

To simplify programming of each of the four decoder channels, a single I²C write transaction can be transmitted to any one or more of the four cores in parallel. This reduces the time required to download firmware or to configure the device when all channels are to be configured in the same manner. It also enables the addresses for all registers to be common across all decoders.

I²C sub-address 0xFE contains four bits, with each bit corresponding to one of the decoder cores. If this bit is set, I²C write transactions are sent to the corresponding decoder core. If the bit is 0, the corresponding decoder does not receive the I²C write transactions.

I²C sub-address 0xFF contains four bits, with each bit corresponding to one of the decoder cores. If this bit is set, I²C read transactions are sent to the corresponding decoder core. Note, only one of the bits in this register should be set at a given time, ensuring that only one decoder core is accessed at a time for read operations. If more than one bit is set, the lowest set bit number corresponds to the core that responds to the read transaction.

Note that, when register 0xFE is written to with any value, register 0xFF is set to 0x00. Likewise, when register 0xFF is written to with any value, register 0xFE is set to 0x00.

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4.1 I²C Write Operation

Data transfers occur utilizing the following illustrated formats.

An I²C master initiates a write operation to the TVP5154A decoder by generating a start condition (S) followed by the TVP5154A I²C address (as shown below), in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the TVP5154A decoder, the master presents the sub-address of the register, or the first of a block of registers it wants to write, followed by one or more bytes of data, MSB first. The TVP5154A decoder acknowledges each byte after completion of each transfer. The I²C master terminates the write operation by generating a stop condition (P).

Step 1	**0**
I²C start (master)	S

Step 2	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C general address (master)	1	0	1	1	1	0	X	0

Step 3	**9**
I²C acknowledge (slave)	A

Step 4	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C write register address (master)	addr	addr	addr	addr	addr	addr	addr	addr

Step 5	**9**
I²C acknowledge (slave)	A

Step 6	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C write data (master)	Data	Data	Data	Data	Data	Data	Data	Data

Step 7 (1)	**9**
I²C acknowledge (slave)	A

Step 8	**0**
I²C stop (master)	P

(1) Repeat steps 6 and 7 until all data have been written.

4.2 I²C Read Operation

The read operation consists of two phases. The first phase is the address phase. In this phase, an I²C master initiates a write operation to the TVP5154A decoder by generating a start condition (S) followed by the TVP5154A I²C address, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving acknowledges from the TVP5154A decoder, the master presents the sub-address of the register or the first of a block of registers it wants to read. After the cycle is acknowledged, the master terminates the cycle immediately by generating a stop condition (P).

The second phase is the data phase. In this phase, an I²C master initiates a read operation to the TVP5154A decoder by generating a start condition followed by the TVP5154A I²C address (as shown below for a read operation), in MSB first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from the TVP5154A decoder, the I²C master receives one or more bytes of data from the TVP5154A decoder. The I²C master acknowledges the transfer at the end of each byte. After the last data byte desired has been transferred from the TVP5154A decoder to the master, the master generates a not acknowledge followed by a stop.

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Read Phase 1

Step 1	0
I²C start (master)	S

Step 2	7	6	5	4	3	2	1	0
I²C general address (master)	1	0	1	1	1	0	X	0

Step 3	9
I²C acknowledge (slave)	A

Step 4	7	6	5	4	3	2	1	0
I²C read register address (master)	addr	addr	addr	addr	addr	addr	addr	addr

Step 5	9
I²C acknowledge (slave)	A

Step 6	0
I²C stop (master)	P

Read Phase 2

Step 7	0
I²C start (master)	S

Step 8	7	6	5	4	3	2	1	0
I²C general address (master)	1	0	1	1	1	0	X	1

Step 9	9
I²C acknowledge (slave)	A

Step 10	7	6	5	4	3	2	1	0
I²C read data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

Step 11(1)	9
I²C not acknowledge (master)	A

Step 12	0
I²C stop (master)	P

(1) Repeat steps 10 and 11 for all bytes read. Master does not acknowledge the last read data received.

4.2.1 I²C Timing Requirements

The TVP5154A decoder requires delays in the I²C accesses to accommodate its internal processor's timing. In accordance with I²C specifications, the TVP5154A decoder holds the I²C clock line (SCL) low to indicate the wait period to the I²C master. If the I²C master is not designed to check for the I²C clock line held-low condition, the maximum delays must always be inserted where required. These delays are of variable length; maximum delays are indicated in the following diagram:

Table 4-3. I²C Timing

Start	Slave address (B8h)	Ack	Subaddress	Ack	Data (XXh)	Ack	Wait 128 µs(1)	Stop

(1) If the SCL pin is not monitored by the master to enable pausing, a delay of 128 µs should be inserted between transactions for registers 00h through 8Fh.

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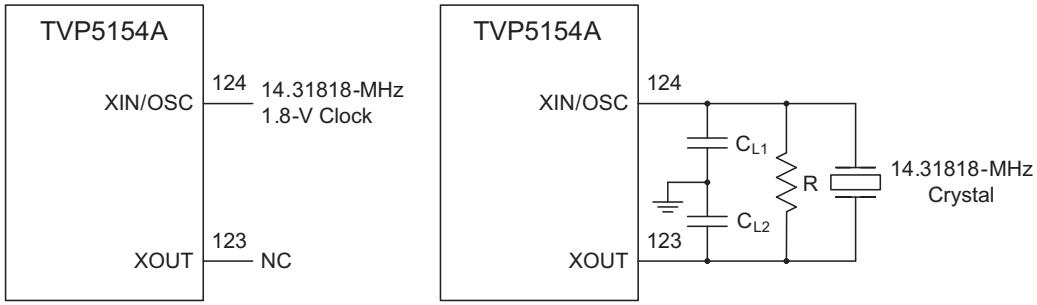
5 Clock Circuits

An internal line-locked PLL generates the system and pixel clocks. A 14.31818-MHz clock is required to drive the PLL. This may be input to the TVP5154A decoder on terminal 124 (XIN), or a crystal of 14.31818-MHz fundamental resonant frequency may be connected across terminals 123 and 124 (XIN and XOUT). Figure 5-1 shows the reference clock configurations. For the example crystal circuit shown (a parallel-resonant crystal with 14.31818-MHz fundamental frequency), the external capacitors must have the following relationship:

$$C_{L1} = C_{L2} = 2C_L - C_{STRAY}$$

where C_{STRAY} is the terminal capacitance with respect to ground and C_L is the crystal load capacitance specified by the crystal manufacturer. Figure 5-1 shows the reference clock configurations.



NOTE: The resistor (R) in parallel with the crystal is recommended to support a wide range of crystal types. A 100-kΩ resistor may be used for most crystal types.

Figure 5-1. Clock and Crystal Connectivity

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6 Genlock Control and RTC

A Genlock control (GLCO) function is provided to support a standard video encoder to synchronize its internal color oscillator for properly reproduced color with unstable timebase sources like VCRs.

The frequency control word of the internal color subcarrier digital control oscillator (DTO) and the subcarrier phase reset bit are transmitted via the GLCO terminal. The frequency control word is a 23-bit binary number. The frequency of the DTO can be calculated from the following equation:

$$F_{dto} = \frac{F_{ctrl}}{2^{23}} \times F_{clk} \quad (1)$$

where F_{dto} is the frequency of the DTO, F_{ctrl} is the 23–bit DTO frequency control, and F_{clk} is the frequency of the CLK.

6.1 TVP5154A Genlock Control Interface

A write of 1 to bit 4 of the chrominance control register at I^2C subaddress 1Ah causes the subcarrier DTO phase reset bit to be sent on the next scan line on GLCO. The active-low reset bit occurs seven CLKs after the transmission of the last bit of DCO frequency control. Upon the transmission of the reset bit, the phase of the TVP5154A internal subcarrier DCO is reset to zero.

A Genlock slave device can be connected to the GLCO terminal and uses the information on GLCO to synchronize its internal color phase DCO to achieve clean line and color lock.

6.2 RTC Mode

Figure 6-1 shows the timing diagram of the RTC mode. Clock rate for the RTC mode is four times slower than the GLCO clock rate. For PLL frequency control, the upper 22 bits are used. Each frequency control bit is two clock cycles long. The active-low reset bit occurs six CLKs after the transmission of the last bit of PLL frequency control.

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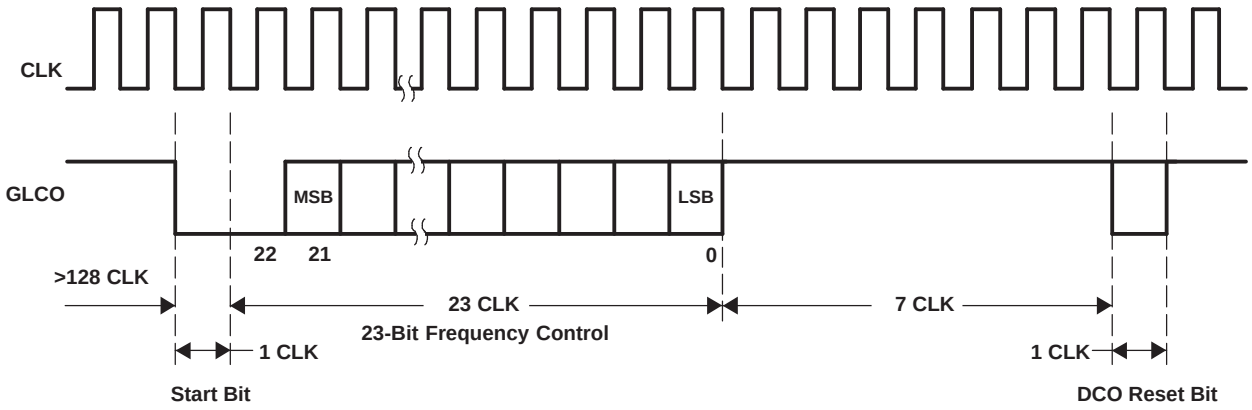

GLCO Timing

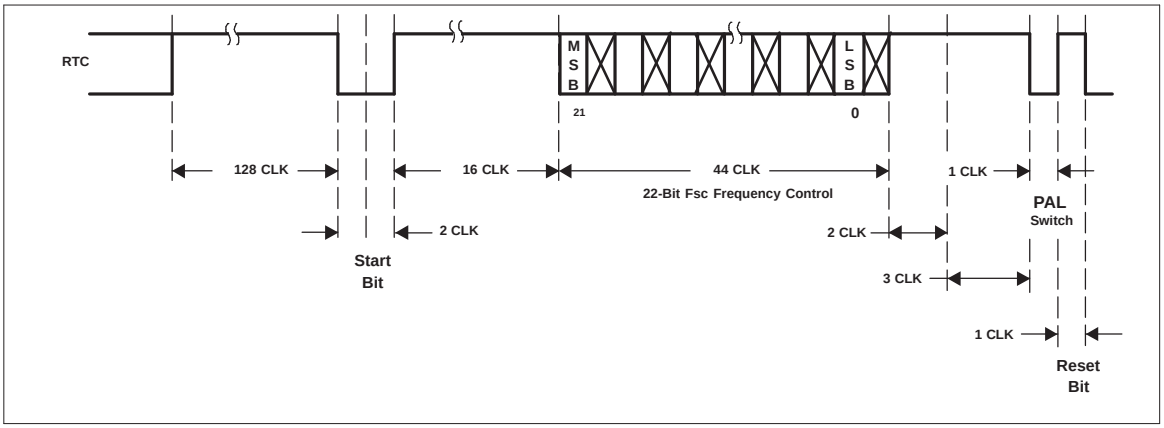

Figure 6-1. RTC Timing

6.3 Reset and Power Down

The RESETB and PDN terminals work together to put the TVP5154A decoder into one of the two modes. Table 6-1 shows the configuration.

After power-up, the device is in an unknown state with its outputs undefined, until it receives a RESETB signal as depicted in Figure 6-2. After RESETB is released, the data (CHn_OUT[7:0]), sync (HSYNCn, VSYNCn/PALIn), and clock (CLKn, SCLKn) outputs are Hi-Z until the chip is initialized and the outputs are activated.

NOTE

I2C SCL and SDA signals must not change state until the TVP5154A reset sequence has been completed.

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Table 6-1. Reset and Power-Down Modes

PDN	RESETB	CONFIGURATION
0	0	Reserved (unknown state)
0	1	Powers down the decoder
1	0	Resets the decoder
1	1	Normal operation

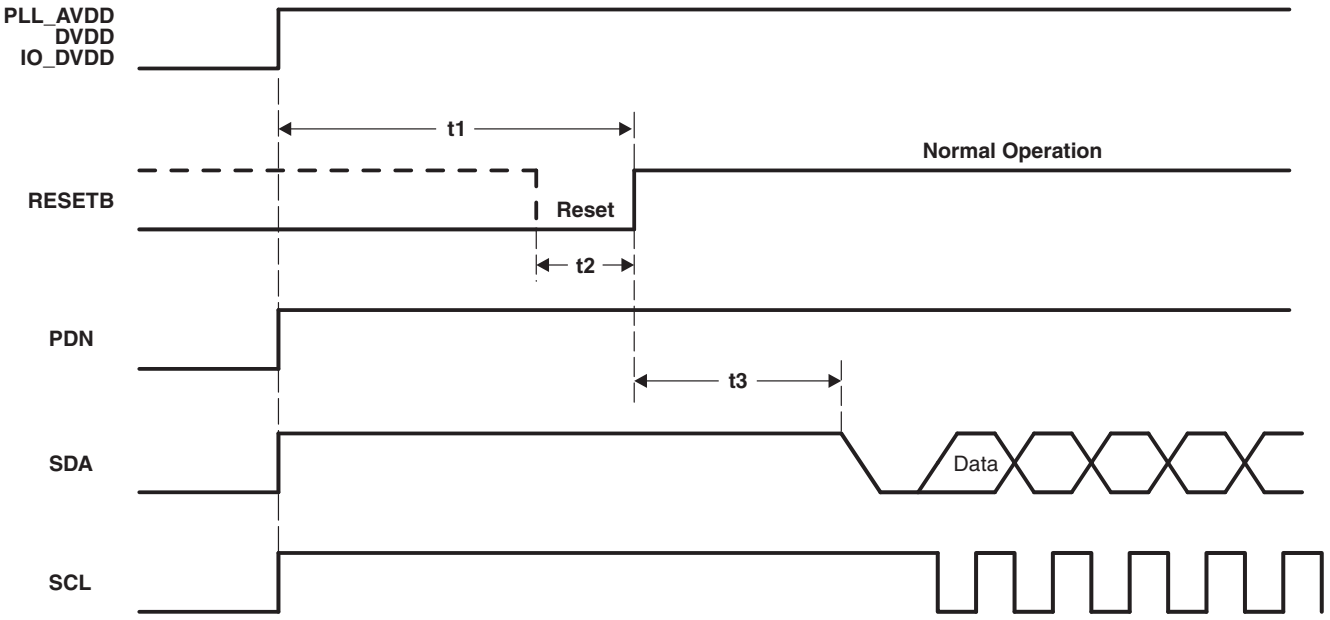

Figure 6-2. Power-On Reset Timing

Table 6-2. Power-On Reset Timing

NO.	PARAMETER	MIN	MAX	UNIT
t1	Delay time between power supplies active and reset	20		ms
t2	RESETB pulse duration	500		ns
t3	Delay time between end of reset to I^2C active	200		µs

6.4 Reset Sequence

Table 6-3 shows the reset sequence of the TVP5154A pins status during reset time and immediately after reset time.

Table 6-3. Reset Sequence

PIN DESCRIPTION	DURING RESETB	IMMEDIATELY AFTER RESETB
INTREQ1/GPCL1/VBLK1, INTREQ2/GPCL2/VBLK2, INTREQ3/GPCL3/VBLK3, INTREQ4/GPCL4/VBLK4, HSYNC1, HSYNC2, HSYNC3, HSYNC4, VSYNC1/PALI1, VSYNC2/PALI2, VSYNC3/PALI3, VSYNC4/PALI4, CH1_OUT[7:0], CH2_OUT[7:0], CH3_OUT[7:0], CH4_OUT[7:0],	3-state	3-state
AIP1A, AIP1B, AIP2A, AIP2B, AIP3A, AIP3B, AIP4A, AIP4B, RESETB, PDN, SDA, SCL, I2CA0, I2CA1, XIN/OSC, TMS	Input	Input
FID1/GLCO1, FID2/GLCO2, FID3/GLCO3, FID4/GLCO4, AVID1, AVID2, AVID3, AVID4, CLK1, CLK2, CLK3, CLK4, SCLK1, SCLK2, SCLK3, SCLK4, XOUT	Output	Output

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7 Internal Control Registers

7.1 Overview

The TVP5154A decoder is initialized and controlled by sets of internal registers that set all device operating parameters. Communication between the external controller and the TVP5154A decoder is through the I^2C. Two sets of registers exist, direct and indirect. Table 7-1 shows the summary of the direct registers. Reserved registers must not be written. Reserved bits in the defined registers must be written with zeros, unless otherwise noted. The detailed programming information of each register is described in the following sections.

I^2C register FEh controls which of the four decoders receives I^2C commands. I^2C register FFh controls which decoder core responds to I^2C reads. Note, for a read operation, it is necessary to perform a write first, to set the desired sub-address for reading.

After power up and the hardware reset, each decoder must be started by writing 00h to register 7Fh for all four decoders.

Table 7-1. Direct Register Summary

REGISTER FUNCTION	ADDRESS	DEFAULT	R/W(1)
Video input source selection #1	00h	00h	R/W
Analog channel controls	01h	15h	R/W
Operation mode controls	02h	00h	R/W
Miscellaneous controls	03h	01h	R/W
Autoswitch mask	04h	DCh	R/W
Clock control	05h	08h	R/W
Color killer threshold control	06h	10h	R/W
Luminance processing control #1	07h	60h	R/W
Luminance processing control #2	08h	00h	R/W
Brightness control	09h	80h	R/W
Color saturation control	0Ah	80h	R/W
Hue control	0Bh	00h	R/W
Contrast control	0Ch	80h	R/W
Outputs and data rates select	0Dh	47h	R/W
Luminance processing control #3	0Eh	00h	R/W
Configuration shared pins	0Fh	08h	R/W
Reserved	10h		
Active video cropping start MSB for unscaled data	11h	00h	R/W
Active video cropping start LSB for unscaled data	12h	00h	R/W
Active video cropping stop MSB for unscaled data	13h	00h	R/W
Active video cropping stop LSB for unscaled data	14h	00h	R/W
Genlock/RTC	15h	01h	R/W
Horizontal sync start	16h	80h	R/W
Ancillary SAV/EAV control	17h	52h	R/W
Vertical blanking start	18h	00h	R/W
Vertical blanking stop	19h	00h	R/W
Chrominance processing control #1	1Ah	0Ch	R/W
Chrominance processing control #2	1Bh	14h	R/W
Interrupt reset register B	1Ch	00h	R/W
Interrupt enable register B	1Dh	00h	R/W

(1) R = Read only, W = Write only, R/W = Read and write

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Table 7-1. Direct Register Summary (continued)

REGISTER FUNCTION	ADDRESS	DEFAULT	R/W(1)
Interrupt configuration register B	1Eh	00h	R/W
Output control	1Fh	00h	R/W
Reserved	20h		
Indirect Register Data	21h–22h	00h	R/W
Indirect Register Address	23h	00h	R/W
Indirect Register Read/Write Strobe	24h	00h	R/W
AVID start/control for scaled data	25h–26h	00h	R/W
Reserved	27h		
Video standard	28h	00h	R/W
AVID stop for scaled data	29h–2Ah	00h	R/W
Reserved	2Bh		
Cb gain factor	2Ch		R
Cr gain factor	2Dh		R
Reserved	2Eh–2Fh		
656 Revision Select	30	00h	R/W
Reserved	31h–7Dh		
Patch Write Address	7Eh	00h	R/W(2)
Patch Code Execute	7Fh	00h	R/W(2)
MSB of device ID	80h	51h	R
LSB of device ID	81h	54h	R
ROM major version	82h	02h	R
ROM minor version	83h	00h	R
Vertical line count MSB	84h		R
Vertical line count LSB	85h		R
Interrupt status register B	86h		R
Interrupt active register B	87h		R
Status register #1	88h		R
Status register #2	89h		R
Status register #3	8Ah		R
Status register #4	8Bh		R
Status register #5	8Ch		R
Reserved	8Dh		
Patch Read Address	8Eh	00h	R/W(2)
Reserved	8Fh		
Closed caption data registers	90h–93h		R
WSS/CGMS-A data registers	94h–99h		R
VPS/Gemstar 2x data registers	9Ah–A6h		R
VITC data registers	A7h–AFh		R
VBI FIFO read data	B0h		R
Teletext filter 1	B1h–B5h	00h	R/W
Teletext filter 2	B6h–BAh	00h	R/W
Teletext filter enable	BBh	00h	R/W
Reserved	BCh–BFh		
Interrupt status register A	C0h	00h	R/W
Interrupt enable register A	C1h	00h	R/W
Interrupt configuration	C2h	04h	R/W

(2) These registers are used for firmware patch code and should not be written to or read from during normal operation.

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Table 7-1. Direct Register Summary (continued)

REGISTER FUNCTION	ADDRESS	DEFAULT	R/W[1]
VDP configuration RAM data	C3h	B8h	R/W
Configuration RAM address low byte	C4h	1Fh	R/W
Configuration RAM address high byte	C5h	00h	R/W
VDP status register	C6h		R
FIFO word count	C7h		R
FIFO interrupt threshold	C8h	80h	R/W
FIFO reset	C9h	00h	W
Line number interrupt	CAh	00h	R/W
Pixel alignment register low byte	CBh	4Eh	R/W
Pixel alignment register high byte	CCh	00h	R/W
FIFO output control	CDh	01h	R/W
Reserved	CEh		
Full field enable	CFh	00h	R/W
Line mode registers	D0h D1h–FBh	00h FFh	R/W
Full field mode register	FCh	7Fh	R/W
Reserved	FDh		
Decoder core write enables	FEh	0Fh	R/W
Decoder core read enables	FFh	00h	R/W

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7.2 Direct Register Definitions

Direct registers are written to by performing a 3-byte I^2C transaction:

START : DEVICE_ID : SUB_ADDRESS : DATA : STOP

Each direct register is eight bits wide.

7.2.1 Video Input Source Selection #1 Register

Address 00h
Default 00h

7	6	5	4	3	2	1	0
Reserved				Black output	Reserved	Channel n source selection	S-video selection

Channel n source selection:

0 = AIPnA selected (default)
1 = AIPnB selected

Table 7-2. Analog Channel and Video Mode Selection

	INPUT(S) SELECTED	ADDRESS 00	
		BIT 1	BIT 0
Composite	AIPnA (default)	0	0
	AIPnB	1	0
S-Video	AIPnA (luma), AIPnB (chroma)	x	1

Where n = 1, 2, 3, 4

Black output:

0 = Normal operation (default)
1 = Force black screen output (outputs synchronized)
a. Forced to 10h in normal mode
b. Forced to 01h in extended mode

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7.2.2 Analog Channel Controls Register

Address 01h
Default 15h

7	6	5	4	3	2	1	0
Reserved			1	0	1	Automatic gain control	

Automatic gain control (AGC):

00 = AGC disabled (fixed gain value)
01 = AGC enabled (default)
10 = Reserved
11 = AGC frozen to the previously set value

7.2.3 Operation Mode Controls Register

Address 02h
Default 00h

7	6	5	4	3	2	1	0
Fast lock mode	Color burst reference enable	TV/VCR mode		Composite peak disable	Color subcarrier PLL frozen	Luma peak disable	Power down mode

Fast lock mode:

0 = Normal operation (default)
1 = Fast lock mode. Locks within three fields if stable input signal and forced video standard.

Color burst reference enable:

0 = Color burst reference for AGC disabled (default)
1 = Color burst reference for AGC enabled (not recommended)

TV/VCR mode:

00 = Automatic mode determined by the internal detection circuit (default)
01 = Reserved
10 = VCR (nonstandard video) mode (recommended when using a camera locked to the AC line frequency)
11 = TV (standard video) mode

With automatic detection enabled, unstable or nonstandard syncs on the input video forces the detector into the VCR mode. This turns off the comb filters and turns on the chroma trap filter.

Composite peak disable:

0 = Composite peak protection enabled (default)
1 = Composite peak protection disabled

Color subcarrier PLL frozen:

0 = Color subcarrier PLL increments by the internally generated phase increment (default).
GLCO pin outputs the frequency increment.
1 = Color subcarrier PLL stops operating.
GLCO pin outputs the frozen frequency increment.

Luma peak disable

0 = Luma peak processing enabled (default)
1 = Luma peak processing disabled (recommended)

Power-down mode:

0 = Normal operation (default)
1 = Power-down mode. A/Ds are turned off and internal clocks are reduced to minimum.

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7.2.4 Miscellaneous Control Register

Address 03h
Default 01h

7	6	5	4	3	2	1	0
VBKO	GPCL pin	GPCL output enable	Lock status (HVLK)	YCbCr output enable(TVPOE)	HSYNC, VSYNC/PALI, AVID, FID/GLCO output enable	Vertical blanking on/off	CLK output enable

VBKO (pins 41, 60, 83, 102) function select:

0 = GPCL (default)

1 = VBLK

Note, if these pins are not configured as outputs, they must not be left floating. A 10-kΩ pulldown resistor is recommended if not driven externally.

GPCL (data is output based on state of bit 5):

0 = GPCL outputs 0 (default)

1 = GPCL outputs 1

GPCL output enable:

0 = GPCL is inactive (default). GPCL should not be programmed to 0 when register 0Fh bit 1 is 1 (programmed to be GPCL/VBLK).

1 = GPCL is output.

Note that, if these pins are not configured as outputs, they must not be left floating. A 10-kΩ pulldown resistor is recommended if not driven externally.

Lock status (HVLK) (configured along with register 0Fh, see Figure 7-1 for the relationship between the configuration shared pins):

0 = Terminal VSYNC/PALI outputs the PAL indicator (PALI) signal and terminal FID/GLCO outputs the field ID (FID) signal (default) (if terminals are configured to output PALI and FID in register 0Fh).

1 = Terminal VSYNC/PALI outputs the horizontal lock indicator (HLK) and terminal FID outputs the vertical lock indicator (VLK) (if terminals are configured to output PALI and FID in register 0Fh).

These are additional functionalities that are provided for ease of use.

YCbCr output enable:

0 = YOUT[7:0] high impedance (default)

1 = YOUT[7:0] active

Note, if these pins are not configured as outputs, they must not be left floating. A 10-kΩ pulldown resistor is recommended if not driven externally.

HSYNC, VSYNC/PALI, active video indicator (AVID), and FID/GLCO output enables:

0 = HSYNC, VSYNC/PALI, AVID, and FID/GLCO are high impedance (default).

1 = HSYNC, VSYNC/PALI, AVID, and FID/GLCO are active.

Note, if these pins are not configured as outputs, they must not be left floating. A 10-kΩ pulldown resistor is recommended if not driven externally.

Vertical blanking on/off:

0 = Vertical blanking (VBLK) off (default)

1 = Vertical blanking (VBLK) on

CLK output enable:

0 = CLK output is high impedance.

1 = CLK output is enabled (default).

Note: CLK edge and SCLK are configured through register 05h.

Table 7-3. Digital Output Control

REGISTER 03h, BIT 3 (TVPOE)(1)	REGISTER C2h, BIT 2 (VDPOE)(1)	YCbCr OUTPUT
0	X	High impedance
X	0	High impedance
1	1	Active

(1) VDPOE default is 1 and TVPOE default is 0.

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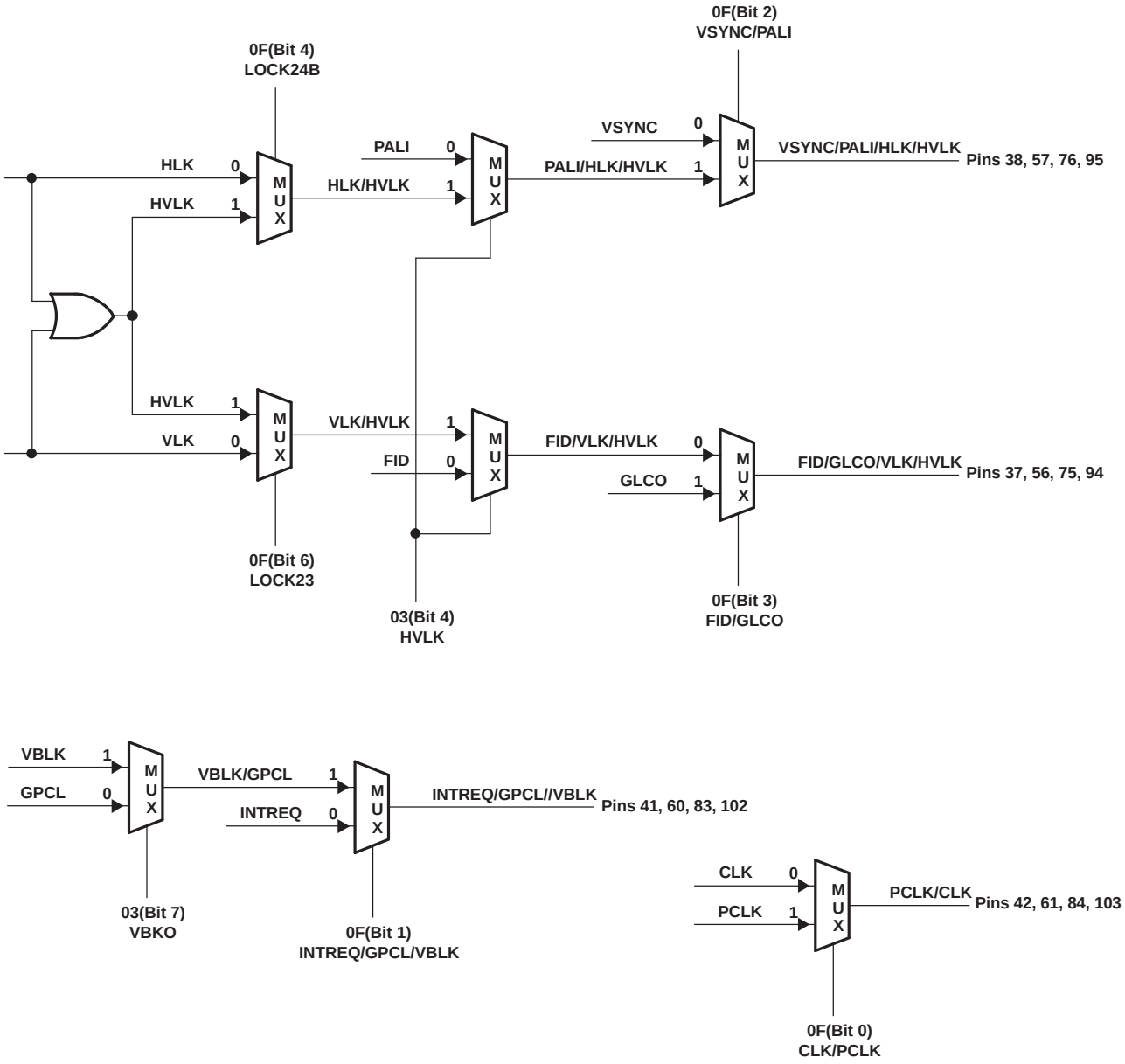

NOTE: Also see the configuration shared pins register at subaddress 0Fh (Section 7.2.16).

Figure 7-1. Configuration Shared Pins

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7.2.5 Autoswitch Mask Register

Address 04h
Default DCh

7	6	5	4	3	2	1	0
Reserved		SEC_OFF	N443_OFF	PALN_OFF	PALM_OFF	Reserved	

N443_OFF:
0 = NTSC443 is unmasked from the autoswitch process. Autoswitch does switch to NTSC443.
1 = NTSC443 is masked from the autoswitch process. Autoswitch does not switch to NTSC443 (default).

PALN_OFF:
0 = PAL-N is unmasked from the autoswitch process. Autoswitch does switch to PAL-N.
1 = PAL-N is masked from the autoswitch process. Autoswitch does not switch to PAL-N (default).

PALM_OFF:
0 = PAL-M is unmasked from the autoswitch process. Autoswitch does switch to PAL-M.
1 = PAL-M is masked from the autoswitch process. Autoswitch does not switch to PAL-M (default).

SEC_OFF:
0 = SECAM is unmasked from the autoswitch process. Autoswitch does switch to SECAM (default).
1 = SECAM is masked from the autoswitch process. Autoswitch does not switch to SECAM.

7.2.6 Clock Control Register

Address 05h
Default 08h

7	6	5	4	3	2	1	0
Reserved				SCLK OE	Reserved	SCLK edge	CLK edge

CLK edge
0 = CLK data changes on falling edge of CLK.
1 = CLK data changes on rising edge of CLK.

SCLK edge
0 = SCLK data changes on falling edge of SCLK.
1 = SCLK data changes on rising edge of SCLK.

SCLK OE
0 = SCLK output disabled. Output is high impedance.
1 = SCLK output enabled.

NOTE: CLK OE is configured through register 0x03 to maintain compatibility with the TVP5150 family of devices.

7.2.7 Color Killer Threshold Control Register

Address 06h
Default 10h

7	6	5	4	3	2	1	0
Reserved	Automatic color killer		Color killer threshold				

Automatic color killer:
00 = Automatic mode (default)
01 = Reserved
10 = Color killer enabled, the CbCr terminals are forced to a zero color state.
11 = Color killer disabled

Color killer threshold:
11111 = –30 dB (minimum)
10000 = –24 dB (default)
00000 = –18 dB (maximum)

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7.2.8 Luminance Processing Control #1 Register

Address 07h
Default 60h

7	6	5	4	3	2	1	0
2× luma output enable	Pedestal not present	Disable raw header	Luma bypass enabled during vertical blanking	Luminance signal delay with respect to chrominance signal			

2× luma output enable:

0 = Output depends on bit 4, luminance bypass enabled during vertical blanking (default).

1 = Outputs 2x luma samples during the entire frame. This bit takes precedence over bit 4.

Pedestal not present:

0 = 7.5 IRE pedestal is present on the analog video input signal.

1 = Pedestal is not present on the analog video input signal (default).

Disable raw header:

0 = Insert 656 ancillary headers for raw data

1 = Disable 656 ancillary headers and instead force dummy ones (0x40) (default)

Luminance bypass enabled during vertical blanking:

0 = Disabled. If bit 7, 2× luma output enable, is 0, normal luminance processing occurs and YCbCr samples are output during the entire frame (default).

1 = Enabled. If bit 7, 2× luma output enable, is 0, normal luminance processing occurs and YCbCr samples are output during VACTIVE and 2× luma samples are output during VBLK. Luminance bypass occurs for the duration of the vertical blanking as defined by registers 18h and 19h.

Luma signal delay with respect to chroma signal in pixel clock increments (range –8 to 7 pixel clocks):

1111 = –8 pixel clocks delay

1011 = –4 pixel clocks delay

1000 = –1 pixel clocks delay

0000 = 0 pixel clocks delay (default)

0011 = 3 pixel clocks delay

0111 = 7 pixel clocks delay

7.2.9 Luminance Processing Control #2 Register

Address 08h
Default 00h

7	6	5	4	3	2	1	0
Reserved	Luminance filter select	Reserved		Peaking gain		Reserved	

Luminance filter select:

0 = Luminance comb filter enabled (default)

1 = Luminance chroma trap filter enabled

Peaking gain (sharpness):

00 = 0 (default)

01 = 0.5

10 = 1

11 = 2

Information on peaking frequency: ITU-R BT.601 sampling rate: all standards — peaking center frequency is 2.6 MHz

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7.2.10 Brightness Control Register

Address 09h
Default 80h

7	6	5	4	3	2	1	0
Brightness control							

Brightness control: This register works for CVBS and S-Video luminance.

1111 1111 = 255 (bright)
1000 0000 = 128 (default)
0000 0000 = 0 (dark)

The output black level relative to the nominal black level (16 out of 256) as a function of the Brightness[7:0] setting and the Contrast[7:0] setting is as follows.

Black Level = nominal_black_level + (Brightness[7:0] - 128) + (438 / 4) × (1 – Contrast[7:0] / 128)

7.2.11 Color Saturation Control Register

Address 0Ah
Default 80h

7	6	5	4	3	2	1	0
Saturation control							

Saturation control: This register works for CVBS and S-Video chrominance.

1111 1111 = 255 (maximum)
1000 0000 = 128 (default)
0000 0000 = 0 (no color)

The total chrominance gain relative to the nominal chrominance gain as a function of the Saturation [7:0] setting is as follows.

Chrominance Gain = nominal_chrominance_gain × (Saturation[7:0] / 128)

7.2.12 Hue Control Register (does not apply to SECAM)

Address 0Bh
Default 00h

7	6	5	4	3	2	1	0
Hue control							

Hue control:

0111 1111 = +180 degrees
0000 0000 = 0 degrees (default)
1000 0000 = –180 degrees

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7.2.13 Contrast Control Register

Address 0Ch
Default 80h

7	6	5	4	3	2	1	0
Contrast [7:0]							

Contrast [7:0]: This register works for CVBS and S-Video luminance.

1111 1111 to 1101 0000 = Reserved
1100 1111 = 207 (maximum contrast)
1000 0000 = 128 (default)
0000 0000 = 0 (minimum contrast)

The total luminance gain relative to the nominal luminance gain as a function of the Contrast [7:0] setting is as follows.

Luminance Gain = nominal_luminance_gain × (Contrast[7:0] / 128)

Note: Luminance peak processing (see bit 1 of subaddress: 02h) may limit the upper end of the contrast control range.

Note: Whenever the contrast control setting is modified, the brightness control setting must be modified immediately afterward to maintain the proper output black level.

7.2.14 Outputs and Data Rates Select Register

Address 0Dh
Default 47h

7	6	5	4	3	2	1	0
Reserved	YCbCr output code range	CbCr code format	YCbCr data path bypass		YCbCr output format		

YCbCr output code range:

0 = ITU-R BT.601 coding range (Y ranges from 16 to 235. U and V range from 16 to 240)
1 = Extended coding range (Y, U, and V range from 1 to 254) (default)

CbCr code format:

0 = Offset binary code (2s complement + 128) (default)
1 = Straight binary code (2s complement)

YCbCr data path bypass:

00 = Normal operation (default)
01 = Decimation filter output connects directly to the YCbCr output pins. This data is similar to the digitized composite data, but the HBLANK area is replaced with ITU-R BT.656 digital blanking.
10 = Digitized composite (or digitized S-video luma). A/D output connects directly to the YCbCr output pins.
11 = Reserved

YCbCr output format:

000 = 8-bit 4:2:2 YCbCr with discrete sync output
001 = Reserved
010 = Reserved
011 = Reserved
100 = Reserved
101 = Reserved
110 = Reserved
111 = 8-bit ITU-R BT.656 interface with embedded sync output (default)

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7.2.15 Luminance Processing Control #3 Register

Address 0Eh
Default 00h

7	6	5	4	3	2	1	0
Reserved						Luminance trap filter select	

Luminance filter stop band bandwidth (MHz):

00 = No notch (default)
01 = Notch 1
10 = Notch 2
11 = Notch

Luminance filter select [1:0] selects one of the four chroma trap (notch) filters to produce luminance signal by removing the chrominance signal from the composite video signal. The stopband of the chroma trap filter is centered at the chroma subcarrier frequency, with stopband bandwidth controlled by the two control bits. See Table 7-4 for the stopband bandwidths. The WCF bit is controlled in the chrominance control #2 register.

Table 7-4. Luma Filter Selection

WCF	FILTER SELECT	NTSC/PAL/SECAM ITU-R BT.601
0	00	1.2214
	01	0.8782
	10	0.7297
	11	0.4986
1	00	1.4170
	01	1.0303
	10	0.8438
	11	0.5537

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7.2.16 Configuration Shared Pins Register

Address 0Fh
Default 08h

7	6	5	4	3	2	1	0
Reserved	FID PIN	Reserved	PALI PIN	FID/GLCO	VSYNC/PALI	INTREQ/GPCL/VBLK	CLK/PCLK

FID PIN function select:

0 = FID (default, if bit 3 is selected to output FID)

1 = Lock indicator (indicates whether the device is locked vertically)

PALI PIN function select:

0 = PALI (default, if bit 2 is selected to output PALI)

1 = Lock indicator (indicates whether the device is locked horizontally)

FID/GLCO function select (see register 03h, Section 7.2.4, for enhanced functionality):

0 = FID

1 = GLCO (default)

VSYNC/PALI function select (see register 03h, Section 7.2.4, for enhanced functionality):

0 = VSYNC (default)

1 = PALI

INTREQ/GPCL/VBLK function select:

0 = INTREQ (default)

1 = GPCL or VBLK depending on bit 7 of register 03h

CLK/PCLK (pins 42, 61, 84, 103) function select:

0 = CLK at 27 MHz (default)

1 = PCLK (1× pixel clock frequency at 13.5 MHz)

See Figure 7-1 for the relationship between the configuration shared pins.

7.2.17 Active Video Cropping Start Pixel MSB for Unscaled Data Register

Address 11h
Default 00h

7	6	5	4	3	2	1	0
AVID start pixel MSB [9:2]							

Active video cropping start pixel MSB [9:2], set this register first before setting register 12h. The TVP5154A decoder updates the AVID start values only when register 12h is written to. This start pixel value is relative to the default values of the AVID start pixel.

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7.2.18 Active Video Cropping Start Pixel LSB for Unscaled Data Register

Address 12h
Default 00h

7	6	5	4	3	2	1	0
Reserved					AVID active	AVID start pixel LSB [1:0]	

AVID active:

0 = AVID out active in VBLK (default)
1 = AVID out inactive in VBLK

AVID start [9:0] (combined registers 11h and 12h):

01 1111 1111 = 511
00 0000 0001 = 1
00 0000 0000 = 0 (default)
11 1111 1111 = –1
10 0000 0000 = –512

Active video cropping start pixel LSB [1:0]: The TVP5154A decoder updates the AVID start values only when this register is written to.

7.2.19 Active Video Cropping Stop Pixel MSB LSB for Unscaled Data Register

Address 13h
Default 00h

7	6	5	4	3	2	1	0
AVID stop pixel MSB [9:2]							

Active video cropping stop pixel MSB [9:2], set this register first before setting the register 14h. The TVP5154A decoder updates the AVID stop values only when register 14h is written to. This stop pixel value is relative to the default values of the AVID stop pixel.

7.2.20 Active Video Cropping Stop Pixel LSB for Unscaled Data Register

Address 14h
Default 00h

7	6	5	4	3	2	1	0
Reserved						AVID stop pixel LSB [1:0]	

Active video cropping stop pixel LSB [1:0]: The number of pixels of active video must be an even number. The TVP5154A decoder updates the AVID stop values only when this register is written to.

AVID stop [9:0] (combined registers 13h and 14h):

01 1111 1111 = 511
00 0000 0001 = 1
00 0000 0000 = 0 (default) (see Figure 3-5) and Figure 3-6)
11 1111 1111 = –1
10 0000 0000 = –512

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7.2.21 Genlock and RTC Register

Address 15h
Default 01h

7	6	5	4	3	2	1	0
Stable syncs	Reserved	F/V bit control		Auto inc	GLCO/RTC		

Stable syncs

0 = Output F and V bits follow the input signal producing fixed vertical blanking periods by adapting the active video.

1 = Output F and V bits produce fixed active video periods by adapting the vertical blanking.

F/V bit control

Table 7-5. F/V Bit Control

BIT 5	BIT 4	NUMBER OF LINES	F BIT	V BIT
0	0	Standard	ITU-R BT.656	ITU-R BT.656
		Nonstandard even	Force to 1	Switch at field boundary
		Nonstandard odd	Toggles	Switch at field boundary
0	1	Standard	ITU-R BT.656	ITU-R BT.656
		Nonstandard	Toggles	Switch at field boundary
1	0	Standard	ITU-R BT.656	ITU-R BT.656
		Nonstandard	Pulse mode	Switch at field boundary
1	1	Illegal		

Auto inc: When this bit is set to 1, subsequent reading/writing from/to back door registers automatically increment the address index.

GLCO/RTC: Table 7-6 for different modes.

Table 7-6. GLCO/RTC Control

BIT 2	BIT 1	BIT 0	GENLOCK/RTC MODE
0	x	0	GLCO
0	x	1	RTC output mode 0 (default)
1	x	0	GLCO
1	x	1	RTC output mode 1

All other values are reserved.

Figure 6-1 shows the timing of GLCO and the timing of RTC.

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7.2.22 Horizontal Sync (HSYNC) Start Register

Address 16h
Default 80h

7	6	5	4	3	2	1	0
HSYNC start							

HSYNC start:

1111 1111 = –127 × 4 pixel clocks
1111 1110 = –126 × 4 pixel clocks
1000 0001 = –1 × 4 pixel clocks
1000 0000 = 0 pixel clocks (default)
0111 1111 = 1 × 4 pixel clocks
0111 1110 = 2 × 4 pixel clocks
0000 0000 = 128 × 4 pixel clocks

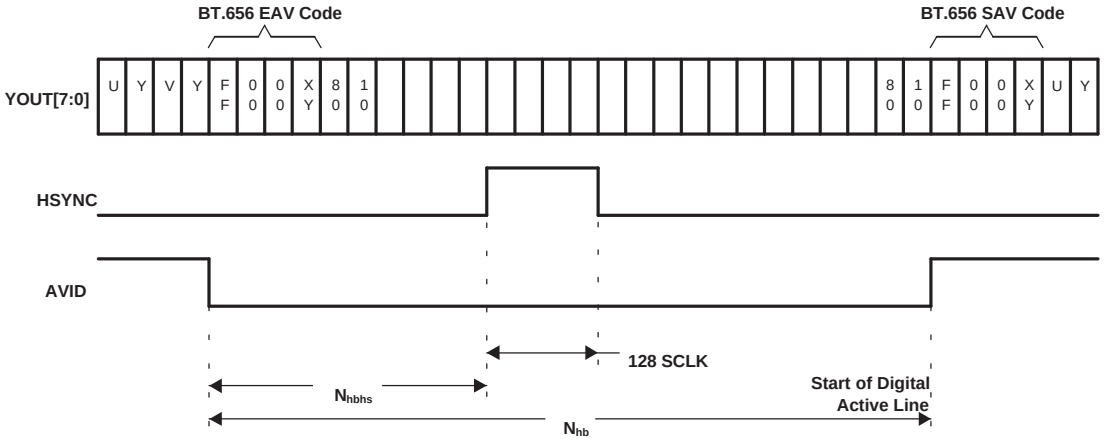

Figure 7-2. Horizontal Sync

Table 7-7. Clock Delays (CLKs)

STANDARD	N_{hbhs}	N_{hb}
NTSC	16	272
PAL	20	284
SECAM	40	280

Detailed timing information is also available in Section 3.12, *Synchronization Signals*.

7.2.23 Ancillary SAV/EAV Control

Address 17h
Default 52h

7	6	5	4	3	2	1	0
Reserved	Scaler PD	Include scale ancillary	Include scale SAV	Include scale EAV	Include unscale ancillary	Include unscale SAV	Include unscale EAV

Include unscaled EAV:

0 = AVID period does not include the EAV sync codes (default).

1 = AVID period includes the EAV sync codes.

Include unscaled SAV:

0 = AVID period does not include the SAV sync codes.

1 = AVID period includes the SAV sync codes (default).

Include unscaled ancillary data:

0 = AVID period includes the ancillary data region (default).

1 = AVID period does not include the ancillary data region.

Include scaled EAV:

0 = AVID period does not include the EAV sync codes (default).

1 = AVID period includes the EAV sync codes.

Include scaled SAV:

0 = AVID period does not include the SAV sync codes.

1 = AVID period includes the SAV sync codes (default).

Include scaled ancillary data:

0 = AVID period includes the ancillary data region (default).

1 = AVID period does not include the ancillary data region.

Scaler PD (scaler power down):

0 = Scaler active

1 = Scaler powered down (default)

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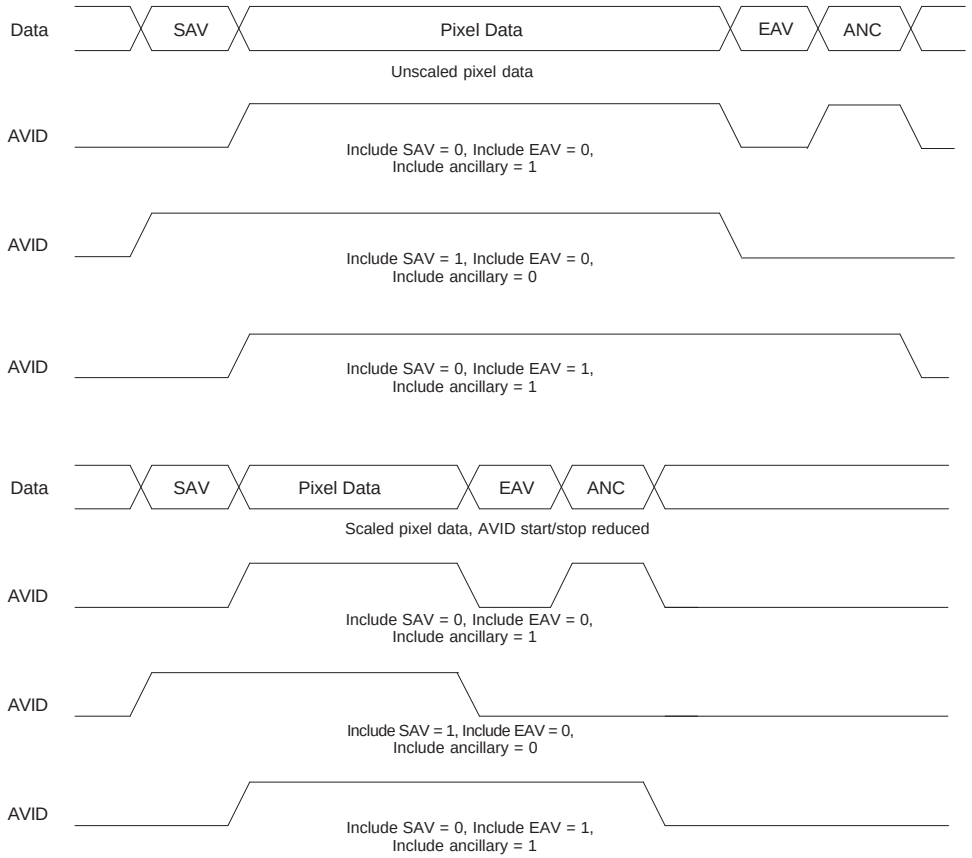

Figure 7-3. AVID Behavior When Ancillary Data Present

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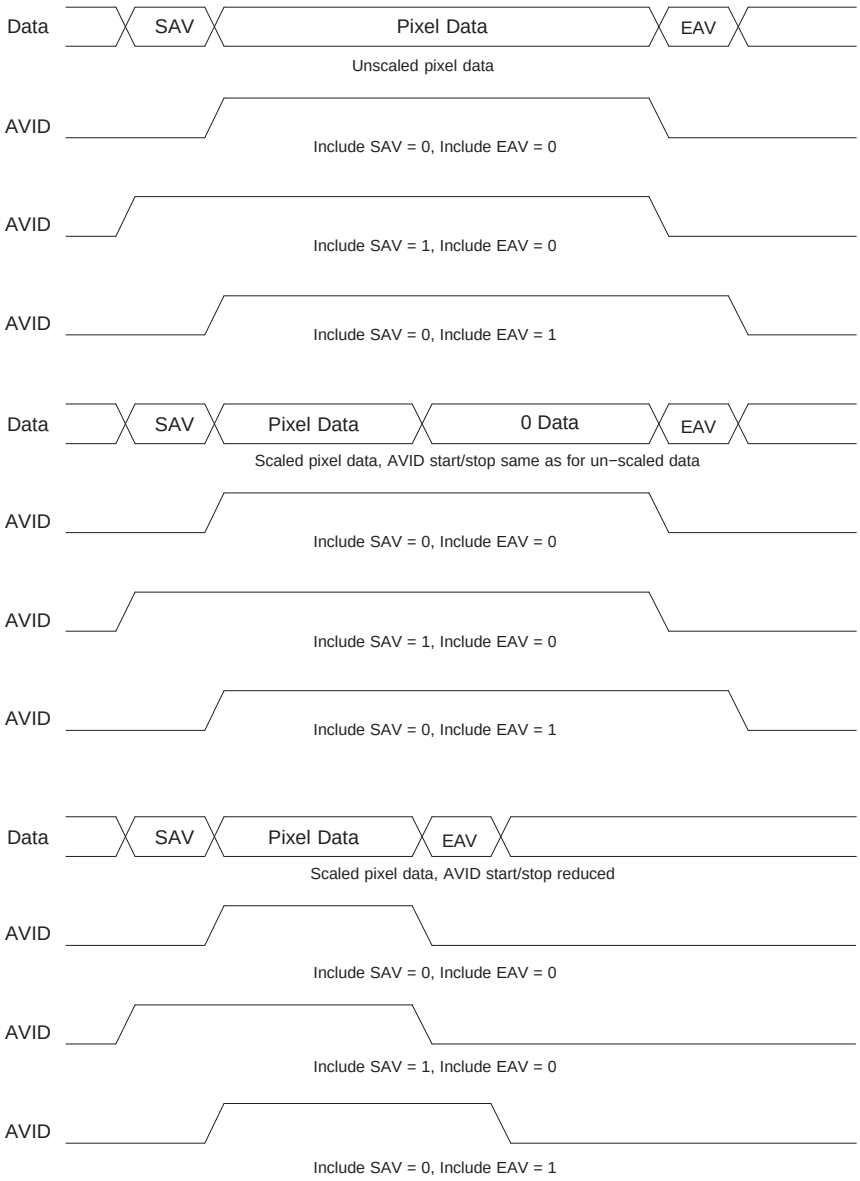

Figure 7-4. AVID Behavior When No Ancillary Data Present

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7.2.24 Vertical Blanking Start Register

Address 18h
Default 00h

7	6	5	4	3	2	1	0
Vertical blanking start							

Vertical blanking (VBLK) start:

0111 1111 = 127 lines after start of vertical blanking interval
0000 0001 = 1 line after start of vertical blanking interval
0000 0000 = Same time as start of vertical blanking interval (default) (see Figure 3-4, Figure 3-5, and Figure 3-6)
1111 1111 = 1 line before start of vertical blanking interval
1000 0000 = 128 lines before start of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals. The setting in this register determines the timing of the GPCL/VBLK signal when it is configured to output vertical blank (see register 03h). The setting in this register also determines the duration of the luma bypass function (see register 07h).

7.2.25 Vertical Blanking Stop Register

Address 19h
Default 00h

7	6	5	4	3	2	1	0
Vertical blanking stop							

Vertical blanking (VBLK) stop:

0111 1111 = 127 lines after stop of vertical blanking interval
0000 0001 = 1 line after stop of vertical blanking interval
0000 0000 = Same time as stop of vertical blanking interval (default) (see Figure 3-4, Figure 3-5, and Figure 3-6)
1111 1111 = 1 line before stop of vertical blanking interval
1000 0000 = 128 lines before stop of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals. The setting in this register determines the timing of the GPCL/VBLK signal when it is configured to output vertical blank (see register 03h). The setting in this register also determines the duration of the luma bypass function (see register 07h).

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7.2.26 Chrominance Control #1 Register

Address 1Ah
Default 0Ch

7	6	5	4	3	2	1	0
Reserved color			PLL reset	Chrominance adaptive comb filter enable (ACE)	Chrominance comb filter enable (CE)	Automatic color gain control	

Color PLL reset:

0 = Color PLL not reset (default)

1 = Color PLL reset

Writing a 1 to this bit resets the color PLL and transmits a 1 in the reset bit of the GLCO output stream.

Chrominance adaptive comb filter enable (ACE):

0 = Disable

1 = Enable (default)

Chrominance comb filter enable (CE):

0 = Disable

1 = Enable (default)

Automatic color gain control (ACGC):

00 = ACGC enabled (default)

01 = Reserved

10 = ACGC disabled

11 = ACGC frozen to the previously set value

7.2.27 Chrominance Control #2 Register

Address 1Bh
Default 14h

7	6	5	4	3	2	1	0
Reserved				Reserved	WCF	Chrominance filter select	

Wideband chroma filter (WCF):

0 = Disable

1 = Enable (default)

Chrominance filter select:

00 = No notch (default)

01 = Notch 1

10 = Notch 2

11 = Notch 3

Chrominance output bandwidth (MHz), see Table 7-8

Table 7-8. Chroma Output Bandwidth Select

WCF	FILTER SELECT	NTSC/PAL/SECAM ITU-R BT.601
0	00	1.2214
	01	0.8782
	10	0.7297
	11	0.4986
1	00	1.4170
	01	1.0303
	10	0.8438
	11	0.5537

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7.2.28 Interrupt Reset Register B

Address 1Ch
Default 00h

7	6	5	4	3	2	1	0
Software initialization reset	Reserved	Reserved	Field rate changed reset	Line alternation changed reset	Color lock changed reset	H/V lock changed reset	TV/VCR changed reset

Interrupt reset register B is used by the external processor to reset the interrupt status bits in interrupt status register B. Bits loaded with a 1 allow the corresponding interrupt status bit to reset to 0. Bits loaded with a 0 have no effect on the interrupt status bits.

Software initialization reset:

0 = No effect (default)
1 = Reset software initialization bit

Field rate changed reset:

0 = No effect (default)
1 = Reset field rate changed bit

Line alternation changed reset:

0 = No effect (default)
1 = Reset line alternation changed bit

Color lock changed reset:

0 = No effect (default)
1 = Reset color lock changed bit

H/V lock changed reset:

0 = No effect (default)
1 = Reset H/V lock changed bit

TV/VCR changed reset [TV/VCR mode is determined by counting the total number of lines/frame. The mode switches to VCR for nonstandard number of lines]:

0 = No effect (default)
1 = Reset TV/VCR changed bit

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7.2.29 Interrupt Enable Register B

Address 1Dh
Default 00h

7	6	5	4	3	2	1	0
Software initialization occurred enable	Reserved	Reserved	Field rate changed	Line alternation changed	Color lock changed	H/V lock changed	TV/VCR changed

Software initialization occurred enable:
0 = Disabled (default)
1 = Enabled
Field rate changed:
0 = Disabled (default)
1 = Enabled
Line alternation changed:
0 = Disabled (default)
1 = Enabled
Color lock changed:
0 = Disabled (default)
1 = Enabled
H/V lock changed:
0 = Disabled (default)
1 = Enabled
TV/VCR changed:
0 = Disabled (default)
1 = Enabled

Interrupt enable register B is used by the external processor to mask unnecessary interrupt sources for interrupt B. Bits loaded with a 1 allow the corresponding interrupt condition to generate an interrupt on the external pin. Conversely, bits loaded with zeros mask the corresponding interrupt condition from generating an interrupt on the external pin. This register only affects the external pin; it does not affect the bits in the interrupt status register. A given condition can set the appropriate bit in the status register and not cause an interrupt on the external pin. To determine if this device is driving the interrupt pin, either AND interrupt status register B with interrupt enable register B, or check the state of interrupt B in the interrupt B active register.

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7.2.30 Interrupt Configuration Register B

Address 1Eh
Default 00h

7	6	5	4	3	2	1	0
Reserved							Interrupt polarity B

Interrupt polarity B:

0 = Interrupt B is active low (default).

1 = Interrupt B is active high.

Interrupt polarity B must be same as interrupt polarity A bit at bit 0 of the interrupt configuration register A at address C2h.

Interrupt configuration register B is used to configure the polarity of interrupt B on the external interrupt pin. When the interrupt B is configured for active low, the pin is driven low when active and high impedance when inactive (open drain). Conversely, when the interrupt B is configured for active high, it is driven high for active and driven low for inactive.

7.2.31 Indirect Register Data

Address 21h-22h
Default 00h

Address	7	6	5	4	3	2	1	0
22h	Data[15:8]							
21h	Data[7:0]							

I^2C registers 21h and 22h can be used to write data to or read data from indirect registers. See I^2C registers 23h and 24h.

7.2.32 Indirect Register Address

Address 23h
Default 00h

7	6	5	4	3	2	1	0
ADDR[7:0]							

ADDR[7:0] = LSB of indirect address

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7.2.33 Indirect Register Read/Write Strobe

Address 24h
Default 00h

7	6	5	4	3	2	1	0
R/W[7:0]							

This register selects the most significant bits of the indirect register address and performs either an indirect read or write operation. Data will be written from are read to Indirect Register Data registers 21h-22h.

R/W[7:0]:

01h = read from 00h-1FFh address bank
02h = write to 00h-1FFh address bank
03h = read from 200h-3FFh address bank
04h = write to 200h-3FFh address bank
05h = read from 300h-3FFh address bank
06h = write to 300h-3FFh address bank

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7.2.34 Output Control

Address 1Fh
Default 00h

7	6	5	4	3	2	1	0
	Bit swap	Ancillary Enable	Parity modifier	SAV/EAV modifier	Output mode		

Output mode:

000 = Mode 0 : Unscaled data clocked by clock 1
001 = Mode 1 : Scaled data clocked by clock 1
010 = Mode 2 : Multiplexed data with separate clocks
011 = Mode 3 : Multiplexed data with clock 1 at 54 MHz
100 = Mode 4 : Unscaled/scaled field toggled data clocked by clock 1

SAV/EAV modifier:

0 = SAV/EAV codes not modified
1 = SAV/EAV MSB modified. MSB = 1 indicates unscaled data, MSB = 0 indicates scaled data

Parity modifier:

0 = Parity calculation includes SAV/EAV MSB.
1 = Parity calculation does not include SAV/EAV MSB.

Ancillary enable:

0 = Ancillary data not enabled
1 = Ancillary data packet added to indicate scaled or unscaled data
Note : Scaled/unscaled ancillary data cannot be enabled at the same time as VBI ancillary data

Bit swap:

0 = chx_out(0) corresponds to data LSB, chx_out(7) corresponds to data MSB
1 = chx_out(0) corresponds to data MSB, chx_out(7) corresponds to data LSB

Table 7-9. Ancillary Data Format and Sequence

BYTE NO.	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	DESCRIPTION	
0	0	0	0	0	0	0	0	0	Ancillary data preamble	
1	1	1	1	1	1	1	1	1		
2	1	1	1	1	1	1	1	1		
3	NEP	EP	0	1	DID3	DID2	DID1	DID0	Data ID (DID)	
4	1	0	0	0	0	0	0	0	Secondary data ID (SDID)	
5	0	1	0	0	0	0	0	1	Number of 32 bit data (NN)	
6	Video line # [7:0]								Internal data ID0 (IDID0)	
Z	0	0	0	0	0	0	Video line # [9:8]		Internal data ID1 (IDID1)	
8	00h								Data byte	Data
9	00h								Data byte	
10	1	0	00h						Check sum	
11	1	0	0	0	0	0	0	0	Fill byte	

EP: Even parity for D0–D5
NEP: Negated even parity
DID: For unscaled data D0–D3 taken from EAV DID value for unscaled data stream register low nibble for field 0 and from high nibble for field 1
For scaled data D0–D3 taken from EAV DID value for scaled data stream register low nibble for field 0 and from high nibble for field 1
SDID: Zero data
NN: Indicates 1 D word of data
IDID0: Transaction video line number [7:0]
IDID1: Bit 0/1 = Transaction video line number [9:8]
CS: Sum of D0–D7 of DID through last data byte
Fill byte: Fill bytes make a multiple of four bytes from byte 0 to last fill byte. For teletext modes, byte 8 is the sync pattern byte. Byte 9 is 1. Data (the first data byte).

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7.2.35 Active Video Cropping Start Pixel MSB for Scaled Data Register

Address 25h
Default 00h

7	6	5	4	3	2	1	0
AVID start pixel MSB [9:2]							

Active video cropping start pixel MSB [9:2], set this register first before setting register 26h. The TVP5154A decoder updates the AVID start values only when register 26h is written to. This start pixel value is relative to the default values of the AVID start pixel.

7.2.36 Active Video Cropping Start Pixel LSB for Scaled Data Register

Address 26h
Default 00h

7	6	5	4	3	2	1	0
Reserved					Active	AVID start pixel LSB [1:0]	

AVID active:

0 = AVID out active in VBLK (default)

1 = AVID out inactive in VBLK

Active video cropping start pixel LSB [1:0]: The TVP5154A decoder updates the AVID start values only when this register is written to.

AVID start [9:0]:

01 1111 1111 = 511
00 0000 0001 = 1
00 0000 0000 = 0 (default)
11 1111 1111 = –1
10 0000 0000 = –512

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7.2.37 Video Standard Register

Address 28h
Default 00h

7	6	5	4	3	2	1	0
Reserved				Video standard			

Video standard:

0000 = Autoswitch mode (default)
0001 = Reserved
0010 = (M, J) NTSC ITU-R BT.601
0011 = Reserved
0100 = (B, G, H, I, N) PAL ITU-R BT.601
0101 = Reserved
0110 = (M) PAL ITU-R BT.601
0111 = Reserved
1000 = (Combination-N) PAL ITU-R BT.601
1001 = Reserved
1010 = NTSC 4.43 ITU-R BT.601
1011 = Reserved
1100 = SECAM ITU-R BT.601

With the autoswitch code running, the user can force the device to operate in a particular video standard mode and sample rate by writing the appropriate value into this register.

7.2.38 Active Video Cropping Stop Pixel MSB for Scaled Data Register

Address 29h
Default 00h

7	6	5	4	3	2	1	0
AVID stop pixel MSB [9:2]							

Active video cropping stop pixel MSB [9:2], set this register first before setting the register 2Ah. The TVP5154A decoder updates the AVID stop values only when register 2Ah is written to. This stop pixel value is relative to the default values of the AVID stop pixel.

7.2.39 Active Video Cropping Stop Pixel LSB for Scaled Data Register

Address 2Ah
Default 00h

7	6	5	4	3	2	1	0
Reserved						AVID stop pixel LSB [1:0]	

AVID stop [9:0]:

01 1111 1111 = 511
00 0000 0001 = 1
00 0000 0000 = 0 (default) (see Figure 3-4, Figure 3-5, and Figure 3-6)
11 1111 1111 = –1
10 0000 0000 = –512

Active video cropping stop pixel LSB [1:0]: The number of pixels of active video must be an even number. The TVP5154A decoder updates the AVID stop values only when this register is written to.

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7.2.40 Cb Gain Factor Register

Address 2Ch

7	6	5	4	3	2	1	0
Cb gain factor							

This is a read-only register that provides the gain applied to the Cb in the YCbCr data stream.

7.2.41 Cr Gain Factor Register

Address 2Dh

7	6	5	4	3	2	1	0
Cr gain factor							

This is a read-only register that provides the gain applied to the Cr in the YCbCr data stream.

7.2.42 656 Revision Select Register

Address 30h
Default 00h

7	6	5	4	3	2	1	0
							656 Rev

656 revision select:

0 = Adheres to ITU-R BT.656-4 and BT.656-5 timing (default)

1 = Adheres to ITU-R BT.656-3 timing

7.2.43 MSB of Device ID Register

Address 80h
Default 51h

7	6	5	4	3	2	1	0
MSB of device ID							

This register identifies the MSB of the device ID. Value = 0x51.

7.2.44 Patch Write Address

Address 7Eh
Default 00h

7	6	5	4	3	2	1	0
R/W[7:0]							

This register is used for downloading firmware patch code. Please refer to the patch load application note for more detail. This register must not be written to or read from during normal operation.

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7.2.45 Patch Code Execute

Address 7Fh
Default 00h

7	6	5	4	3	2	1	0
R/W[7:0]							

Writing to this register following a firmware patch load restarts the CPU and initiates execution of the patch code. This register must not be written to or read from during normal operation.

7.2.46 LSB of Device ID Register

Address 81h
Default 54h

7	6	5	4	3	2	1	0
LSB of device ID							

This register identifies the LSB of the device ID. Value = 0x54.

7.2.47 ROM Major Version Register

Address 82h
Default 02h

7	6	5	4	3	2	1	0
ROM major version(1)							

(1) This register can contain a number from 0x01 to 0xFF.

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7.2.48 ROM Minor Version Register

Address 83h
Default 00h

7	6	5	4	3	2	1	0
ROM minor version(1)							

(1) This register can contain a number from 0x01 to 0xFF.

7.2.49 Vertical Line Count MSB Register

Address 84h

7	6	5	4	3	2	1	0
Reserved						Vertical line count MSB	

Vertical line count bits [9:8]

7.2.50 Vertical Line Count LSB Register

Address 85h

7	6	5	4	3	2	1	0
Vertical line count LSB							

Vertical line count bits [7:0]

Registers 84h and 85h can be read and combined to extract the detected number of lines per frame. This can be used with nonstandard video signals, such as a VCR in fast-forward or rewind modes, to synchronize the downstream video circuitry.

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7.2.51 Interrupt Status Register B

Address 86h

7	6	5	4	3	2	1	0
Software initialization	Reserved	Command ready	Field rate changed	Line alternation changed	Color lock changed	H/V lock changed	TV/VCR changed

Software initialization:

0 = Software initialization is not ready (default).

1 = Software initialization is ready.

Command ready:

0 = TVP5154A is not ready to accept a new command (default).

1 = TVP5154A is ready to accept a new command.

Field rate changed:

0 = Field rate has not changed (default).

1 = Field rate has changed.

Line alternation changed:

0 = Line alteration has not changed (default).

1 = Line alternation has changed.

Color lock changed:

0 = Color lock status has not changed (default).

1 = Color lock status has changed.

H/V lock changed:

0 = H/V lock status has not changed (default).

1 = H/V lock status has changed.

TV/VCR changed:

0 = TV/VCR status has not changed (default).

1 = TV/VCR status has changed.

Interrupt status register B is polled by the external processor to determine the interrupt source for interrupt B. After an interrupt condition is set, it can be reset by writing to the interrupt reset register B at subaddress 1Ch with a 1 in the appropriate bit.

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7.2.52 Interrupt Active Register B

Address 87h

7	6	5	4	3	2	1	0
Reserved							Interrupt B

Interrupt B:

0 = Interrupt B is not active on the external terminal (default).

1 = Interrupt B is active on the external terminal.

The interrupt active register B is polled by the external processor to determine if interrupt B is active.

7.2.53 Status Register #1

Address 88h

7	6	5	4	3	2	1	0
Peak white detect status	Line-alternating status	Field rate status	Lost lock detect	Color subcarrier lock status	Vertical sync lock status	Horizontal sync lock status	TV/VCR status

Peak white detect status:

0 = Peak white is not detected.

1 = Peak white is detected.

Line–alternating status:

0 = Nonline alternating

1 = Line alternating

Field rate status:

0 = 60 Hz

1 = 50 Hz

Lost lock detect:

0 = No lost lock since status register #1 was last read

1 = Lost lock since status register #1 was last read

Color subcarrier lock status:

0 = Color subcarrier is not locked.

1 = Color subcarrier is locked.

Vertical sync lock status:

0 = Vertical sync is not locked.

1 = Vertical sync is locked.

Horizontal sync lock status:

0 = Horizontal sync is not locked.

1 = Horizontal sync is locked.

TV/VCR status. TV mode is determined by detecting standard line-to-line variations and specific chroma SCH phases based on the standard input video format. VCR mode is determined by detecting variations in the chroma SCH phases compared to the chroma SCH phases of the standard input video format.

0 = TV

1 = VCR

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7.2.54 Status Register #2

Address 89h

7	6	5	4	3	2	1	0
Reserved	Weak signal detection	PAL switch polarity	Field sequence status	AGC and offset frozen status	Reserved		

Weak signal detection:

0 = No weak signal

1 = Weak signal mode

PAL switch polarity of first line of odd field:

0 = PAL switch is 0.

1 = PAL switch is 1.

Field sequence status:

0 = Even field

1 = Odd field

AGC and offset frozen status:

0 = AGC and offset are not frozen.

1 = AGC and offset are frozen.

7.2.55 Status Register #3

Address 8Ah

7	6	5	4	3	2	1	0
Analog gain				Digital gain			

Analog gain: 4-bit front-end AGC analog gain setting

Digital gain: 4 MSBs of 6-bit front-end AGC digital gain setting

The product of the analog and digital gain is given below.

Gain Product = (1 + 3 × analog_gain/15) × (1 + gain_step × digital_gain/4096)

Where,

0 ≤ analog_gain ≤ 15

0 ≤ digital_gain ≤ 63

The gain_step setting as a function of the analog_gain setting is shown below.

analog_gain	gain_step
0	61
1	55
2	48
3	44
4	38
5	33
6	29
7	26
8	24
9	22
10	20
11	19
12	18
13	17
14	16
15	15

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7.2.56 Status Register #4

Address 8Bh

7	6	5	4	3	2	1	0
Subcarrier to horizontal (SCH) phase							

SCH (color PLL subcarrier phase at 50% of the falling edge of horizontal sync of line one of odd field; step size 360°/256):

0000 0000 = 0.00^{o}
0000 0001 = 1.41^{o}
0000 0010 = 2.81^{o}
1111 1110 = 357.2^{o}
1111 1111 = 358.6^{o}

7.2.57 Status Register #5

Address 8Ch

7	6	5	4	3	2	1	0
Autoswitch mode	Reserved			Video standard			Sampling rate

Autoswitch mode:

0 = Stand-alone (forced video standard) mode
1 = Autoswitch mode

This register contains information about the detected video standard and the sampling rate at which the device is currently operating. When autoswitch code is running, this register must be tested to determine which video standard has been detected.

Table 7-10. Auto Switch Video Standard

VIDEO STANDARD [3:1]			SR(1)	VIDEO STANDARD
BIT 3	BIT 2	BIT 1	BIT 0	
0	0	0	0	Reserved
0	0	0	1	(M, J) NTSC ITU-R BT.601
0	0	1	0	Reserved
0	0	1	1	(B, G, H, I, N) PAL ITU-R BT.601
0	1	0	0	Reserved
0	1	0	1	(M) PAL ITU-R BT.601
0	1	1	0	Reserved
0	1	1	1	PAL-Nc ITU-R BT.601
1	0	0	0	Reserved
1	0	0	1	NTSC 4.43 ITU-R BT.601
1	0	1	0	Reserved
1	0	1	1	SECAM ITU-R BT.601

(1) Sampling rate (SR): 0 = Reserved, 1 = ITU-R BT.601

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7.2.58 Patch Read Address

Address 8Eh
Default 00h

7	6	5	4	3	2	1	0
R/W[7:0]							

This register can be used for patch code read-back. This register must not be written to or read from during normal operation.

7.2.59 Closed Caption Data Registers

Address 90h–93h

Address	7	6	5	4	3	2	1	0
90h	Closed caption field 1 byte 1							
91h	Closed caption field 1 byte 2							
92h	Closed caption field 2 byte 1							
93h	Closed caption field 2 byte 2							

These registers contain the closed caption data arranged in bytes per field.

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7.2.60 WSS/CGMS-A Data Registers

Address 94h–99h

NTSC

Address	7	6	5	4	3	2	1	0	BYTE
94h			b5	b4	b3	b2	b1	b0	WSS field 1 byte 1
95h	b13	b12	b11	b10	b9	b8	b7	b6	WSS field 1 byte 2
96h			b19	b18	b17	b16	b15	b14	WSS field 1 byte 3
97h			b5	b4	b3	b2	b1	b0	WSS field 2 byte 1
98h	b13	b12	b11	b10	b9	b8	b7	b6	WSS field 2 byte 2
99h			b19	b18	b17	b16	b15	b14	WSS field 2 byte 3

These registers contain the wide screen signaling (WSS/CGMS-A) data for NTSC.

Bits 0–1 represent word 0, aspect ratio.

Bits 2–5 represent word 1, header code for word 2.

Bits 6–13 represent word 2, copy control.

Bits 14–19 represent word 3, CRC.

PAL/SECAM

Address	7	6	5	4	3	2	1	0	BYTE
94h	b7	b6	b5	b4	b3	b2	b1	b0	WSS field 1 byte 1
95h			b13	b12	b11	b10	b9	b8	WSS field 1 byte 2
96h	Reserved								
97h	b7	b6	b5	b4	b3	b2	b1	b0	WSS field 2 byte 1
98h			b13	b12	b11	b10	b9	b8	WSS field 2 byte 2
99h	Reserved								

Bits 0–3 represent group 1, aspect ratio.

Bits 4–7 represent group 2, enhanced services.

Bits 8–10 represent group 3, subtitles.

Bits 11–13 represent group 4, others.

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7.2.61 VPS/Gemstar 2x Data Registers

Address 9Ah–A6h

Address	7	6	5	4	3	2	1	0
9Ah	VPS/Gemstar 2x byte 1							
9Bh	VPS/Gemstar 2x byte 2							
9Ch	VPS/Gemstar 2x byte 3							
9Dh	VPS/Gemstar 2x byte 4							
9Eh	VPS/Gemstar 2x byte 5							
9Fh	VPS/Gemstar 2x byte 6							
A0h	VPS/Gemstar 2x byte 7							
A1h	VPS/Gemstar 2x byte 8							
A2h	VPS/Gemstar 2x byte 9							
A3h	VPS/Gemstar 2x byte 10							
A4h	VPS/Gemstar 2x byte 11							
A5h	VPS/Gemstar 2x byte 12							
A6h	VPS/Gemstar 2x byte 13							

When PAL VPS is used, these registers contain the entire VPS data line except the clock run-in code and the start code. When NTSC Gemstar 2x is used, these registers contain the Gemstar 2x data.

7.2.62 VITC Data Registers

Address A7h–AFh

Address	7	6	5	4	3	2	1	0
A7h	VITC byte 1, frame byte 1							
A8h	VITC byte 2, frame byte 2							
A9h	VITC byte 3, seconds byte 1							
AAh	VITC byte 4, seconds byte 2							
ABh	VITC byte 5, minutes byte 1							
ACh	VITC byte 6, minutes byte 2							
ADh	VITC byte 7, hour byte 1							
AEh	VITC byte 8, hour byte 2							
AFh	VITC byte 9, CRC							

These registers contain the VITC data.

7.2.63 VBI FIFO Read Data Register

Address B0h

7	6	5	4	3	2	1	0
FIFO read data							

This address is provided to access VBI data in the FIFO through the host port. All forms of teletext data come directly from the FIFO, while all other forms of VBI data can be programmed to come from the registers or from the FIFO. Current status of the FIFO can be found at address C6h and the number of bytes in the FIFO is located at address C7h. If the host port is to be used to read data from the FIFO, the output formatter must be disabled at address CDh bit 0. The format used for the VBI FIFO is shown in Section 3.9.

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7.2.64 Teletext Filter and Mask Registers

Address B1h–BAh
Default 00h

Address	7	6	5	4	3	2	1	0
B1h	Filter 1 mask 1				Filter 1 pattern 1			
B2h	Filter 1 mask 2				Filter 1 pattern 2			
B3h	Filter 1 mask 3				Filter 1 pattern 3			
B4h	Filter 1 mask 4				Filter 1 pattern 4			
B5h	Filter 1 mask 5				Filter 1 pattern 5			
B6h	Filter 2 mask 1				Filter 2 pattern 1			
B7h	Filter 2 mask 2				Filter 2 pattern 2			
B8h	Filter 2 mask 3				Filter 2 pattern 3			
B9h	Filter 2 mask 4				Filter 2 pattern 4			
BAh	Filter 2 mask 5				Filter 2 pattern 5			

For an NABTS system, the packet prefix consists of five bytes. Each byte contains four data bits (D[3:0]) interlaced with four Hamming protection bits (H[3:0]):

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D[3]	H[3]	D[2]	H[2]	D[1]	H[1]	D[0]	H[0]

Only the data portion D[3:0] from each byte is applied to a teletext filter function with the corresponding pattern bits P[3:0] and mask bits M[3:0]. Hamming protection bits are ignored by the filter.

For a WST system (PAL or NTSC), the packet prefix consists of two bytes so that two patterns are used. Patterns 3, 4, and 5 are ignored.

The mask bits enable filtering using the corresponding bit in the pattern register. For example, a 1 in the LSB of mask 1 means that the filter module must compare the LSB of nibble 1 in the pattern register to the first data bit on the transaction. If these match, a true result is returned. A 0 in a bit of mask 1 means that the filter module must ignore that data bit of the transaction. If all zeros are programmed in the mask bits, the filter matches all patterns returning a true result (default 00h).

Pattern and mask for each byte and filter are referred as <1,2><P,M><1,2,3,4,5> where:

<1,2> identifies the filter 1 or 2

<P,M> identifies the pattern or mask

<1,2,3,4,5> identifies the byte number

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7.2.65 Teletext Filter Control Register

Address BBh
Default 00h

7	6	5	4	3	2	1	0
Reserved			Filter logic		Mode	TTX filter 2 enable	TTX filter 1 enable

Filter logic: Allows different logic to be applied when combining the decision of filter 1 and filter 2 as follows:

00 = NOR (default)
01 = NAND
10 = OR
11 = AND

Mode:

0 = Teletext WST PAL mode B (2 header bytes) (default)
1 = Teletext NABTS NTSC mode C (5 header bytes)

TTX filter 2 enable:

0 = Disabled (default)
1 = Enabled

TTX filter 1 enable:

0 = Disabled (default)
1 = Enabled

If the filter matches or if the filter mask is all zeros, a true result is returned.

7.2.66 Interrupt Status Register A

Address C0h
Default 00h

7	6	5	4	3	2	1	0
Lock state interrupt	Lock interrupt	Reserved			FIFO threshold interrupt	Line interrupt	Data interrupt

Lock state interrupt:

0 = TVP5154A is not locked to the video signal (default)
1 = TVP5154A is locked to the video signal.

Lock interrupt:

0 = A transition has not occurred on the lock signal (default).
1 = A transition has occurred on the lock signal.

FIFO threshold interrupt:

0 = The amount of data in the FIFO has not yet crossed the threshold programmed at address C8h (default).
1 = The amount of data in the FIFO has crossed the threshold programmed at address C8h.

Line interrupt:

0 = The video line number has not yet been reached (default).
1 = The video line number programmed in address CAh has occurred.

Data interrupt:

0 = No data is available (default).
1 = VBI data is available either in the FIFO or in the VBI data registers.

The interrupt status register A can be polled by the host processor to determine the source of an interrupt. After an interrupt condition is set it can be reset by writing to this register with a 1 in the appropriate bit(s).

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7.2.67 Interrupt Enable Register A

Address C1h
Default 00h

7	6	5	4	3	2	1	0
Reserved	Lock interrupt enable	Cycle complete interrupt enable	Bus error interrupt enable	Reserved	FIFO threshold interrupt enable	Line interrupt enable	Data interrupt enable

Lock interrupt enable:
0 = Disabled (default)
1 = Enabled
Cycle complete interrupt enable:
0 = Disabled (default)
1 = Enabled
Bus error interrupt enable:
0 = Disabled (default)
1 = Enabled
FIFO threshold interrupt enable:
0 = Disabled (default)
1 = Enabled
Line interrupt enable:
0 = Disabled (default)
1 = Enabled
Data interrupt enable:
0 = Disabled (default)
1 = Enabled

The interrupt enable register A is used by the host processor to mask unnecessary interrupt sources. Bits loaded with a 1 allow the corresponding interrupt condition to generate an interrupt on the external pin. Conversely, bits loaded with a 0 mask the corresponding interrupt condition from generating an interrupt on the external pin. This register only affects the interrupt on the external terminal, it does not affect the bits in interrupt status register A. A given condition can set the appropriate bit in the status register and not cause an interrupt on the external terminal. To determine if this device is driving the interrupt terminal either perform a logical AND of interrupt status register A with interrupt enable register A, or check the state of the interrupt A bit in the interrupt configuration register at address C2h.

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7.2.68 Interrupt Configuration Register A

Address C2h
Default 04h

7	6	5	4	3	2	1	0
Reserved					YCbCr enable (VDPOE)	Interrupt A	Interrupt polarity A

YCbCr enable (VDPOE):

0 = YCbCr pins are high impedance.

1 = YCbCr pins are active if other conditions are met (default).

Interrupt A (read only):

0 = Interrupt A is not active on the external pin (default).

1 = Interrupt A is active on the external pin.

Interrupt polarity A:

0 = Interrupt A is active low (default).

1 = Interrupt A is active high.

Interrupt configuration register A is used to configure the polarity of the external interrupt terminal. When interrupt A is configured as active low, the terminal is driven low when active and high impedance when inactive (open collector). Conversely, when the terminal is configured as active high, it is driven high when active and driven low when inactive.

7.2.69 VDP Configuration RAM Register

Address C3h C4h C5h
Default B8h 1Fh 00h

Address	7	6	5	4	3	2	1	0
C3h	Configuration data							
C4h	RAM address (7:0)							
C5h	Reserved							RAM address 8

The configuration RAM data is provided to initialize the VDP with initial constants. The configuration RAM is 512 bytes organized as 32 different configurations of 16 bytes each. The first 12 configurations are defined for the current VBI standards. An additional two configurations can be used as a custom programmed mode for unique standards, such as Gemstar.

Address C3h is used to read or write to the RAM. The RAM internal address counter is automatically incremented with each transaction. Addresses C5h and C4h make up a 9-bit address to load the internal address counter with a specific start address. This can be used to write a subset of the RAM for only those standards of interest. Registers D0h–FBh must all be programmed with FFh before writing or reading the configuration RAM. Full field mode (CFh) must be disabled as well.

The suggested RAM contents are shown in Table 7-11. All values are hexadecimal.

Table 7-11. VBI Configuration RAM for Signals With Pedestal

INDEX	ADDRESS	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
WST SECAM	000	AA	AA	FF	FF	E7	2E	20	A6	E4	B4	0E	0	7	0	10	0
WST SECAM	010	AA	AA	FF	FF	E7	2E	20	A6	E4	B4	0E	0	7	0	10	0
WST PAL B	020	AA	AA	FF	FF	27	2E	20	AB	A4	72	10	0	7	0	10	0
WST PAL B	030	AA	AA	FF	FF	27	2E	20	AB	A4	72	10	0	7	0	10	0
WST PAL C	040	AA	AA	FF	FF	E7	2E	20	22	A4	98	0D	0	0	0	10	0
WST PAL C	050	AA	AA	FF	FF	E7	2E	20	22	A4	98	0D	0	0	0	10	0
WST NTSC	060	AA	AA	FF	FF	27	2E	20	23	63	93	0D	0	0	0	10	0
WST NTSC	070	AA	AA	FF	FF	27	2E	20	23	63	93	0D	0	0	0	10	0
NABTS, NTSC	080	AA	AA	FF	FF	E7	2E	20	A2	63	93	0D	0	7	0	15	0

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Table 7-11. VBI Configuration RAM for Signals With Pedestal (continued)

INDEX	ADDRESS	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
NABTS, NTSC	090	AA	AA	FF	FF	E7	2E	20	A2	63	93	0D	0	7	0	15	0
NABTS, NTSC-J	0A0	AA	AA	FF	FF	A7	2E	20	A3	63	93	0D	0	7	0	10	0
NABTS, NTSC-J	0B0	AA	AA	FF	FF	A7	2E	20	A3	63	93	0D	0	7	0	10	0
CC, PAL/SECAM	0C0	AA	2A	FF	3F	04	51	6E	02	A4	7B	09	0	0	0	27	0
CC, PAL/SECAM	0D0	AA	2A	FF	3F	04	51	6E	02	A4	7B	09	0	0	0	27	0
CC, NTSC	0E0	AA	2A	FF	3F	04	51	6E	02	63	8C	09	0	0	0	27	0
CC, NTSC	0F0	AA	2A	FF	3F	04	51	6E	02	63	8C	09	0	0	0	27	0
WSS/CGMS-A, PAL/SECAM	100	5B	55	C5	FF	0	71	6E	42	A4	CD	0F	0	0	0	3A	0
WSS/CGMS-A, PAL/SECAM	110	5B	55	C5	FF	0	71	6E	42	A4	CD	0F	0	0	0	3A	0
WSS/CGMS-A, NTSC C	120	38	00	3F	00	0	71	6E	43	63	7C	08	0	0	0	39	0
WSS/CGMS-A, NTSC C	130	38	00	3F	00	0	71	6E	43	63	7C	08	0	0	0	39	0
VITC, PAL/SECAM	140	0	0	0	0	0	8F	6D	49	A4	85	08	0	0	0	4C	0
VITC, PAL/SECAM	150	0	0	0	0	0	8F	6D	49	A4	85	08	0	0	0	4C	0
VITC, NTSC	160	0	0	0	0	0	8F	6D	49	63	94	08	0	0	0	4C	0
VITC, NTSC	170	0	0	0	0	0	8F	6D	49	63	94	08	0	0	0	4C	0
VPS, PAL	180	AA	AA	FF	FF	BA	CE	2B	8D	A4	DA	0B	0	7	0	60	0
VPS, PAL	190	AA	AA	FF	FF	BA	CE	2B	8D	A4	DA	0B	0	7	0	60	0
Gemstar 2x Custom 1	1A0	99	99	FF	FF	05	51	6E	05	63	18	13	80	00	00	60	00
Gemstar 2x Custom 1	1B0	99	99	FF	FF	05	51	6E	05	63	18	13	80	00	00	60	00
Custom 2	1C0	Programmable															
Custom 2	1D0	Programmable															

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7.2.70 VDP Status Register

Address C6h

7	6	5	4	3	2	1	0
FIFO full error	FIFO empty	TTX available	CC field 1 available	CC field 2 available	WSS/CGMS-A available	VPS/Gemstar 2x available	VITC available

The VDP status register indicates whether data is available in either the FIFO or data registers, and status information about the FIFO. Reading data from the corresponding register does not clear the status flags automatically. These flags are only reset by writing a 1 to the respective bit. However, bit 6 is updated automatically.

FIFO full error:

0 = No FIFO full error

1 = FIFO was full during a write to FIFO.

The FIFO full error flag is set when the current line of VBI data can not enter the FIFO. For example, if the FIFO has only ten bytes left and teletext is the current VBI line, the FIFO full error flag is set, but no data is written because the entire teletext line will not fit. However, if the next VBI line is closed caption requiring only two bytes of data plus the header, this goes into the FIFO (even if the full error flag is set).

FIFO empty:

0 = FIFO is not empty.

1 = FIFO is empty.

TTX available:

0 = Teletext data is not available.

1 = Teletext data is available.

CC field 1 available:

0 = Closed caption data from field 1 is not available.

1 = Closed caption data from field 1 is available.

CC field 2 available:

0 = Closed caption data from field 2 is not available.

1 = Closed caption data from field 2 is available.

WSS/CGMS-A available:

0 = WSS/CGMS-A data is not available.

1 = WSS/CGMS-A data is available.

VPS/Gemstar 2x available

0 = VPS/Gemstar 2x data is not available.

1 = VPS/Gemstar 2x data is available.

VITC available:

0 = VITC data is not available.

1 = VITC data is available.

7.2.71 FIFO Word Count Register

Address C7h

7	6	5	4	3	2	1	0
Number of words							

This register provides the number of words in the FIFO. One word equals two bytes.

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7.2.72 FIFO Interrupt Threshold Register

Address C8h
Default 80h

7	6	5	4	3	2	1	0
Number of words							

This register is programmed to trigger an interrupt when the number of words in the FIFO exceeds this value (default 80h). This interrupt must be enabled at address C1h. One word equals two bytes.

7.2.73 FIFO Reset Register

Address C9h
Default 00h

7	6	5	4	3	2	1	0
Any data							

Writing any data to this register resets the FIFO and clears any data present in both the FIFO and the VDP registers.

7.2.74 Line Number Interrupt Register

Address CAh
Default 00h

7	6	5	4	3	2	1	0
Field 1 enable	Field 2 enable	Line number					

This register is programmed to trigger an interrupt when the video line number matches this value in bits 5:0. This interrupt must be enabled at address C1h. The value of 0 or 1 does not generate an interrupt.

Field 1 enable:

0 = Disabled (default)

1 = Enabled

Field 2 enable:

0 = Disabled (default)

1 = Enabled

Line number: (default 00h)

7.2.75 Pixel Alignment Registers

Address CBh CCh
Default 4Eh 00h

Address	7	6	5	4	3	2	1	0
CBh	Switch pixel [7:0]							
CCh	Reserved						Switch pixel [9:8]	

These registers form a 10-bit horizontal pixel position from the falling edge of sync, where the VDP controller initiates the program from one line standard to the next line standard; for example, the previous line of teletext to the next line of closed caption. This value must be set so that the switch occurs after the previous transaction has cleared the delay in the VDP, but early enough to allow the new values to be programmed before the current settings are required.

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7.2.76 FIFO Output Control Register

Address CDh
Default 01h

7	6	5	4	3	2	1	0
Reserved							Host access enable

This register is programmed to allow I^2C access to the FIFO or allowing all VDP data to go out the video port.

Host access enable:

0 = Output FIFO data to the video output Y[7:0]
1 = Allow I^2C access to the FIFO data (default)

7.2.77 Full Field Enable Register

Address CFh
Default 00h

7	6	5	4	3	2	1	0
Reserved							Full field enable

This register enables the full field mode. In this mode, all lines outside the vertical blank area and all lines in the line mode registers programmed with FFh are sliced with the definition of register FCh. Values other than FFh in the line mode registers allow a different slice mode for that particular line.

Full field enable:

0 = Disable full field mode (default)
1 = Enable full field mode

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7.2.78 Line Mode Registers

Address	D0h	D1h–FBh
Default	00h	FFh

Address	7	6	5	4	3	2	1	0
D0h	Line 6 Field 1							
D1h	Line 6 Field 2							
D2h	Line 7 Field 1							
D3h	Line 7 Field 2							
D4h	Line 8 Field 1							
D5h	Line 8 Field 2							
D6h	Line 9 Field 1							
D7h	Line 9 Field 2							
D8h	Line 10 Field 1							
D9h	Line 10 Field 2							
DAh	Line 11 Field 1							
DBh	Line 11 Field 2							
DCh	Line 12 Field 1							
DDh	Line 12 Field 2							
DEh	Line 13 Field 1							
DFh	Line 13 Field 2							
E0h	Line 14 Field 1							
E1h	Line 14 Field 2							
E2h	Line 15 Field 1							
E3h	Line 15 Field 2							
E4h	Line 16 Field 1							
E5h	Line 16 Field 2							
E6h	Line 17 Field 1							
E7h	Line 17 Field 2							
E8h	Line 18 Field 1							
E9h	Line 18 Field 2							
EAh	Line 19 Field 1							
EBh	Line 19 Field 2							
ECh	Line 20 Field 1							
EDh	Line 20 Field 2							
EEh	Line 21 Field 1							
EFh	Line 21 Field 2							
F0h	Line 22 Field 1							
F1h	Line 22 Field 2							
F2h	Line 23 Field 1							
F3h	Line 23 Field 2							
F4h	Line 24 Field 1							
F5h	Line 24 Field 2							
F6h	Line 25 Field 1							
F7h	Line 25 Field 2							
F8h	Line 26 Field 1							
F9h	Line 26 Field 2							
FAh	Line 27 Field 1							
FBh	Line 27 Field 2							

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These registers program the specific VBI standard at a specific line in the video field.

Bit 7:

0 = Disable filtering of null bytes in closed caption modes.

1 = Enable filtering of null bytes in closed caption modes (default).

In teletext modes, bit 7 enables the data filter function for that particular line. If it is set to 0, the data filter passes all data on that line.

Bit 6:

0 = Send VBI data to registers only.

1 = Send VBI data to FIFO and the registers. Teletext data only goes to FIFO. (default)

Bit 5:

0 = Allow VBI data with errors in the FIFO.

1 = Do not allow VBI data with errors in the FIFO (default).

Bit 4:

0 = Do not enable error detection and correction.

1 = Enable error detection and correction (when bits [3:0] = 1 2, 3, and 4 only) (default).

Bits [3:0]:

0000 = WST SECAM
0001 = WST PAL B
0010 = WST PAL C
0011 = WST NTSC
0100 = NABTS NTSC C
0101 = NABTS NTSC D
0110 = CC PAL
0111 = CC NTSC
1000 = WSS/CGMS-A PAL
1001 = WSS/CGMS-A NTSC
1010 = VITC PAL
1011 = VITC NTSC
1100 = VPS PAL
1101 = Gemstar 2x Custom 1
1110 = Custom 2
1111 = Active video (VDP off) (default)

A value of FFh in the line mode registers is required for any line to be sliced as part of the full field mode.

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7.2.79 Full Field Mode Register

Address FCh
Default 7Fh

7	6	5	4	3	2	1	0	
Full field mode								

This register programs the specific VBI standard for full field mode. It can be any VBI standard. Individual line settings take priority over the full field register. This allows each VBI line to be programmed independently but have the remaining lines in full field mode. The full field mode register has the same definitions as the line mode registers (default 7Fh).

7.2.80 Decoder Write Enable Register

Address FEh
Default 0Fh

7	6	5	4	3	2	1	0
Reserved				Decoder 4	Decoder 3	Decoder 2	Decoder 1

This register controls which of the four decoder cores receives I^2C write transactions. A 1 in the corresponding bit position enables the decoder to receive write commands.

Any combination of decoders can be configured to receive write commands, allowing all four decoders to be programmed concurrently.

7.2.81 Decoder Read Enable Register

Address FFh
Default 00h

7	6	5	4	3	2	1	0
Reserved				Decoder 4	Decoder 3	Decoder 2	Decoder 1

This register controls which of the four decoder cores responds to I^2C read transactions. A 1 in the corresponding bit position enables the decoder to respond to read commands.

If more than one decoder is enabled for reading, only the lowest numbered decoder responds. Reads from multiple decoders at the same time is not possible.

Note that when register 0xFE is written to with any value, register 0xFF is set to 0x00. Likewise, when register 0xFF is written to with any value, register 0xFE is set to 0x00.

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7.3 Indirect Register Definitions

To write to the TVP5154A indirect registers, it is required that the registers be unlocked using a password. The password prevents undesirable writes into the device at start-up due to power surges, for example.

The following example demonstrates the method for unlocking the indirect registers.

After writing to the desired indirect registers described in the following text, it is recommended that the device be locked again.

- Unlock the device
  1. Write 0x51 to I2C_0x21. //MSB data
  2. Write 0x54 to I2C_0x22. //LSB data
  3. Write 0xFF to I2C_0x23. //Data address
  4. Write 0x04 to I2C_0x24. //Write command
- Lock the device
  1. Write 0x00 to I2C_0x21. //MSB data
  2. Write 0x00 to I2C_0x22. //LSB data
  3. Write 0xFF to I2C_0x23. //Data address
  4. Write 0x04 to I2C_0x24. //Write command

Indirect registers are written to by performing the following I^2C transaction:

START : DEVICE_ID_w : 0x21 : DATA_HIGH : STOP
START : DEVICE_ID_w : 0x22 : DATA_LOW : STOP
START : DEVICE_ID_w : 0x23 : ADDRESS_LOW : STOP
START : DEVICE_ID_w : 0x24 : WR_STROBE : STOP

To read from an indirect register, the following I^2C transaction should be performed:

START : DEVICE_ID_w : 0x23 : ADDRESS_LOW : STOP
START : DEVICE_ID_w : 0x24 : RD_STROBE : STOP
START : DEVICE_ID_r : 0x21 : data_msb : STOP
START : DEVICE_ID_r : 0x22 : data_lsb : STOP

Where:

DEVICE_ID_w is the selected TVP5154A device ID with the read/write bit (LSB) set to write.

DEVICE_ID_r is the selected TVP5154A device ID with the read/write bit (LSB) set to read.

ADDRESS_LOW is the low byte of the register address.

WR_STROBE is 0x06.

RD_STROBE is 0x05.

Note, the upper byte of the address is not directly used but is replaced by the corresponding STROBE signal.

Each indirect register is 16 bits wide.

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7.3.1 DID Control

Address 36Ah
Default 000h

7	6	5	4	3	2	1	0
Unscaled field 1 DID				Unscaled field 0 DID			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Scaled field 1 DID				Scaled field 0 DID			

This register controls the value of the EAV DID bytes for scaled and unscaled data. The value for each field can be independently set, allowing identification of both which field is being processed and whether the data comes from the scaled or unscaled channel.

7.3.2 Misc Control

Address 36Bh
Default 0Ch

7	6	5	4	3	2	1	0
Clock rate				Clock OE		Clock edge	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Scaled blank data							

Scaled blank data:

When no active scaled data is available, this value is output during the active video region.

Clock rate:

This register controls various clock modes. Since this register is modified by the device during normal operation, the clock rate bits should not be modified by the user.

Clock OE:

This register controls various clock modes. Since this register is modified by the device during normal operation, the clock rate bits should not be modified by the user.

Clock edge:

This register controls various clock modes. Since this register is modified by the device during normal operation, the clock rate bits should not be modified by the user.

7.3.3 Interleave Field Control 1

Address 36Dh
Default 0h

7	6	5	4	3	2	1	0
End pixel count[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field count				Reserved	Blank timing	End pixel count[9:8]	

End pixel count:

Pixel count at which the frame status is updated. Do not change this value.

Blank timing:

0: No timing signals are generated for blank fields.

1: H, V, and F timing generated for blank fields based on unscaled video timing sequences

Field count:

Number of output fields in field interleaved sequence

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7.3.4 Interleave Field Control 2

Address 36Eh
Default 0h

7	6	5	4	3	2	1	0
Field mode(3)		Field mode(2)		Field mode(1)		Field mode(0)	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field mode(7)		Field mode(6)		Field mode(5)		Field mode(4)	

7.3.5 Interleave Field Control 3

Address 36Fh
Default 0h

7	6	5	4	3	2	1	0
Field mode(11)		Field mode(10)		Field mode(9)		Field mode(8)	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field mode(15)		Field mode(14)		Field mode(13)		Field mode(12)	

These registers allow the output data stream to toggle between unscaled and scaled data on a field basis. By setting Field mode[n] appropriately, it is possible to use the available output bandwidth to interleave unscaled and scaled frames to achieve reduced frame rates, while still maintaining compatibility with legacy data receivers. These registers can also be used to reduce the frame rate of either unscaled data or scaled data by disabling fields within the sequence.

A counter automatically moves from Field mode[0] to Field mode[n] where n can be 0 through 15, then returns back to Field mode[0]. Depending on the value of Field mode[n], either unscaled data, scaled data, or no data is sent for the current frame.

00 = Unscaled data
01 = Null frame (no SAV/EAV sequence will be generated)
10 = Scaled data
11 = Reserved

The values programmed for registers 3A8h and 3A9h are different for NTSC (also NTSC4.43 and PAL-M) and for PAL (also PAL-Nc and SECAM).

7.3.6 Vertical Scaling Field 1 Control

Address 3A8h
Default 0h

7	6	5	4	3	2	1	0
V_Field1[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							V_Field1[8]

Vertical scaling initial value in field 1 [8:0]: Initial value of vertical accumulator for field 1

For NTSC:
V_Field1 = (1.5 × V_Field2) – 128
If V_Field 1 is negative, add V_Field2 to V_Field1 and add V_Field2 to V_Field2 until V_Field1 is positive.
For PAL:
V_Field1 = (Vdesired/Vactive) × 256

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7.3.7 Vertical Scaling Field 2 Control

Address 3A9h
Default 0h

7	6	5	4	3	2	1	0
V_Field2[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							V_Field2[8]

Vertical scaling initial value in field 2 [8:0]: Initial value of vertical accumulator for field 2

For NTSC:
V_Field2 = (Vdesired/Vactive) × 256
For PAL:
V_Field2 = (1.5 × V_Field1) – 128
If V_Field 2 is negative, add V_Field1 to V_Field2 and add V_Field1 to V_Field1 until V_Field2 is positive.

7.3.8 Scaler Output Active Pixels

Address 3ABh
Default 2D0h

7	6	5	4	3	2	1	0
SCAL_PIXEL[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved						SCAL_PIXEL[9:8]	

SCAL_PIXEL [9:0]: Scaler active pixel outputs per line

7.3.9 Vertical Scaling Control

Address 3ACh
Default 2100h

7	6	5	4	3	2	1	0
VERT_COEF[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved		1	Enable	Reserved			VERT_COEF[8]

Enabled: Enable vertical and horizontal scaler
0 = Disable scaler (default)
1 = Enable scaler
VERT_COEF [8:0]: Vertical scaling coefficient
VERT_COEF = (Vdesired/Vactive) × 256

7.3.10 Horizontal Scaling Control

Address 3ADh
Default 400h

7	6	5	4	3	2	1	0
HORZ_COEF[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved	HORZ_COEF[14:8]						

HORZ_COEF[14:0]: Horizontal scaling coefficient, MSB five bits are integer values and LSB ten bits are fraction numbers.
HORZ_COEF = Hactive/Hdesired

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8 Scaler Configuration

8.1 Overview

The TVP5154A contains four independent scalers, one for each video decoder channel. Each scaler is able to filter and scale both horizontally and vertically to different ratios.

Horizontally, a 7-tap poly-phase filter is used to ensure optimal scaling performance and can be configured to scale to any output size below the input resolution, in decrements of two pixels. Vertically a running average filter is used to filter vertically and can be configured to scale to any output size below the input resolution.

When scaling horizontally, the output pixels are packed together to allow continuous reading of the pixels. AVID should be configured so that it qualifies the active pixels, allowing the receiving back end to ignore nonactive pixels. When scaling vertically, inactive lines are not removed from the output since there is no internal frame memory. The receiving back end must use AVID to qualify active lines/pixels. AVID can be configured to be either active or inactive during invalid output lines.

Due to the fact that vertical scaling is performed on a field basis, it is possible that the vertical resolution will be reduced due to filtering across lines within the field, rather than adjacent lines in the frame. Aliasing will not occur, but the output image will appear soft vertically. If the desired scaling ration is 0.5, this can be achieved by simply ignoring every other field. This maintains sharpness, but may introduce aliasing artifacts.

8.2 Horizontal Scaling

8.2.1 Registers

The horizontal scaler uses a 32-phase polymorphic filter. Excellent performance can be achieved by using the set of coefficients programmed into the 5154 for all scaling ratios.

It is necessary to program the input and output scaling control registers (3AB and 3AD).

Figure 8-1 shows how data is packed horizontally when scaled.

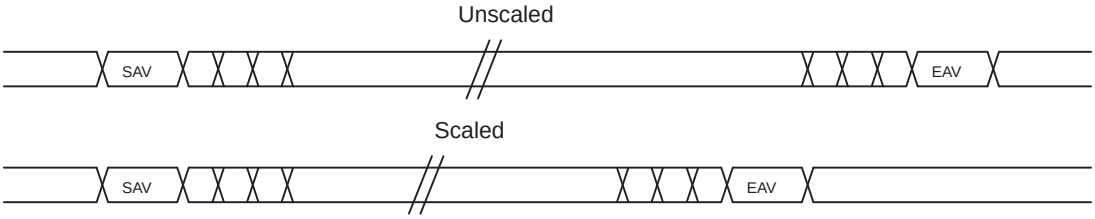

Figure 8-1. Unscaled and Scaled Pixel Data Alignment

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8.3 Vertical Scaling

8.3.1 Registers

The vertical scaler implements a weighted running average filter, which requires the initial weights and the ratio registers to be configured.

Additionally, it is necessary to program the input and output scaling control registers (3A8, 3A9, and 3AC).

Figure 8-2 shows the active and inactive data lines when scaled vertically.

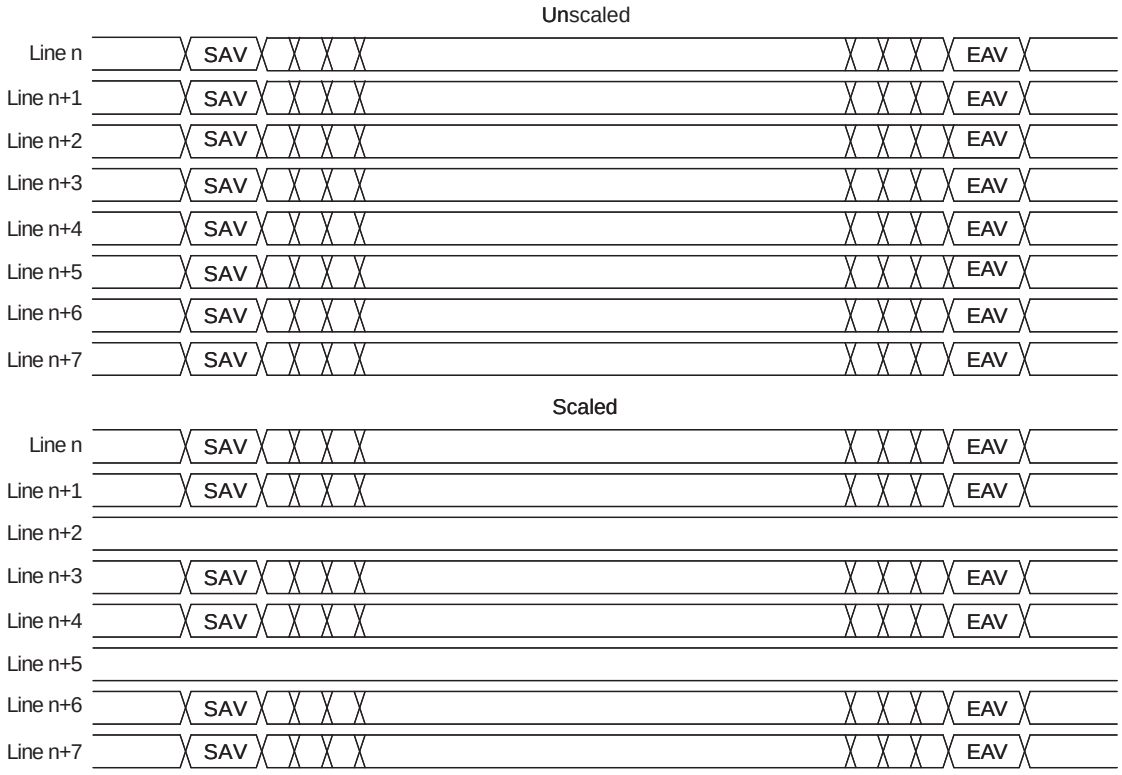

Figure 8-2. Unscaled and Scaled Vertical Data Formatting

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8.4 Field Interleaving

In systems where either there are insufficient video ports on the back end processor to accommodate both scaled and unscaled video streams, or where the back end processor does not have sufficient processing power to perform compression on the unscaled image at the same time as other video processing, such as composting of scaled images for display, it is possible to configure the TVP5154A to output different image types on consecutive fields. In this configuration, the field rates for each of the scaled and unscaled images is reduced to accommodate the interleaving of fields, while maintaining a 27-MHz pixel clock.

This is useful in video recording systems that are required to display a scaled image but still wish to compress and store full resolution images, albeit at reduced field rates.

Field interleaving can generate a sequence of up to 16 fields, where each field can be either unscaled, scaled, or blank.

8.4.1 Registers

The field loop count register controls how many fields are in the sequence. The field mode registers control the output field type for each field.

Figure 8-3 shows how to configure field interleaving for a sequence of five fields where the first field is unscaled, the second field is scaled, the third field is blank, the fourth field is scaled, and the fifth field is blank.

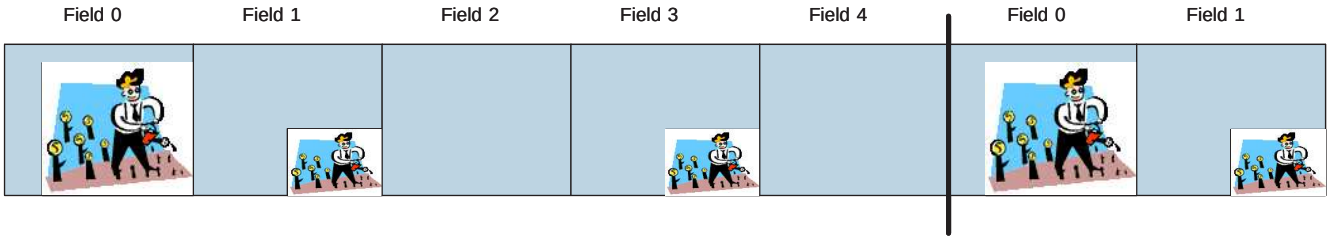

Figure 8-3. Field Interleaving

Various additional registers exist to configure how the TVP5154A indicates to the back-end processor the state of the current field. The Output Control register 1Fh allows the scaled/unscaled status to be indicated by the upper bit of the SAV/EAV codes. The Output Control register 1Fh also allows the scaled/unscaled status to be indicated by the DID codes of ancillary data.

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9 Electrical Specifications

9.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
	Supply voltage range	IOVDD to DGND	–0.5 to 3.6	V
		DVDD to DGND	–0.5 to 2	
		PLL_AVDD to PLL_AGND	–0.5 to 2	
		AVDD to AGND	–0.5 to 2	
	Digital input voltage range, V_I to DGND		–0.5 to 3.6	V
	Input voltage range, XIN to PLL_GND		–0.5 to 2	V
	Analog input voltage range, A_I to AGND		–0.2 to 2	V
	Digital output voltage range, V_O to DGND		–0.5 to 3.6	V
T_A	Operating free-air temperature range	Commercial	0 to 70	°C
		Industrial	–40 to 85	
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

9.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
IOVDD	Digital I/O supply voltage		3.0	3.3	3.6	V
DVDD	Digital supply voltage		1.65	1.8	1.95	V
PLL_AVDD	Analog PLL supply voltage		1.65	1.8	1.95	V
AVDD	Analog core supply voltage		1.65	1.8	1.95	V
$V_{I(P–P)}$	Analog input voltage (ac-coupling necessary)		0		0.75	V
V_{IH}	Digital input voltage high		0.7 IOVDD			V
V_{IL}	Digital input voltage low				0.3 IOVDD	V
V_{IH_XIN}	XIN input voltage high		0.7 PLL_AVDD			V
V_{IL_XIN}	XIN input voltage low				0.3 PLL_AVDD	V
I_{OH}	High-level output current		2	4		mA
I_{OL}	Low-level output current		–2	–4		mA
I_{OH_CLK}	CLK high-level output current		4	8		mA
I_{OL_CLK}	CLK low-level output current		–4	–8		mA
T_A	Operating free-air temperature	Commercial	0		70	°C
		Industrial	–40		85	

9.3 Reference Clock Specifications

		MIN	NOM	MAX	UNIT
f	Frequency		14.31818		MHz
Δf	Frequency tolerance(1)	–50		+50	ppm

(1) Specified by design

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9.4 Electrical Characteristics

For typical values: Nominal conditions, T_A = 25°C
For minimum/maximum values: Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
DC						
$I_{DD(IO_D)}$	I/O digital supply current at 27 MHz	Color bar input (2)		46	52	mA
	I/O digital supply current at 54 MHz	Color bar input (2)		84	90	mA
$I_{DD(D)}$	Digital supply current	Color bar input (2)		154	174	mA
$I_{DD(PLL_A)}$	Analog PLL supply current	Color bar input (2)		20	29	mA
$I_{DD(A)}$	Analog core supply current	Color bar input (2)		134	168	mA
P_{TOT}	Total power dissipation, normal mode at 27 MHz	Color bar input (2)		706	910	mW
	Total power dissipation, normal mode at 54 MHz	Color bar input (2)		832	1050	mW
C_i	Input capacitance (3)				10	pF
V_{OH}	Output voltage high	I_{OH} = 2 mA	0.8 IOVDD			V
V_{OL}	Output voltage low	I_{OL} = –2 mA			0.22 IOVDD	V
V_{OH_CLK}	CLK output voltage high	I_{OH} = 4 mA	0.8 IOVDD			V
V_{OL_CLK}	CLK output voltage low	I_{OL} = –4 mA			0.22 IOVDD	V
I_{IH}	High-level input current	$V_I = V_{IH}$			±22	µA
I_{IL}	Low-level input current	$V_I = V_{IL}$			±22	µA
Analog Processing and ADCs (at FS = 30 MSPS)						
Z_i	Input impedance, analog video inputs	By design	200	500		kΩ
C_i	Input capacitance, analog video inputs	By design			10	pF
$V_{I(pp)}$	Input voltage range(4)	$C_{coupling}$ = 0.1 µF	0		0.75	V
DG	Gain control minimum			0		dB
DG	Gain control maximum			12		dB
DNL	DC differential nonlinearity	A/D only		±0.5	±1	LSB
INL	DC integral nonlinearity	A/D only		±1	±2.5	LSB
Fr	Frequency response	6 MHz		–0.9	–3	dB
SNR	Signal-to-noise ratio	1 MHz, 0.5 V_{P-P}	48	50		dB
NS	Noise spectrum ∞	50% flat field	48	50		dB
DP	Differential phase (5)	Modulated ramp		1.5		deg
DG	Differential gain (5)	Modulated ramp		0.5		%

(1) Measured with a load of 15 pF.
(2) For typical measurements only
(3) Specified by design
(4) The 0.75-V maximum applies to the sync-chroma amplitude, not sync-white. The recommended termination resistors are 37.4 Ω.
(5) Specified by design

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9.5 Timing Requirements

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
	Duty cycle SCL			50		%
t_1	CLK high time (at 27 MHz)		13.5			ns
t_2	CLK low time (at 27 MHz)		13.5			ns
t_3	CLK fall time (at 27 MHz)	90% to 10%			5	ns
t_4	CLK rise time (at 27 MHz)	10% to 90%			5	ns
t_5	Output hold time		10			ns
t_6	Output delay time				25	ns
t_7	Output hold time		4			ns
t_8	Output delay time				16.5	ns
t_9	Data period			18.5		ns
t_{10}	Output hold time		4			ns
t_{11}	Output delay time				16.5	ns
t_{12}	Data period			18.5		ns
t_{13}	CLK high time (at 54 MHz)		3			ns
t_{14}	CLK low time (at 54 MHz)		3			ns
t_{15}	CLK fall time (at 54 MHz)	90% to 10%			6	ns
t_{16}	CLK rise time (at 54 MHz)	10% to 90%			6	ns

(1) Measured with a load of 15 pF for 27-MHz signals, 25 pF for 54-MHz signals. Specified by design.

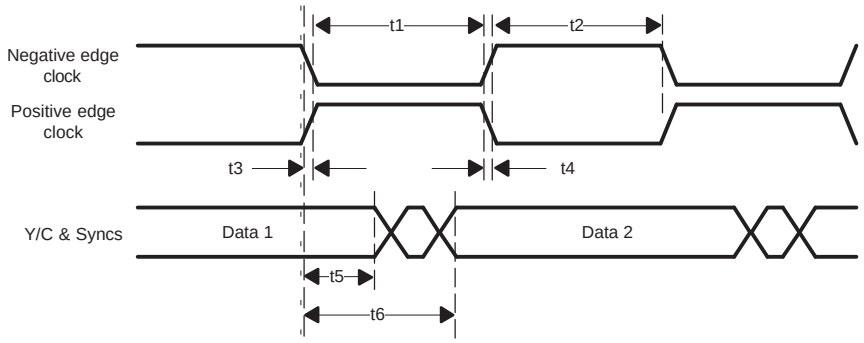

Figure 9-1. Output Modes 0 and 1: Clocks, Video Data, and Sync

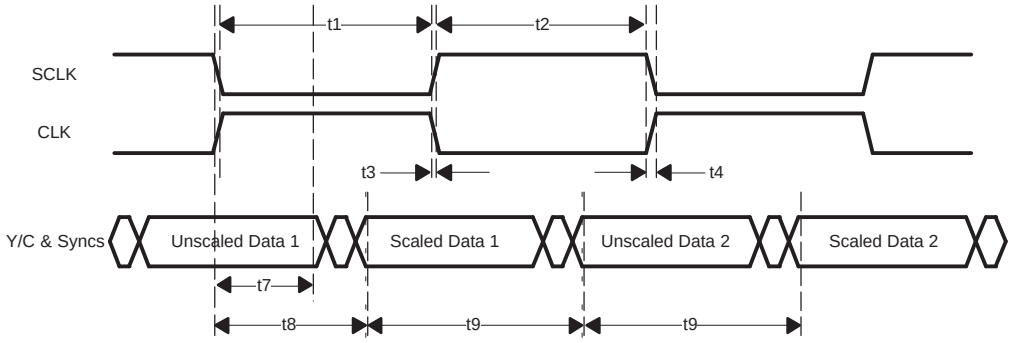

Figure 9-2. Output Mode 2: Clocks, Video Data, and Sync

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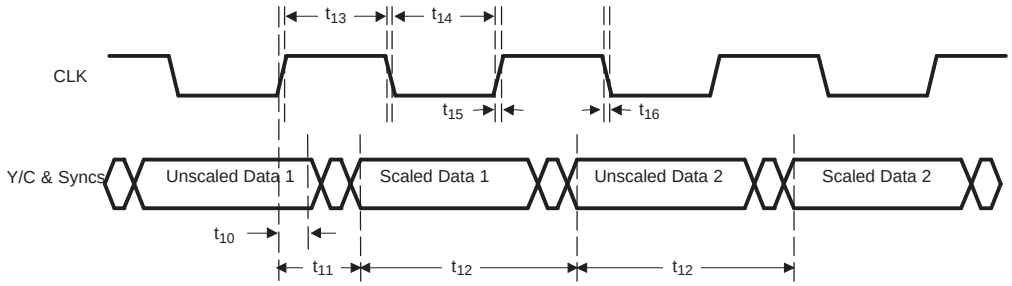

Figure 9-3. Output Mode 3: Clock, Video Data, and Sync (Positive Edge Clock)

9.6 I²C Host Port Timing

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_1	Bus free time, between STOP and START		1.3		µs
t_2	Setup time, (repeated) START condition		0.6		µs
t_3	Hold time, (repeated) START condition		0.6		µs
t_4	Setup time, STOP condition		0.6		ns
t_5	Data setup time		100		ns
t_6	Data hold time		0	0.9	µs
t_7	Rise time, VC1(SDA) and VC0(SCL) signal	Specified by design		250	ns
t_8	Fall time, VC1(SDA) and VC0(SCL) signal	Specified by design		250	ns
C_b	Capacitive load for each bus line	Specified by design		400	pF
f_{I2C}	I²C clock frequency			400	kHz

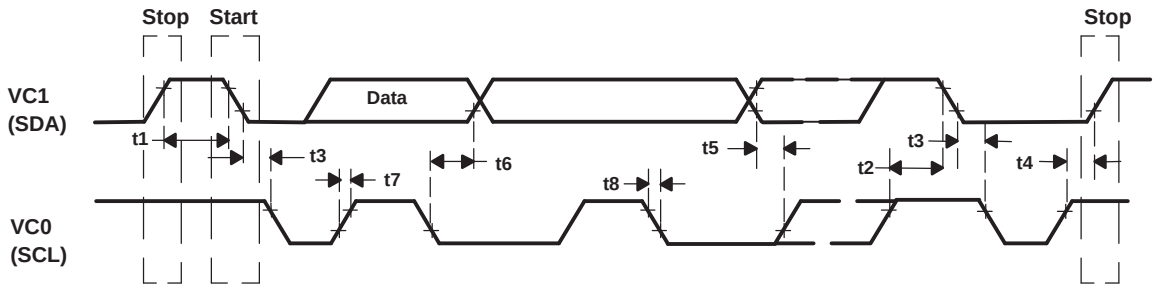

Figure 9-4. I²C Host Port Timing

9.7 Thermal Specifications

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, still air	Thermal pad soldered to 4-layer High-K PCB		17.17		°C/W
θ_{JC}	Junction-to-case thermal resistance, still air	Thermal pad soldered to 4-layer High-K PCB		0.12		°C/W
$T_{J(MAX)}$	Maximum junction temperature for reliable operation				105	°C

(1) The exposed thermal pad must be soldered to a JEDEC High-K PCB with adequate ground plane.

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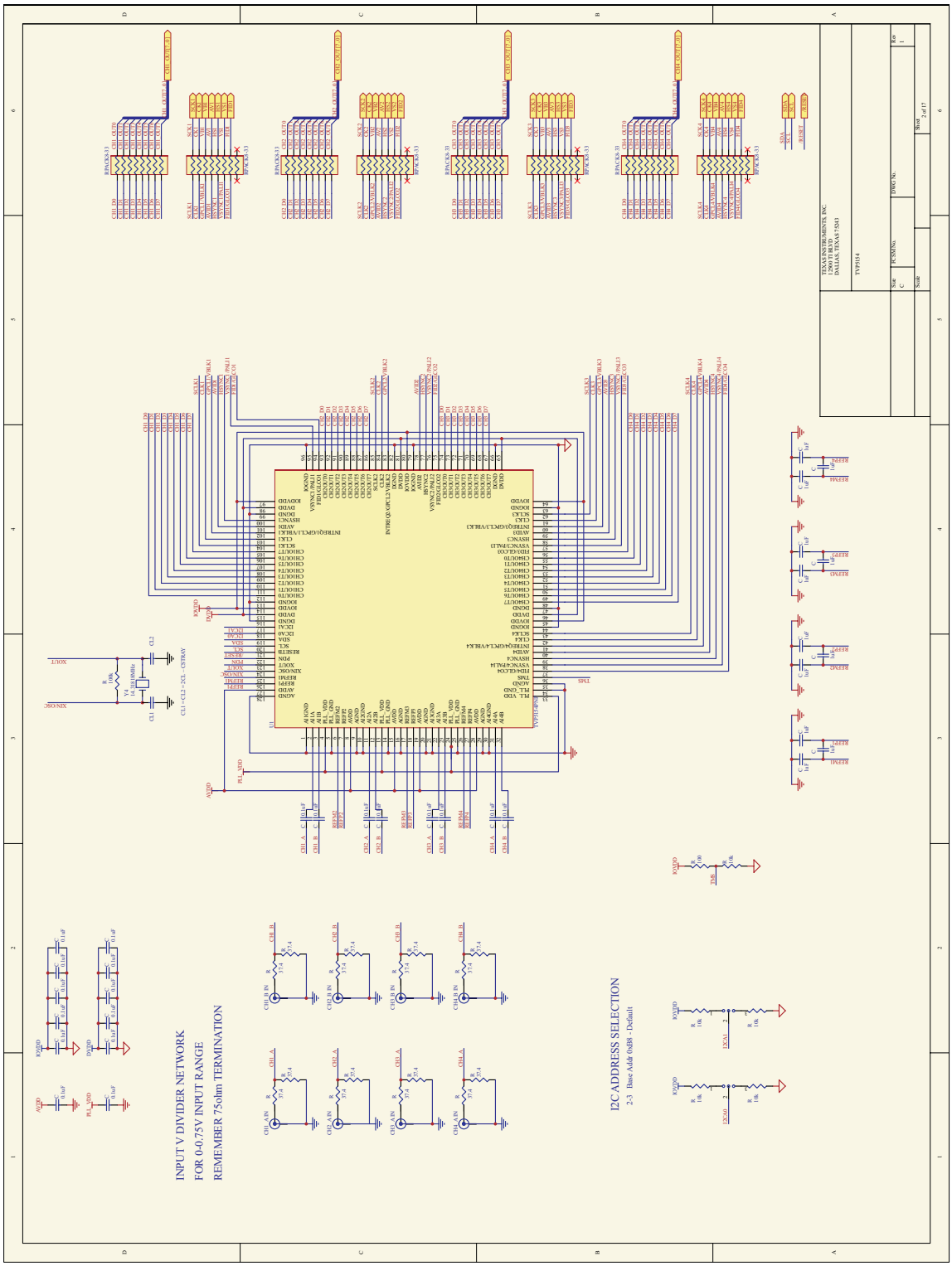
10 Schematic



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11 Revision History

Table 11-1. Revision History

REVISION	COMMENTS
SLES214	Initial release
SLES214A	Industrial temperature devices added
SLES214B	Section 1.1, NTSC-J and PAL-Nc support added to feature list. Section 1.2, Application list modified. Section 1.4, Related Products modified. Section 1.5, Trademarks added. Section 1.6, Document conventions added. Section 2, Figure 2-1, Block diagram modified. Section 3.2, I/O type modified for ground pins. Section 4.3, Figure 4-1, Chroma trap filter characteristics for NTSC added. Section 4.3, Figure 4-2, Chroma trap filter characteristics for PAL added. Section 4.4, Figure 4-3, Color low-pass filter characteristics added. Section 4.8, Table 4-1, CGMS-A and Gemstar 2x support added. Section 4.11, Table 4-3, NTSC-J and PAL-Nc support added. Lines per frame and color subcarrier frequency columns also added. Section 6, Figure 6.1, Crystal parallel resistor recommendation added. Section 7.3, Reset and power down information added. Section 8.1, Table 8-1, CGMS-A support added to address 94h-99h. Gemstar 2x support added to address 9Ah-A6h. Section 8.2.2, Automatic offset control description removed. Section 8.2.3, Changed white peak to composite peak. Recommendations added. Section 8.2.10, Brightness control register description modified. Section 8.2.11, Color saturation control register description modified. Section 8.2.13, Contrast control register description modified. Section 8.2.34, NTSC-J support added. Section 8.2.39, Reference to ITU-R BT.656-5 standard added. Section 8.2.50, Status Register #3 description modified. Section 8.2.52, Table 8-10, NTSC-J and PAL-Nc support added. Section 8.2.54, CGMS-A support added. Section 8.2.63, Recommended VBI Configuration RAM settings modifications. Gemstar support included. Section 8.2.64, CGMS-A and Gemstar 2x support added. Section 8.2.72, CGMS-A and Gemstar 2x support added. Section 10.1, Units for temperature corrected. Section 10.2, Units for temperature corrected. Section 10.3, Table formatting modified. Made minor editorial changes (throughout).
SLES214C	Changed order of some sections in chapters 1, 2, and 3 Section 3.6, Modified when color killer suppresses chrominance processing. Section 9.7, Added thermal specifications. Section 7.2.31, Added Indirect Register Data Section 7.2.32, Added Indirect Register Address Section 7.2.33, Added Indirect Register Read/Write Strobe Section 7.2.44, Added Patch Write Address Section 7.2.45, Added Patch Code Execute Section 7.2.58, Added Patch Read Address

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TVP5154AIPNP	ACTIVE	HTQFP	PNP	128	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TVP5154AI	Samples
TVP5154AIPNPR	ACTIVE	HTQFP	PNP	128	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TVP5154AI	Samples
TVP5154APNP	ACTIVE	HTQFP	PNP	128	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TVP5154A	Samples
TVP5154APNPR	ACTIVE	HTQFP	PNP	128	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TVP5154A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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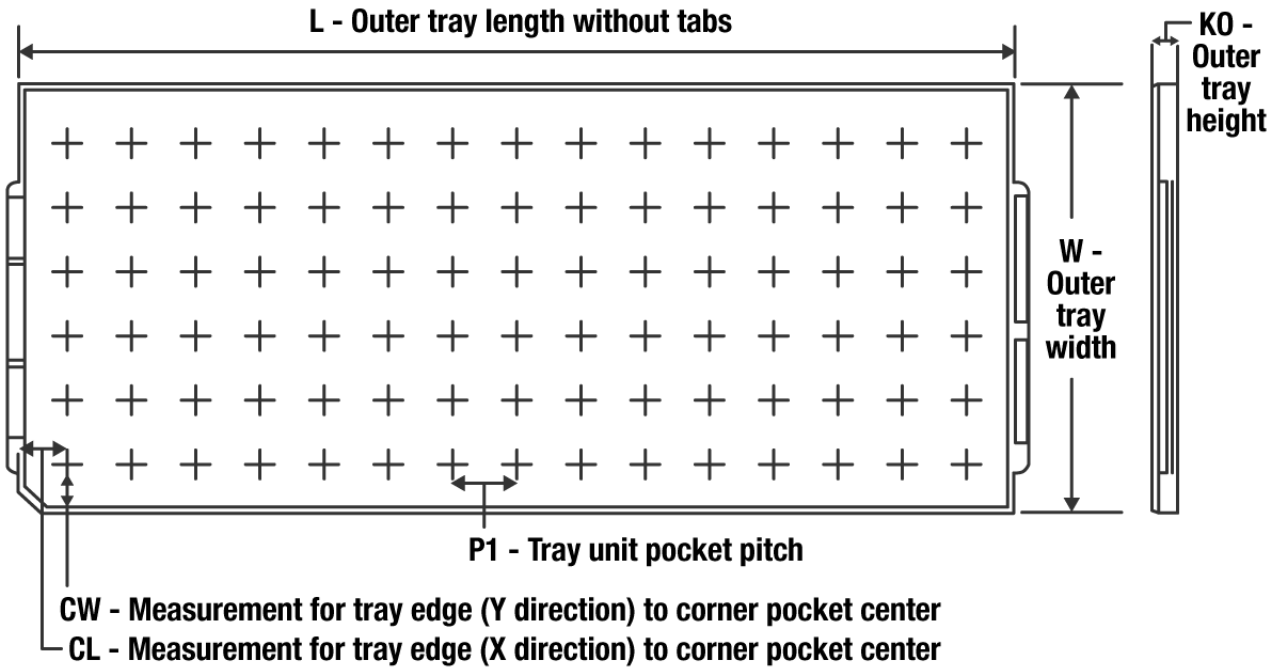
TRAY

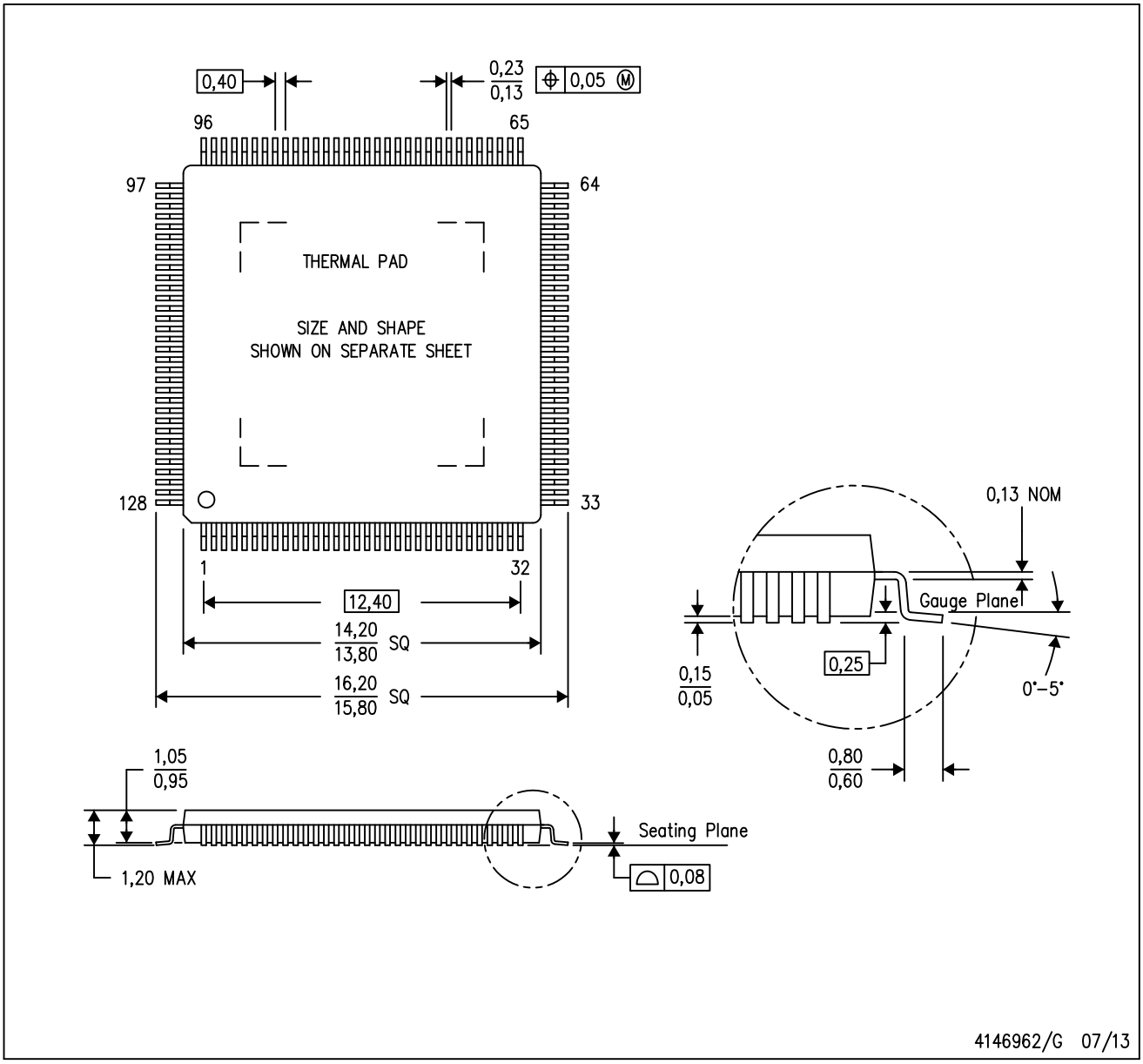


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TVP5154AIPNP	PNP	HTQFP	128	90	6 X 15	150	315	135.9	7620	20.3	15.4	15.45
TVP5154APNP	PNP	HTQFP	128	90	6 X 15	150	315	135.9	7620	20.3	15.4	15.45

PNP (S–PQFP–G128) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

PowerPAD is a trademark of Texas Instruments.

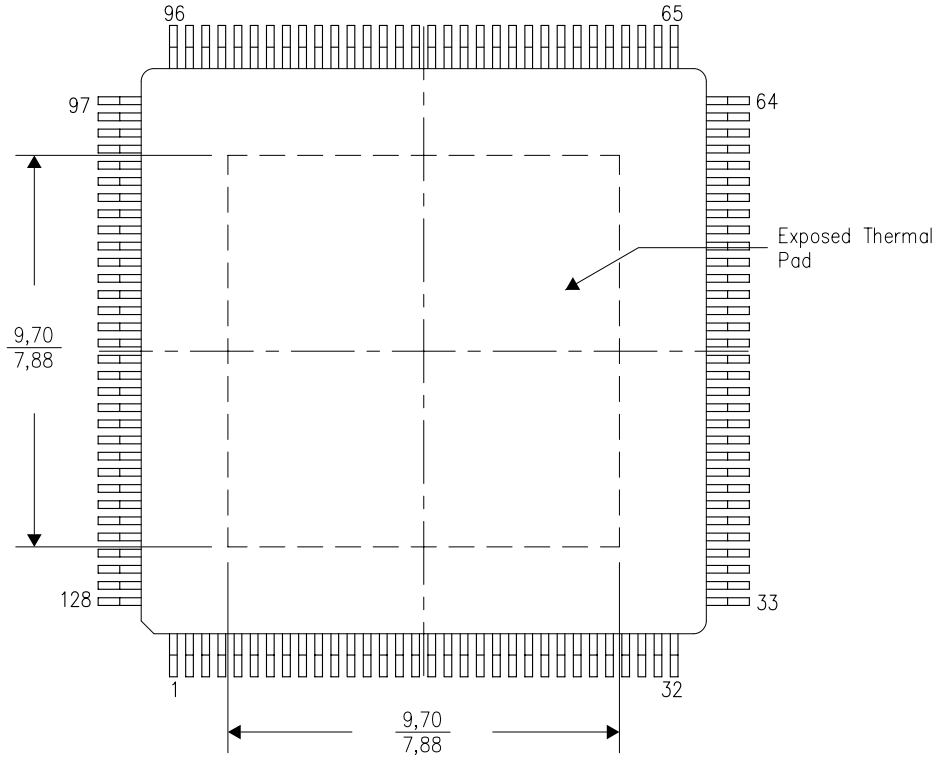
PNP (S–PQFP–G128) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

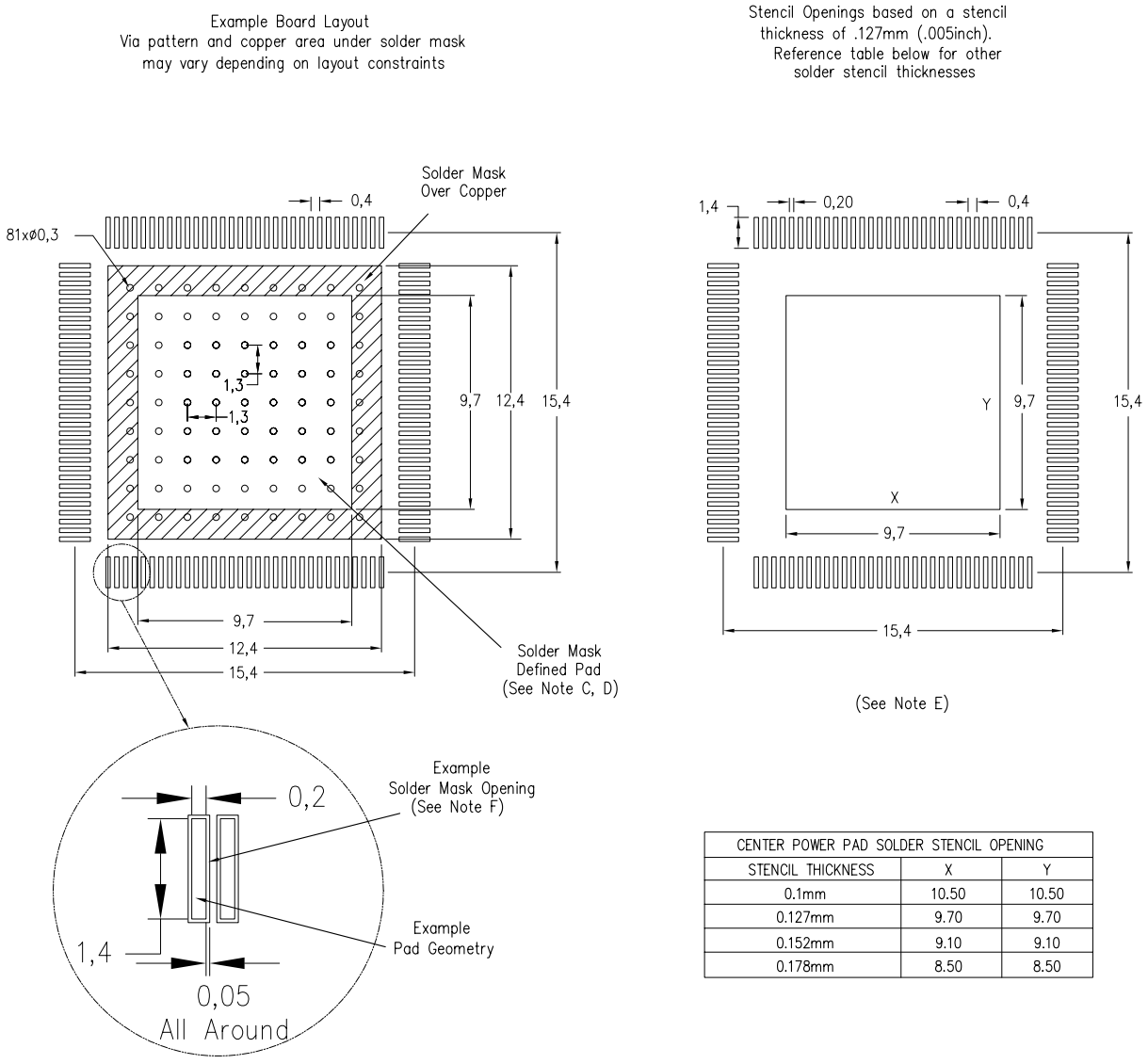
Exposed Thermal Pad Dimensions

4206232–3/L 10/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PNP (S–PQFP–G128) PowerPAD™ PLASTIC QUAD FLAT PACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	10.50	10.50
0.127mm	9.70	9.70
0.152mm	9.10	9.10
0.178mm	8.50	8.50

4209649–2/C 09/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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