

MtronPTI
...when timing matters

M2702/M2703 Series
SPECIFICATION FOR 5.0x7.0mm LVPECL/LVDS SMT OSCILLATOR

FEATURES

LVPECL/LVDS Differential Output
Low RMS Jitter Performance 12 kHz to 20 MHz
(1 ps max, 156.25 MHz)
RoHS 6/6 Compliant

APPLICATIONS

10G Reference
NIC Card
Ethernet
Test and Measurement

Ordering Information:

Product Family (Supply Voltage Option)	Temperature Range		Stability		Enable/Disable		Logic Type		Package/Lead Configuration		Frequency MHz
	Code	Value	Code	Value	Code	Value	Code	Value	Code	Value	
M2702 (3.3V) **M2703** (2.5V)	**6** **2**	-20 °C to +70 °C -40 °C to +85 °C	**3** **4** **6** **8**	±100 ppm ±50 ppm ±25 ppm ±20 ppm	**B**	Enable High (pad 1)	**P** **L**	LVPECL LVDS	**N**	Leadless	XXX.XXXXXX
Example: M270224BPN 100.000000 MHz											
M2702	**2**		**4**		**B**		**P**		**N**		**100.000000**

LVPECL Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency of Operation	F_O	10		1500	MHz	
Frequency Stability						
Frequency Stability	ΔF/F	See ordering information				
Aging			±2		ppm	1st year
RF Output						
Output Type		LVPECL Compatible				
Output Load		50 Ω to (Vcc-2.0) V_{DC}			V	
Symmetry (duty cycle)		45		55	%	Ref. to 50% of waveform
Logic Level "0"	V_{OL}	V_{cc}-1.85		V_{cc}-1.63	V	
Logic Level "1"	V_{OH}	V_{cc}-1.03		V_{cc}-0.60	V	
Rise/Fall Time	T_R/T_F		0.3	0.4	ns	20% to 80% of waveform
Start-up Time	T_{SU}			10	ms	$T_{ambient}$ = +25°C
Enable Logic (Pad 1)		70% V_{CC} or N/C			V	Output Enabled
Disable Logic (Pad 1)				30% V_{CC}	V	Output Disabled to high-Z
Supply Voltage & Power Consumption						
Operating Voltage	V_{CC}	3.135	3.300	3.465	V	(M2702)
		2.375	2.500	2.625	V	(M2703)
Supply Current	I_{CC}			80	mA	

Revision B
10/09/17

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LVDS Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency of Operation	F_O	10		1500	MHz	
Frequency Stability						
Frequency Stability	ΔF/F	See ordering information				
Aging			±2		ppm	1st year
RF Output						
Output Type		LVDS Compatible				
Output Load		100 Ω Differential			V	
Symmetry (duty cycle)	V_{OH}	45		55	%	Ref. to 50% of waveform
Differential Output Voltage	V_{DIFF}	175	350		mV	peak-to-peak differential output voltage
Output Offset Voltage	V_{OS}		1.250		V	
Rise/Fall Time	T_R/T_F			0.6	ns	20% to 80% of waveform
Start-up Time	T_{SU}			10	ms	$T_{ambient}$ = +25°C
Enable Logic (Pad 1)		70% V_{CC} or N/C			V	Output Enabled
Disable Logic (Pad 1)				30% V_{CC}	V	Output Disabled to high-Z
Supply Voltage & Power Consumption						
Operating Voltage	V_{CC}	3.135	3.300	3.465	V	(M2702)
		2.375	2.500	2.625	V	(M2703)
Supply Current	I_{CC}			60	mA	

Environmental & Packaging Requirements:

Storage Temperature	-55°C to 125°C
Mechanical Shock	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 ms)
Vibration	Per MIL-STD-202, Method 204D, Condition C (10 g's, 55 – 2000 Hz)
Aging	+85°C ±3°C, 720H (No BIAS)
Humidity	+40°C ±2°CX90~95%, 96H (NO BIAS)
Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B (-55 °C to +125 °C, 10 cycles)
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10^{-8} atm cc/s of Helium)
Moisture Sensitivity Level	MSL1
Solderability	Per EIAJ-STD-002, Method 208
Max. Soldering Conditions	See solder profile, Figure 1
Pad Termination	Gold, 1 µm maximum thickness
Package Type	6-pad 5.0 X 7.0 mm leadless ceramic. RoHS compliant.

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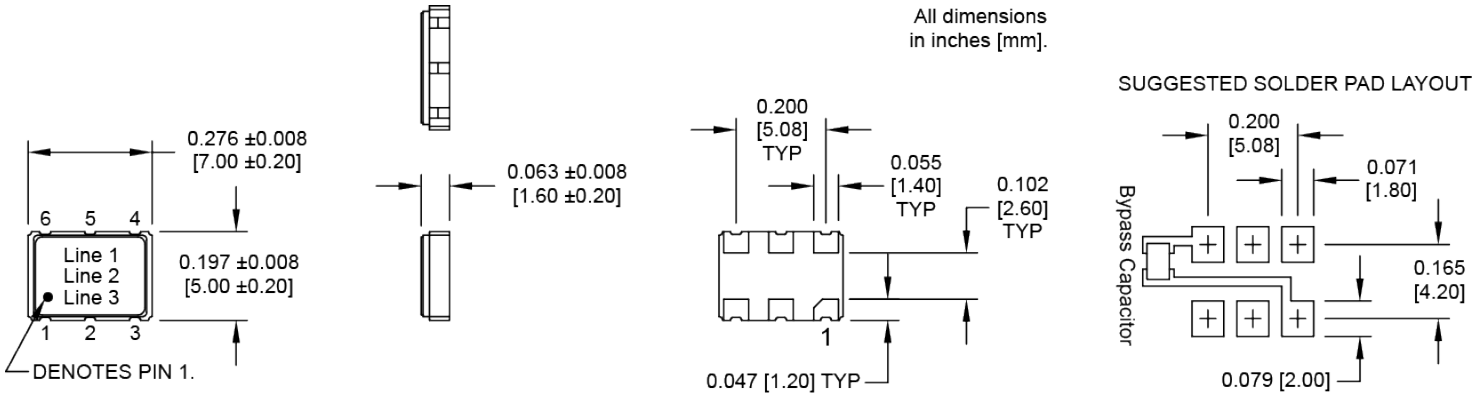
Marking, Pin Out:

Pad	Function
1	Enable/Disable
2	No Connection
3	Ground
4	Output
5	Complementary Output
6	$+V_{CC}$

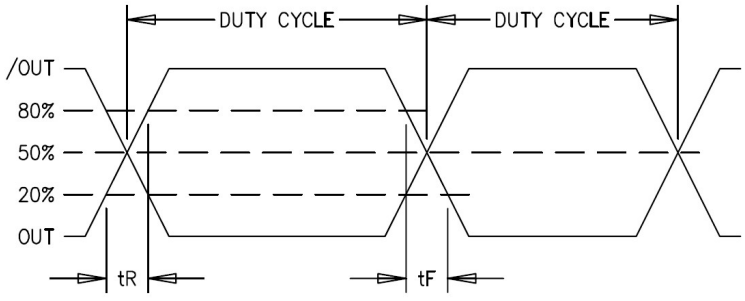
Part Marking	
Line 1	[part designation]
Line 2	FFFMFFFF
Line 3	M yy ww vv

Legend	
M	MtronPTI
F	Frequency
yy	Year
ww	Work Week
vv	Factory code

Dimensions:



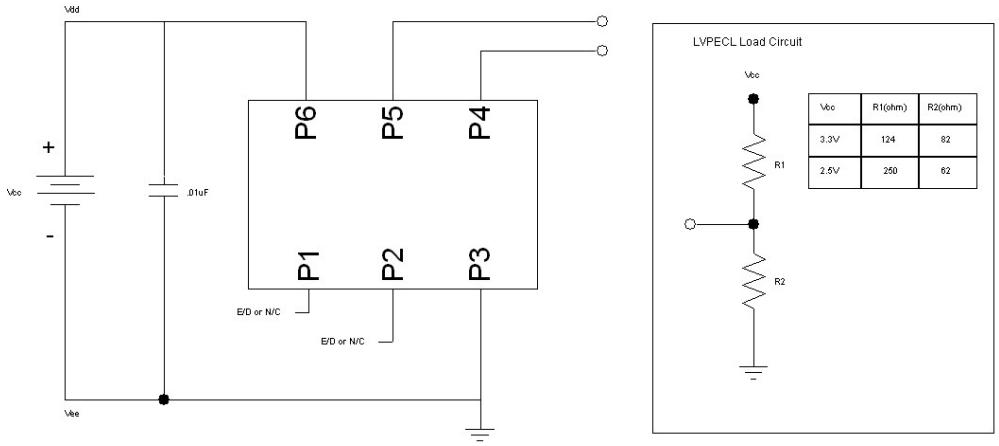
Output Waveform:



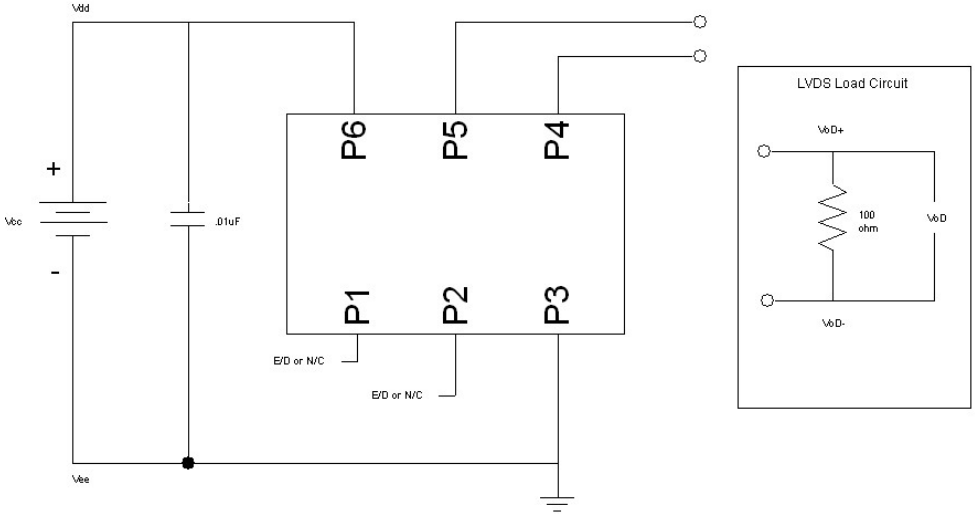
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Typical LVPECL Test Circuit & Load Circuit Diagrams:



Typical LVDS Test Circuit & Load Circuit Diagrams:



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Soldering Conditions:

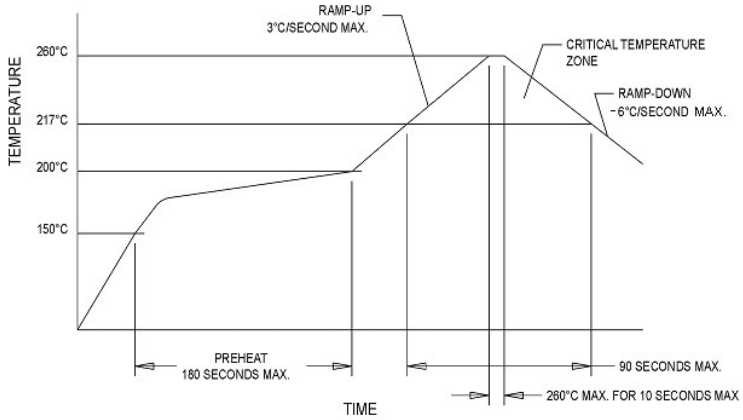
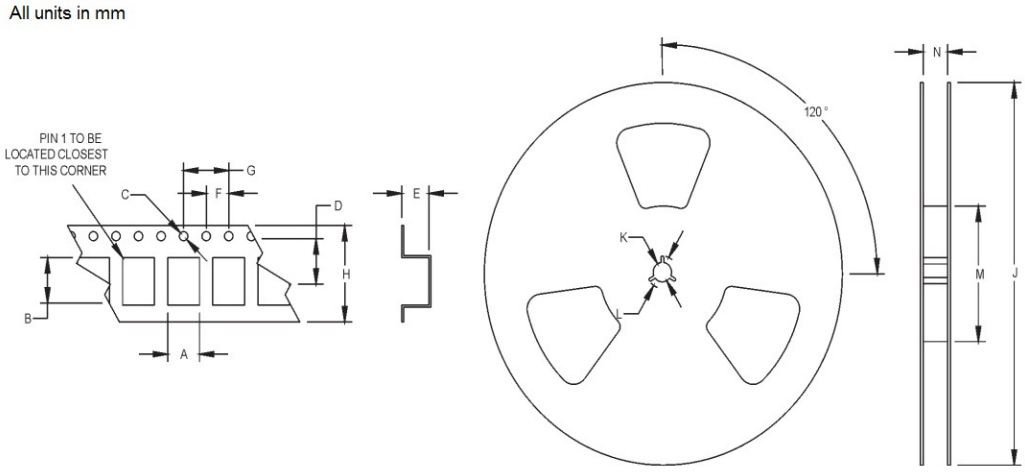


Figure 1

Tape and Reel Specifications:



Tape and Reel Specifications											
A	B	C	D	E	F	G	H	J	K	L	M
5.32	7.28	1.5	7.5	2.2	4	8	16	178	13.5	24.8	80

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