DATA SHEET

GPCR06C

SINGLE-CHIP VOICE RECORD/PLAYBACK DEVICE

JAN. 09, 2009

Version 1.0

GENERALPLUS TECHNOLOGY INC. reserves the right to change this documentation without prior notice. Information provided by GENERALPLUS TECHNOLOGY INC. is believed to be accurate and reliable. However, GENERALPLUS TECHNOLOGY INC. makes no warranty for any errors which may appear in this document. Contact GENERALPLUS TECHNOLOGY INC. to obtain the latest version of device specifications before placing your order. No responsibility is assumed by GENERALPLUS TECHNOLOGY INC. for any infringement of patent or other rights of third parties which may result from its use. In addition, GENERALPLUS products are not authorized for use as critical components in life support devices/systems or aviation devices/systems, where a malfunction or failure of the product may reasonably be expected to result in significant injury to the user, without the express written approval of Generalplus.

Table of Contents

PAGE

1. GENERAL DESCRIPTION 3

2. FEATURES 3

3. BLOCK DIAGRAM 3

4. SIGNAL DESCRIPTIONS 4

5. PACKAGE/PAD LOCATIONS 5

6. TIMING DIAGRAM 6

6.1. RECORDING MODE 6

6.2. PLAYBACK MODE 6

7. ELECTRICAL SPECIFICATIONS 8

7.1. ABSOLUTE MAXIMUM RATINGS 8

7.2. DC CHARACTERISTICS (T_A = 25℃,VDD = 3.0V) 8

7.3. DC CHARACTERISTICS (T_A = 25℃,VDD = 5.0V) 8

7.4. SAMPLE RATE VS. DURATION 8

7.5. THE RELATIONSHIPS BETWEEN THE R_{OSC} AND THE SR 9

7.5.1. VDD = 3.0V, T_A = 25℃ 9

7.5.2. VDD = 4.5V, T_A = 25℃ 9

7.6. THE RELATIONSHIPS BETWEEN THE SR AND THE VDD 9

8. APPLICATION CIRCUITS 10

8.1. APPLICATION CIRCUIT - (SPEAKER/MICROPHONE ALONE) 10

8.2. APPLICATION CIRCUIT - (SPEAKER/MICROPHONE SHARED) 11

8.3. KEY IN PIN PULL-HIGH RESISTANCE 11

9. ORDERING INFORMATION 12

10. DISCLAIMER 13

11. REVISION HISTORY 14

SINGLE-CHIP VOICE RECORD/PLAYBACK DEVICE

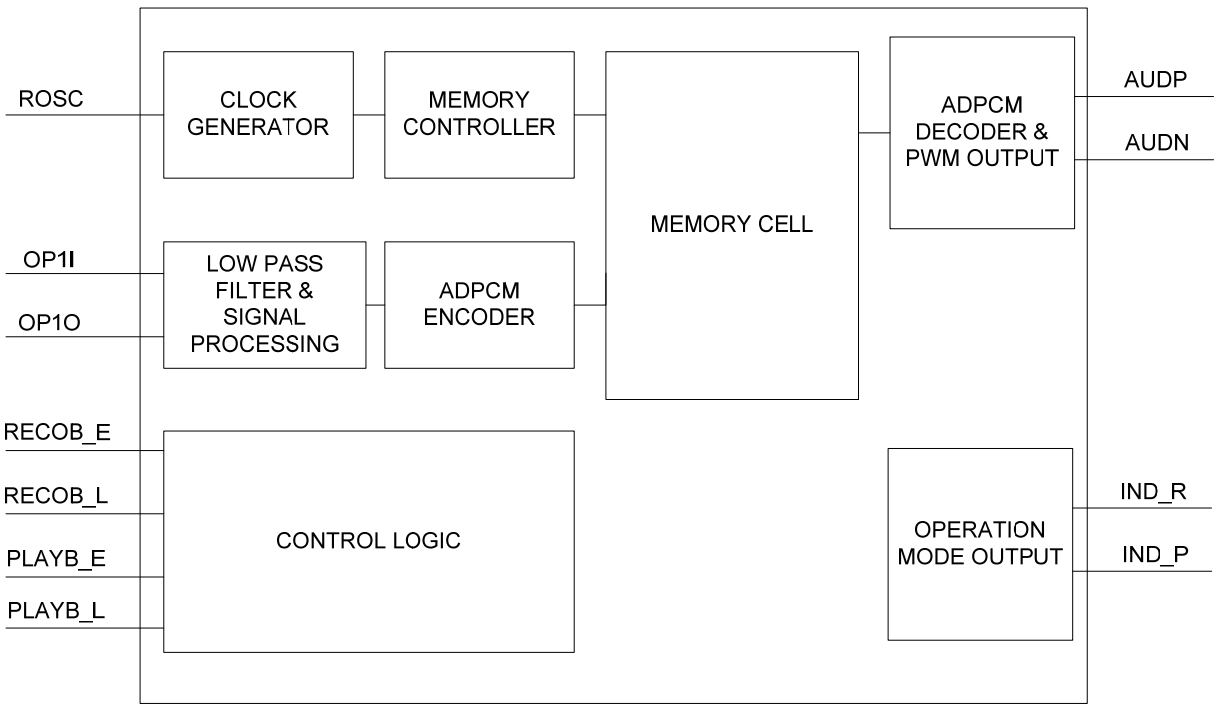
1. GENERAL DESCRIPTION

GPCR06C, a new recordable and playback voice device, which stores 4 to 8 seconds of audio or speech voice by oscillator resistor options. Two recording modes and selective recording and playback triggers are built-in. In addition to two recording/playback LED indicators, GPCR06C also features PWM output to individually drive speaker or buzzer. The GPCR06C contains all of necessary functions to enhance the voice quality in recording and playback. It can be widely used in compact message recorder, recordable toys and other similar products as well.

2. FEATURES

- Operation Voltage: 2.4V-3.6V (for 2-battery)
  3.6V-5.5V (for 3-battery)
  - Bonding option BAT_OPT: selects 2 or 3 batteries
- Standby current: <2uA @ 3V
- Recording duration adjustment by changing sample rate (4k~8KHz)
- Low pass filter built-in
- Selective recording and playback triggers
  - RECOB_E: Falling edge trigger recording on/off
  - RECOB_L: Low level trigger recording on
  - PALYB_E: Falling edge trigger playing on/off
  - PALYB_L: Low level trigger playing on
- Play one-beep sound at the beginning of record and three-beep when stop recording
  - Bonding option BEEP_OPT: beep sound enabled or disabled
- Two recording/playback indicators to drive LED
- PWM output to drive speaker or buzzer directly
- Two recording modes available
  - Speaker/microphone alone or shared mode

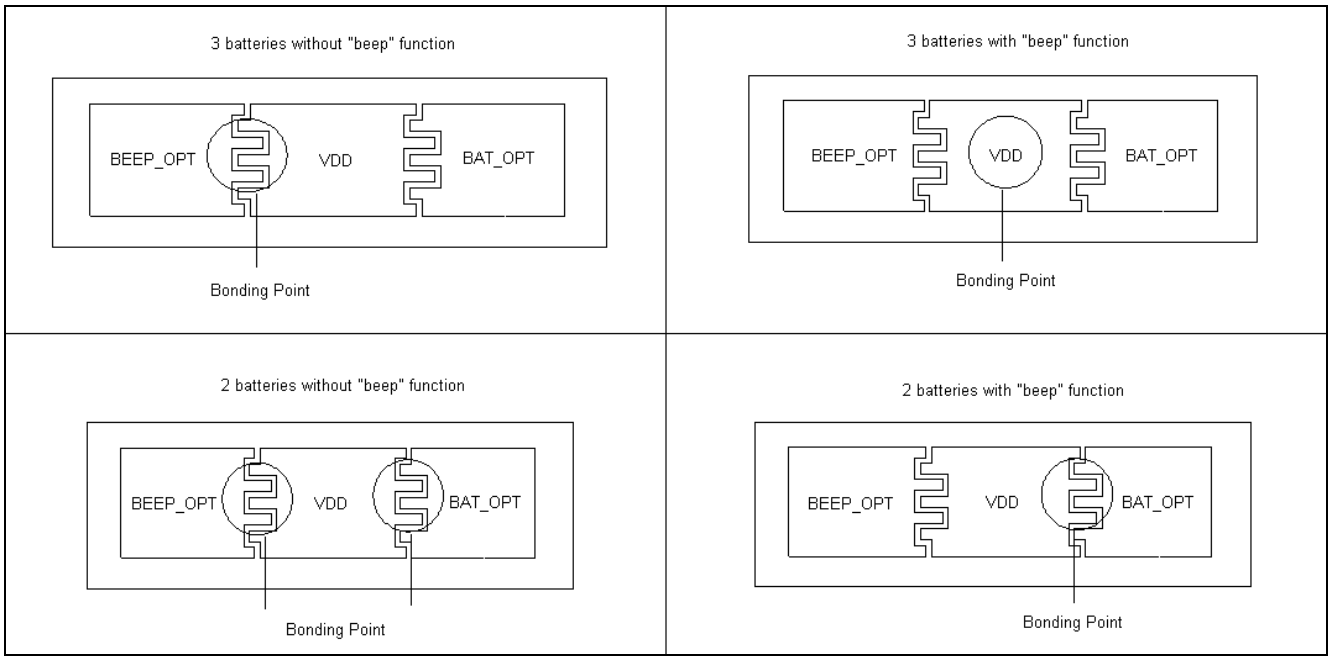
3. BLOCK DIAGRAM



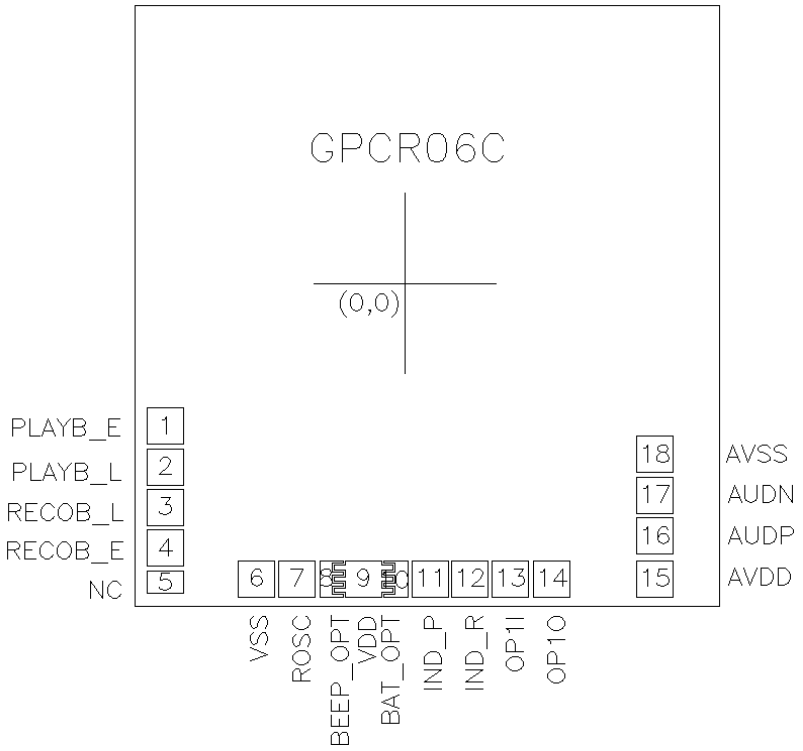
4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
PLAYB_E	1	I	Trigger input for playback, Edge/non-hold/non-retrigger mode (i.e. One-shot)
PLAYB_L	2	I	Trigger input for playback, Level/Hold mode
RECOB_L	3	I	Trigger input for recording, Level/Hold mode
RECOB_E	4	I	Trigger input for recording, Edge/non-hold/non-retrigger mode (i.e. One-shot)
NC	5	-	N/A
VSS, AVSS	6, 18	G	Digital and Analog ground buses
ROSC	7	I	R oscillator input
BEEP_OPT	8	I	Option pin for “Beep” function enable (not bonding to VDD)/disable(bonding to VDD)
VDD, AVDD	9, 15	P	Digital and Analog power buses
BAT_OPT	10	I	Option pin to select 3 batteries (not bonding to VDD)/2 batteries (bonding to VDD)
IND_P	11	O	Playback indicator, low active
IND_R	12	O	Recording indicator, low active
OP1I	13	I	OP input of microphone Preamplifier
OP1O	14	O	OP output of microphone Preamplifier
AUDP	16	O	PWM driver positive output
AUDN	17	O	PWM driver negative output

Note: The shape of bonding option pad looks like in the figure.



5. PACKAGE/PAD LOCATIONS



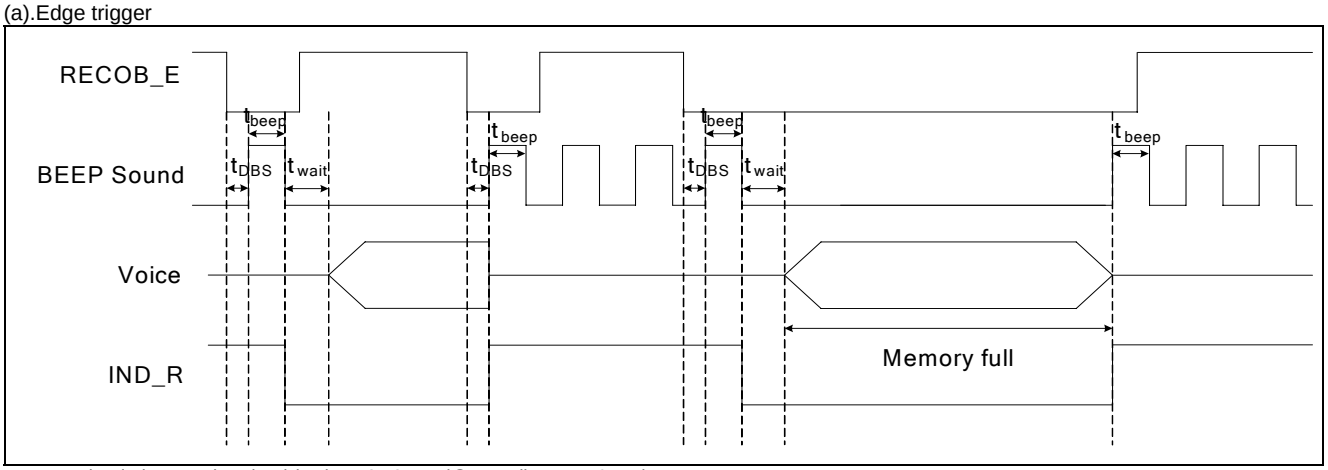
This IC substrate should be floated

Note1: To ensure IC functioning properly, please bond all of VDD and VSS pins.

6. TIMING DIAGRAM

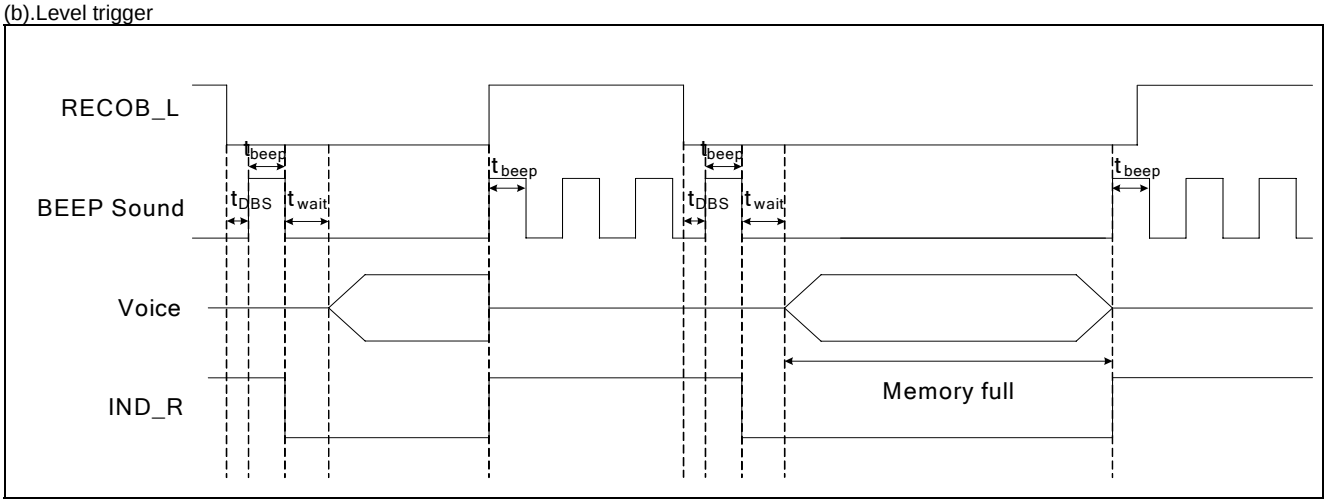
6.1. Recording Mode

(a).Edge trigger



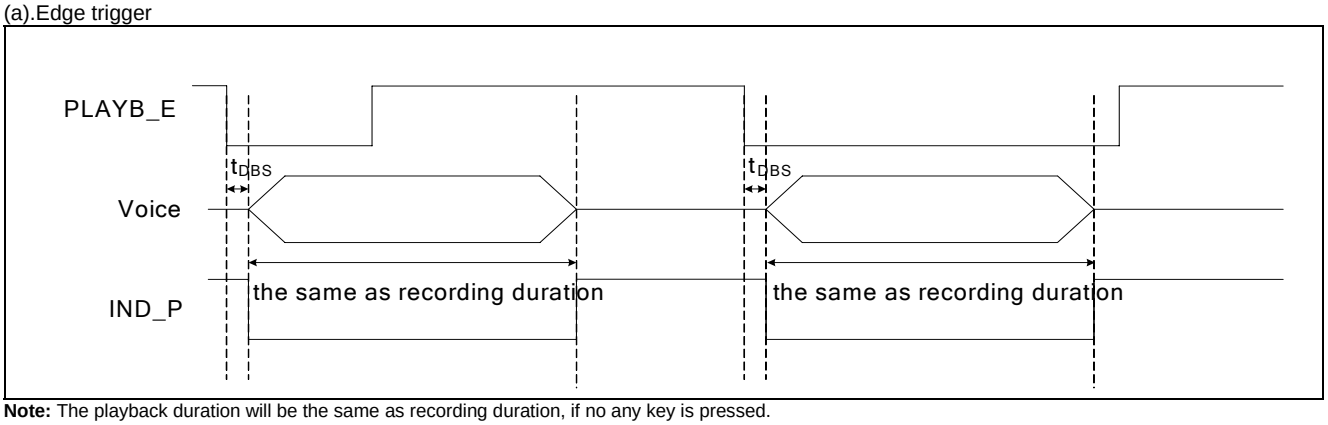
Note: 1. The de-bounce time (t_{DBS}) is about 37.3 ms, (@ sampling rate=6KHz).
2. The beep time (t_{beep}) is beep sound duration, which is about 64 ms, (@ sampling rate=6KHz).
3. The wait time (t_{wait}) is for internal circuit setup time, which is about 85.3 ms, (@ sampling rate=6KHz).

(b).Level trigger

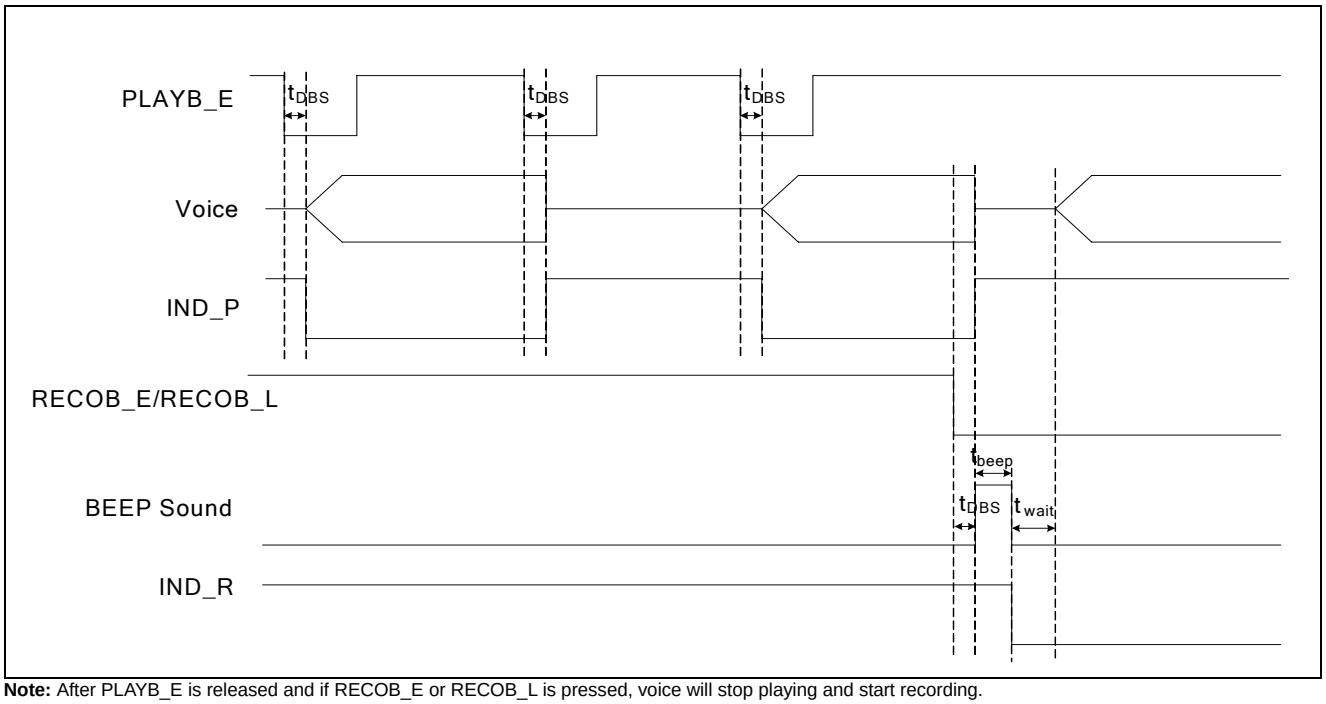


6.2. Playback Mode

(a).Edge trigger

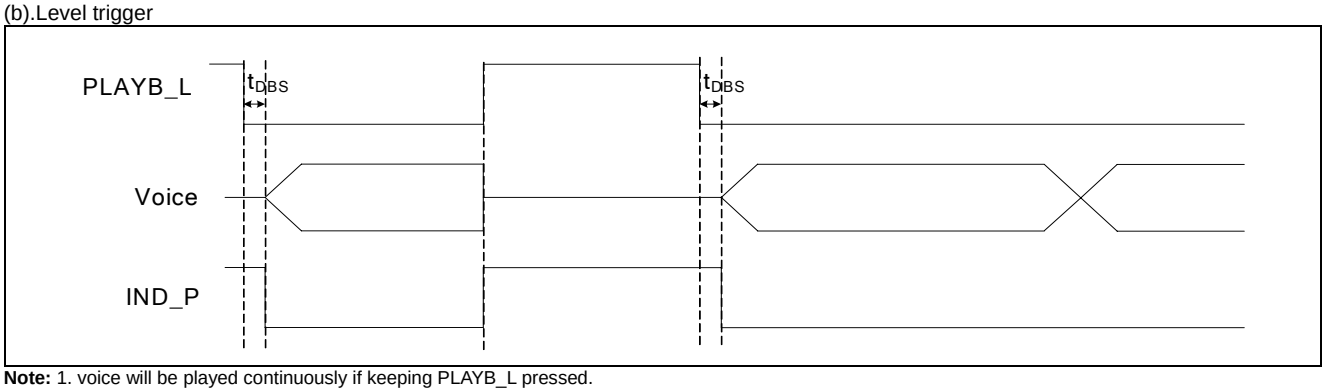


Note: The playback duration will be the same as recording duration, if no any key is pressed.



Note: After PLAYB_E is released and if RECOB_E or RECOB_L is pressed, voice will stop playing and start recording.

(b).Level trigger



Note: 1. voice will be played continuously if keeping PLAYB_L pressed.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Ratings
Operating Temperature	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Voltage Applied to Any Pin	(VSS-0.3V) to (VDD+0.3V)

Note: Stresses beyond those given in the Absolute Maximum Ratings table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics (T_A = 25℃,VDD = 3.0V)

Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Input Low Voltage	V_{IL}	VSS	-	0.2xVDD	V	-
Input High Voltage	V_{IH}	0.7xVDD	-	VDD	V	-
Operation Voltage	V_{DD}	2.4	-	3.6	V	For 2-battery
Operation Current	I_{OP1}	-	3	-	mA	Recording, No load, VDD = 3.0V
	I_{OP2}	-	0.3	-	mA	Playing, No load, VDD = 3.0V
Standby Current	I_{SB}	-	-	2.0	uA	VDD = 3.0V
IND_P/IND_R Output Current	I_{OL}	-	30	-	mA	VDD = 3.0V, V_{OL} = 0.6V
PWM Output Current	I_{OL}	-	120	-	mA	VDD = 3.0V, V_{OL} = 0.6V
	I_{OH}	-	-80	-	mA	VDD = 3.0V, V_{OH} = 2.4V
R_{OSC} Resistor	R_{OSC}	-	620	-	KΩ	VDD = 3.0V, SR = 4.0KHz
Input Current for KEY in	I_{IN}	-	1	-	uA	VDD = 3.0V, V_{IN} = VSS

7.3. DC Characteristics (T_A = 25℃,VDD = 5.0V)

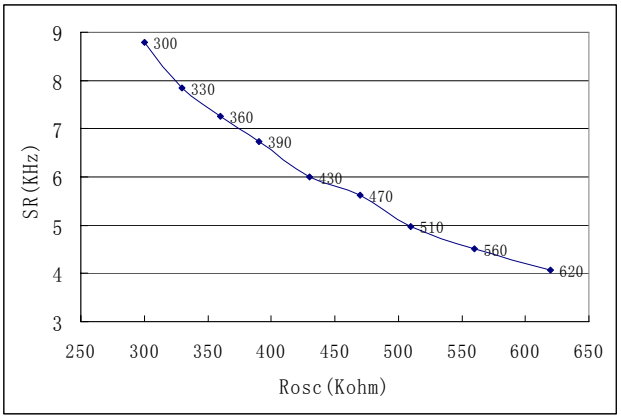
Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Input Low Voltage	V_{IL}	VSS	-	0.2xVDD	V	-
Input High Voltage	V_{IH}	0.7xVDD	-	VDD	V	-
Operation Voltage	V_{DD}	3.6	-	5.5	V	For 3-battery
Operation Current	I_{OP1}	-	4	-	mA	Recording, No load, VDD = 5.0V
	I_{OP2}	-	0.6	-	mA	Playing, No load, VDD = 5.0V
Standby Current	I_{SB}	-	-	2.0	uA	VDD = 5.0V
IND_P/IND_R Output Current	I_{OL}	-	75	-	mA	VDD = 5.0V, V_{OL} = 1.0V
PWM Output Current	I_{OL}	-	260	-	mA	VDD = 5.0V, V_{OL} = 1.0V
	I_{OH}	-	-180	-	mA	VDD = 5.0V, V_{OH} = 4.0V
R_{OSC} Resistor	R_{OSC}	-	430	-	KΩ	VDD = 5.0V, SR = 6.0KHz
Input Current for KEY in	I_{IN}	-	3.5	-	uA	VDD = 5.0V, V_{IN} = VSS

7.4. Sample rate VS. Duration

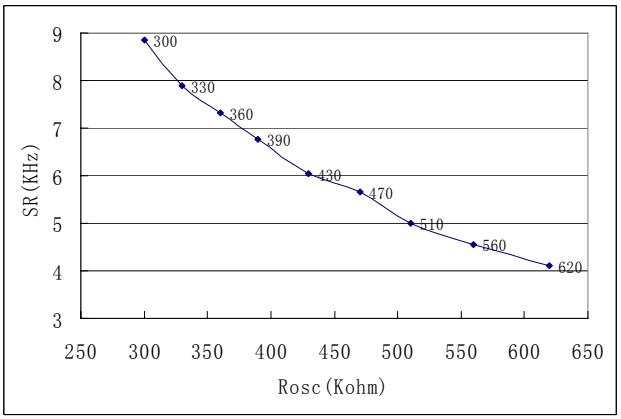
Sample Rate	**4.0KHz**	**5.0KHz**	**5.3KHz**	**6.0KHz**	**6.4KHz**	**7.0KHz**	**8.0KHz**
Duration	**8.0 sec**	**6.4sec**	**6.0 sec**	**5.3 sec**	**5.0 sec**	**4.6sec**	**4.0sec**

7.5. The Relationships between the R_{OSC} and the SR

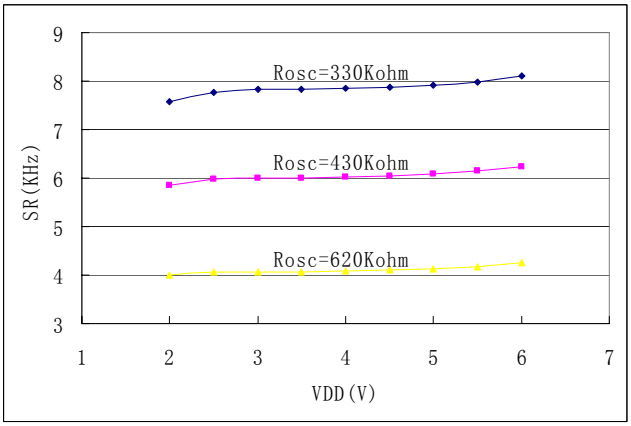
7.5.1. VDD = 3.0V, T_A = 25℃



7.5.2. VDD = 4.5V, T_A = 25℃

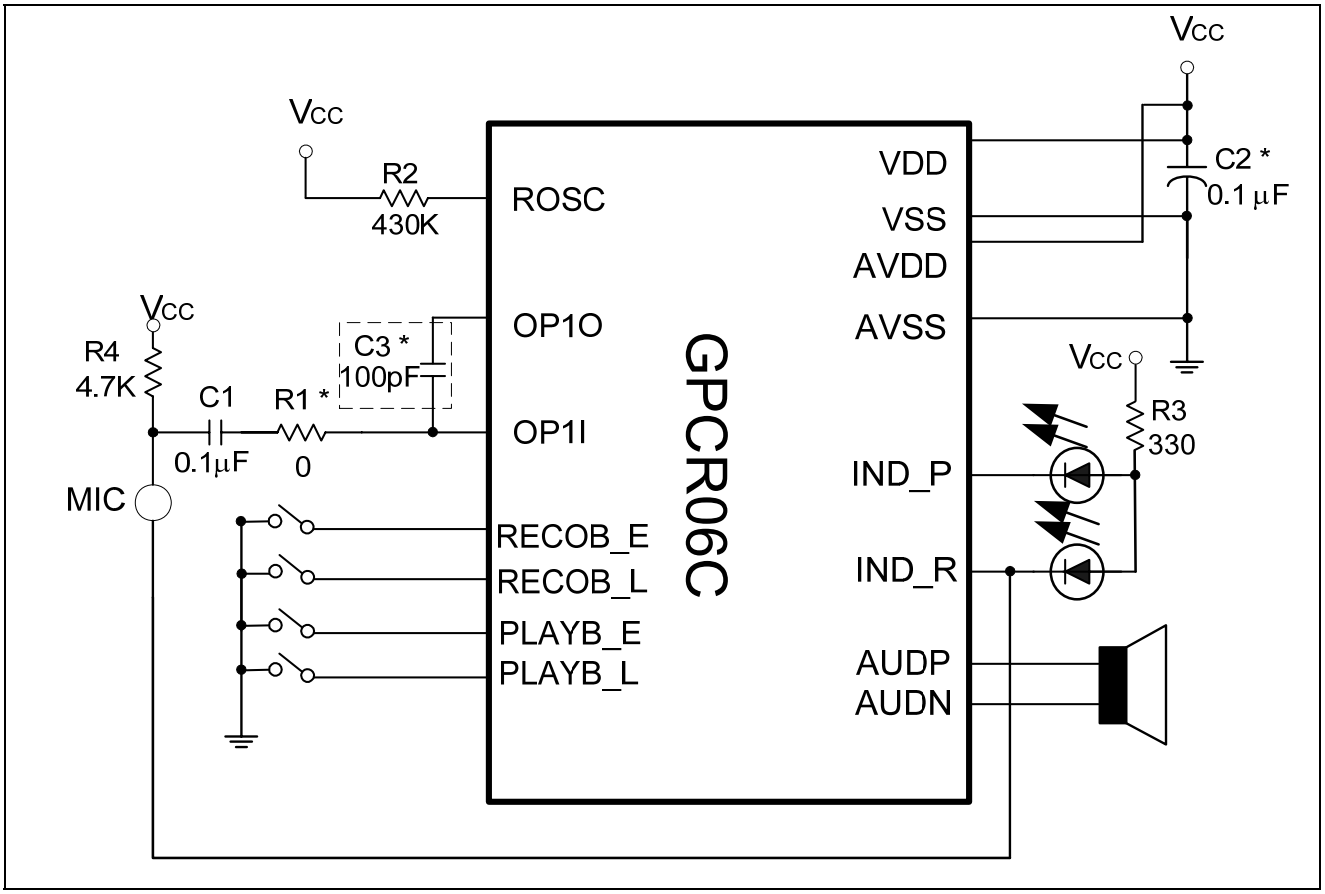


7.6. The Relationships between the SR and the VDD



8. APPLICATION CIRCUITS

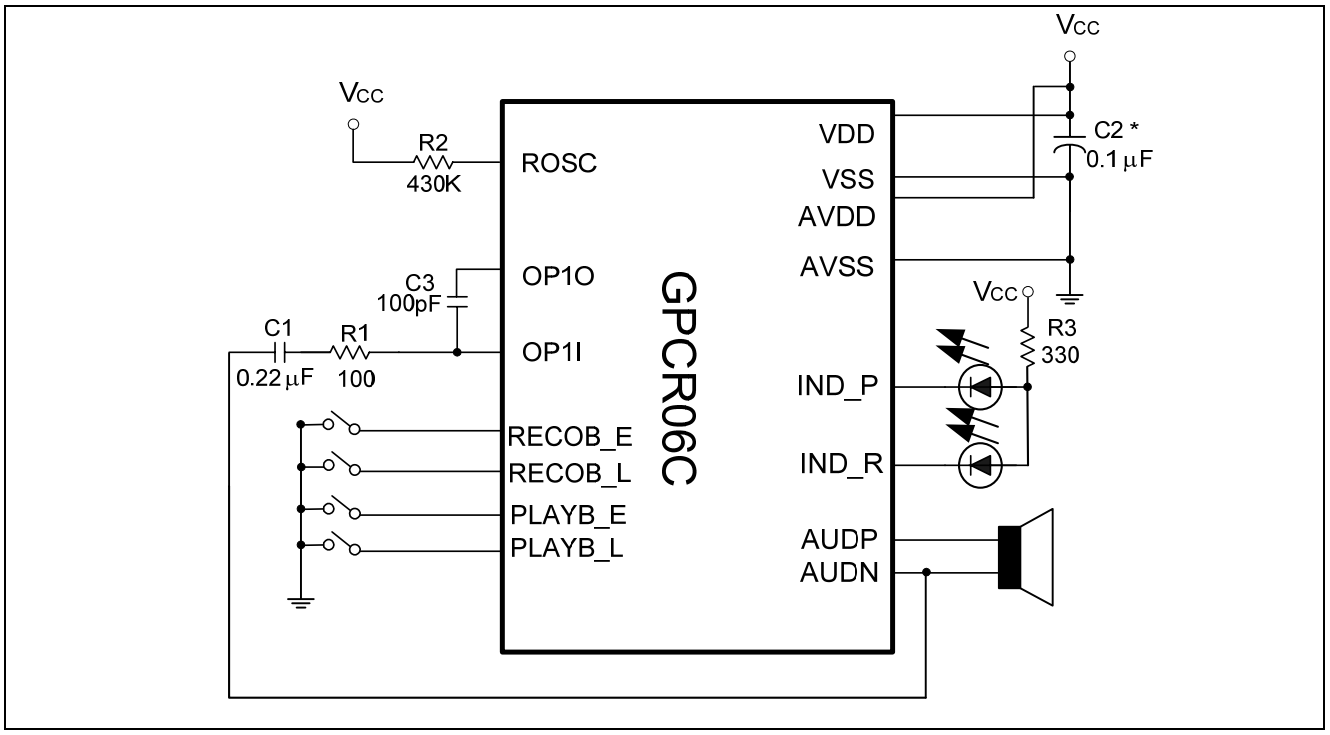
8.1. Application Circuit - (Speaker/Microphone Alone)



PCB Layout Guidelines:

1. VDD and AVDD must be connected to power input port (V_{CC}) directly and independently, meaning not branch from one or another.
2. VSS and AVSS must be connected to power input port (GND) directly and independently, meaning not branch from one or another.
3. When R1=0, the MIC is most sensitive. And R1 should be increased to improve noise immunity in different application.
4. C2 is suggested 0.1uF, the IC power is more stable if increase C2. And C2 should be as closed as possible in between VDD/AVDD connecting points to V_{CC} and VSS/AVSS connecting points to GND.
5. C3 may be eliminated in stable power supply.

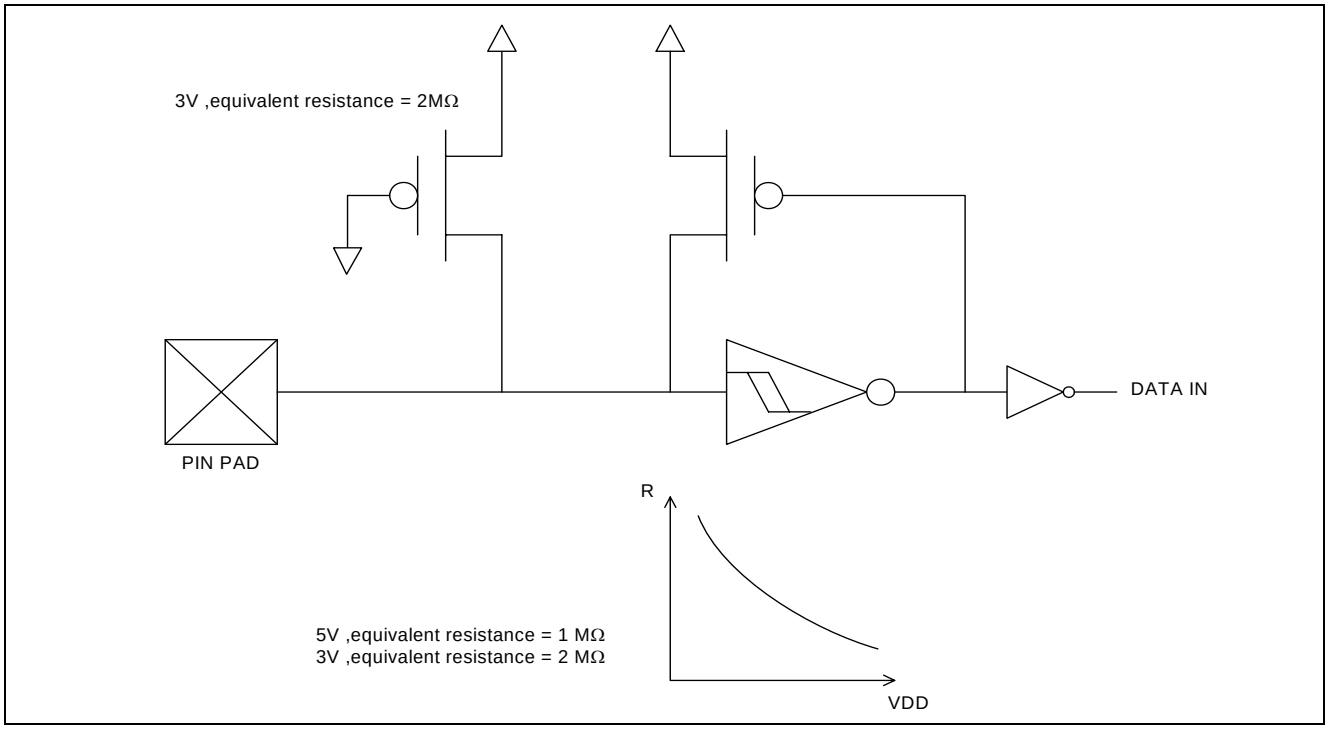
8.2. Application Circuit - (Speaker/Microphone Shared)



PCB Layout Guidelines:

1. VDD and AVDD must be connected to power input port (V_{CC}) directly and independently, meaning not branch from one or another.
2. VSS and AVSS must be connected to power input port (GND) directly and independently, meaning not branch from one or another.
3. C2 is suggested 0.1uF, the IC power is more stable if increase C2. And C2 should be as closed as possible in between VDD/AVDD connecting points to V_{CC} and VSS/AVSS connecting points to GND.

8.3. Key in Pin Pull-High Resistance



9. ORDERING INFORMATION

Product Number	Package Type
GPCR06C-C	Chip form

10. DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by Generalplus Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. GENERALPLUS makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, GENERALPLUS MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. GENERALPLUS reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by GENERALPLUS for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

11. REVISION HISTORY

Date	Revision #	Description	Page
JAN. 09, 2009	1.0	Modify “8.2 Application circuit “.	11
OCT. 20, 2008	0.1	Original.	14