EL5132, EL5133

670MHz Low Noise Amplifiers

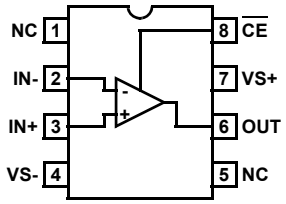
FN7382
Rev 8.00
May 4, 2007

The EL5132 and EL5133 are ultra-low voltage noise, high speed voltage feedback amplifiers that are ideal for applications requiring low voltage noise, including communications and imaging. These devices offer extremely low power consumption for exceptional noise performance. Stable at gains as low as 10, these devices offer 120mA of drive performance. Not only do these devices find perfect application in high gain applications, they maintain their performance down to lower gain settings.

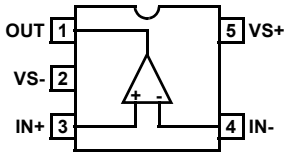
These amplifiers are available in small package options (SOT-23) as well as the industry-standard SOIC packages. All parts are specified for operation over the -40°C to +85°C temperature range.

Pinout

EL5132
(8 LD SOIC)
TOP VIEW



EL5133
(5 LD SOT-23)
TOP VIEW



Features

- 670MHz -3dB bandwidth
- Ultra low noise 0.9nV/√Hz
- 1000V/µs slew rate
- Low supply current = 12mA
- Single supplies from 5V to 12V
- Dual supplies from ±2.5V to ±6V
- Fast disable on the EL5132
- Pb-free plus anneal available (RoHS compliant)

Applications

- Pre-amplifier
- Receiver
- Filter
- IF and baseband amplifier
- ADC drivers
- DAC buffers
- Instrumentation
- Communications devices

Ordering Information

PART NUMBER	part marking	TAPE AND REEL	PACKAGE	PKG. DWG. #
EL5132IS	5132IS	-	8 Ld SOIC (150 mil)	MDP0027
EL5132IS-T7	5132IS	7”	8 Ld SOIC (150 mil)	MDP0027
EL5132IS-T13	5132IS	13”	8 Ld SOIC (150 mil)	MDP0027
EL5132ISZ (Note)	5132ISZ	-	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5132ISZ-T7 (Note)	5132ISZ	7”	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5132ISZ-T13 (Note)	5132ISZ	13”	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5133IW-T7	BCAA	7” (3k pcs)	5 Ld SOT-23	MDP0038
EL5133IW-T7A	BCAA	7” (250 pcs)	5 Ld SOT-23	MDP0038
EL5133IWZ	BSAA	-	5 Ld SOT-23 (Pb-free)	MDP0038
EL5133IWZ-T7 (Note)	BSAA	7” (3k pcs)	5 Ld SOT-23 (Pb-free)	MDP0038
EL5133IWZ-T7A (Note)	BSAA	7” (250 pcs)	5 Ld SOT-23 (Pb-free)	MDP0038

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage from V_S+ to V_S- 13.2V
Slewrate between V_S+ and V_S- 1V/µs
I_{IN}-, I_{IN}+, CE . . . . . ±5mA
Continuous Output Current 150mA

Thermal Information

Storage Temperature . . . . . -65°C to +125°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . +125°C
Power Dissipation . . . . . See Curves
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_L = 500Ω, R_F = 900Ω, R_G = 100Ω, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Offset Voltage		-1	0.5	1	mV
T_CV_{OS}	Offset Voltage Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		0.8		µV/°C
IB	Input Bias Current	V_{IN} = 0V	8	12	20	µA
I_{OS}	Input Offset Current	V_{IN} = 0V	-1250	400	+1250	nA
T_CI_{OS}	Input Bias Current Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		3		nA/°C
PSRR	Power Supply Rejection Ratio	V_S+ = ±4.75V to ±5.25V	75	87		dB
CMRR	Common Mode Rejection Ratio	V_{IN} = ±3.0 V	80	100		dB
CMIR	Common Mode Input Range	Guaranteed by CMRR test	±3	±3.3		V
R_{IN}	Input Resistance	Common mode	2	5		MΩ
C_{IN}	Input Capacitance			2		pF
I_S	Supply Current		9.2	11	13	mA
AVOL	Open Loop Gain	V_{OUT} = ±2.5V, R_L = 1kΩ to GND	5	8.5		KV/V
V_O	Output Voltage Swing	R_F = 900Ω, R_G = 100Ω, R_L = 150Ω	±3.1	±3.5		V
I_{SC}	Short Circuit Current	R_L = 10Ω	70	140		mA
BW	-3dB Bandwidth	R_F = 225Ω, A_V = +10, R_L = 1kΩ		670		MHz
BW	±0.1dB Bandwidth	R_F = 225Ω, A_V = +10, R_L = 1kΩ		90		MHz
GBWP	Gain Bandwidth Product			3000		MHz
PM	Phase Margin	R_L = 1kΩ, C_L = 6pF		55		°
SR	Slew Rate	R_L = 100Ω, V_{OUT} = ±2.5V	700	1000		V/µs
t_R, t_F	Rise Time, Fall Time	±0.1V_{STEP}		2.0		ns
OS	Overshoot	±0.1V_{STEP}		10		%
t_S	0.01% Settling Time			6.6		ns
dG	Differential Gain	R_F = 1kΩ, R_{Load} = 150Ω		0.01		%
dP	Differential Phase	R_F = 1kΩ, R_{Load} = 150Ω		0.01		°
e_N	Input Noise Voltage	f = 10kHz		0.9		nV/√Hz
i_N	Input Noise Current	f = 10kHz		3.5		pA/√Hz
ENABLE (EL5132 Only)						
t_{EN}	Enable Time			220		nS
t_{DIS}	Disable Time			175		nS
V_{IHCE}	$\overline{CE}$ Input High Voltage for Power-down		V_S+ - 1			V
V_{ILCE}	$\overline{CE}$ Input Low Voltage for Power-up				V_S+ - 3	V
I_{S-OFF}	Supply Current - Disabled	No Load, $\overline{CE}$ = 4V		13	25	µA
$I_{IL-\overline{CE}}$	$\overline{CE}$ Pin Input Low Current	$\overline{CE}$ = V_S-	-1	0	1	µA
$I_{IH-\overline{CE}}$	$\overline{CE}$ Pin Input High Current	$\overline{CE}$ = V_S+		14	25	µA

Typical Performance Curves

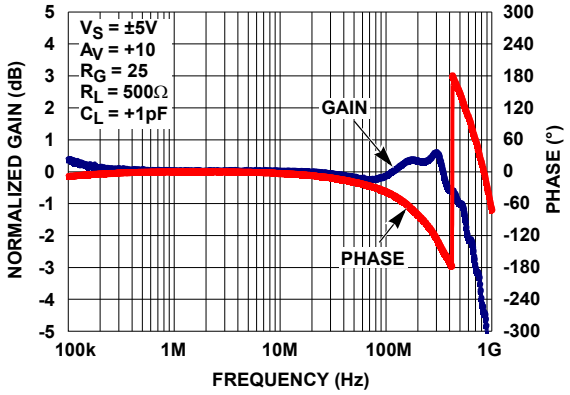


FIGURE 1. GAIN & PHASE vs FREQUENCY

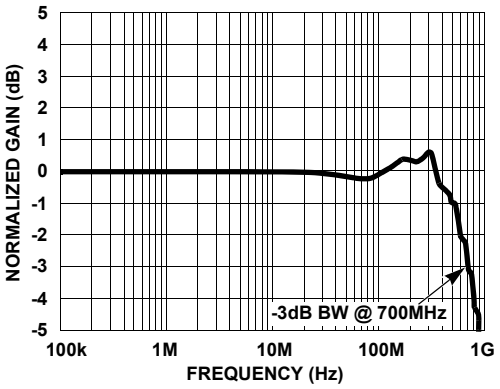


FIGURE 2. -3dB BANDWIDTH

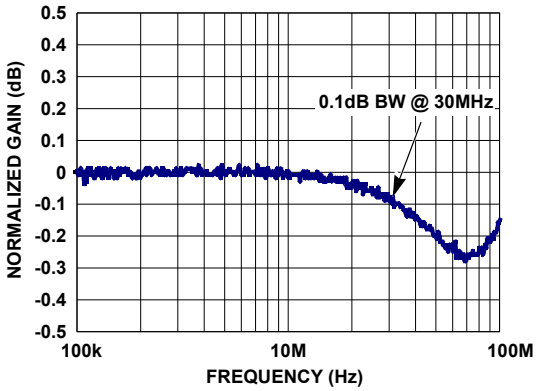


FIGURE 3. 0.1dB BANDWIDTH

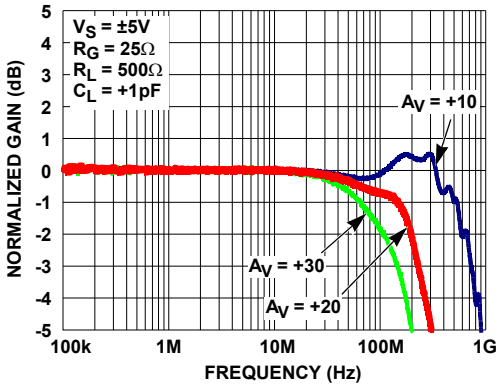


FIGURE 4. GAIN vs FREQUENCY FOR VARIOUS +A_V

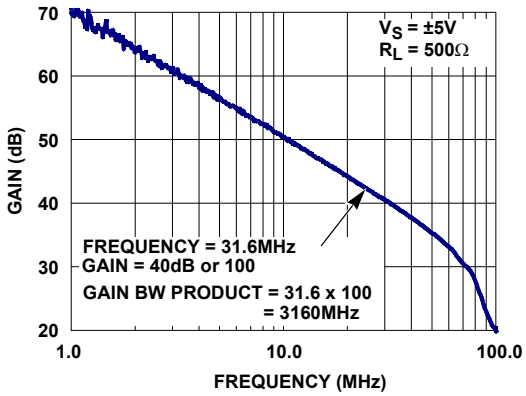


FIGURE 5. GAIN BANDWIDTH PRODUCT

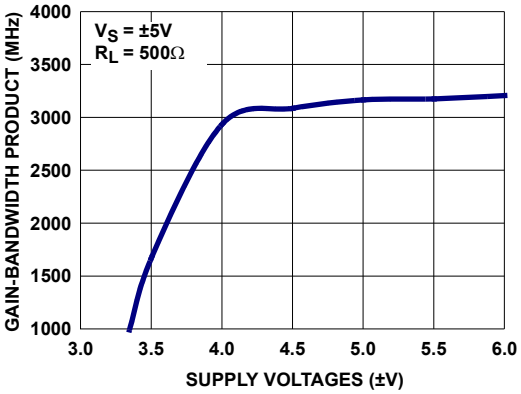


FIGURE 6. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGES

Typical Performance Curves (Continued)

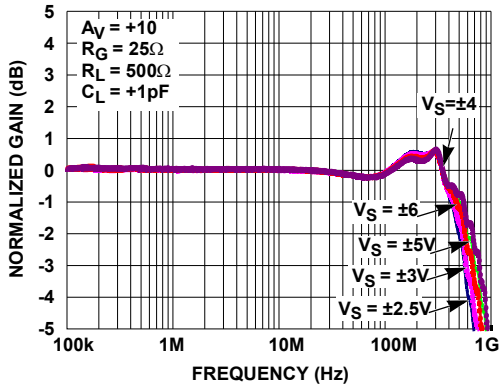


FIGURE 7. GAIN vs FREQUENCY FOR VARIOUS $\pm V_S$

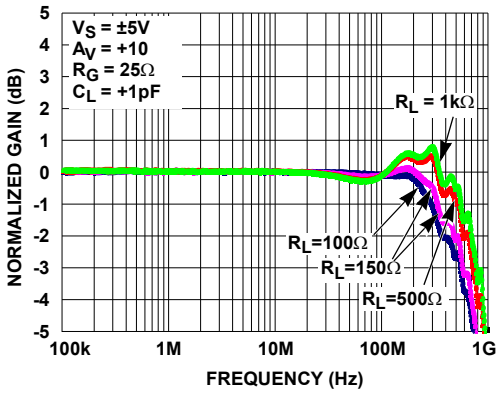


FIGURE 8. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} (A_V = +10)

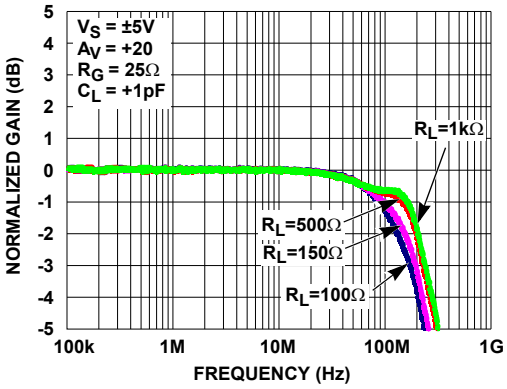


FIGURE 9. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} (A_V = +20)

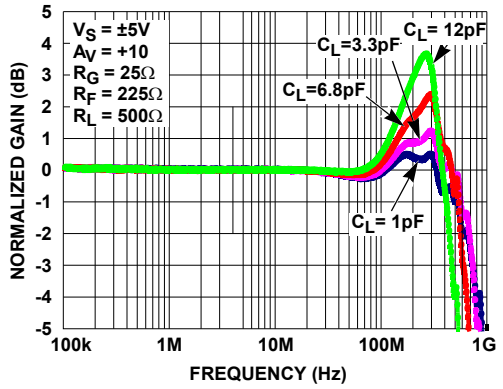


FIGURE 10. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} (A_V = +10)

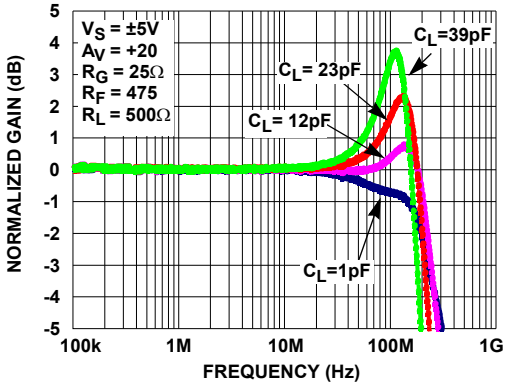


FIGURE 11. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} (A_V = +20)

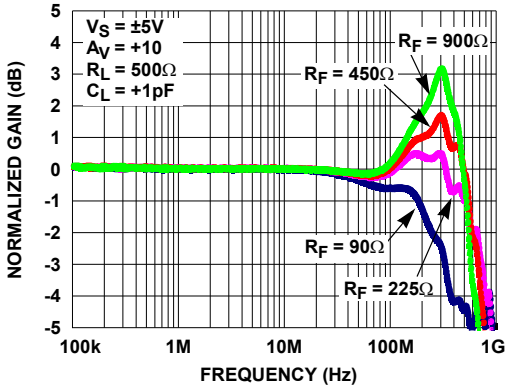


FIGURE 12. GAIN vs FREQUENCY FOR VARIOUS R_F (A_V = +10)

Typical Performance Curves (Continued)

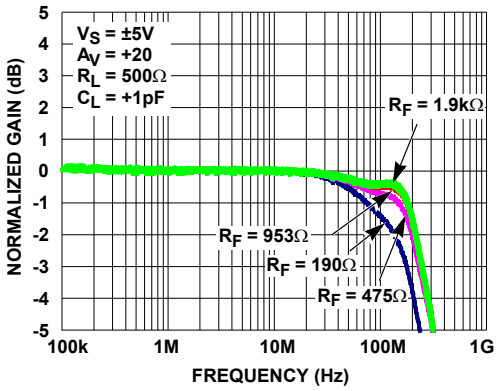


FIGURE 13. GAIN vs FREQUENCY FOR VARIOUS R_F (A_V = +20)

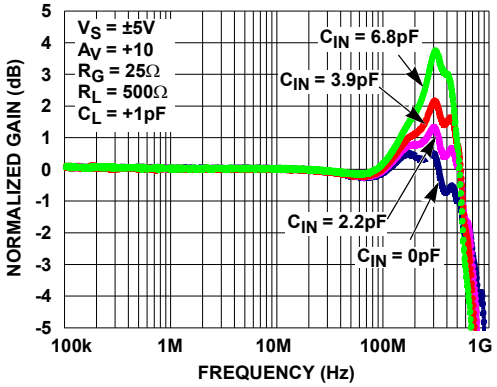


FIGURE 14. GAIN vs FREQUENCY FOR VARIOUS C_{IN}(-) (A_V = +10)

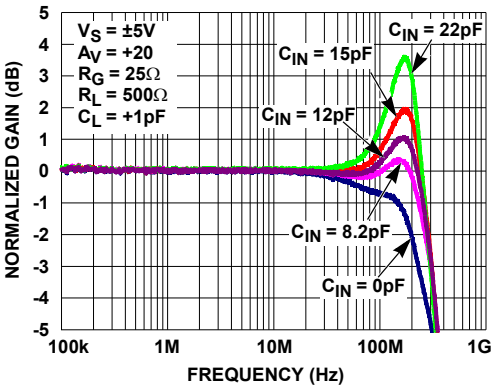


FIGURE 15. GAIN vs FREQUENCY FOR VARIOUS C_{IN} (A_V = +20)

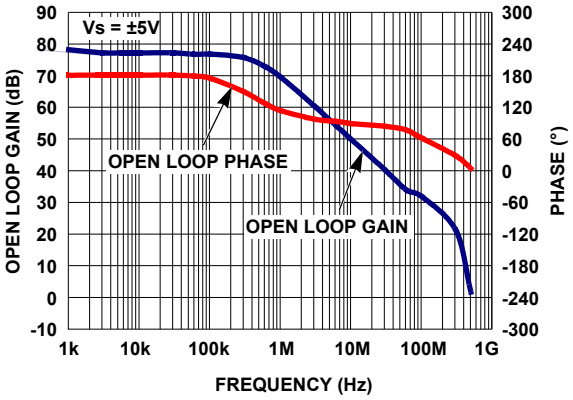


FIGURE 16. OPEN LOOP GAIN AND PHASE vs FREQUENCY

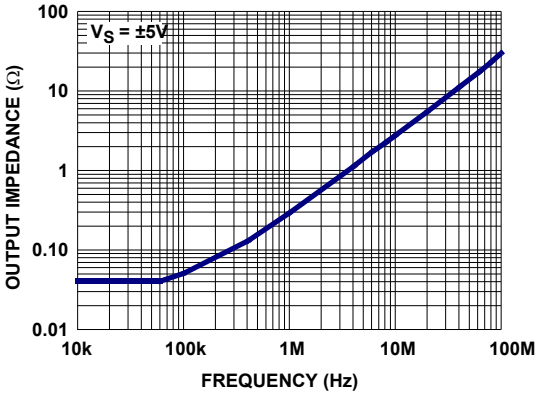


FIGURE 17. OUTPUT IMPEDANCE vs FREQUENCY

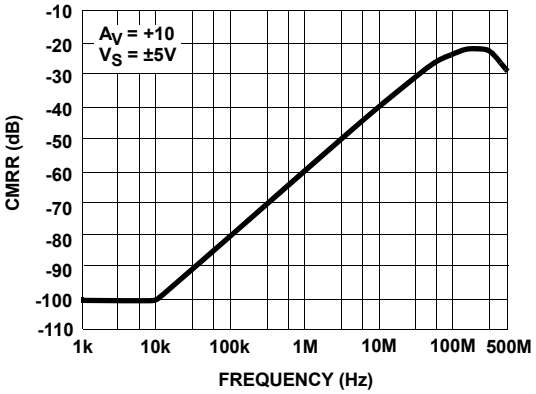


FIGURE 18. CMRR vs FREQUENCY

Typical Performance Curves (Continued)

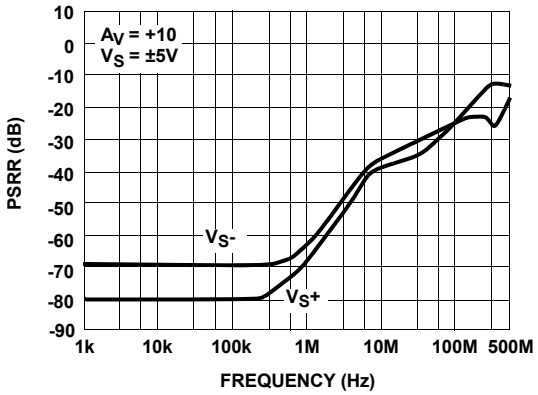


FIGURE 19. PSRR vs FREQUENCY

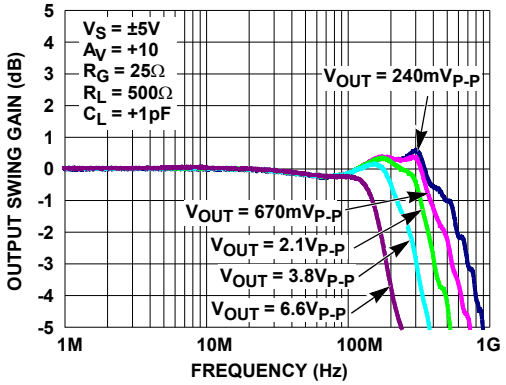


FIGURE 20. OUTPUT SWING vs FREQUENCY

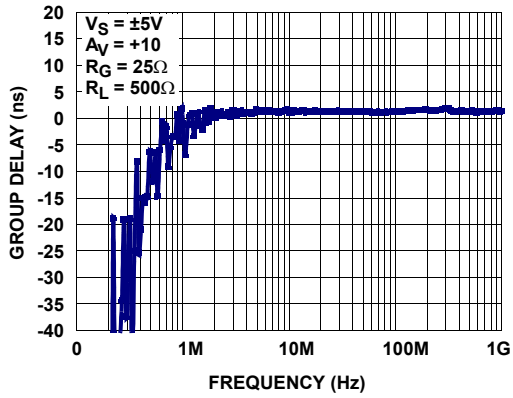


FIGURE 21. GROUP DELAY vs FREQUENCY

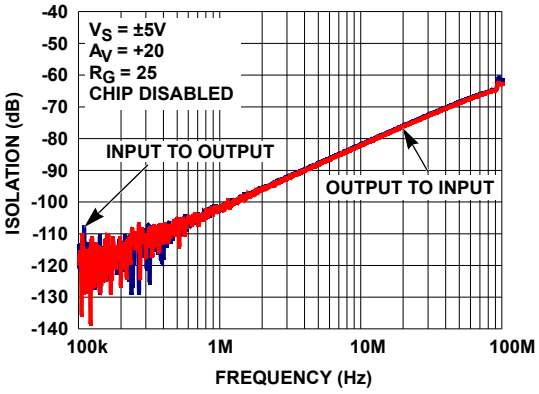


FIGURE 22. INPUT AND OUTPUT ISOLATION

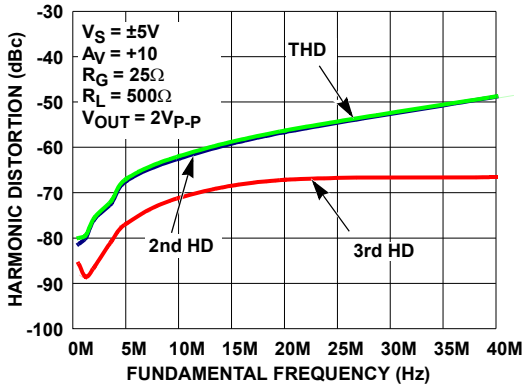


FIGURE 23. HARMONIC DISTORTION vs FREQUENCY

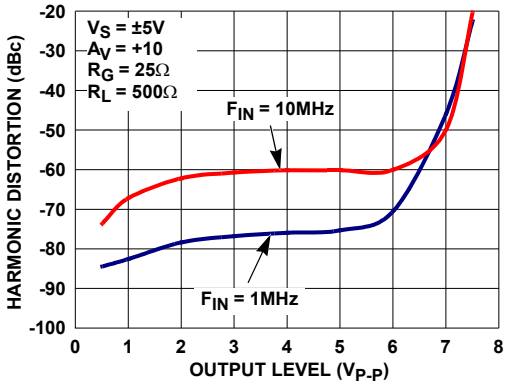


FIGURE 24. TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE

Typical Performance Curves (Continued)

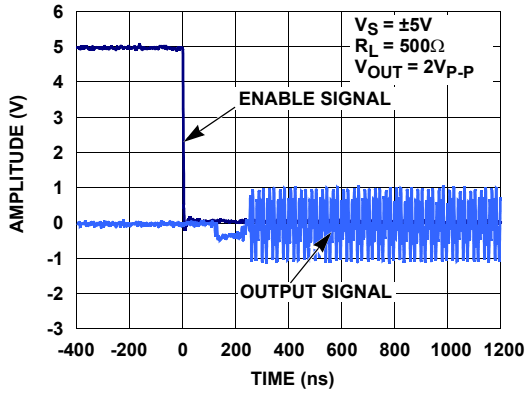


FIGURE 25. ENABLE TIME

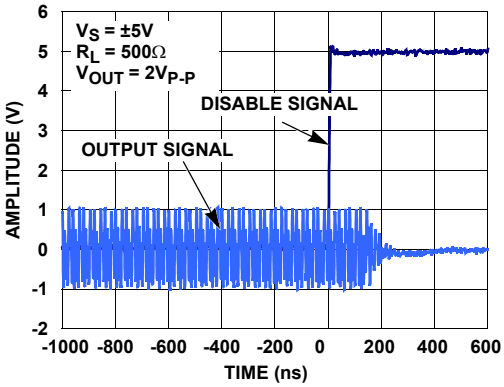


FIGURE 26. DISABLE TIME

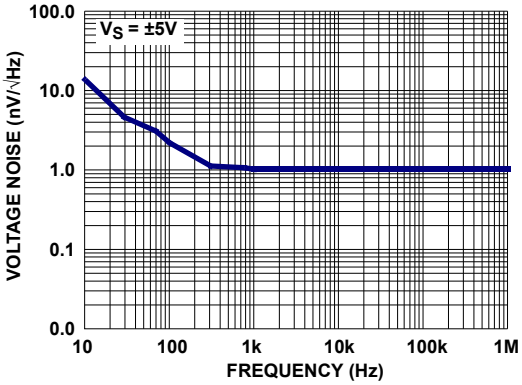


FIGURE 27. EQUIVALENT INPUT VOLTAGE NOISE vs FREQUENCY

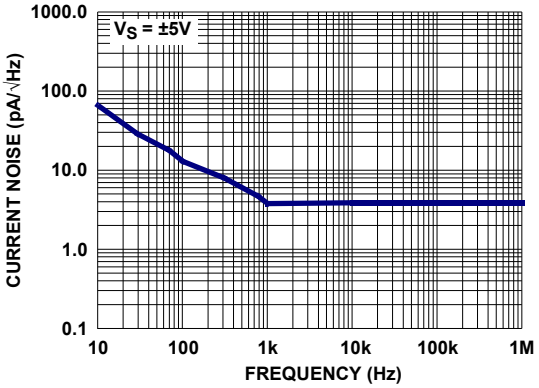


FIGURE 28. EQUIVALENT INPUT CURRENT NOISE vs FREQUENCY

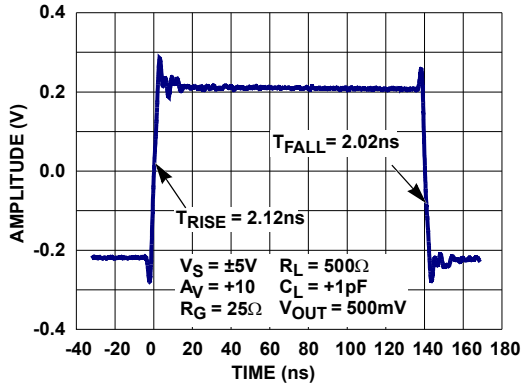


FIGURE 29. SMALL SIGNAL STEP RESPONSE_RISE AND FALL TIME

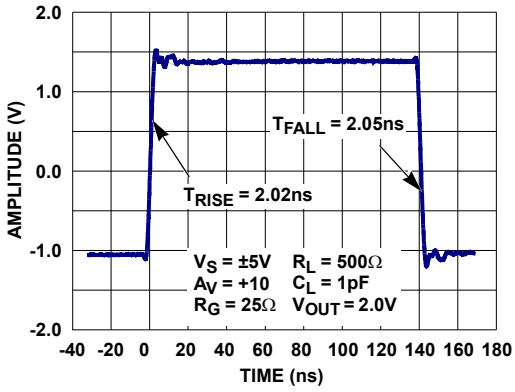


FIGURE 30. LARGE SIGNAL STEP RESPONSE_RISE AND FALL TIME

Typical Performance Curves (Continued)

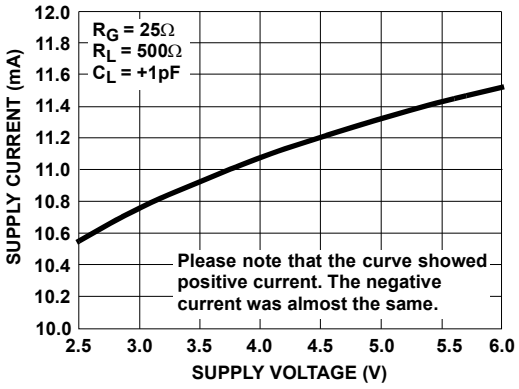


FIGURE 31. SUPPLY CURRENT vs SUPPLY VOLTAGE

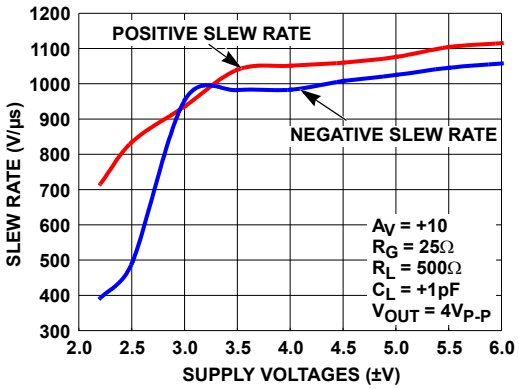


FIGURE 32. SLEW RATE vs SUPPLY VOLTAGES

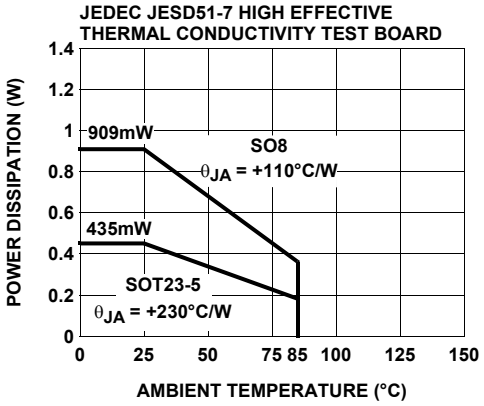


FIGURE 33. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

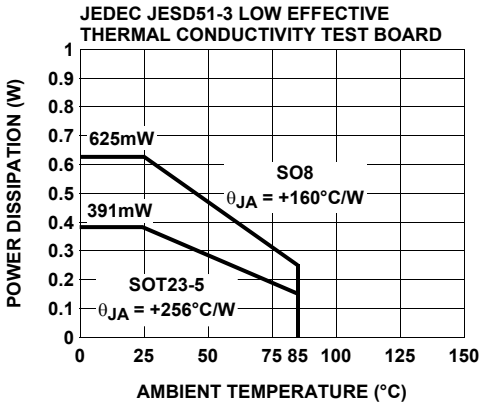


FIGURE 34. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

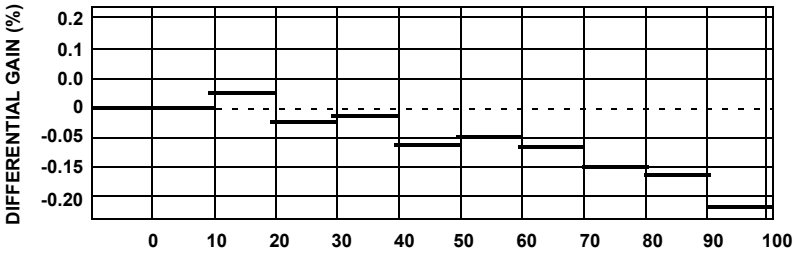


FIGURE 35. DIFFERENTIAL GAIN (%)

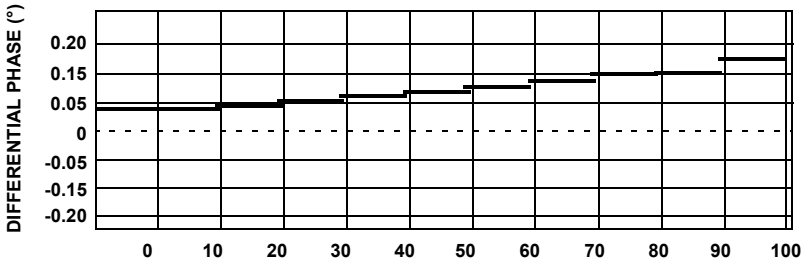


FIGURE 36. DIFFERENTIAL PHASE (°)

Applications Information

Product Description

The EL5132, EL5133 is a voltage feedback operational amplifier designed for communication and imaging applications requiring very low voltage and current noise. It also features low distortion while drawing moderately low supply current and is built on Intersil's proprietary high-speed complementary bipolar process. The EL5132, EL5133 uses a classical voltage-feedback topology which allows them to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier.

Gain-Bandwidth Product and the -3dB Bandwidth

The EL5132, EL5133 has a gain-bandwidth product of 3000MHz while using only 11mA of supply current. For gains greater than 10, their closed-loop -3dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains of 10, higher-order poles in the amplifiers' transfer function contribute to even higher closed loop bandwidths. For example, the EL5132, EL5133 have a -3dB bandwidth of 670MHz at a gain of 10, dropping to 150MHz at a gain of 30. It is important to note that the EL5132, EL5133 is designed so that this “extra” bandwidth in low-gain application does not come at the expense of stability. As seen in the typical performance curves, the EL5132, EL5133 in a gain of only 10 exhibited 0.5dB of peaking with a 500Ω load.

Output Drive Capability

The EL5132 and EL5133 are is designed to drive a low impedance load. It can easily drive $6V_{P-P}$ signal into a 500Ω load. This high output drive capability makes the EL5132, EL5133 an ideal choice for RF, IF, and video applications. Furthermore, the EL5132, EL5133 is current-limited at the output, allowing it to withstand momentary short to ground. However, the power dissipation with output-shorted cannot exceed the power dissipation capability of the package.

Driving Cables and Capacitive Loads

Although the EL5132, EL5133 is designed to drive low impedance load, capacitive loads will decreases the amplifier's phase margin. As shown in the performance curves, capacitive load can result in peaking, overshoot and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated with a series resistor between 5Ω to 20Ω. When driving coaxial cables, double termination is always recommended for reflection-free performance. When properly terminated, the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier.

Disable/Power-Down

The EL5132 amplifier can be disabled placing its output in a high impedance state. When disable, the amplifier current is reduced to 12µA. The EL5132 is disabled when it $\overline{CE}$ pin is pulled up to within 1V of the power supply. Similarly, the amplifier is enabled by floating or pulling its $\overline{CE}$ pin to at least 3V below the positive supply. For ±5V supply, this means that an EL5132 amplifier will be enabled when $\overline{CE}$ is 2V or

less, and disabled when $\overline{CE}$ is above 4V. Although the logic levels are not standard TTL, this choice of logic voltages allows the EL5132 to be enabled by typing $\overline{CE}$ to ground, even in 5V single supply applications. The $\overline{CE}$ pin can be driving from CMOS outputs.

Supply Voltage Range and Single-Supply Operation

The EL5132 and EL5133 have been designed to operate with supply voltages having a span of greater than 5V and less than 12V. In practical terms, this means that they will operate on dual supplies ranging from ±2.5V to ±6V. With single-supply, the EL5132 and EL5133 will operate from 5V to 12V. To prevent internal circuit latch-up, the slew rate between the negative and positve supplies must be less than 1V/µs.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL5132 and EL5133 have an input range which extends to within 2V of either supply. So, for example, on ±5V supplies, the EL5132 and EL5133 have an input range which spans ±3V. The output range of the EL5132 and EL5133 are also quite large, extending to within 2V of the supply rail. On a ±5V supply, the output is therefore capable of swinging from -3.1V to +3.1V. Single-supply output range is larger because of the increased negative swing due to the external pull-down resistor to ground.

Power Dissipation

With the wide power supply range and large output drive capability of the EL5132 and EL5133, it is possible to exceed the 150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified for the EL5132 and EL5133 to remain in the safe operating area. These parameters are related as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated as follows:

$$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

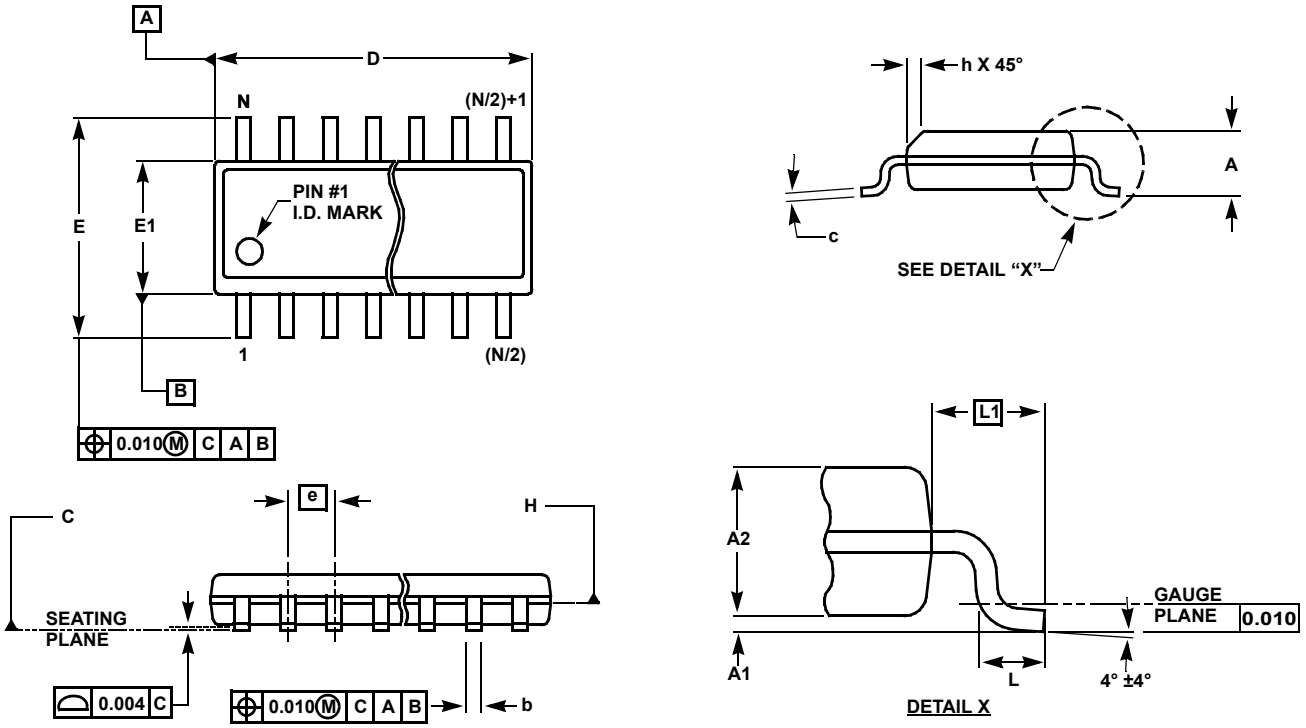
- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Power Supply Bypassing And Printed Circuit Board Layout

As with any high frequency devices, good printed circuit board layout is essential for optimum performance. Ground plane construction is highly recommended. Pin lengths should be kept as short as possible. The power supply pins must be closely bypassed to reduce the risk of oscillation. The combination of a 4.7µF tantalum capacitor in parallel with 0.1µF ceramic capacitor has been proven to work well when placed at each supply pin. For single supply operation, where pin 4 (V_S-) is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor across pin 8 (V_S+).

For good AC performance, parasitic capacitance should be kept to a minimum. Ground plane construction again should be used. Small chip resistors are recommended to minimize series inductance. Use of sockets should be avoided since they add parasitic inductance and capacitance which will result in additional peaking and overshoot.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

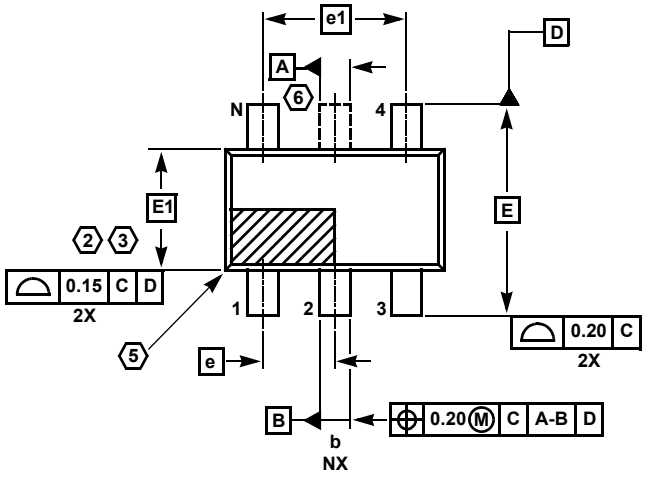
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

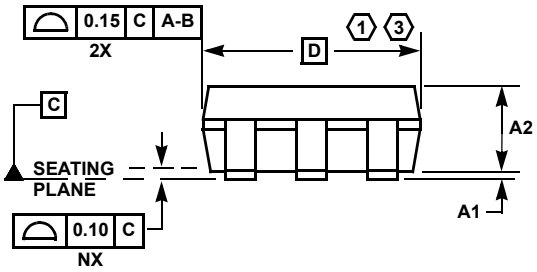
Rev. M 2/07

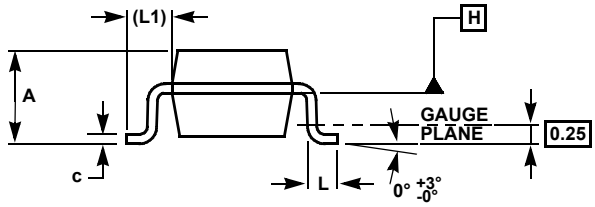
NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

SOT-23 Package Family







MDP0038

SOT-23 PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

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