

FEATURES

- Maximum supply current: 80 μ A
- Minimum CMRR: 100 dB
- Drives heavy capacitive loads: $\sim$ 700 pF
- Rail-to-rail output
- Input voltage range goes below ground
- Gain set with 2 external resistors
- Can achieve low gain drift at any gain
- Very wide power supply range
 - Single supply: 2.7 V to 36 V
 - Dual supply: $\pm$ 2.7 V to $\pm$ 18 V
- Bandwidth (G = 100): 2.5 kHz
- Input voltage noise: 55 nV/ $\sqrt$ Hz
- High dc precision
 - Maximum offset voltage: 125 μ V
 - Maximum offset drift: 1 μ V/ $^{\circ}$ C
- Maximum differential input voltage: $\pm$ 1 V
- 8-lead MSOP package

APPLICATIONS

- Bridge amplifiers
- Pressure measurement
- Medical instrumentation
- Portable data acquisition
- Multichannel systems

GENERAL DESCRIPTION

The **AD8420** is a low cost, micropower, wide supply range, instrumentation amplifier with a rail-to-rail output and a novel architecture that allows for extremely flexible design. It is optimized to amplify small differential voltages in the presence of large common-mode signals.

The **AD8420** is based on an indirect current feedback architecture that gives it an excellent input common-mode range. Unlike conventional instrumentation amplifiers, the **AD8420** can easily amplify signals at or even slightly below ground without requiring dual supplies. The **AD8420** has rail-to-rail output, and the output voltage swing is completely independent of the input common-mode voltage.

PIN CONFIGURATION

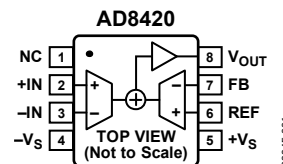


Figure 1.

Table 1. Instrumentation Amplifiers by Category¹

General Purpose	Zero Drift	Military Grade	Low Power	Digital Gain
AD8221, AD8222	AD8231	AD620	AD8420	AD8250
AD8220, AD8224	AD8290	AD621	AD8235, AD8236	AD8251
AD8226, AD8227	AD8293	AD524	AD627	AD8253
AD8228	AD8553	AD526	AD8226, AD8227	AD8231
AD8295, AD8224	AD8556	AD624	AD623	
	AD8557		AD8223	

¹ See www.analog.com for the latest instrumentation amplifiers.

Single-supply operation, micropower current consumption, and rail-to-rail output swing make the **AD8420** ideal for battery-powered applications. Its rail-to-rail output stage maximizes dynamic range when operating from low supply voltages. Dual-supply operation ($\pm$ 15 V) and low power consumption make the **AD8420** ideal for a wide variety of applications in medical or industrial instrumentation.

The **AD8420** is available in an 8-lead MSOP package. Performance is specified over the full temperature range of -40° C to $+85^{\circ}$ C, and the part is operational from -40° C to $+125^{\circ}$ C.

Rev. 0

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REVISION HISTORY

3/12—Revision 0: Initial Version

SPECIFICATIONS

+V_S = +5 V, -V_S = 0 V, V_{REF} = 0 V, V_{+IN} = 0 V, V_{-IN} = 0 V, T_A = 25°C, G = 1 to 1000, R_L = 20 kΩ, specifications referred to input, unless otherwise noted. All Table 2 limits are valid from V_S = 3 V to V_S = ±5 V, unless otherwise specified.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	V _{CM} = 0 V to 2.7 V				
CMRR DC to 60 Hz		100			dB
CMRR at 1 kHz		100			dB
NOISE					
Voltage Noise					
Spectral Density	f = 1 kHz, V _{DIFF} ≤ 100 mV		55		nV/√Hz
Peak to Peak	f = 0.1 Hz to 10 Hz, V _{DIFF} ≤ 100 mV		1.5		μV p-p
Current Noise					
Spectral Density	f = 1 kHz		80		fA/√Hz
Peak to Peak	f = 0.1 Hz to 10 Hz		3		pA p-p
VOLTAGE OFFSET					
Offset	V _S = 3 V to V _S = 5 V			125	μV
	V _S = ±5 V			150	μV
Average Temperature Coefficient	T _A = -40°C to +85°C			1	μV/°C
Offset RTI vs. Supply (PSR)	V _S = 2.7 V to 5 V	86			dB
INPUTS					
Input Bias Current ¹	Valid for REF and FB pair, as well as +IN and -IN				
	T _A = +25°C		20	27	nA
	T _A = +85°C			24	nA
	T _A = -40°C			30	nA
Average Temperature Coefficient	T _A = -40°C to +85°C		30		pA/°C
Input Offset Current	T _A = +25°C			1	nA
	T _A = +85°C			1	nA
	T _A = -40°C			1	nA
Average Temperature Coefficient	T _A = -40°C to +85°C		0.5		pA/°C
Input Impedance					
Differential			130 2		MΩ pF
Common Mode			1000 2		MΩ pF
Differential Input Operating Voltage	T _A = -40°C to +85°C	-1		+1	V
Input Operating Voltage (+IN, -IN, REF, or FB)	T _A = +25°C	-V _S - 0.15		+V _S - 2.2	V
	T _A = +85°C	-V _S - 0.05		+V _S - 1.8	V
	T _A = -40°C	-V _S - 0.2		+V _S - 2.7	V
DYNAMIC RESPONSE					
Small Signal -3 dB Bandwidth					
G = 1			250		kHz
G = 10			25		kHz
G = 100			2.5		kHz
G = 1000			0.25		kHz
Settling Time 0.01%	V _S = ±5 V				
G = 1	-1 V to +1 V output step		3		μs
G = 10	-4.5 V to +4.5 V output step		130		μs
G = 100	-4.5 V to +4.5 V output step		1		ms
Slew Rate			1		V/μs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GAIN²	$G = 1 + (R2/R1)$				
Gain Range		1		1000	V/V
Gain Error					
$G = 1$	$V_{OUT} = 0.1 \text{ V to } 1.1 \text{ V}, V_{REF} = 0.1 \text{ V}$			0.02	%
$G = 10 \text{ to } 1000$	$V_{OUT} = 0.2 \text{ V to } 4.8 \text{ V}$		0.05	0.1	%
Gain vs. Temperature	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			10	ppm/°C
OUTPUT					
Output Swing	$V_S = 5 \text{ V}, R_L = 10 \text{ k}\Omega$ to midsupply $V_S = \pm 5 \text{ V}, R_L = 20 \text{ k}\Omega$ to ground $T_A = +25^\circ\text{C}$ $T_A = +85^\circ\text{C}$ $T_A = -40^\circ\text{C}$	$-V_S + 0.1$ $-V_S + 0.1$ $-V_S + 0.1$		$+V_S - 0.15$ $+V_S - 0.2$ $+V_S - 0.15$	V V V
Short-Circuit Current			10		mA
POWER SUPPLY					
Operating Range	Single-supply operation ³	2.7		36	V
Quiescent Current	$V_S = 5 \text{ V}$ $T_A = +25^\circ\text{C}$ $T_A = +85^\circ\text{C}$ $T_A = -40^\circ\text{C}$	55	70	80 95 65	μA μA μA
TEMPERATURE RANGE					
Specified		-40		+85	°C
Operational ⁴		-40		+125	°C

¹ The input stage uses PNP transistors; therefore, input bias current always flows out of the part.

² For $G > 1$, errors from External Resistor R1 and External Resistor R2 should be considered in addition to these specifications, including error from FB pin bias current.

³ Minimum supply voltage indicated for V_{+IN} , V_{-IN} , and $V_{REF} = 0 \text{ V}$.

⁴ See the Typical Performance Characteristics section for operation between 85°C and 125°C .

+V_S = +15 V, -V_S = -15 V, V_{REF} = 0 V, T_A = 25°C, G = 1 to 1000, R_L = 20 kΩ, specifications referred to input, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	V _{CM} = -10 V to +10 V				
CMRR DC to 60 Hz		100			dB
CMRR at 1 kHz		100			dB
NOISE					
Voltage Noise					
Spectral Density	f = 1 kHz, V _{DIFF} ≤ 100 mV		55		nV/√Hz
Peak to Peak	f = 0.1 Hz to 10 Hz, V _{DIFF} ≤ 100 mV		1.5		μV p-p
Current Noise					
Spectral Density	f = 1 kHz		80		fA/√Hz
Peak to Peak	f = 0.1 Hz to 10 Hz		3		pA p-p
VOLTAGE OFFSET					
Offset	V _S = ±15 V ¹			250	μV
Average Temperature Coefficient	T _A = -40°C to +85°C			1	μV/°C
Offset RTI vs. Supply (PSR)	V _S = ±15 V	100			dB
INPUTS	Valid for REF and FB pair, as well as +IN and -IN				
Input Bias Current ²	T _A = +25°C		20	27	nA
	T _A = +85°C			24	nA
	T _A = -40°C			30	nA
Average Temperature Coefficient	T _A = -40°C to +85°C		30		pA/°C
Input Offset Current	T _A = +25°C			1	nA
	T _A = +85°C			1	nA
	T _A = -40°C			1	nA
Average Temperature Coefficient	T _A = -40°C to +85°C		0.5		pA/°C
Input Impedance					
Differential			130 3		MΩ pF
Common Mode			1000 3		MΩ pF
Differential Input Operating Voltage	T _A = -40°C to +85°C	-1		1	V
Input Operating Voltage (+IN, -IN, REF, or FB)	T _A = +25°C	-V _S - 0.15		+V _S - 2.2	V
	T _A = +85°C	-V _S - 0.05		+V _S - 1.8	V
	T _A = -40°C	-V _S - 0.2		+V _S - 2.7	V
DYNAMIC RESPONSE					
Small Signal -3 dB Bandwidth					
G = 1			250		kHz
G = 10			25		kHz
G = 100			2.5		kHz
G = 1000			0.25		kHz
Settling Time 0.01%					
G = 1	-1 V to +1 V output step		3		μs
G = 10	-5 V to +5 V output step		130		μs
G = 100	-5 V to +5 V output step		1		ms
Slew Rate			1		V/μs
GAIN ³	G = 1 + (R2/R1)				
Gain Range		1		1000	V/V
Gain Error					
G = 1	V _{OUT} = ±1 V			0.02	%
G = 10 to 1000	V _{OUT} = ±10 V		0.05	0.1	%
Gain vs. Temperature	T _A = -40°C to +85°C			10	ppm/°C

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT					
Output Swing					
$R_L = 20\text{ k}\Omega$ to Ground	$T_A = +25^\circ\text{C}$	$-V_S + 0.13$		$+V_S - 0.2$	V
	$T_A = +85^\circ\text{C}$	$-V_S + 0.15$		$+V_S - 0.23$	V
	$T_A = -40^\circ\text{C}$	$-V_S + 0.11$		$+V_S - 0.16$	V
Short-Circuit Current			10		mA
POWER SUPPLY					
Operating Range	Dual-supply operation ⁴	± 2.7		± 18	V
Quiescent Current	$V_S = \pm 15\text{ V}$				
	$T_A = +25^\circ\text{C}$	70	85	100	μA
	$T_A = +85^\circ\text{C}$			120	μA
	$T_A = -40^\circ\text{C}$			90	μA
TEMPERATURE RANGE					
Specified		-40		$+85$	$^\circ\text{C}$
Operational ⁵		-40		$+125$	$^\circ\text{C}$

¹ See the Typical Performance Characteristics section for the offset voltage vs. supply.

² The input stage uses PNP transistors; therefore, input bias current always flows out of the part.

³ For $G > 1$, errors from External Resistor R1 and External Resistor R2 should be considered in addition to these specifications, including error from FB pin bias current.

⁴ Minimum positive supply voltage indicated for V_{+IN} , V_{-IN} , and $V_{REF} = 0\text{ V}$. With V_{+IN} , V_{-IN} , and $V_{REF} = -V_S$, minimum supply is $\pm 1.35\text{ V}$.

⁵ See the Typical Performance Characteristics section for operation between 85°C and 125°C .

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	± 18 V
Output Short-Circuit Current	Indefinite
Maximum Voltage at $-IN$ or $+IN$	$-V_S + 40$ V
Minimum Voltage at $-IN$ or $+IN$	$-V_S - 0.5$ V
Maximum Voltage at REF or FB	$+V_S + 0.5$ V
Minimum Voltage at REF or FB	$-V_S - 0.5$ V
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
ESD	
Human Body Model	2.5 kV
Charge Device Model	1.5 kV
Machine Model	0.1 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device in free air.

Table 5.

Package	θ_{JA}	Unit
8-Lead MSOP, 4-Layer JEDEC Board	135	$^{\circ}\text{C}/\text{W}$

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

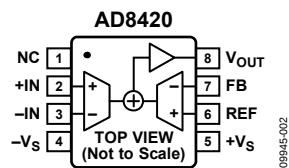


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	This pin is not connected internally. For best CMRR vs. frequency and leakage performance, connect this pin to negative supply.
2	+IN	Positive Input.
3	-IN	Negative Input
4	-Vs	Negative Supply.
5	+Vs	Positive Supply.
6	REF	Reference Input.
7	FB	Feedback Input.
8	V _{OUT}	Output.

TYPICAL PERFORMANCE CHARACTERISTICS

T = 25°C, +V_S = 5 V, R_L = 20 kΩ, unless otherwise noted.

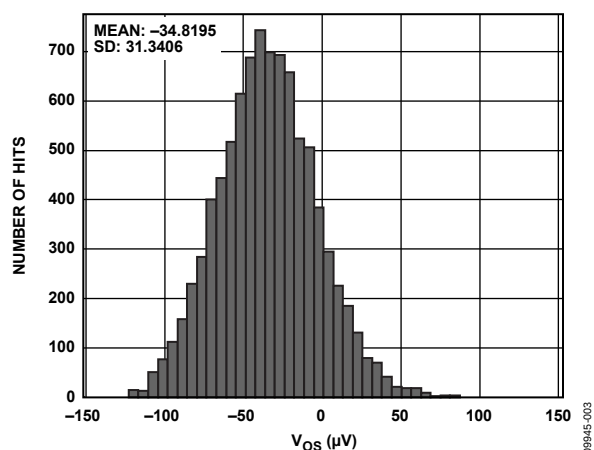


Figure 3. Typical Distribution of Input Offset Voltage

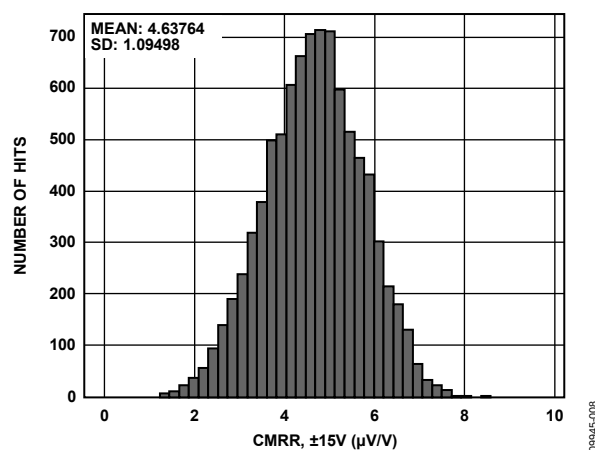


Figure 6. Typical Distribution of CMRR

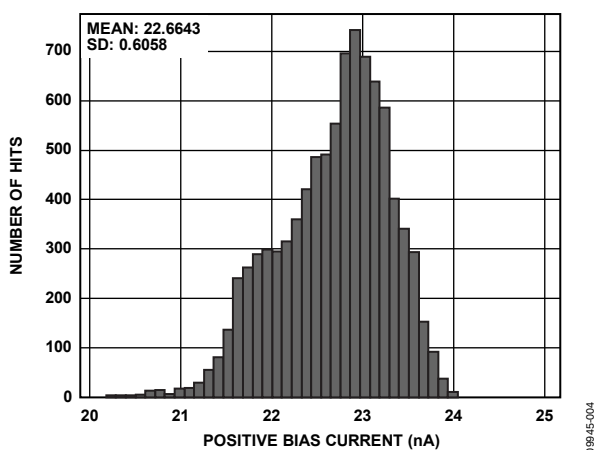


Figure 4. Typical Distribution of Input Bias Current

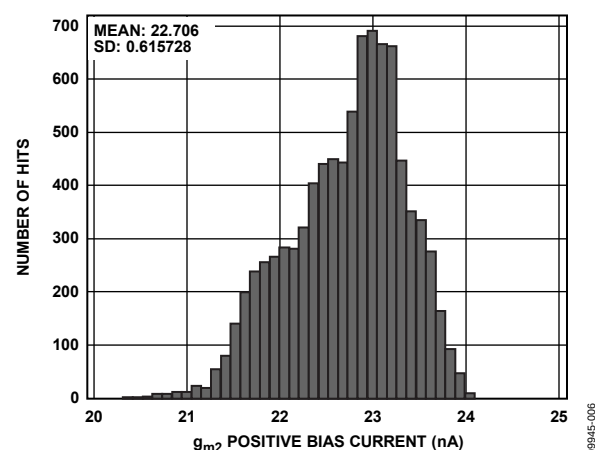


Figure 7. Typical Distribution of REF, FB Bias Current

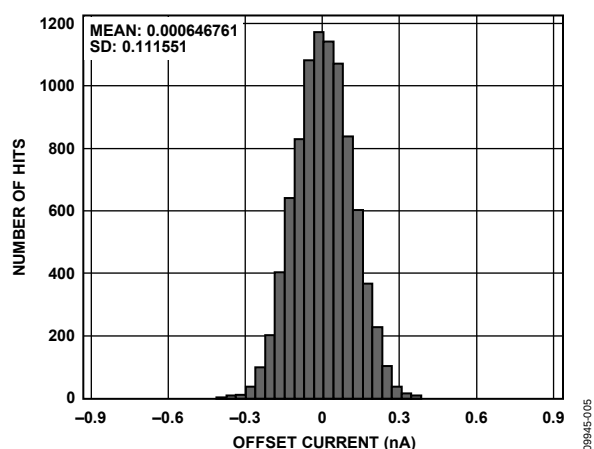


Figure 5. Typical Distribution of Input Offset Current

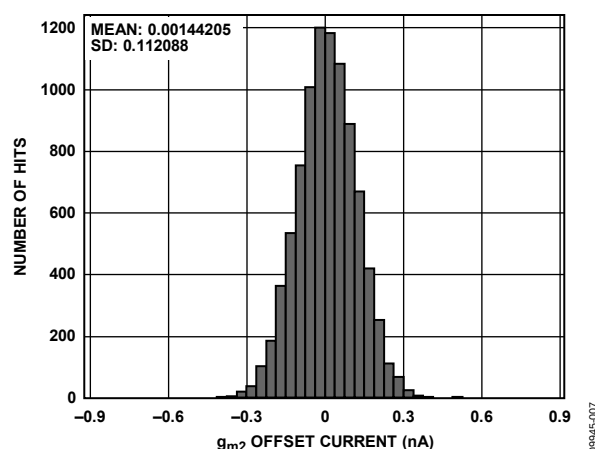
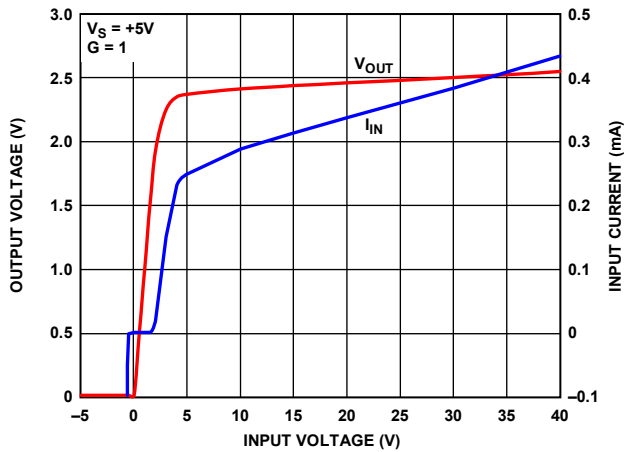
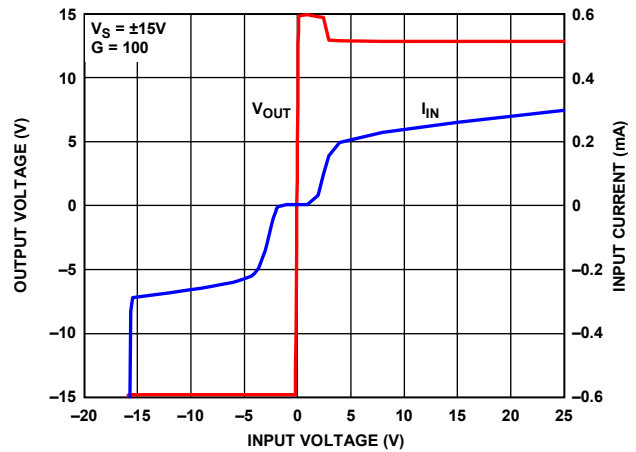


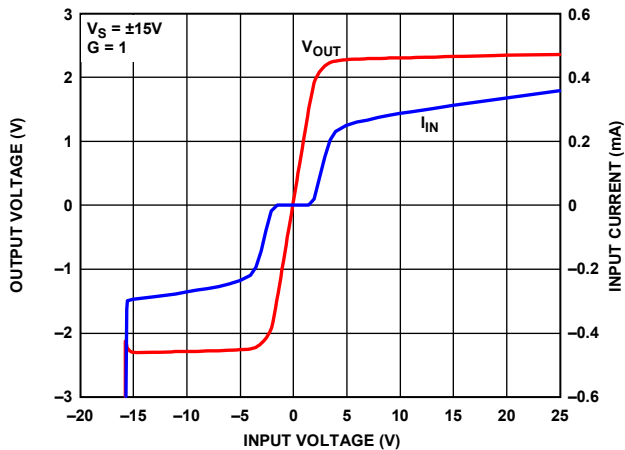
Figure 8. Typical Distribution of REF, FB Offset Current

Figure 9. Input Overvoltage Performance, $G = 1$

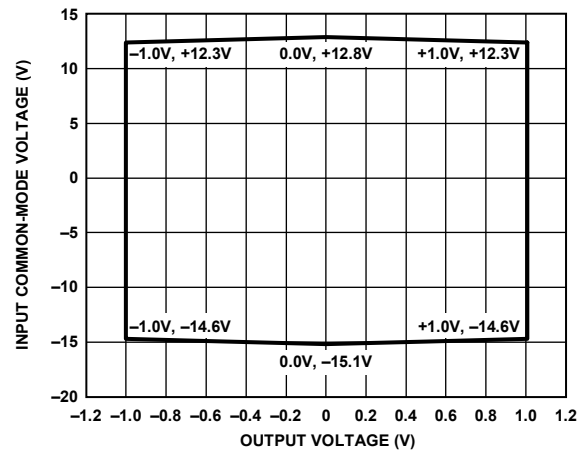
09945-309

Figure 12. Input Overvoltage Performance, $G = 100$, $V_S = \pm 15\text{ V}$

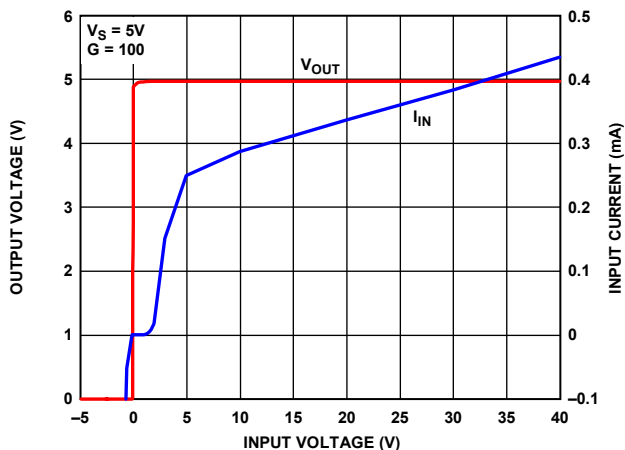
09945-312

Figure 10. Input Overvoltage Performance, $G = 1$, $V_S = \pm 15\text{ V}$

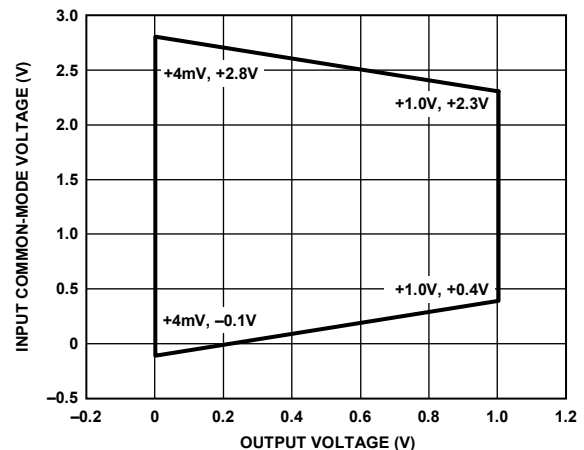
09945-310

Figure 13. Input Common-Mode Voltage vs. Output Voltage, $G = 1$, $V_S = \pm 15\text{ V}$

09945-313

Figure 11. Input Overvoltage Performance, $G = 100$

09945-311

Figure 14. Input Common-Mode Voltage vs. Output Voltage, $G = 1$, $V_S = 5\text{ V}$

09945-314

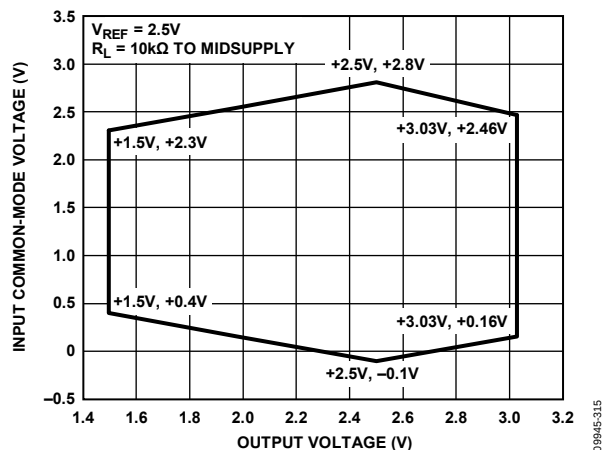


Figure 15. Input Common-Mode Voltage vs. Output Voltage, $G = 1$, $V_S = 5\text{ V}$, $V_{REF} = 2.5\text{ V}$

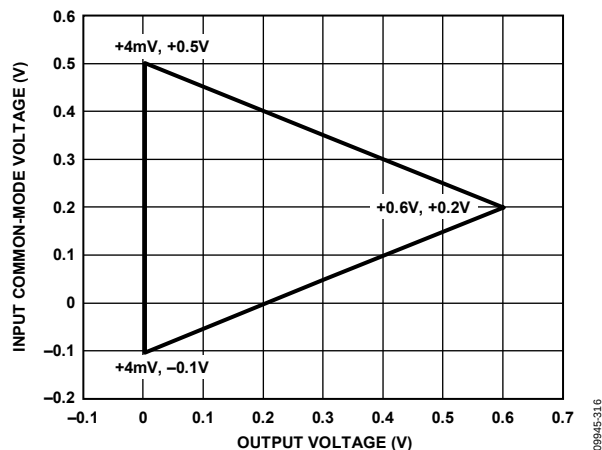


Figure 16. Input Common-Mode Voltage vs. Output Voltage, $G = 1$, $V_S = 2.7\text{ V}$

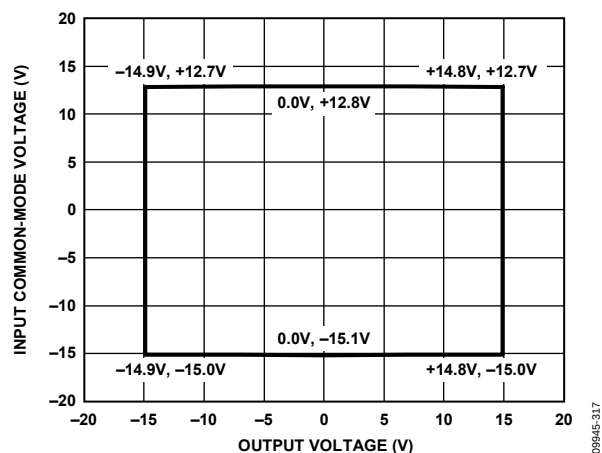


Figure 17. Input Common-Mode Voltage vs. Output Voltage, $G = 100$, $V_S = \pm 15\text{ V}$

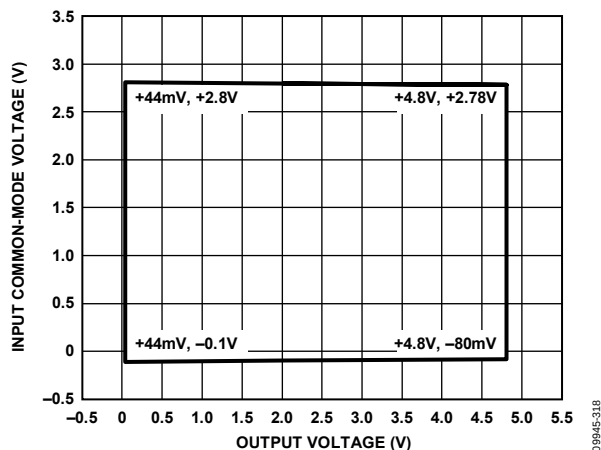


Figure 18. Input Common-Mode Voltage vs. Output Voltage, $G = 100$, $V_S = 5\text{ V}$

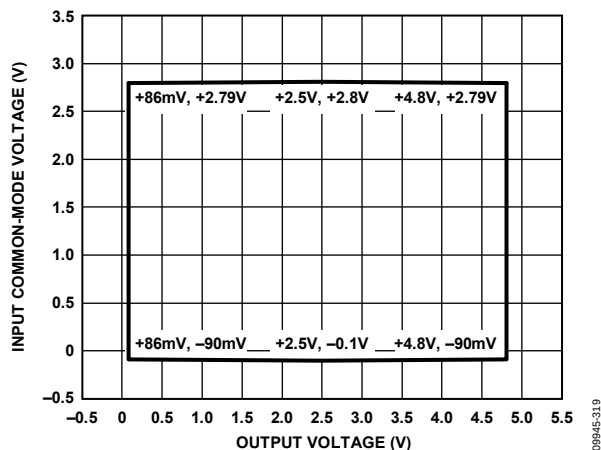


Figure 19. Input Common-Mode Voltage vs. Output Voltage, $G = 100$, $V_S = 5\text{ V}$, $V_{REF} = 2.5\text{ V}$

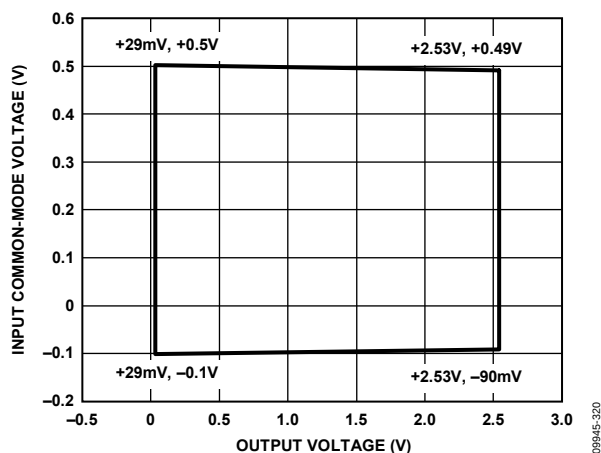


Figure 20. Input Common-Mode Voltage vs. Output Voltage, $G = 100$, $V_S = 2.7\text{ V}$

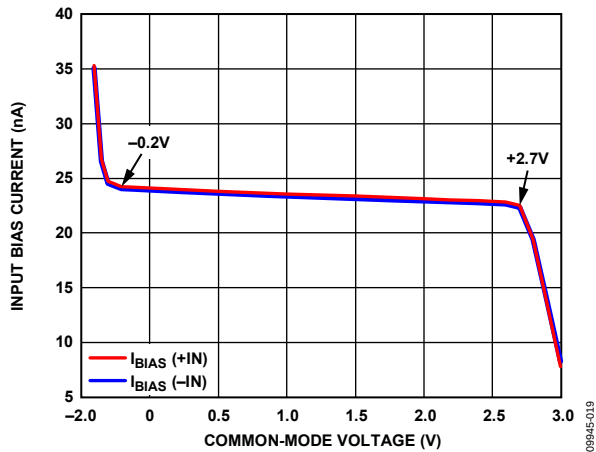


Figure 21. Input Bias Current vs. Common-Mode Voltage

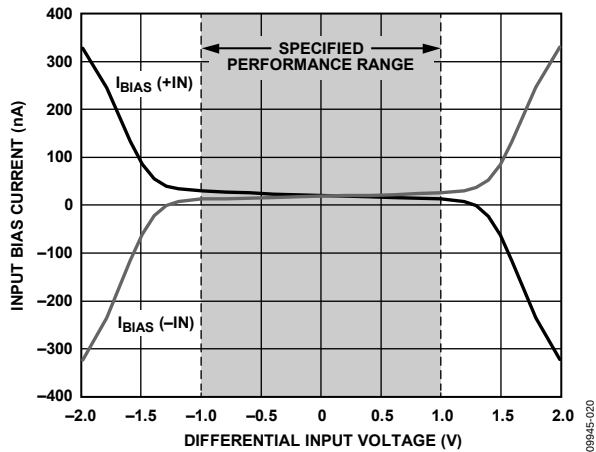
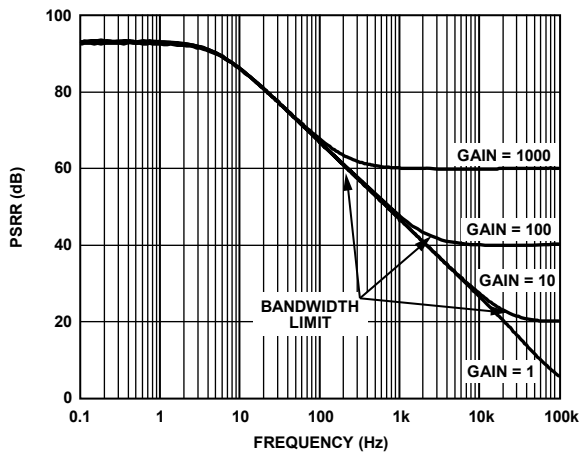
Figure 22. Input Bias Current vs. Differential Input Voltage, $V_S = \pm 15V$ 

Figure 23. PSRR vs. Frequency on 5 V Supply

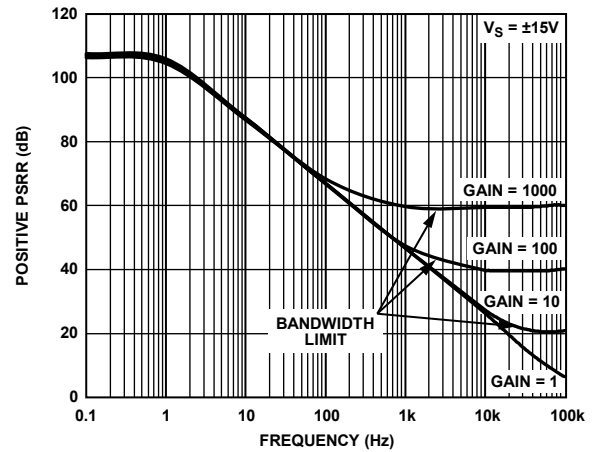
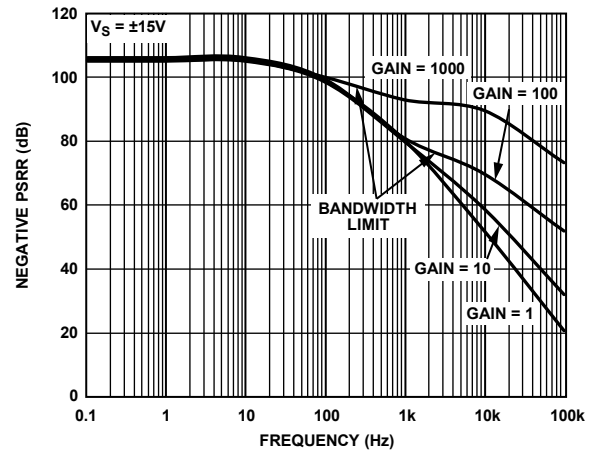
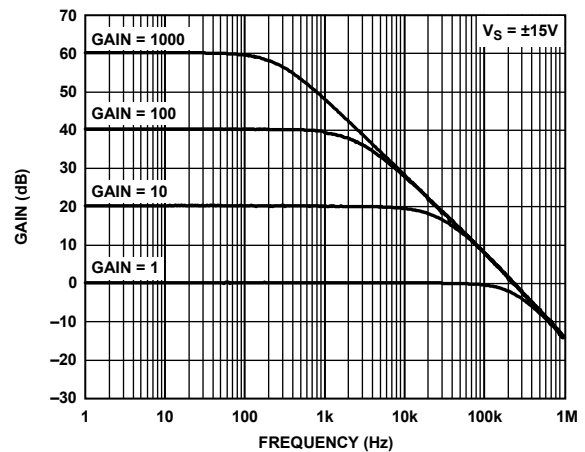
Figure 24. Positive PSRR vs. Frequency, RTI, $V_S = \pm 15V$ Figure 25. Negative PSRR vs. Frequency, RTI, $V_S = \pm 15V$ 

Figure 26. Gain vs. Frequency

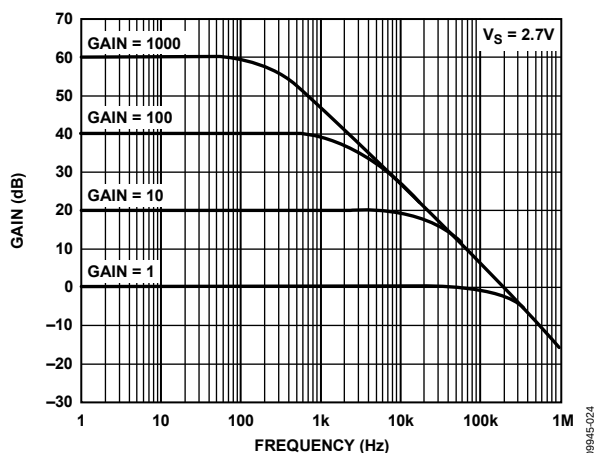


Figure 27. Gain vs. Frequency, 2.7 V Single Supply

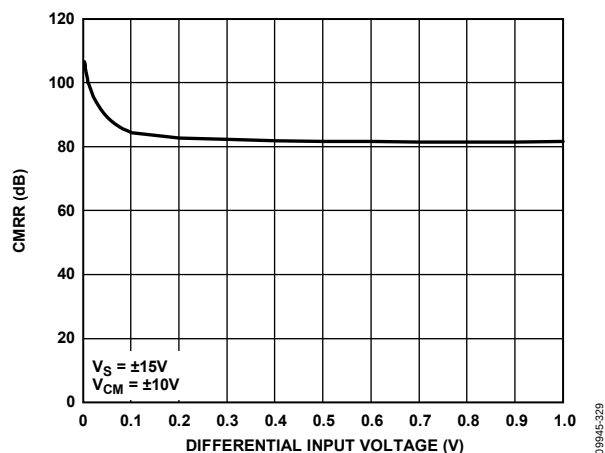


Figure 30. CMRR vs. Differential Input Voltage

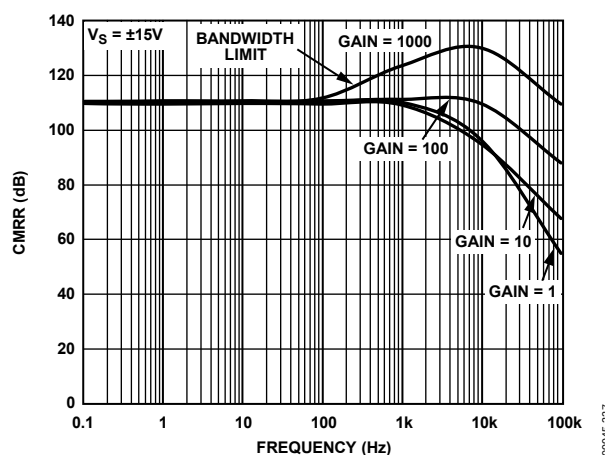
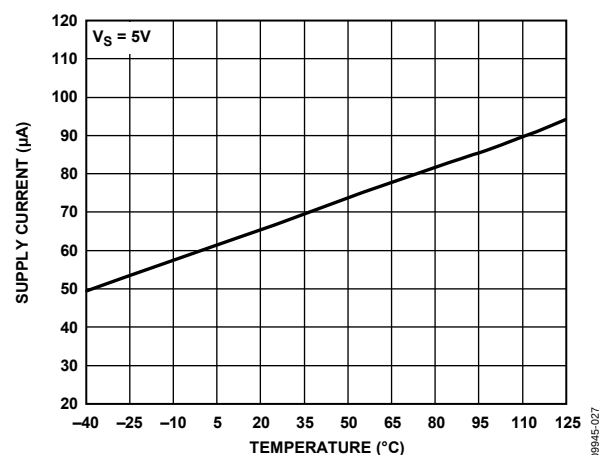
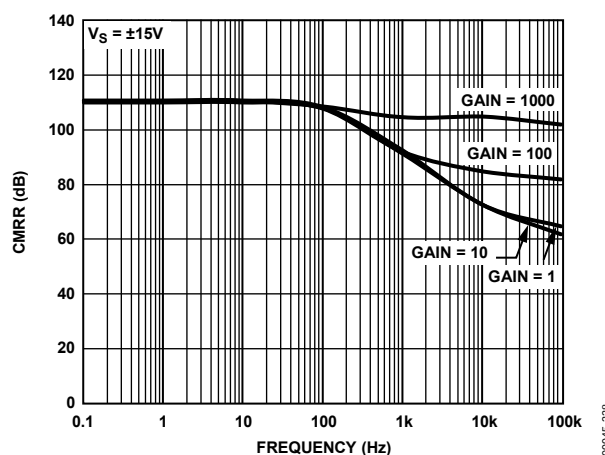
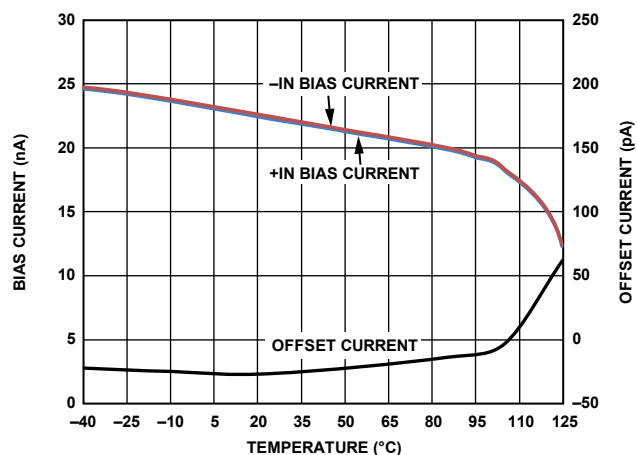
Figure 28. CMRR vs. Frequency, RTI, $V_S = \pm 15V$ Figure 31. Supply Current vs. Temperature, $V_S = +5 V$ Figure 29. CMRR vs. Frequency, RTI, 1 k Ω Source Imbalance, $V_S = \pm 15V$ 

Figure 32. Input Bias Current and Input Offset Current vs. Temperature

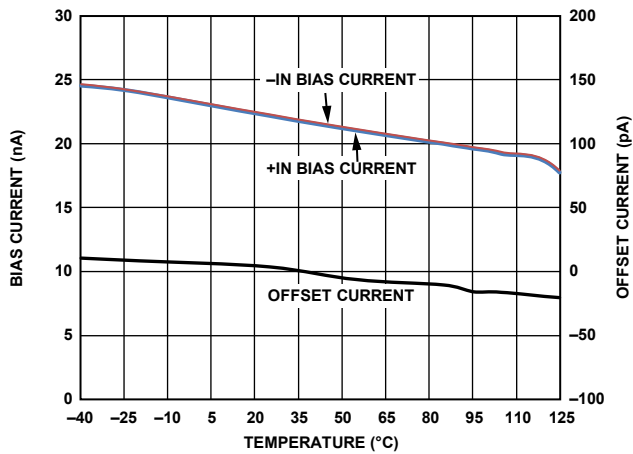


Figure 33. FB, REF Bias Current and FB, REF Offset Current vs. Temperature

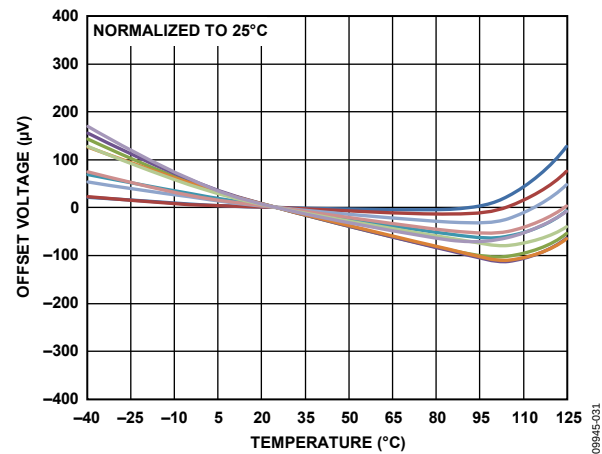
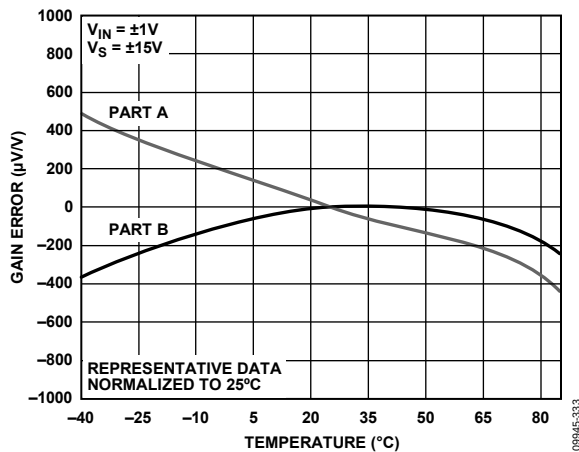
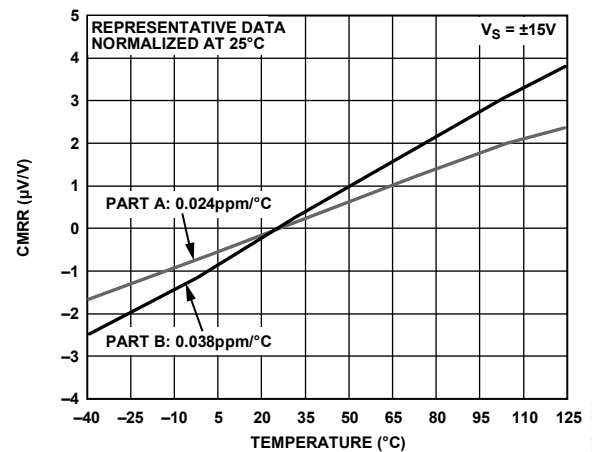
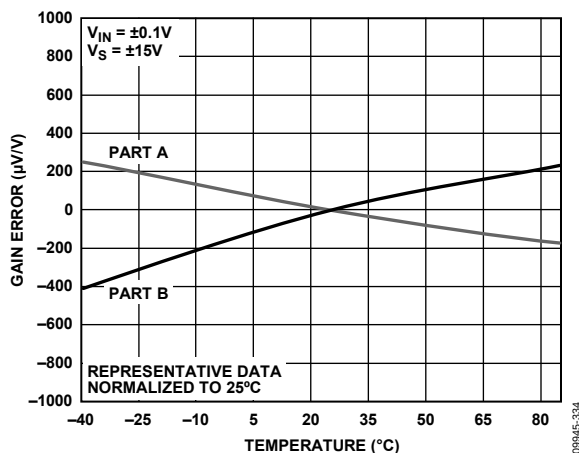
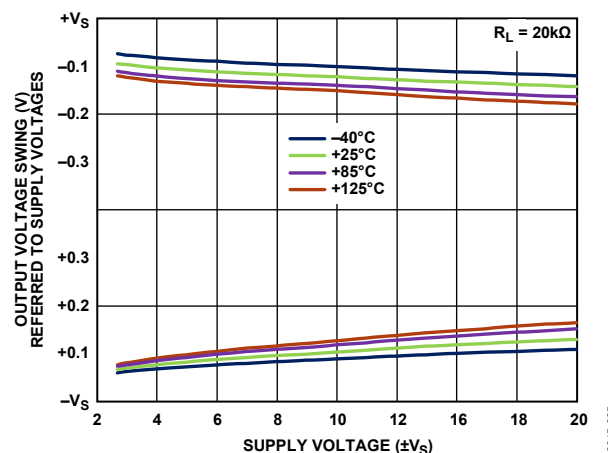


Figure 36. Offset Drift

Figure 34. Gain Error vs. Temperature, $G = 1$, $V_{IN} = \pm 1 V$, $V_S = \pm 15 V$ Figure 37. CMRR vs. Temperature, $G = 1$, $V_S = \pm 15 V$ Figure 35. Gain Error vs. Temperature, $G = 1$, $V_{IN} = \pm 0.1 V$, $V_S = \pm 15 V$ Figure 38. Output Voltage Swing vs. Supply Voltage, $R_L = 20 k\Omega$

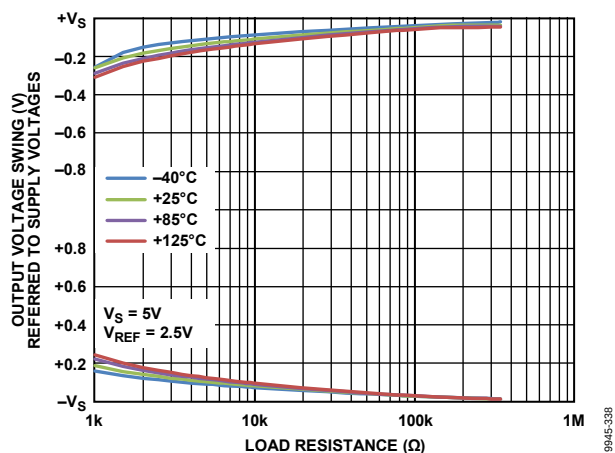
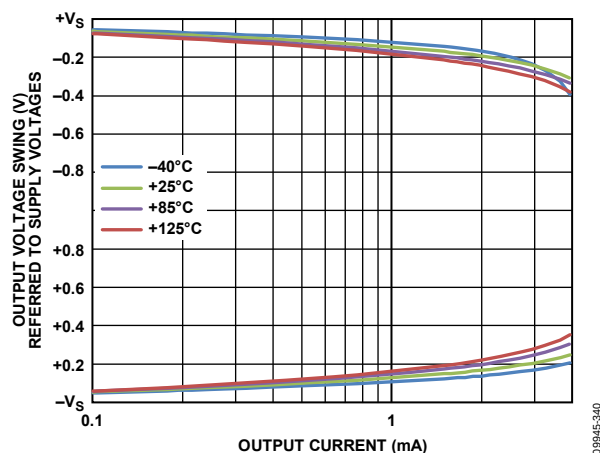
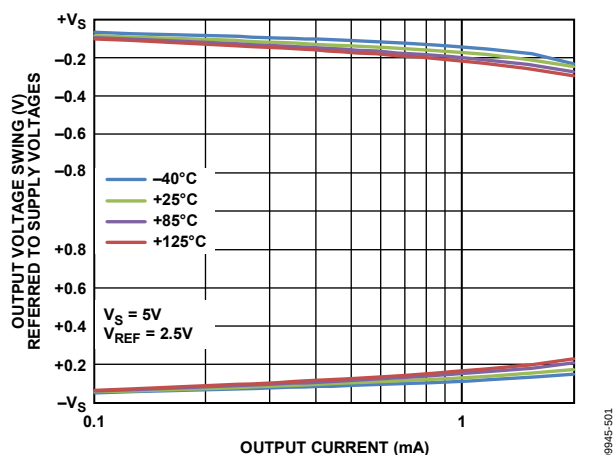
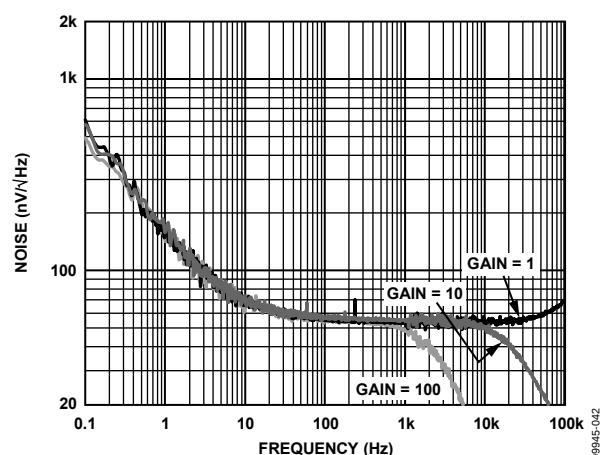
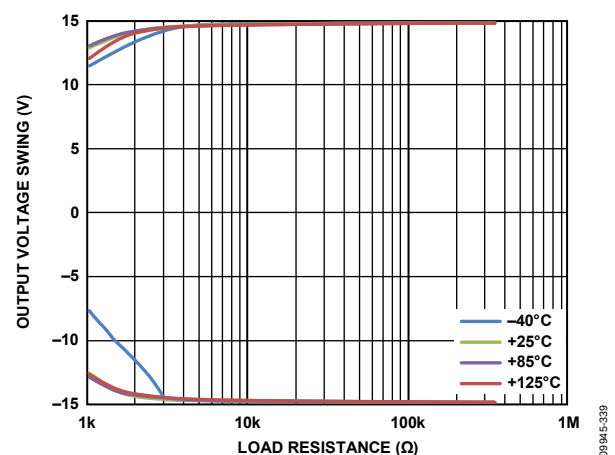
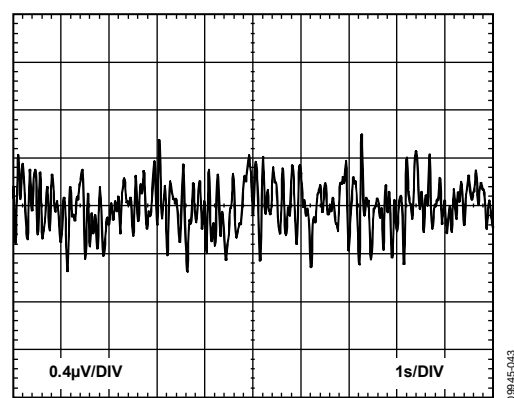
Figure 39. Output Voltage Swing vs. Load Resistance, $V_S = 5\text{ V}$ Figure 42. Output Voltage Swing vs. Output Current, $V_S = \pm 15\text{ V}$ Figure 40. Output Voltage Swing vs. Load Resistance, $V_S = 5\text{ V}$ 

Figure 43. Voltage Noise Spectral Density vs. Frequency, RTI

Figure 41. Output Voltage Swing vs. Load Resistance, $V_S = \pm 15\text{ V}$ Figure 44. 0.1 Hz to 10 Hz RTI Voltage Noise, $G = 1$

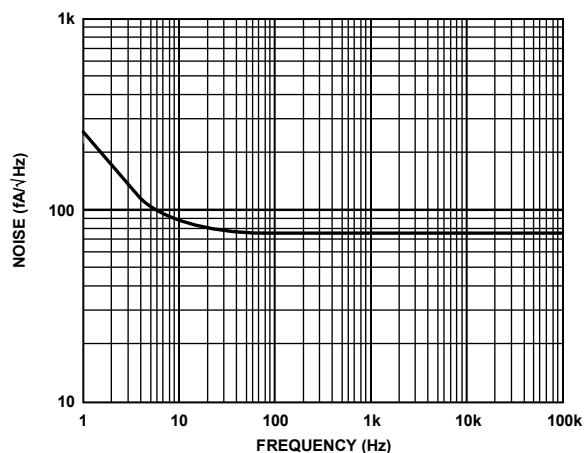


Figure 45. Current Noise Spectral Density vs. Frequency

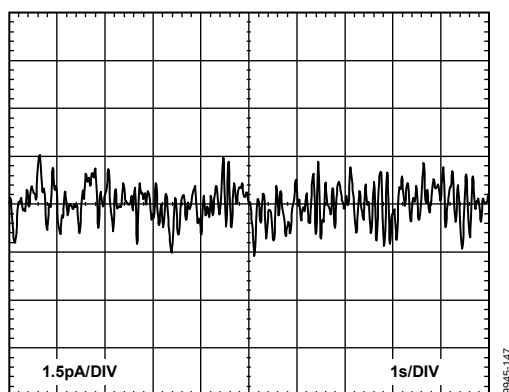


Figure 46. 0.1 Hz to 10 Hz Current Noise

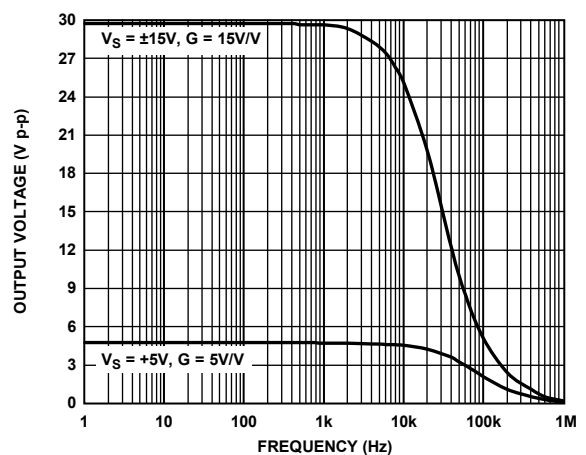
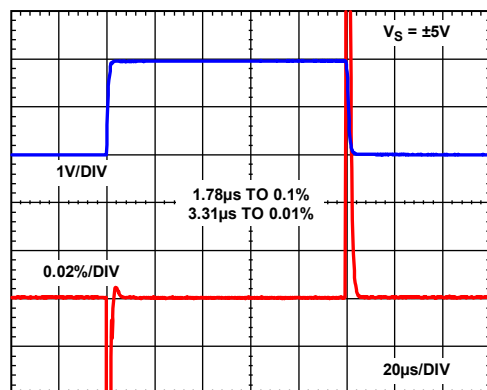
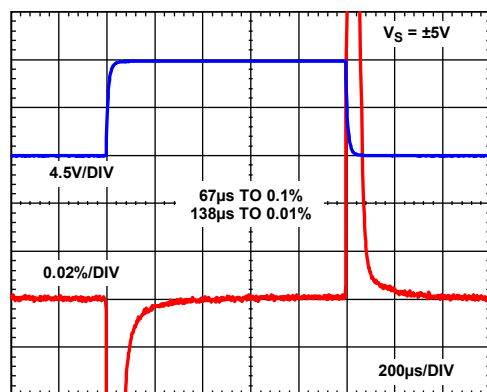
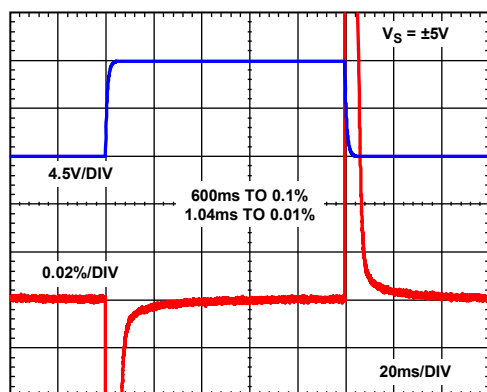


Figure 47. Large Signal Frequency Response

Figure 48. Large Signal Pulse Response and Settling Time, $G = 1$ Figure 49. Large Signal Pulse Response and Settling Time, $G = 10$ Figure 50. Large Signal Pulse Response and Settling Time, $G = 100$

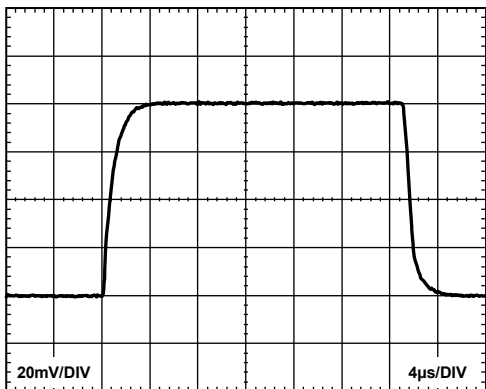
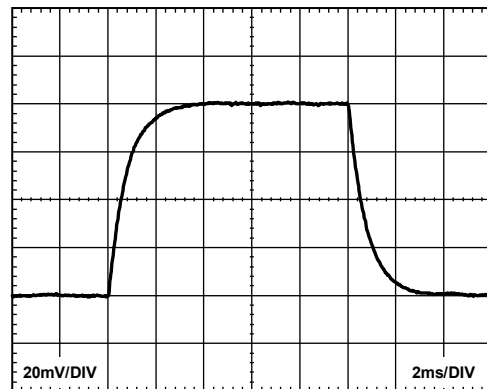
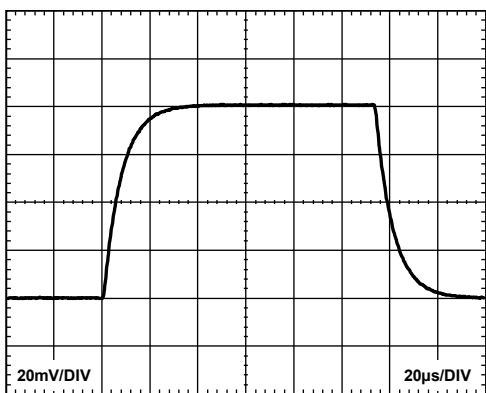
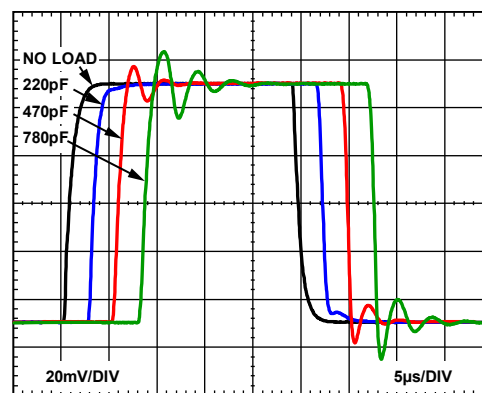
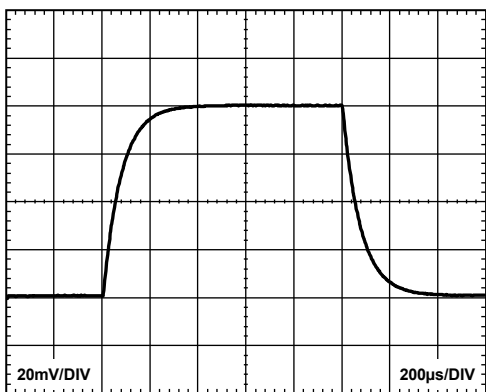
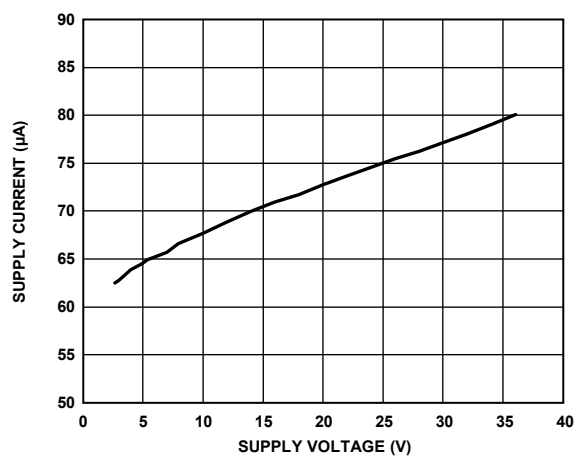
Figure 51. Small Signal Pulse Response, $G = 1$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$ Figure 54. Small Signal Pulse Response, $G = 1000$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$ Figure 52. Small Signal Pulse Response, $G = 10$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$ Figure 55. Small Signal Response with Various Capacitive Loads, $G = 1$, $R_L = \infty$ Figure 53. Small Signal Pulse Response, $G = 100$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$ 

Figure 56. Supply Current vs. Supply Voltage

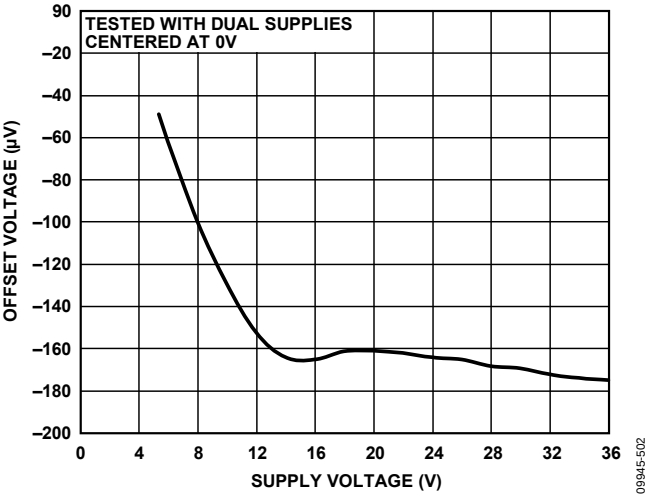


Figure 57. Offset Voltage vs. Supply Voltage

THEORY OF OPERATION

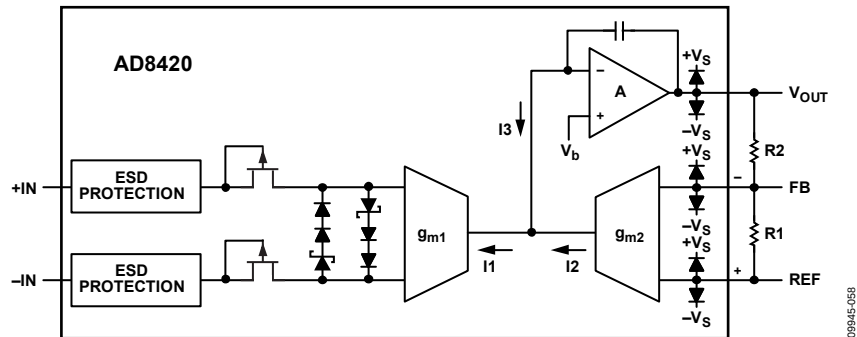


Figure 58. Simplified Schematic

ARCHITECTURE

The **AD8420** is based on an indirect current feedback topology consisting of three amplifiers: two matched transconductance amplifiers that convert voltage to current and one integrator amplifier that converts current to voltage.

For the **AD8420**, assume that all initial voltages and currents are zero until a positive differential voltage is applied between the inputs, +IN and -IN. Transconductance Amplifier g_{m1} converts this input voltage into a current, I_1 . Because the voltage across g_{m2} is initially zero, I_2 is zero and I_3 equals I_1 .

I_3 is integrated to the output, making the output voltage, V_{OUT} , increase. This voltage continues to increase until the same differential input voltage across the inputs of g_{m1} is replicated across the inputs of g_{m2} , generating a current (I_2) equal to I_1 . This reduces the Difference Current I_3 to zero so that the output remains at a stable voltage. The gain in the configuration shown in Figure 58 is set by R_2 and R_1 .

In traditional instrumentation amplifiers, the input common-mode voltage can limit the available output swing, typically depicted in a hexagon plot. Because the **AD8420** converts the input differential signals to current, this limit does not apply. This is particularly important when amplifying a signal with a common-mode voltage near one of the supply rails.

To improve robustness and ease of use, the **AD8420** includes overvoltage protection on its inputs. This protection scheme allows wide differential input voltages without damaging the part.

SETTING THE GAIN

The transfer function of the **AD8420** is

$$V_{OUT} = G(V_{+IN} - V_{-IN}) + V_{REF}$$

where:

$$G = 1 + \frac{R_2}{R_1}$$

Table 7. Suggested Resistors for Various Gains, 1% Resistors

R1 (kΩ)	R2 (kΩ)	Gain
None	Short	1.00
49.9	49.9	2.00
20	80.6	5.03
10	90.9	10.09
5	95.3	20.06
2	97.6	49.8
1	100	101
1	200	201
1	499	500
1	1000	1001

While the ratio of R_2 to R_1 sets the gain, the designer determines the absolute value of the resistors. Larger values reduce power consumption and output loading; smaller values limit the FB input bias current and offset current error. For best output swing and distortion performance, keep $(R_1 + R_2) \parallel R_L \geq 20 \text{ k}\Omega$.

A method that allows large value feedback resistors while limiting FB bias current error is to place a resistor of value $R_1 \parallel R_2$ in series with the REF terminal, as shown in Figure 59. At higher gains, this resistor can simply be the same value as R_1 .

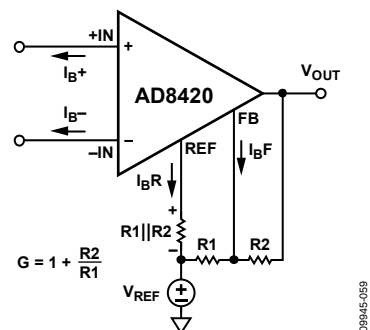


Figure 59. Cancelling Out Error from FB Input Bias Current

GAIN ACCURACY

Unlike most instrumentation amplifiers, the relative match of the two gain setting resistors determines the gain accuracy of the AD8420 rather than a single resistor. For example, if two resistors have exactly the same absolute error, there is no error in gain. Conversely, two 1% resistors can cause approximately 2% maximum gain error at high gains. Temperature coefficient mismatch of the gain setting resistors increases the gain drift of the instrumentation amplifier circuit. Because these external resistors do not have to match any on-chip resistors, resistors with good TC tracking can achieve excellent gain drift.

When the differential voltage at the inputs approaches the differential input limit, the diodes start to conduct, limiting the voltage seen by the inputs. This can look like increased gain error at large differential inputs. Performance of the AD8420 is specified for ± 1 V differential from -40°C to $+85^{\circ}\text{C}$. However, at higher temperatures, the reduced forward voltage of the diodes limits the differential input to a smaller voltage. Figure 60 tracks 1% error across the operating temperature range to show the effect of temperature on the input limit.

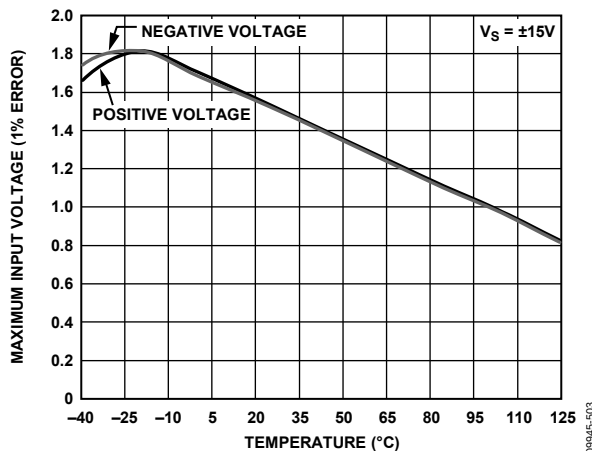


Figure 60. Differential Input Limit vs. Temperature

INPUT VOLTAGE RANGE

The allowed input range of the AD8420 is much simpler than traditional architectures. For the transfer function of the AD8420 to be valid, the input voltage should follow two rules:

- Keep the differential input voltage within ± 1 V.
- Keep the voltage on the +IN, -IN, REF, and FB pins in the specified input voltage range.

Because the output swing is completely independent of the input common-mode voltage, there are no hexagonal figures or complicated formulas to follow, and no limitation for the output swing the amplifier has for input signals with changing common mode.

INPUT PROTECTION

The current into the AD8420 inputs is limited internally. This ensures that the diodes that limit the differential voltage seen by the internal amplifier do not draw excessive current when they turn on. The part can handle large differential input voltages, regardless of the amount of gain applied, without damage. As a result, the AD8420 inputs are protected from voltages beyond the positive rail. If voltages beyond the negative rail are expected, external protection must be used.

Keep all of the AD8420 terminals within the voltage range specified in the Absolute Maximum Ratings section. All terminals of the AD8420 are protected against ESD.

Input Voltages Beyond the Rails

For applications that require protection beyond the negative rail, one option is to use an external resistor in series with each input to limit current during overload conditions. In this case, size the resistors to limit the current into the AD8420 to 6 mA.

$$R_{\text{PROTECT}} \geq (\text{Negative Supply} - V_{\text{IN}})/6 \text{ mA}$$

Although the AD8420 inputs must still be kept within the $-V_S + 40$ V limitation, the $I \times R$ drop across the protection resistor increases the protection on the positive side to approximately $(40 \text{ V} + \text{Negative Supply}) + 300 \mu\text{A} \times R_{\text{PROTECT}}$

An alternate protection method is to place diodes at the AD8420 inputs to limit voltage and resistors in series with the inputs to limit the current into these diodes. To keep input bias current at a minimum for normal operation, use low leakage diode clamps, such as the BAV199. The AD8420 also combines well with TVS diodes, such as the PTVSxS1UR.

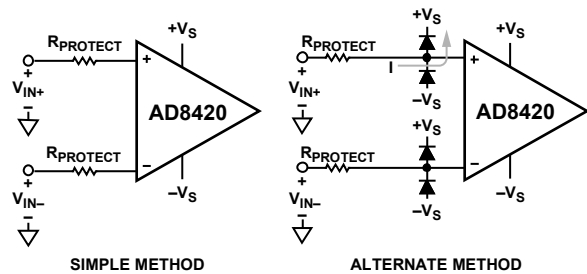


Figure 61. Protection for Voltages Beyond the Rails

Large Differential Input Voltage

The AD8420 is able to handle large differential input voltage without damage to the part. Refer to Figure 9, Figure 10, Figure 11, and Figure 12 for overvoltage performance. The AD8420 differential voltage is internally limited with diodes to ± 1 V. If this limit is exceeded, the diodes start to conduct and draw current, as shown in Figure 22. This current is limited internally to a value that is safe for the AD8420, but if the input current cannot be tolerated in the system, place resistors in series with each input with the following value:

$$R_{\text{PROTECT}} \geq \frac{1}{2} \left(\frac{|V_{\text{DIFF}}| - 1 \text{ V}}{I_{\text{MAX}}} \right)$$

LAYOUT

Common-Mode Rejection Ratio over Frequency

Poor layout can cause some of the common-mode signal to be converted to a differential signal before reaching the in-amp. This conversion can occur when the path to the positive input pin has a different frequency response than the path to the negative input pin. For best CMRR vs. frequency performance, the input source impedance and capacitance of each path should be closely matched. This includes connecting Pin 1 to $-V_S$, which matches the parasitic capacitance and the leakage between the inputs and adjacent pins. Place additional source resistance in the input path (for example, for input protection) close to the in-amp inputs to minimize their interaction with the parasitic capacitance from the printed circuit board (PCB) traces.

Power Supplies

Use a stable dc voltage to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. For more information, see the PSRR performance curves in Figure 24 and Figure 25.

Place a 0.1 μF capacitor as close as possible to each supply pin. As shown in Figure 62, a 10 μF tantalum capacitor can be used farther away from the part. This capacitor, which is intended to be effective at low frequencies, can usually be shared by other precision integrated circuits. Keep the traces between these integrated circuits short to minimize interaction of the trace parasitic inductance with the shared capacitor.

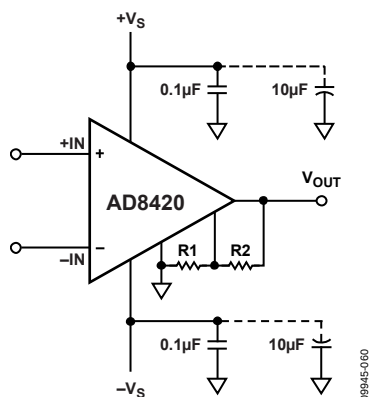


Figure 62. Supply Decoupling, REF, and Output Referred to Local Ground

Reference

The output voltage of the AD8420 is developed with respect to the potential on the reference terminal. Take care to tie REF to the appropriate local ground. The differential voltage at the inputs is reproduced between the REF and FB pins; therefore, it is important to set V_{REF} so that the voltage at FB does not exceed the input range.

DRIVING THE REFERENCE PIN

Traditional instrumentation amplifier architectures require the reference pin to be driven with a low impedance source. In these architectures, impedance at the reference pin degrades both CMRR and gain accuracy. With the AD8420 architecture, resistance at the reference pin has no effect on CMRR.

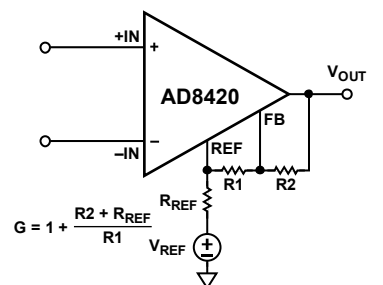


Figure 63. Calculating Gain with Reference Resistance

Resistance at the reference pin does affect the gain of the AD8420, but if this resistance is constant, the gain setting resistors can be adjusted to compensate. For example, the AD8420 can be driven with a voltage divider as shown in Figure 64.

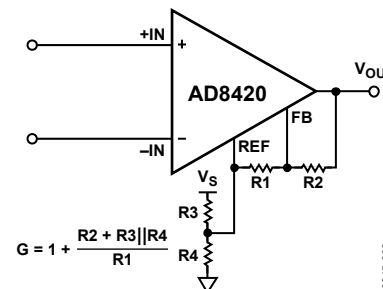
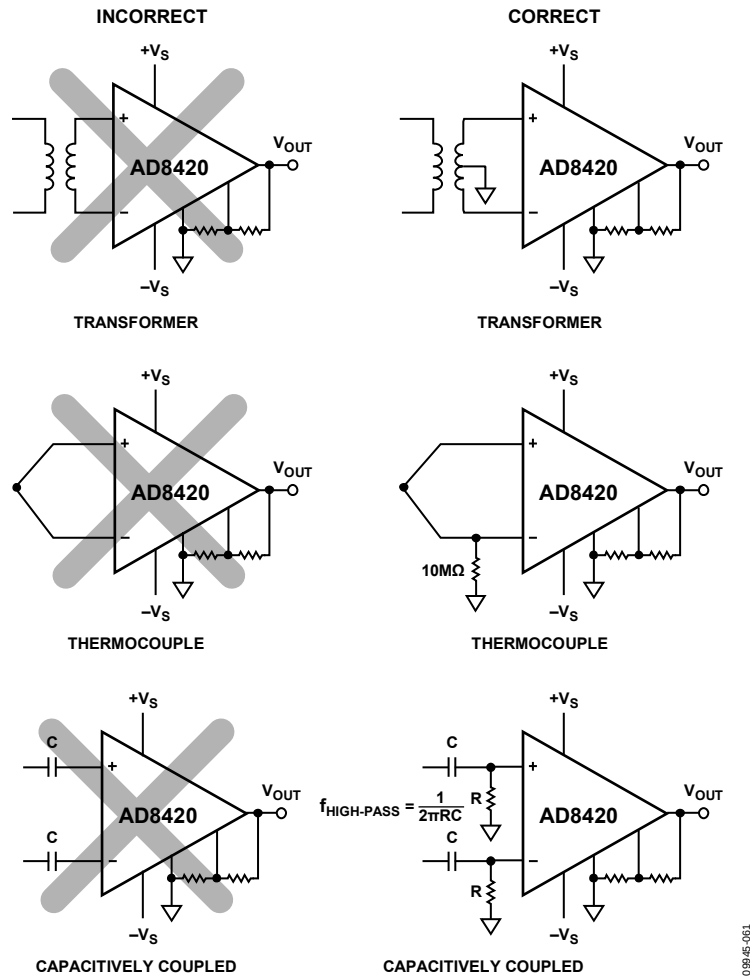


Figure 64. Using Resistor Divider to Set Reference Voltage

Figure 65. Creating an I_{BIAS} Path

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8420 must have a return path to ground. When the source, such as a thermocouple, cannot provide a return current path, create one, as shown in Figure 65.

RADIO FREQUENCY INTERFERENCE (RFI)

All instrumentation amplifiers can rectify high frequency out-of-band signals. Once rectified, these signals appear as dc offset errors at the output. High frequency signals can be filtered with a low-pass RC network placed at the input of the instrumentation amplifier, as shown in Figure 66. The filter limits the input signal bandwidth according to the following relationship:

$$FilterFrequency_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFrequency_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10 C_C$.

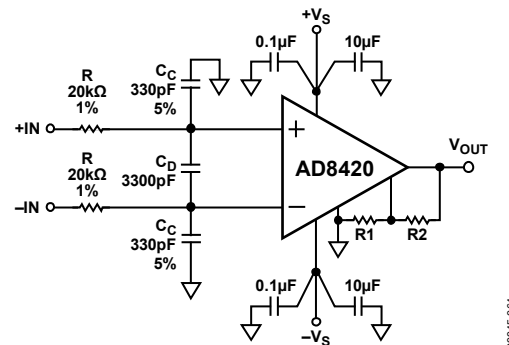


Figure 66. Suggested RFI Suppression Filter

C_D affects the differential signal and C_C affects the common-mode signal. Values of R and C_C are chosen to minimize out of band RFI at the expense of reduced signal bandwidth. Mismatch between the $R \times C_C$ at the positive input and the $R \times C_C$ at the negative input degrades the CMRR of the AD8420. By using a value of C_D that is at least one magnitude larger than C_C , the effect of the mismatch is reduced and performance is improved.

OUTPUT BUFFERING

The AD8420 is designed to drive loads of 20 k Ω or greater but can deliver up to 10 mA to heavier loads at lower output voltage swings (see Figure 42). If more output current is required, buffer the AD8420 output with a precision op amp. Figure 67 shows the recommended configuration using the ADA4692-2 as a single supply. This low power op amp can swing its output from 1 V to 4 V on a single 5 V supply while sourcing or sinking more than 30 mA of current. When using this configuration, the load seen by the AD8420 is approximately $R1 + R2$.

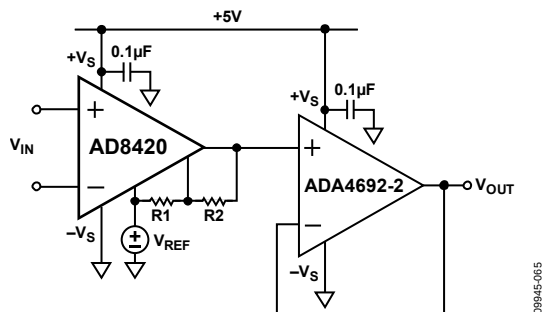
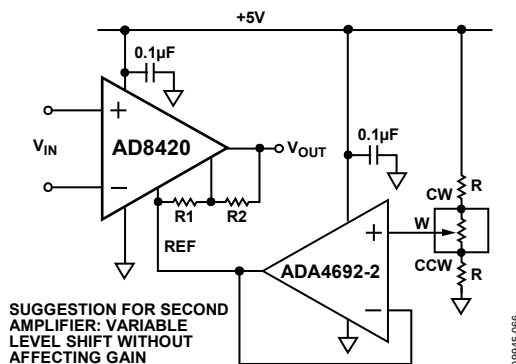


Figure 67. Output Buffering

09945-065

Because the ADA4692-2 is a dual op amp, another op amp is now free for use as an active filter stage or to buffer another AD8420 output on the same PCB. Figure 68 shows another suggestion for how to use this second op amp. In this circuit, the voltage from the wiper of a potentiometer is buffered by the ADA4692-2, allowing a variable level shift of the output. Resistors above and below the potentiometer reduce the total range of the level shift but increase the precision. If the potentiometer were connected directly to the REF pin of the AD8420, gain error would be introduced from the variable resistance. The potentiometer can be tuned in hardware or software, depending on the type of potentiometer chosen. For a list of digital potentiometers made by Analog Devices, Inc., visit www.analog.com/digipots/.



SUGGESTION FOR SECOND
AMPLIFIER: VARIABLE
LEVEL SHIFT WITHOUT
AFFECTING GAIN

Figure 68. Variable Level Shift

09945-066

AD8420 IN ELECTROCARDIOGRAPHY (ECG)

With a 3-op-amp instrumentation amplifier, gain is applied in the first stage. Because of this, the electrode offset is gained and then must be removed afterward with a high-pass filter. In the [AD8420](#)

architecture, the offset can be accounted for in the input stage by unbalancing the transconductance amplifier at the REF and FB pins. In the steady state, the offset at the input is not gained to the output, and higher frequency signals can be gained and passed through. Using the [AD8420](#) in this way, the offset tolerance is nearly the differential input range of the part (± 1 V).

Figure 69 shows an ECG front end that applies a gain of 100 to the signal while rejecting dc and high frequencies. This circuit combines the [AD8420](#) with the [AD8657](#), which is a low power, low cost, dual, precision CMOS op amp.

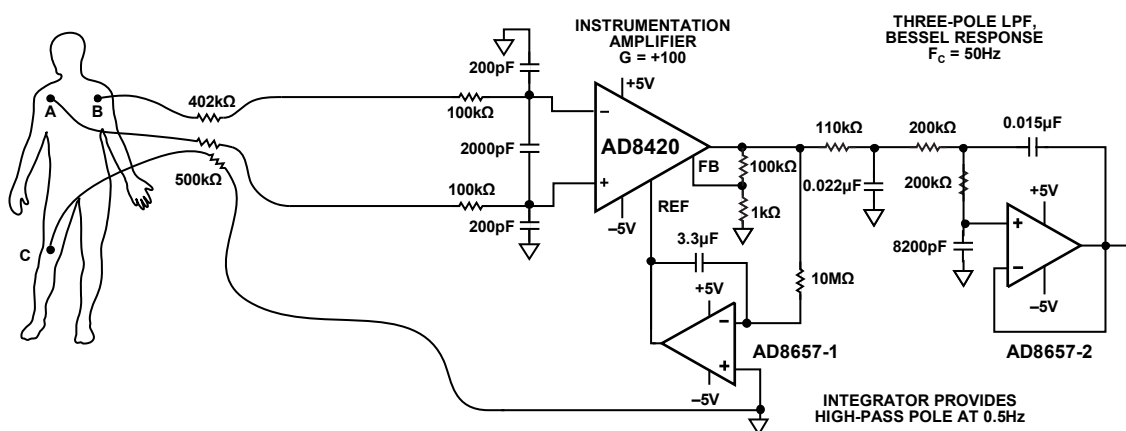


Figure 69. **AD8420** in an ECG Front End

CLASSIC BRIDGE CIRCUIT

Figure 70 shows the AD8420 configured to amplify the signal from a classic resistive bridge. This circuit works in dual-supply mode or single-supply mode. Typically, the same voltage that powers the instrumentation amplifier excites the bridge. Connecting the bottom of the bridge to the negative supply of the instrumentation amplifier sets up an input common-mode voltage that is located midway between the supply voltages. The voltage on the REF pin can be varied to suit the application. For example, the REF pin is tied to the V_{REF} pin of an analog-to-digital converter (ADC) whose input range is $(V_{REF} \pm V_{IN})$. With an available output swing on the AD8420 of $(-V_S + 100 \text{ mV})$ to $(+V_S - 150 \text{ mV})$, the maximum programmable gain is simply this output range divided by the input range.

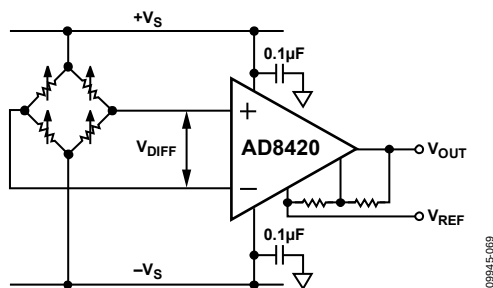


Figure 70. Classic Bridge Circuit

4 mA TO 20 mA SINGLE-SUPPLY RECEIVER

The 80 μA maximum supply current, input range that goes below ground, and low drift characteristics make the AD8420 a very good candidate for use in a 4 mA to 20 mA loop. Figure 71 shows how a signal from a 4 mA to 20 mA transducer can be interfaced to the AD8420. The signal from a 4 mA to 20 mA transducer is single-ended, which initially suggests the need for a simple shunt resistor to ground to convert the current to a voltage. However, any line resistance in the return path (to the transducer) adds a current-dependent offset error; therefore, the current must be sensed differentially.

In this example, a 5 Ω shunt resistor generates a differential voltage at the inputs of the AD8420 between 20 mV (for 4 mA in) and 100 mV (for 20 mA in) with a very low common-mode value. With the gain resistors shown, the AD8420 amplifies the 100 mV input voltage by a factor of 40 to 4.0 V.

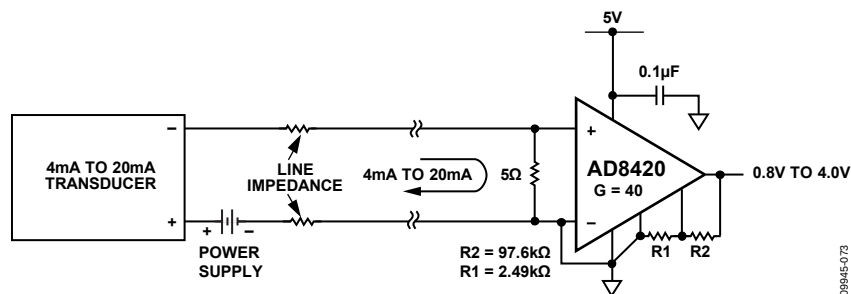
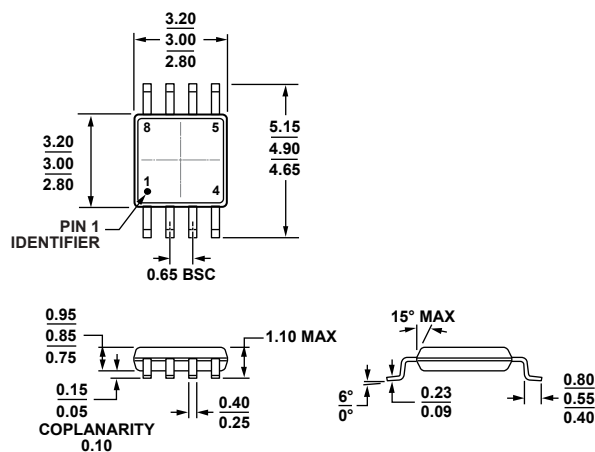


Figure 71. 4 mA to 20 mA Receiver Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 72. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
AD8420ARMZ	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP], Tube	RM-8	Y3Y
AD8420ARMZ-R7	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP], 7-Inch Tape and Reel	RM-8	Y3Y
AD8420ARMZ-RL	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP], 13-Inch Tape and Reel	RM-8	Y3Y

¹ Z = RoHS Compliant Part.

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