100mA CMOS Voltage Converter

FEATURES

- **Simple Conversion of 5V to –5V Supply**
- **Output Drive: 100mA**
- **R_{OUT}: 6.5Ω (0.65V Loss at 100mA)**
- BOOST Pin (Pin 1) for Higher Switching Frequency
- Inverting and Doubling Modes
- Minimum Open Circuit Voltage Conversion Efficiency: 99%
- Typical Power Conversion Efficiency with a 100mA Load: 88%
- Easy to Use

APPLICATIONS

- Conversion of 5V to ±5V Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems
- High Current Upgrade to LTC1044 or LTC7660

DESCRIPTION

The LTC®660 is a monolithic CMOS switched-capacitor voltage converter. It performs supply voltage conversion from positive to negative from an input range of 1.5V to 5.5V, resulting in complementary output voltages of –1.5V to –5.5V. It also performs a doubling at an input voltage range of 2.5V to 5.5V, resulting in a doubled output voltage of 5V to 11V. Only two external capacitors are needed for the charge pump and charge reservoir functions.

The converter has an internal oscillator that can be overdriven by an external clock or slowed down when connected to a capacitor. The oscillator runs at a 10kHz frequency when unloaded. A higher frequency outside the audio band can also be obtained if the BOOST pin is tied to V^+.

The LTC660 contains an internal oscillator, divide-by-two, voltage level shifter and four power MOSFETs.

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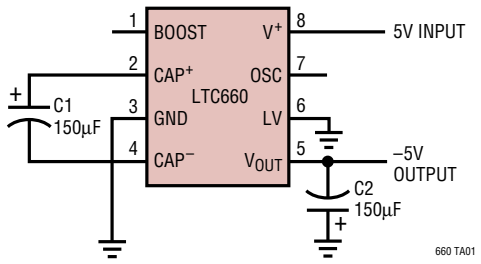
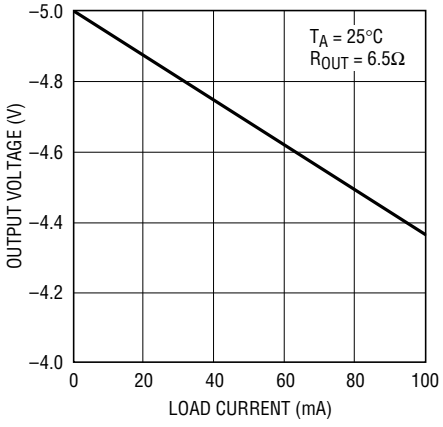
TYPICAL APPLICATION

Generating –5V from 5V



Output Voltage vs Load Current for V^+ = 5V

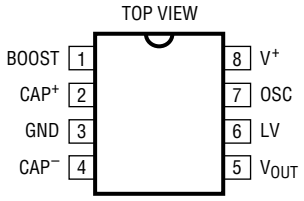


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+) 6V
Input Voltage on Pins 1, 6, 7
(Note 2) ..... $-0.3V < V_{IN} < (V^+ + 0.3V)$
Output Short-Circuit Duration to GND
(Note 5) ..... 1 sec
Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 100°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 100°C, θ_{JA} = 150°C/W (S)

ORDER PART NUMBER
LTC660CN8 LTC660CS8
S8 PART MARKING
660

Consult Factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V^+ = 5V, C1 and C2 = 150µF, Boost = Open, C_{OSC} = 0pF, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Supply Voltage	R_L = 1k Inverter, LV = Open Inverter, LV = GND Doubler, LV = V_{OUT}	● ● ●	3 1.5 2.5		5.5 5.5 5.5	V V V
I_S	Supply Current	No Load Boost = Open Boost = V^+	● ●		0.08 0.23	0.5 3	mA mA
I_{OUT}	Output Current	V_{OUT} More Negative Than –4V	●	100			mA
R_{OUT}	Output Resistance	I_L = 100mA (Note 3)	●		6.5	10	Ω
f_{OSC}	Oscillator Frequency	Boost = Open Boost = V^+ (Note 4)			10 80		kHz kHz
	Power Efficiency	R_L = 1k Connected Between V^+ and V_{OUT} R_L = 500Ω Connected Between V_{OUT} and GND I_L = 100mA to GND	● ●	96 92	98 96 88		% % %
	Voltage Conversion Efficiency	No Load		99	99.96		%
	Oscillator Sink or Source Current	Boost = Open Boost = V^+			±1.1 ±5.0		µA µA

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals are at T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Connecting any input terminal to voltages greater than V^+ or less than ground may cause destructive latch-up. It is recommended that no inputs from source operating from external supplies be applied prior to power-up of the LTC660.

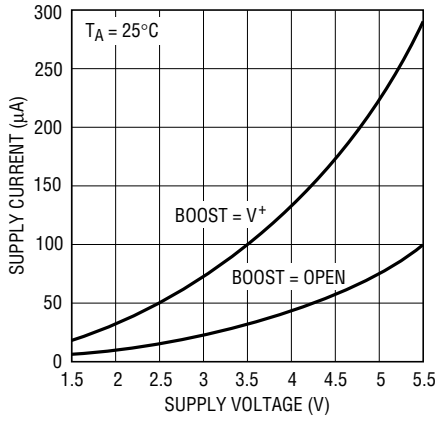
Note 3: The output resistance is a combination of internal switch resistance and external capacitor ESR. To maximize output voltage and efficiency, keep external capacitor ESR < 0.2Ω.

Note 4: f_{OSC} is tested with C_{OSC} = 100pF to minimize the effects of test fixture capacitance loading. The 0pF frequency is correlated to this 100pF test point, and is intended to simulate the capacitance at Pin 7 when the device is plugged into a test socket and no external capacitor is used.

Note 5: OUT may be shorted to GND for 1 sec without damage, but shorting OUT to V^+ may damage the device and should be avoided. Also, for temperatures above 85°C, OUT must not be shorted to GND or V^+, even instantaneously, or device damage may result.

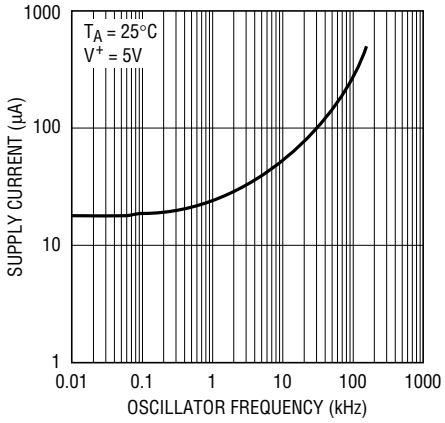
TYPICAL PERFORMANCE CHARACTERISTICS (Using Test Circuit in Figure 1)

Supply Current vs Supply Voltage



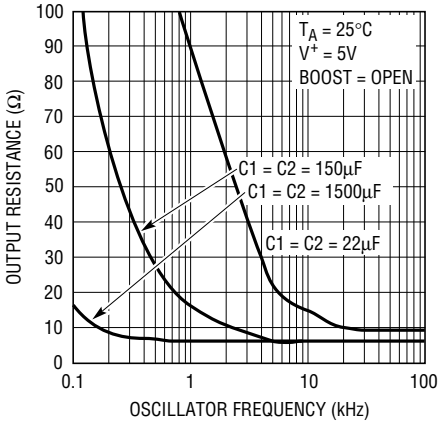
LTC660 • G01

Supply Current vs Oscillator Frequency



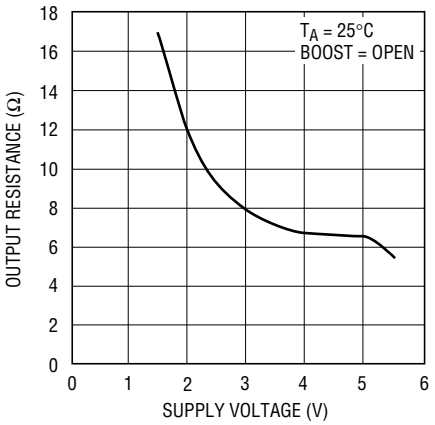
LTC660 • G02

Output Resistance vs Oscillator Frequency



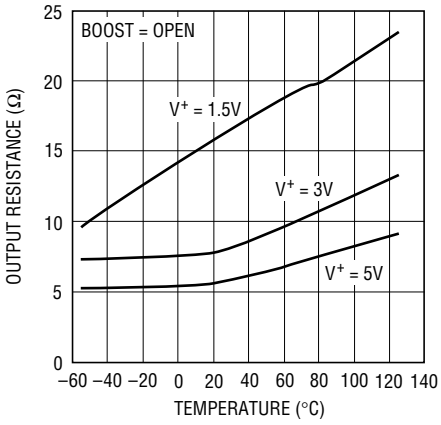
LTC660 • TPC03

Output Resistance vs Supply Voltage



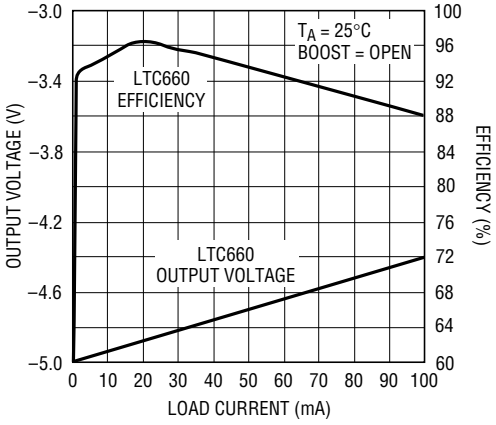
LTC690 • TPC04

Output Resistance vs Temperature



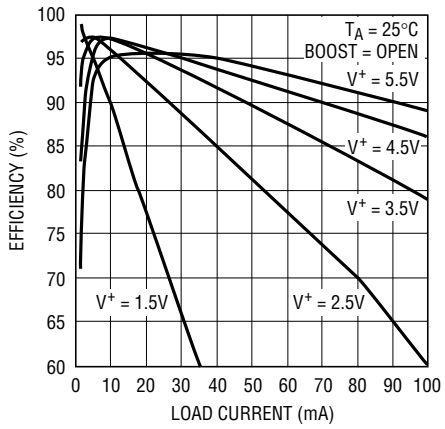
LTC660 • TPC05

Output Voltage and Efficiency vs Load Current, V^+ = 5V



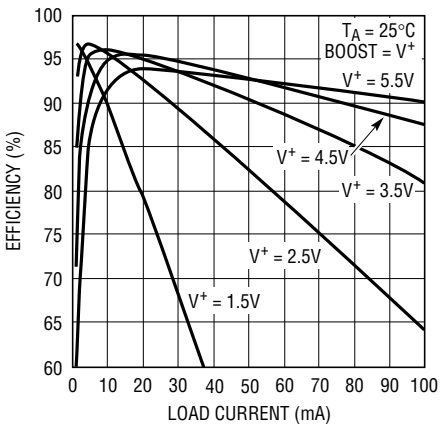
LTC660 • TPC06

Efficiency vs Load Current



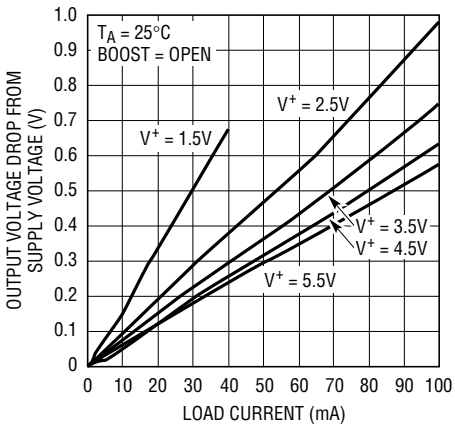
LTC660 • TPC07

Efficiency vs Load Current



LTC660 • TPC08

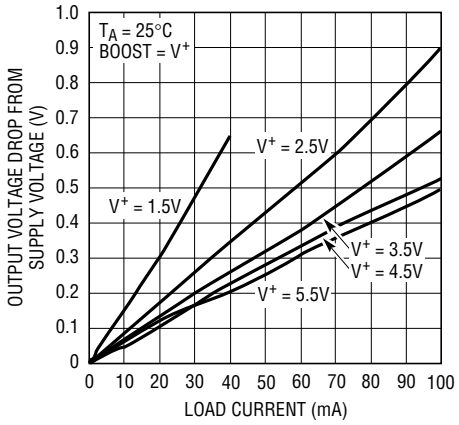
Output Voltage Drop vs Load Current



LTC660 • TPC09

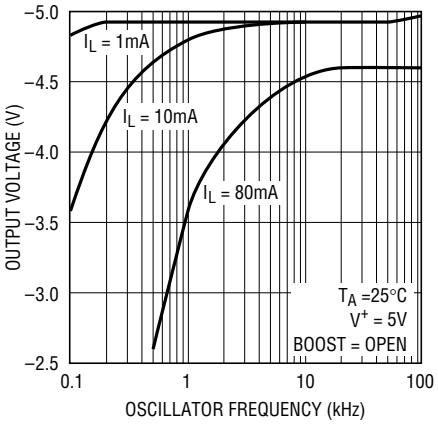
TYPICAL PERFORMANCE CHARACTERISTICS (Using Test Circuit in Figure 1)

Output Voltage Drop vs Load Current



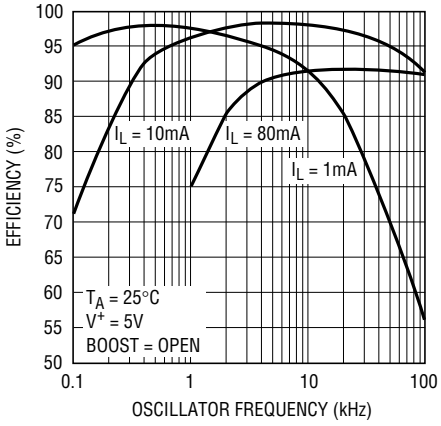
LTC660 • TPC10

Output Voltage vs Oscillator Frequency



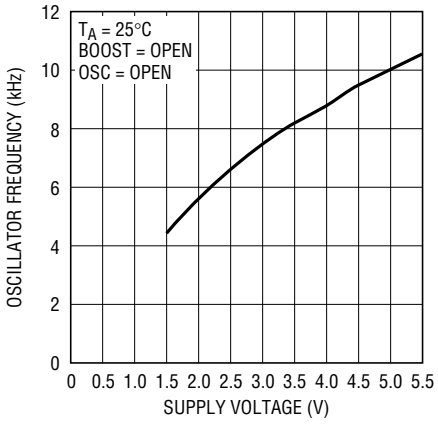
LTC660 • TPC11

Efficiency vs Oscillator Frequency



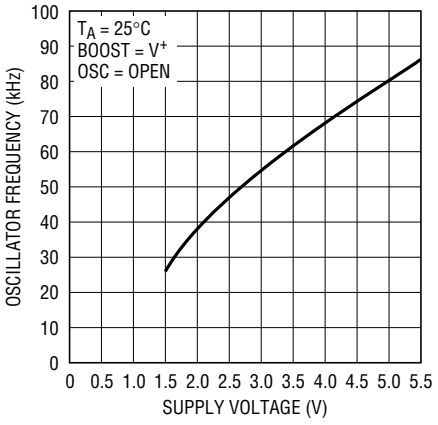
LTC660 • TPC12

Oscillator Frequency vs Supply Voltage



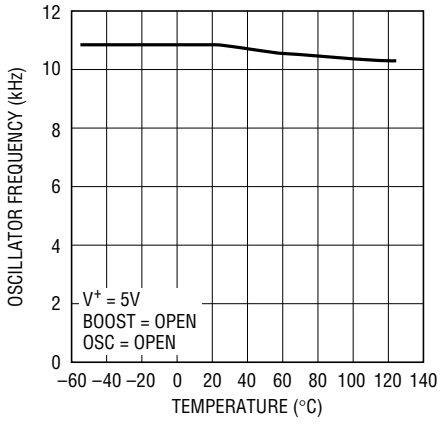
LTC660 • TPC13

Oscillator Frequency vs Supply Voltage



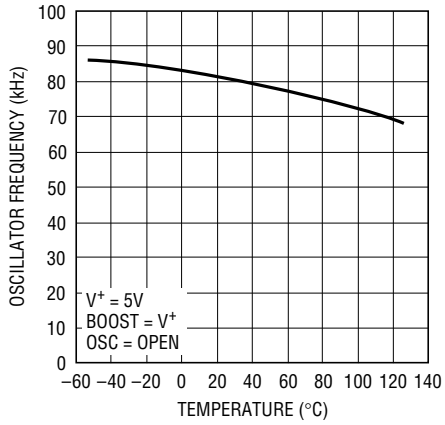
LTC660 • TPC14

Oscillator Frequency vs Temperature



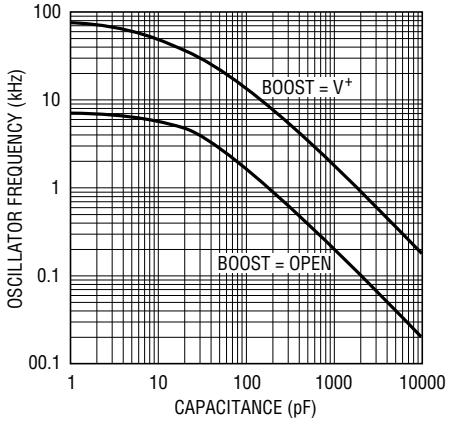
LTC660 • TPC15

Oscillator Frequency vs Temperature



LTC660 • TPC16

Oscillator Frequency vs External Capacitance



LTC660 • TPC17

PIN FUNCTIONS

PIN	NAME	INVERTER	DOUBLER
1	BOOST	Internal Oscillator Frequency Control Pin. BOOST = Open, f_{OSC} = 10kHz typ; BOOST = V^+, f_{OSC} = 80kHz typ; when OSC is driven externally BOOST has no effect.	Same
2	CAP^+	Positive Terminal for Charge Pump Capacitor	Same
3	GND	Power Supply Ground Input	Positive Voltage Input
4	CAP^-	Negative Terminal for Charge Pump Capacitor	Same
5	V_{OUT}	Negative Voltage Output	Power Supply Ground Input
6	LV	Tie LV to GND when the input voltage is less than 3V. LV may be connected to GND or left open for input voltages above 3V. Connect LV to GND when overdriving OSC.	LV must be tied to V_{OUT} for all input voltages.
7	OSC	An external capacitor can be connected to this pin to slow the oscillator frequency. Keep stray capacitance to a minimum. An external oscillator can be applied to this pin to overdrive the internal oscillator.	Same except standard logic levels will not be able to overdrive OSC pin.
8	V^+	Positive Voltage Input	Positive Voltage Output

TEST CIRCUIT

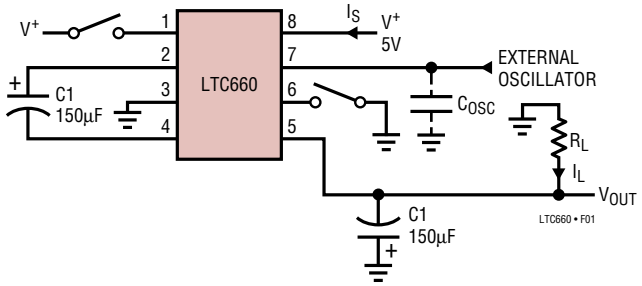


Figure 1. Test Circuit

APPLICATIONS INFORMATION

Theory of Operation

To understand the theory of operation for the LTC660, a review of a basic switched-capacitor building block is helpful. In Figure 2, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be q1 = C1V1. The switch then moves to the right, discharging C1 to voltage V2. After this discharging time, the charge on C1 is q2 = C1V2. Note that charge has been transferred from the source V1 to the output V2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C1\ (V1 - V2)$$

If the switch is cycled "f" times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \bullet \Delta q = f \bullet C1\ (V1 - V2)$$

Rewriting in terms of voltage and impedance equivalence,

$$I = \frac{V1 - V2}{1/fC1} = \frac{V1 - V2}{R_{EQUIV}}$$

A new variable R_{EQUIV} has been defined such that $R_{EQUIV} = 1/fC1$. Thus, the equivalent circuit for the switched-capacitor network is as shown in Figure 3.

Figure 4 shows that the LTC660 has the same switching action as the basic switched-capacitor building block.

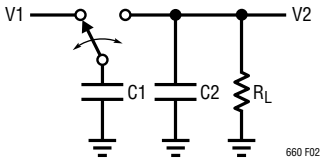


Figure 2. Switched-Capacitor Building Block

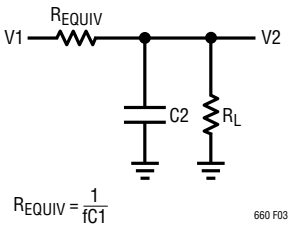


Figure 3. Switched-Capacitor Equivalent Circuit

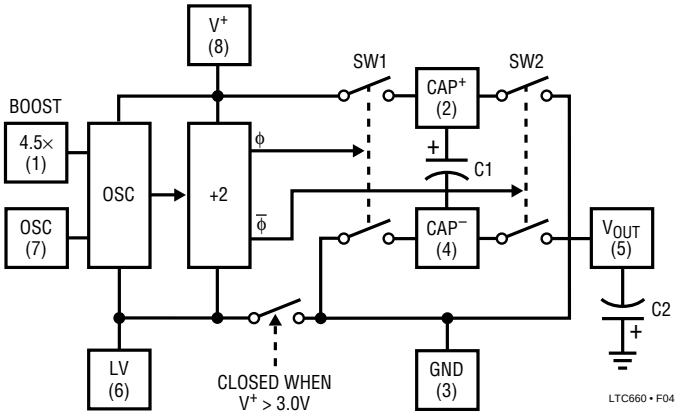


Figure 4. LTC660 Switched-Capacitor Voltage Converter Block Diagram

This simplified circuit does not include finite on-resistance of the switches and output voltage ripple, however, it does give an intuitive feel for how the device works. For example, if you examine power conversion efficiency as a function of frequency this simple theory will explain how the LTC660 behaves. The loss and hence the efficiency is set by the output impedance. As frequency is decreased, the output impedance will eventually be dominated by the 1/fC1 term and voltage losses will rise decreasing the efficiency. As the frequency increases the quiescent current increases. At high frequency this current loss becomes significant and the power efficiency starts to decrease.

The LTC660 oscillator frequency is designed to run where the voltage loss is a minimum. With the external 150µF capacitors the effective output impedance is determined by the internal switch resistances and the capacitor ESRs.

LV (Pin 6)

The internal logic of the LTC660 runs between V^+ and LV (Pin 6). For $V^+ \geq 3V$, an internal switch shorts LV to ground (Pin 3). For $V^+ < 3V$, the LV pin should be tied to ground. For $V^+ \geq 3V$, the LV pin can be tied to ground or left floating.

OSC (Pin 7) and BOOST (Pin 1)

The switching frequency can be raised, lowered or driven from an external source. Figure 5 shows a functional diagram of the oscillator circuit.

APPLICATIONS INFORMATION

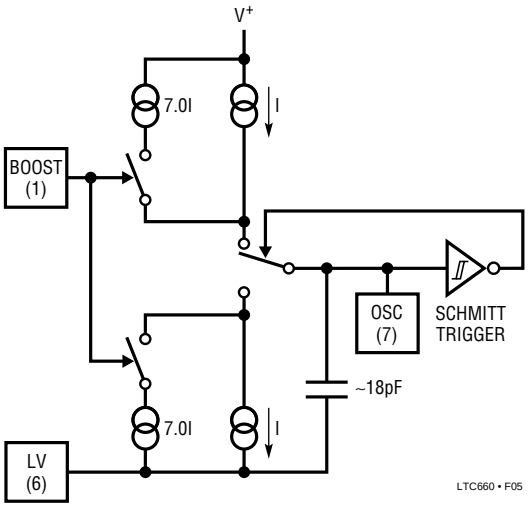


Figure 5. Oscillator

By connecting the BOOST pin (Pin 1) to V+, the charge and discharge current is increased and, hence, the frequency is increased by approximately four and a half times. Increasing the frequency will decrease output impedance and ripple for high load currents.

Loading Pin 7 with more capacitance will lower the frequency. Using the BOOST (Pin 1) in conjunction with external capacitance on Pin 7 allows user selection of the frequency over a wide range.

Driving the LTC660 from an external frequency source can be easily achieved by driving Pin 7 and leaving the BOOST pin open, as shown in Figure 6. The output current from Pin 7 is small, typically 1.1μA to 8μA, so a logic gate is capable of driving this current. (A CMOS logic gate can be used to drive the OSC pin.) For 5V applications, a TTL logic gate can be used by simply adding an external pull-up resistor (see Figure 6).

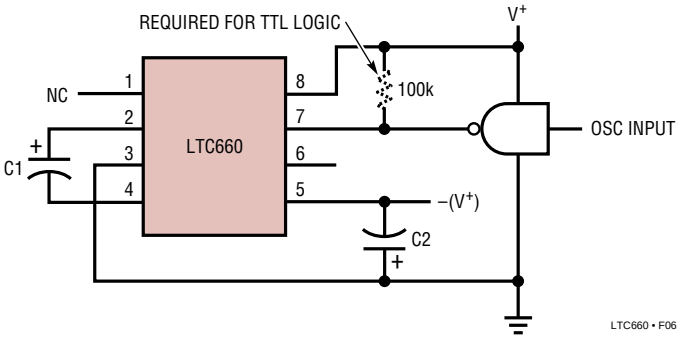


Figure 6. External Clocking

Capacitor Selection

While the exact values of C1 and C2 are noncritical, good quality, low ESR capacitors are necessary to minimize voltage losses at high currents. For C1 the effect of the ESR of the capacitor will be multiplied by four, due to the fact the switch currents are approximately two times higher than the output current and losses will occur on both the charge and discharge cycle. This means using a capacitor with 1Ω of ESR for C1 will have the same effect as increasing the output impedance of the LTC660 by 4Ω. This represents a significant increase in the voltage losses. For C2 the effect of ESR is less dramatic. A C2 with 1Ω of ESR will increase the output impedance by 1Ω. The size of C2 and the load current will determine the output voltage ripple. It is alternately charged and discharged at a current approximately equal to the output current. This will cause a step function to occur in the output voltage at the switch transitions. For example, for a switching frequency of 5kHz (one-half the nominal 10kHz oscillator frequency) and C2 = 150μF with an ESR of 0.2Ω, ripple is approximately 90mV with a 100mA load current.

TYPICAL APPLICATIONS

Negative Voltage Converter

Figure 7 shows a typical connection which will provide a negative supply from an available positive supply. This circuit operates over full temperature and power supply ranges without the need of any external diodes. The LV pin (Pin 6) is shown grounded, but for $V^+ \geq 3V$, it may be floated, since LV is internally switched to ground (Pin 3) for $V^+ \geq 3V$.

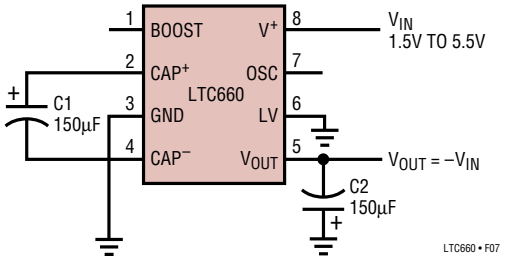


Figure 7. Voltage Inverter

The output voltage (Pin 5) characteristics of the circuit are those of a nearly ideal voltage source in series with a 6.5Ω resistor. The 6.5Ω output impedance is composed of two terms: 1) the equivalent switched-capacitor resistance (see Theory of Operation), and 2) a term related to the on-resistance of the MOS switches.

At an oscillator frequency of 10kHz and C1 = 150µF, the first term is:

$$R_{EQUIV} = \frac{1}{(f_{OSC}/2)C1} =$$

$$\frac{1}{5 \bullet 10^3 \bullet 150 \bullet 10^{-6}} = 1.3\Omega.$$

Notice that the equation for R_{EQUIV} is not a capacitive reactance equation ($X_C = 1/\omega C$) and does not contain a 2π term.

The exact expression for output impedance is complex, but the dominant effect of the capacitor is clearly shown on the typical curves of output impedance and power efficiency versus frequency. For C1 = C2 = 150µF, the output impedance goes from 6.5Ω at f_{OSC} = 10kHz to 110Ω at f_{OSC} = 100Hz. As the 1/fC term becomes large compared to the switch on-resistance term, the output resistance is determined by 1/fC only.

Voltage Doubling

Figure 8 shows the LTC660 operating in the voltage doubling mode. The external Schottky (1N5817) diode is for start-up only. The output voltage is $2 \bullet V_{IN}$ without a load. The diode has no effect on the output voltage.

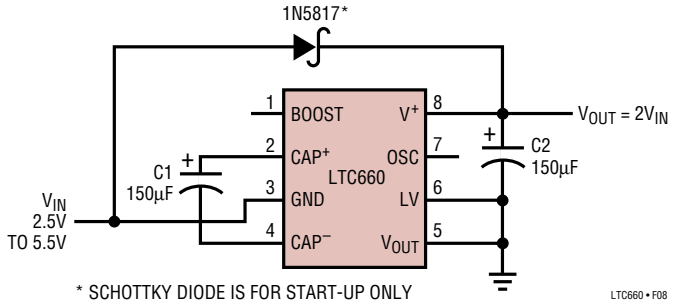


Figure 8. Voltage Doubler

Ultraprecision Voltage Divider

An ultraprecision voltage divider is shown in Figure 9. To achieve the 0.002% accuracy indicated, the load current should be kept below 100nA. However, with a slight loss in accuracy, the load current can be increased.

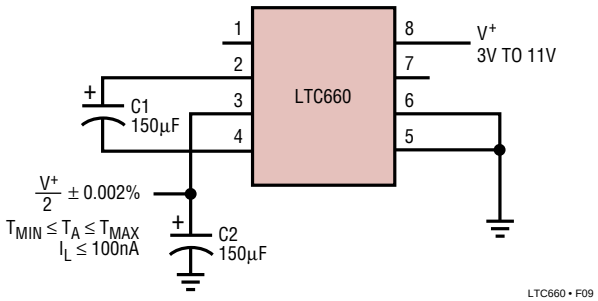


Figure 9. Ultraprecision Voltage Divider

Battery Splitter

A common need in many systems is to obtain positive and negative supplies from a single battery or single power supply system. Where current requirements are small, the circuit shown in Figure 10 is a simple solution. It provides symmetrical positive or negative output voltages, both equal to one-half the input voltage. The output voltages are both referenced to Pin 3 (Output Common).

TYPICAL APPLICATIONS

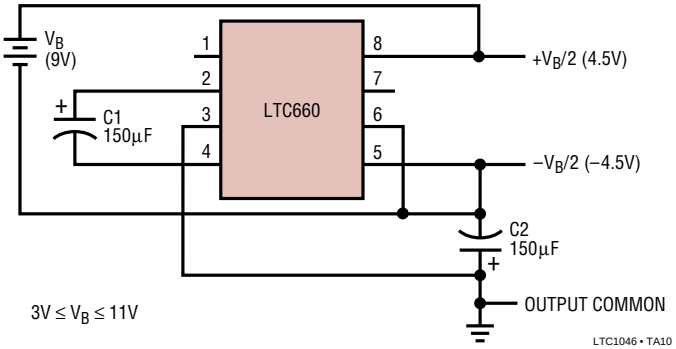


Figure 10. Battery Splitter

Paralleling for Lower Output Resistance

Additional flexibility of the LTC660 is shown in Figures 11 and 12. Figure 11 shows two LTC660s connected in parallel to provide a lower effective output resistance. If, however, the output resistance is dominated by 1/fC1, increasing the capacitor size (C1) or increasing the frequency will be of more benefit than the paralleling circuit shown.

Stacking for Higher Voltage

Figure 12 makes use of "stacking" two LTC660s to provide even higher voltages. In Figure 12, a negative voltage doubler or tripler can be achieved depending upon how Pin 8 of the second LTC660 is connected, as shown schematically by the switch.

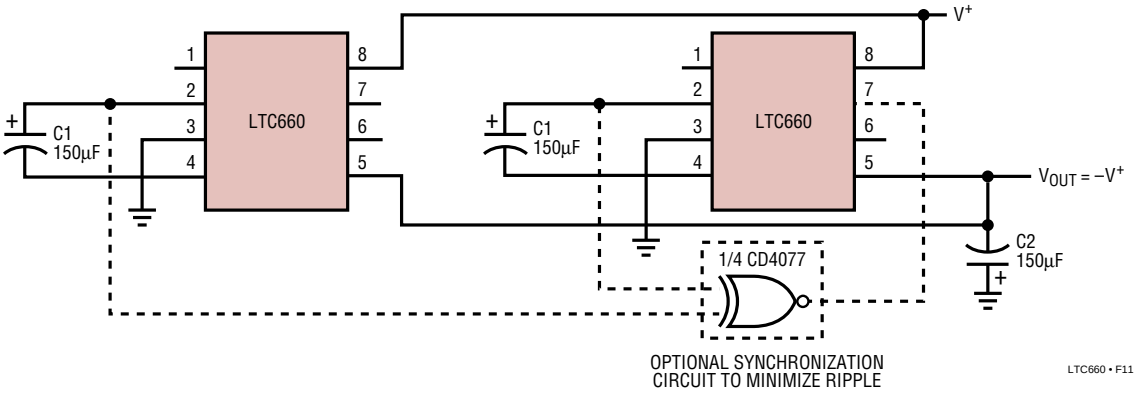


Figure 11. Paralleling for 200mA Load Current

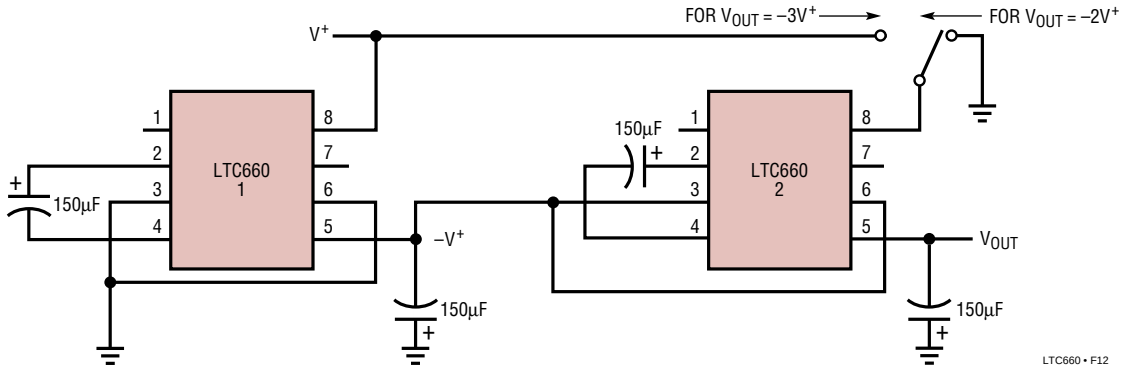
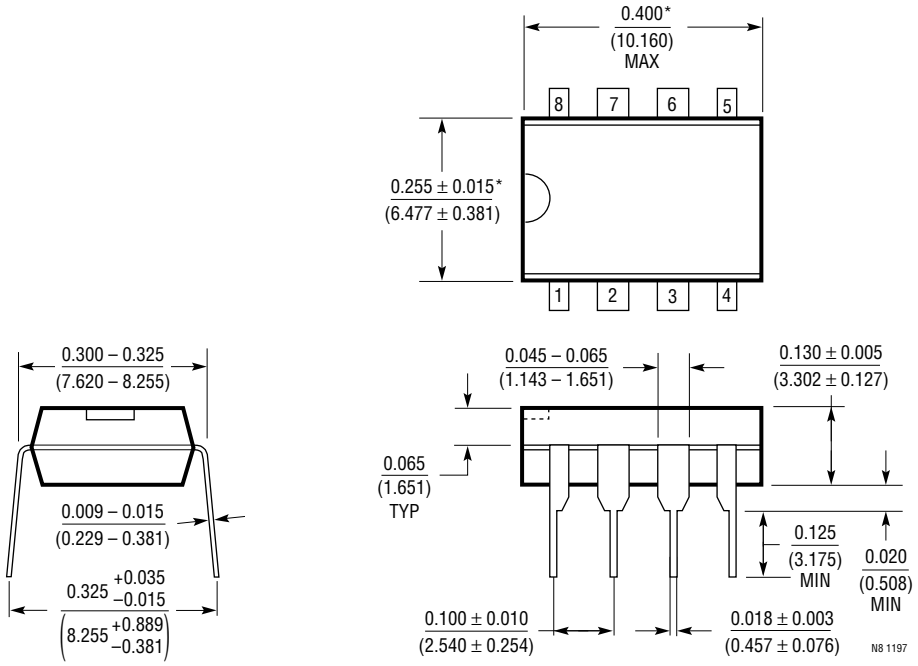


Figure 12. Stacking for High Voltage

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

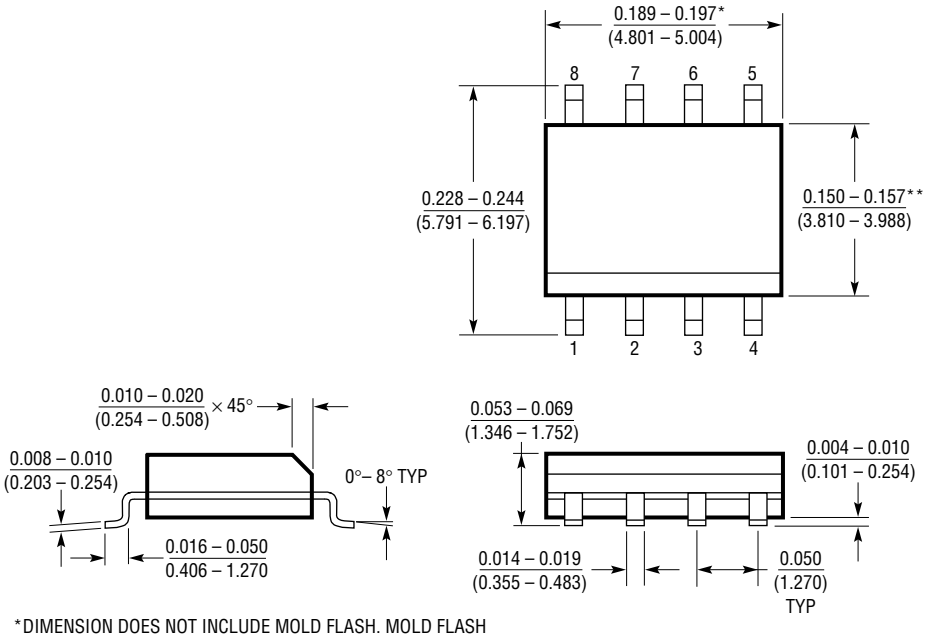


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

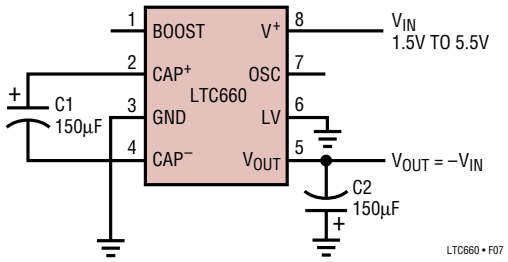
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 0996

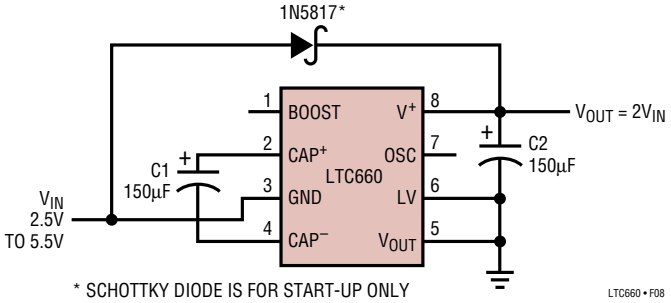
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATIONS

Voltage Inverter



Voltage Doubler



RELATED PARTS

PART NUMBER	OUTPUT CURRENT	MAXIMUM V_{IN}	COMMENTS
Unregulated Output Voltage			
LTC660	100mA	6V	Highest Current
LTC1046	50mA	6V	
LTC1044	20mA	9.5V	Lowest Cost
LTC1044A	20mA	13V	
LTC1144	20mA	20V	Highest Voltage
Regulated Output Voltage			
LT1054	100mA	16V	Adjustable Output
LTC1262	30mA	6V	12V Fixed Output
LTC1261	10mA	9V	–4V, –4.5V and Adjustable Outputs

All devices are available in plastic 8-lead SO and PDIP packages

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