

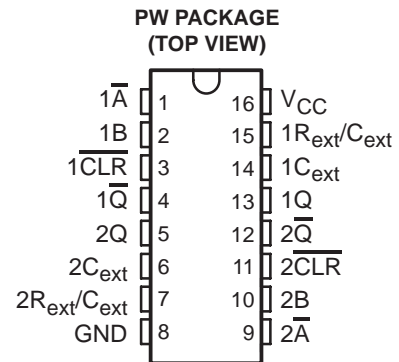
SN74LV123A-EP

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS

SCLS498A – MAY 2003 – REVISED MAY 2004

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –40°C to 105°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Supports Mixed-Mode Voltage Operation on All Ports**
- **Schmitt-Trigger Circuitry on \overline{A} , B, and \overline{CLR} Inputs for Slow Input Transition Rates**
- **Edge Triggered From Active-High or Active-Low Gated Logic Inputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Retriggerable for Very Long Output Pulses, Up To 100% Duty Cycle**
- **Overriding Clear Terminates Output Pulse**
- **Glitch-Free Power-Up Reset on Outputs**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



description/ordering information

The SN74LV123A is a dual retriggerable monostable multivibrator designed for 2-V to 5.5-V V_{CC} operation.

This edge-triggered multivibrator features output pulse-duration control by three methods. In the first method, the \overline{A} input is low, and the B input goes high. In the second method, the B input is high, and the \overline{A} input goes low. In the third method, the \overline{A} input is low, the B input is high, and the clear (\overline{CLR}) input goes high.

The output pulse duration is programmable by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC} . To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC} . The output pulse duration also can be reduced by taking \overline{CLR} low.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The \overline{A} , B, and \overline{CLR} inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	TSSOP – PW	Tape and reel	SN74LV123ATPWREP	L123AEP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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description/ordering information (continued)

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active (\bar{A}) or high-level-active (B) input. Pulse duration can be reduced by taking $\overline{\text{CLR}}$ low. The input/output timing diagram illustrates pulse control by retriggering the inputs and early clearing.

During power up, Q outputs are in the low state, and \bar{Q} outputs are in the high state. The outputs are glitch free, without applying a reset pulse.

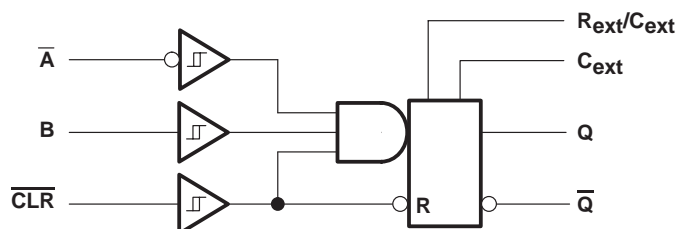
This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE
(each multivibrator)

INPUTS			OUTPUTS	
$\overline{\text{CLR}}$	\bar{A}	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	↑	⌋	⌋
H	↓	H	⌋	⌋
↑	L	H	⌋	⌋

† These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

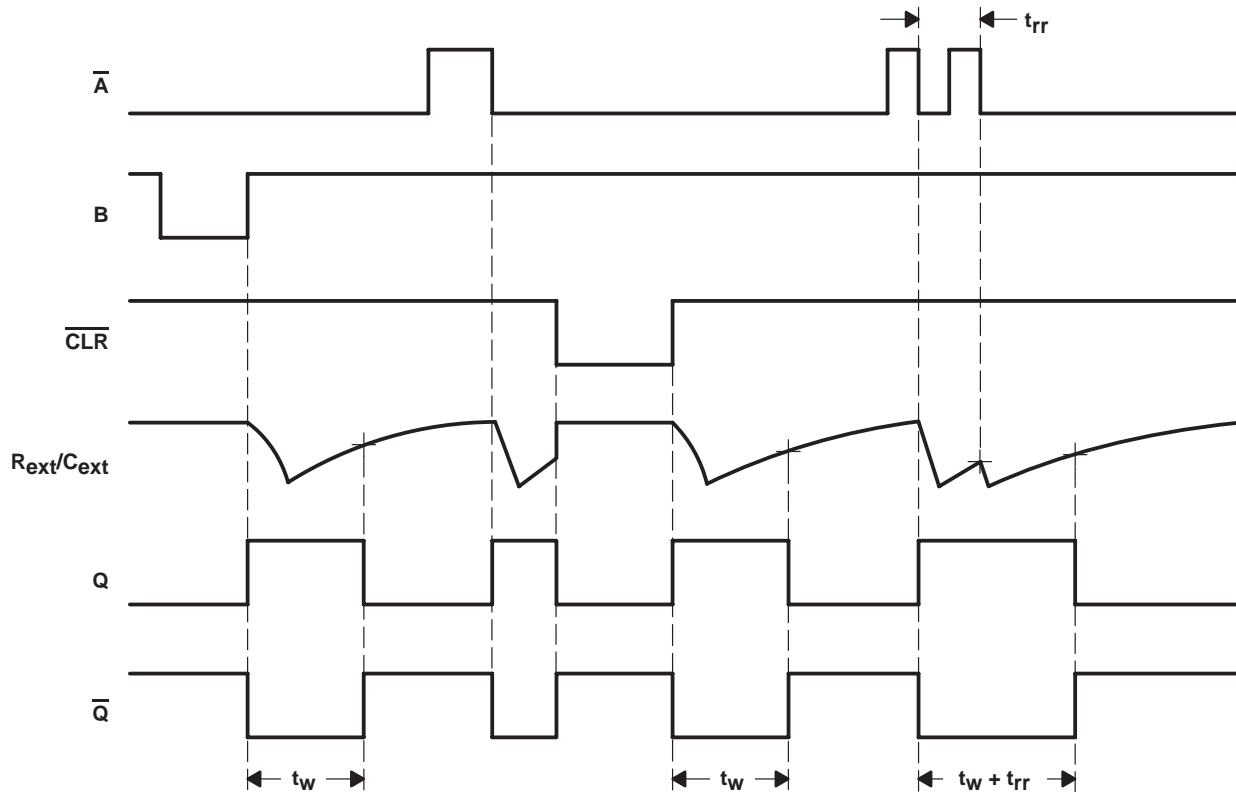
logic diagram, each multivibrator (positive logic)



SN74LV123A-EP DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS

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input/output timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Output voltage range in high or low state, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range in power-off state, V_O (see Note 1)	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 3)	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$	
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.3$	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.3$	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.3$	
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$	-50	μA
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-2	mA
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	-6	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-12	
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$	50	μA
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2	mA
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	6	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	12	
R_{ext}	External timing resistance	$V_{CC} = 2\text{ V}$	5k	Ω
		$V_{CC} \geq 3\text{ V}$	1k	
C_{ext}	External timing capacitance	No restriction		pF
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	1		ms/V
T_A	Operating free-air temperature	-40	105	$^{\circ}\text{C}$

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}		I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V
		I _{OH} = -2 mA	2.3 V	2			
		I _{OH} = -6 mA	3 V	2.48			
		I _{OH} = -12 mA	4.5 V	3.8			
V _{OL}		I _{OL} = 50 μA	2 V to 5.5 V			0.1	V
		I _{OL} = 2 mA	2.3 V			0.4	
		I _{OL} = 6 mA	3 V			0.44	
		I _{OL} = 12 mA	4.5 V			0.55	
I _I	R _{ext} /C _{ext} [†]	V _I = 5.5 V or GND	2 V to 5.5 V			±2.5	μA
	\overline{A} , B, and \overline{CLR}	V _I = 5.5 V or GND	0			±1	
I _{CC}	Quiescent	V _I = V _{CC} or GND, I _O = 0	5.5 V			20	μA
I _{CC}	Active state (per circuit)	V _I = V _{CC} or GND, R _{ext} /C _{ext} = 0.5 V _{CC}	3 V			280	μA
			4.5 V			650	
			5.5 V			975	
I _{off}		V _I or V _O = 0 to 5.5 V	0			5	μA
C _i		V _I = V _{CC} or GND	3.3 V			1.9	pF
			5 V			1.9	

[†] This test is performed with the terminal in the off-state condition.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		TEST CONDITIONS		T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _w	Pulse duration	\overline{CLR}		5			5		ns
		\overline{A} or B trigger		5			5		
t _{rr}	Pulse retrigger time	R _{ext} = 1 kΩ	C _{ext} = 100 pF	‡	76		‡		ns
			C _{ext} = 0.01 μF	‡	1.8		‡		μs

[‡] See retriggering data in the *application information* section.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		TEST CONDITIONS		T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _w	Pulse duration	\overline{CLR}		5			5		ns
		\overline{A} or B trigger		5			5		
t _{rr}	Pulse retrigger time	R _{ext} = 1 kΩ	C _{ext} = 100 pF	‡	59		‡		ns
			C _{ext} = 0.01 μF	‡	1.5		‡		μs

[‡] See retriggering data in the *application information* section.



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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	\bar{A} or B	Q or \bar{Q}	$C_L = 50\text{ pF}$	11.8	24.1		1	27.5	ns
	$\overline{\text{CLR}}$	Q or \bar{Q}		10.5	19.3		1	22	
	$\overline{\text{CLR}}$ trigger	Q or \bar{Q}		12.3	25.9		1	29.5	
t_w^\dagger		Q or \bar{Q}	$C_L = 50\text{ pF}$, $C_{ext} = 28\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$	182	240			300	ns
			$C_L = 50\text{ pF}$, $C_{ext} = 0.01\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$	90	100	110	90	110	μs
			$C_L = 50\text{ pF}$, $C_{ext} = 0.1\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$	0.9	1	1.1	0.9	1.1	ms
Δt_w^\ddagger			$C_L = 50\text{ pF}$	± 1					%

$^\dagger t_w$ = Duration of pulse at Q and \bar{Q} outputs

$^\ddagger \Delta t_w$ = Output pulse-duration variation (Q and \bar{Q}) between circuits in same package

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	\bar{A} or B	Q or \bar{Q}	$C_L = 50\text{ pF}$	8.3	14		1	16	ns
	$\overline{\text{CLR}}$	Q or \bar{Q}		7.4	11.4		1	13	
	$\overline{\text{CLR}}$ trigger	Q or \bar{Q}		8.7	14.9		1	17	
t_w^\dagger		Q or \bar{Q}	$C_L = 50\text{ pF}$, $C_{ext} = 28\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$	167	200			240	ns
			$C_L = 50\text{ pF}$, $C_{ext} = 0.01\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$	90	100	110	90	110	μs
			$C_L = 50\text{ pF}$, $C_{ext} = 0.1\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$	0.9	1	1.1	0.9	1.1	ms
Δt_w^\ddagger				± 1					%

$^\dagger t_w$ = Duration of pulse at Q and \bar{Q} outputs

$^\ddagger \Delta t_w$ = Output pulse-duration variation (Q and \bar{Q}) between circuits in same package

operating characteristics, $T_A = 25^\circ\text{C}$

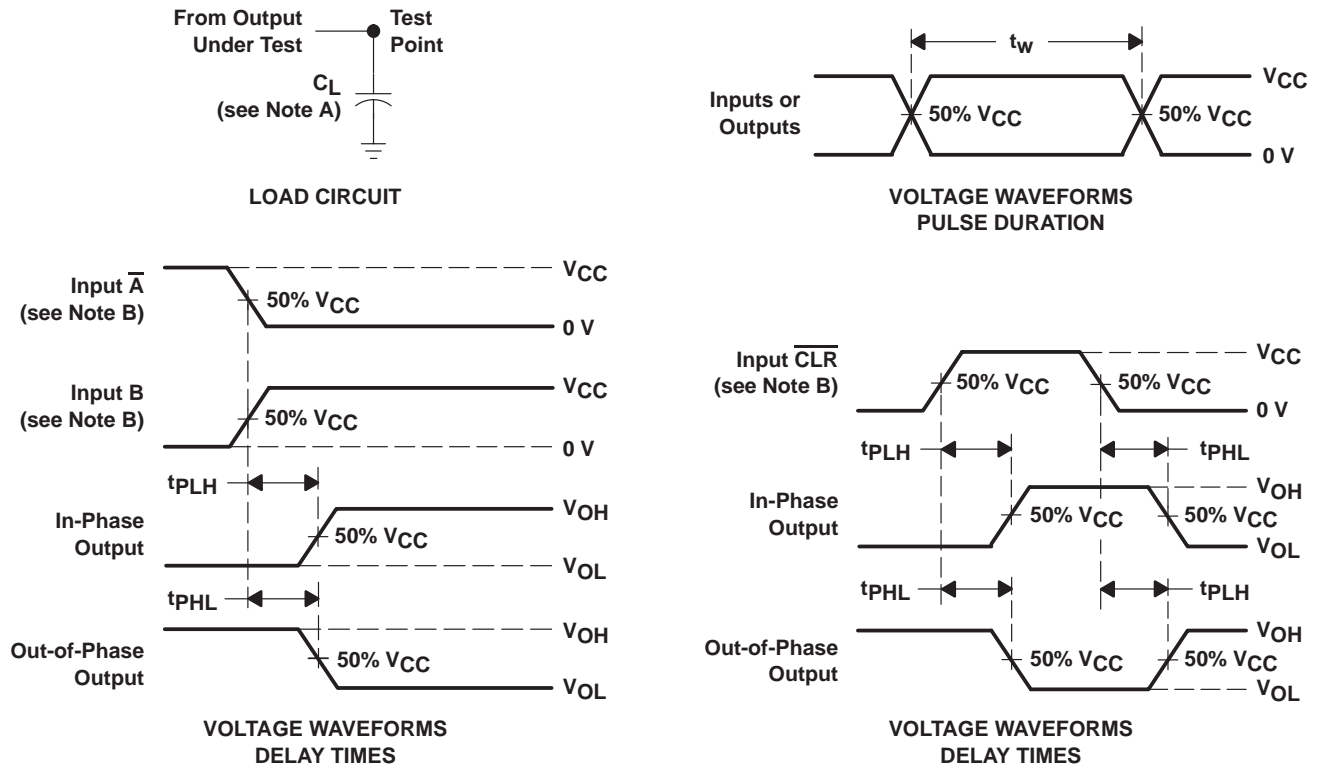
PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	44	pF
		5 V	49	



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 C. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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APPLICATION INFORMATION†

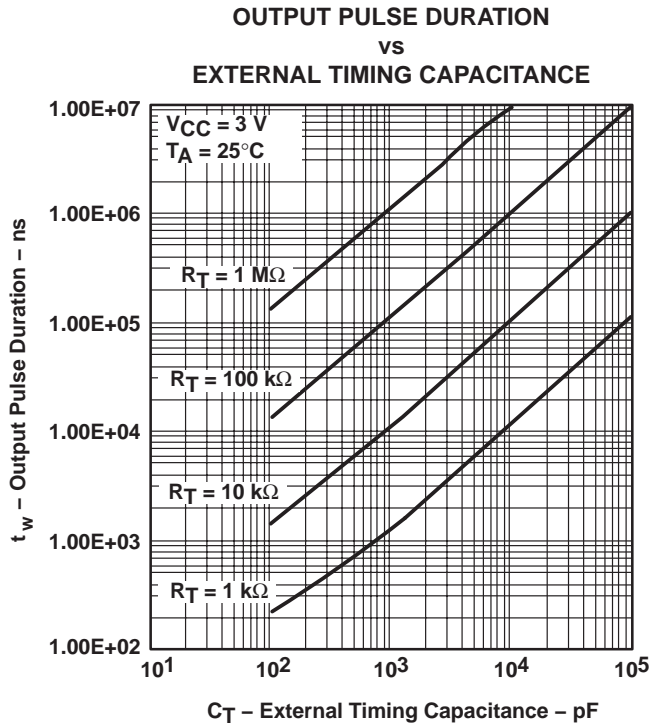


Figure 2

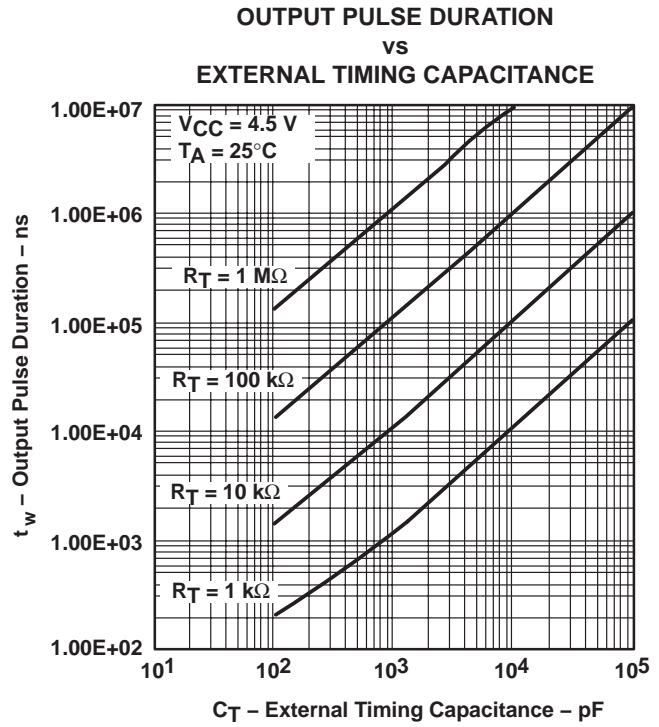


Figure 3

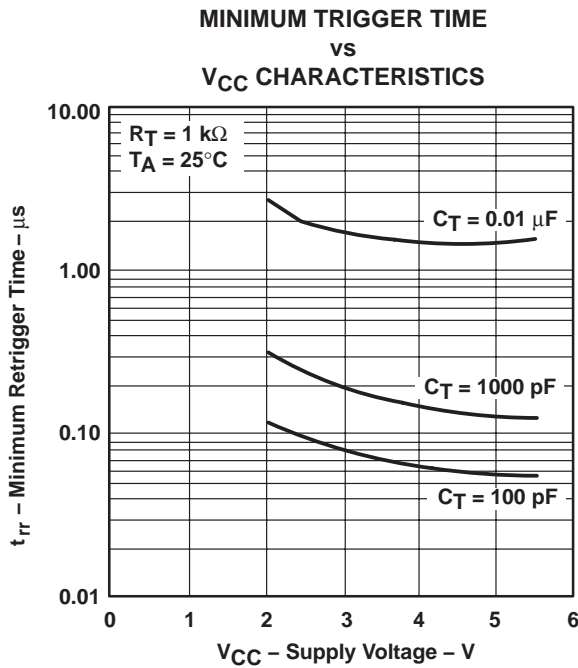


Figure 4

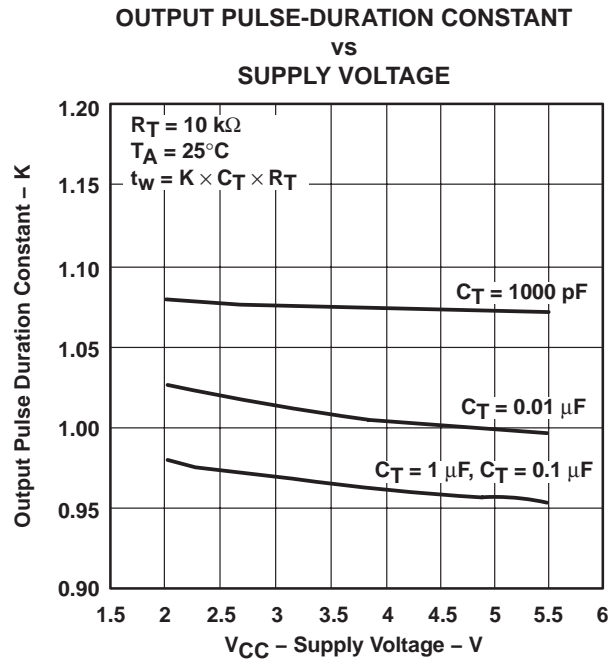


Figure 5

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV123ATPWREP	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L123AEP	Samples
V62/03661-01XE	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L123AEP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LV123A-EP :

- Catalog: [SN74LV123A](#)
- Automotive: [SN74LV123A-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV123ATPWREP	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV123ATPWREP	TSSOP	PW	16	2000	356.0	356.0	35.0

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