National Semiconductor

PRELIMINARY

FEBRUARY 2000

SC14404
Complete Baseband Processor for DECT Handsets

General Description

The SC14404 is a CMOS chip optimized to handle all the audio, signal and data processing needed within a DECT handset. An ADPCM transcoder, a very low power CODEC and Analog Frontend is integrated. Direct connections towards microphone and a (dynamical) loudspeaker are provided. Duplex quality handsfree operation is integrated.

The SC14404 is designed to fit to any radio design.

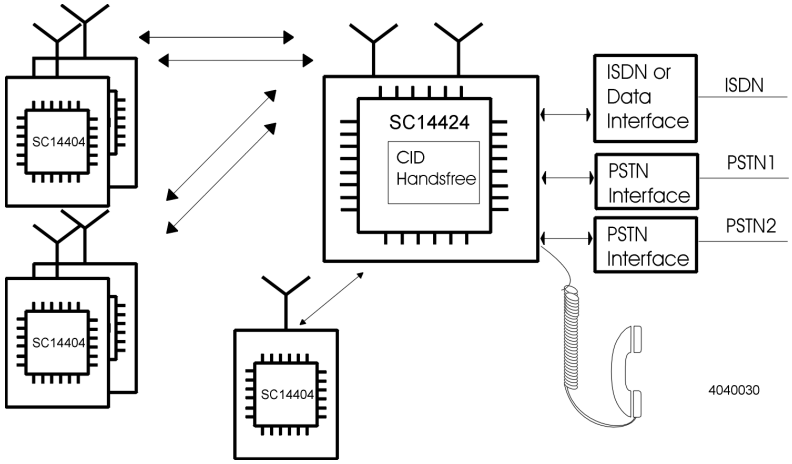
A dedicated TDMA controller handles all physical layer slot formats and radio control.

National Semiconductors standard CompactRISC™ CR16B 16 bit microcontroller takes care of all the higher protocol stack. 4 kilobyte Flash is integrated for parameter and number storage.

Features

- Integrated DECT Baseband transceiver optimized for GAP handsets according to ETS 300 175-2, 175-3 & 175-8.
- Two on board low drop voltage regulators with 2.85V and 3.0- 3.8V (with external resistors the voltage can be determined) output.
- 2V upto 3.6V battery input with onboard step up converter.
- 3V upto 5.0V battery monitor input.
- Advanced battery management unit
- Very low power in active and paging mode.
- Embedded 16 bit CompactRISC™ Micro Controller. (CR16B) with programmable clock speeds.
- 4k byte memory mapped Flash
- 320 kbyte Flash or factory programmed ROM FLASH.
- ACCESSBUS™ or MICROWIRE™ interfaces
- 5,5 kilobyte on-chip Data Memory.
- One full duplex ADPCM transcoder.
- On-chip 14-bit linear CODEC.
- 14 upto 44 dB gain differential microphone input buffer.
- 100 Ω loudspeaker driver.
- Software controlled gain on audio input and output.
- Peak hold ADC for RSSI measurement.
- Five general purpose inputs can be multiplexed on an 8 bit ADC with selectable ranges.
- On-chip dedicated TDMA instruction co-processor which supports 1.152 MHz, 0.576 MHz and 0.288 MHz bit rates.
- Seven programmable control signals for radio front end.
- Full and double slot, protected and unprotected B-fields.
- Duplex quality handsfree operation.
- Tone generator. Tones consisting of 3 frequencies can be programmed
- Linear PCM interface for external codec.

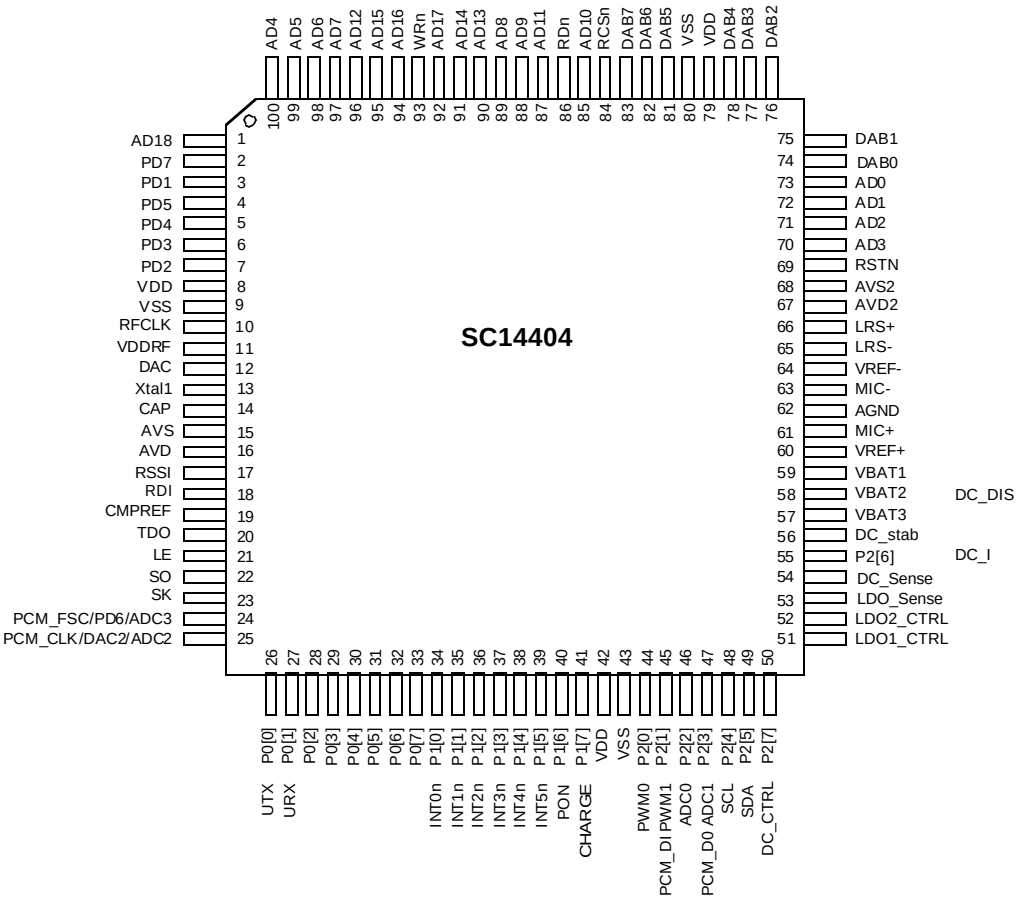
System Diagram



Note: ACCESSBUS™, MICROWIRE™ and CompactRISC™ are trademarks of National Semiconductor Corporation.

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1.0 CONNECTION DIAGRAMS

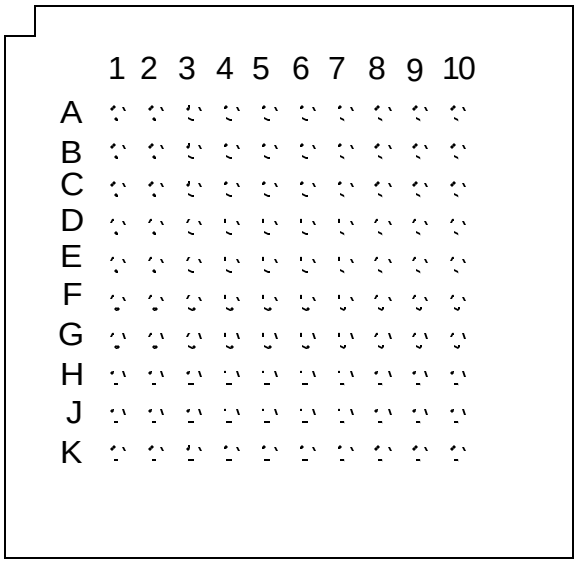


Order Number SC14404BFLAG (320kbyte Full FLASH, Boot mode A, 100 pins TQFP,
Order Number SC14404BFLBG (320kbyte Full FLASH, Boot mode B, 100 pins TQFP
Order Number SC14404BxxAG (320kbyte ROM FLASH, Boot mode A , 100 pins TQFP)
Order Number SC14404BxxBG (320kbyte ROM FLASH, Boot mode B, 100 pins TQFP)

See NS Package Number VJG100A

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SC14404 CSP pin diagram
(TOP View)



Order Number SC14404BFLBC (320kbyte Full FLASH, Boot mode B, 100 pins CSP
Order Number SC14404BxxBC (320kbyte ROM FLASH, Boot mode B, 100 pins CSP

Table 1: TQFP pin mapping onto CSP package (See table 2 for TQFP pin description)

	1	2	3	4	5	6	7	8	9	10
A	1	99	96	93	89	88	86	85	83	76
B	8	2	98	95	92	90	87	80	77	74
C	10	5	3	97	94	84	82	78	73	71
D	11	12	7	6	100	79	81	72	70	68
E	13	15	9	4	16	91	75	69	67	64
F	14	17	19	25	41	66	54	59	65	63
G	18	20	22	31	29	50	56	57	62	61
H	21	23	28	32	34	44	47	53	55	60
J	24	27	30	37	40	42	45	48	52	58
K	26	33	35	36	38	39	43	46	49	51

Note 1: All digital outputs can sink/source 2 mA unless otherwise specified. All digital inputs are Schmitt trigger types. After reset all I/Os are set to input and all pull-up or pull-down resistors are enabled unless otherwise specified.

PU = Pull-up resistor enabled, PD = Pull-down resistor enabled, I = input
A-I, B-I = In Boot mode A or B input and pull-up or pull-down resistor disabled,
A-PD, B-PU = In Boot mode A, Pull-down resistor enabled. In Boot mode B, pull-up resistor enabled.

Note 2: Reset state of address and data bus and WRn, RDn pins:
If SC14404: Hi-Z/1 means Hi-Z if RSTn is LOW, if RSTn goes HIGH it takes 32 SCLK cycles = 25 usec before these pin drives a '1'.

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BLOCK DIAGRAM

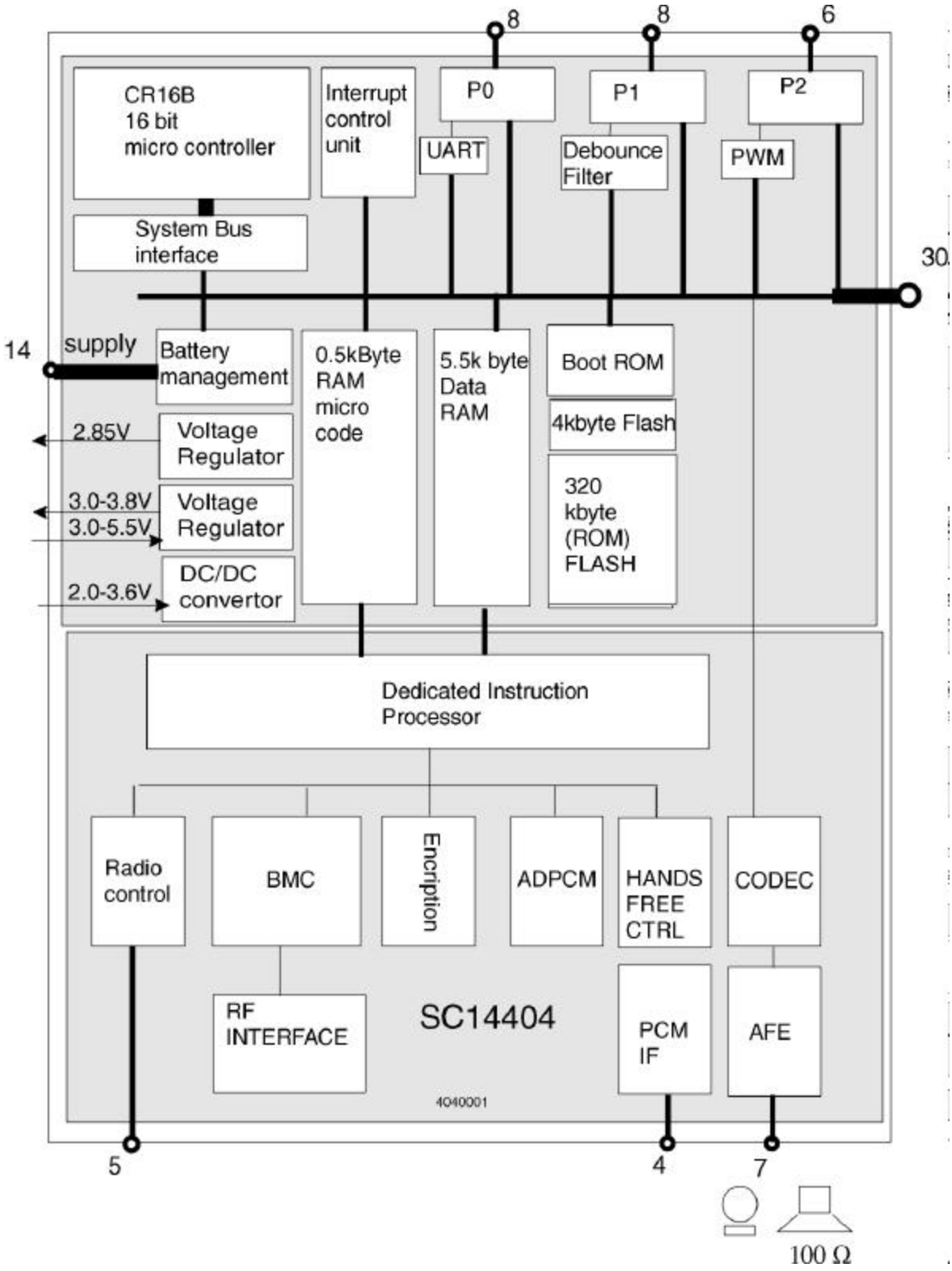


FIGURE 1. SC14404 Block diagram

2.0 Package information

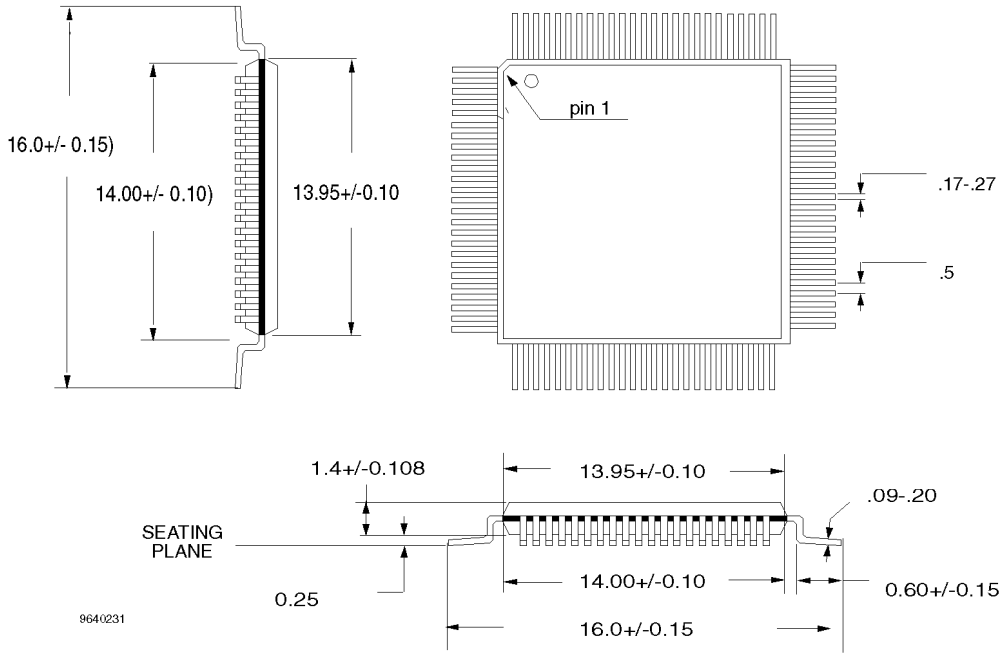
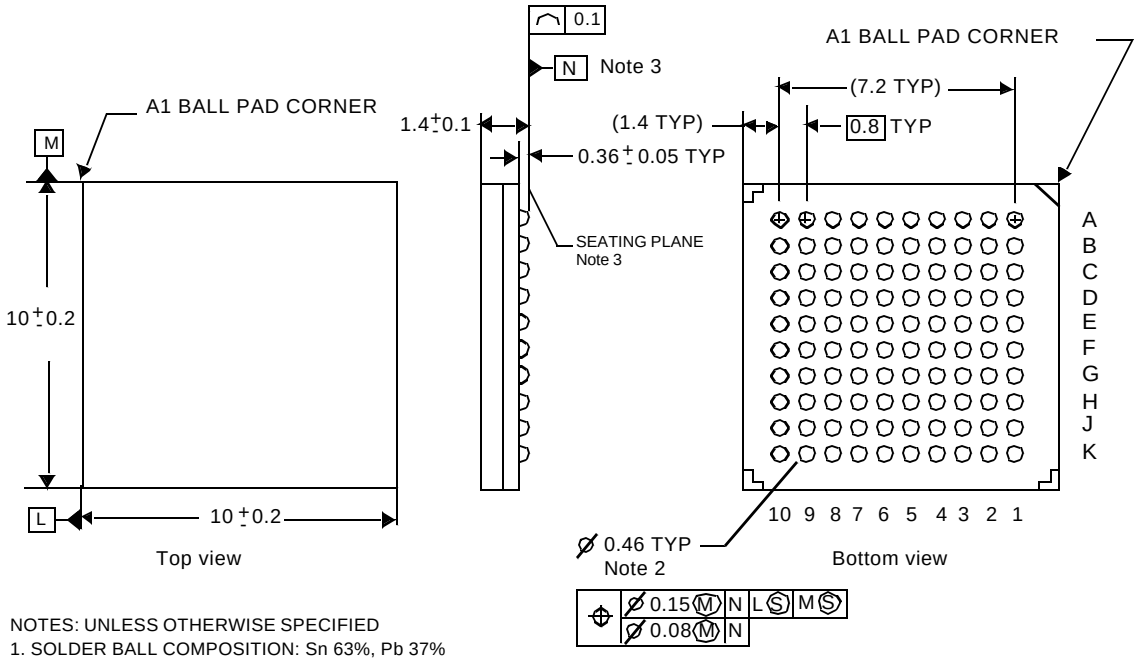


FIGURE 2. 100 pins TP Quad Flat Pack. NS Package Number VJG100A



NOTES: UNLESS OTHERWISE SPECIFIED
1. SOLDER BALL COMPOSITION: Sn 63%, Pb 37%
2. DIMENSIONS MEASURED AT MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM N
3. PRIMARY DATUM N AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
4. NO JEDEC REGISTRATION AS OF JUNE 1998

Dimensions are in milimeters

FIGURE 3. 100 pins Chip Scaled Package. NS package SLC100A

3.0 Product status definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data. Supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by National Semiconductor Corporation. The datasheet is printed for reference information only.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-254-4466
Fax: 65-250-4466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

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