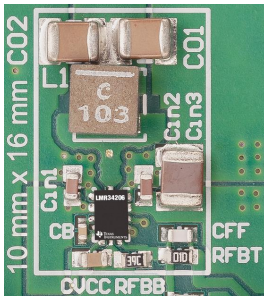
LMR34206-Q1 4.2V 至 42V、0.6A 超小型同步降压转换器

1 特性

- 符合面向汽车 应用的 AEC-Q100 标准：
  - 温度等级 1：–40°C 至 +125°C，T_A
- 专为汽车 应用
  - 结温范围为 –40°C 至 +150°C
  - 保护 功能：热关断、输入欠压锁定、逐周期电流限制和断续短路保护
  - 在 0.6A 负载下具有 0.2V 压降（典型值）
  - ±1.5% 基准电压容差
  - 3.3V、5V固定输出电压选项
- 适合可扩展的电源
  - 与以下器件引脚兼容：
    - LMR36015/06-Q1（60V、0.6A 或 1.5A）
    - LMR33620/30-Q1（36V、2A 或 3A）
  - 2.1MHz 频率选项
- 通过集成技术减小解决方案尺寸，降低成本
  - 小型 2mm × 3mm VQFN 封装（具有可湿性侧面）
  - 很少的外部组件
- 在整个负载范围内具有低功率耗散
  - 在 PFM 模式中提高了轻负载效率
  - 低至 24μA 的工作静态电流
- 进行了优化，可满足超低 EMI 要求
  - 符合 CISPR25 5 类标准
  - Hotrod™封装可最大限度减少开关节点振铃
  - 并行输入路径可最大限度减少寄生电感
  - 扩频频谱可降低峰值辐射发射



2 应用

- ADAS 摄像头模块
- 抬头显示
- 车身控制模块
- 通用宽输入电压电源

3 说明

LMR34206-Q1 稳压器是一款易于使用的同步降压直流/直流转换器。该器件具有集成高侧和低侧功率 MOSFET，可在 4.2V 至 42V 的宽输入电压范围内提供高达 的输出电流。

LMR34206-Q1 采用峰值电流模式控制机制来提供最佳的效率和输出电压精度。精密使能支持直接连接到宽输入电压或对器件启动和关断进行精确控制，因此提供了灵活性。附带内置滤波和延迟功能的电源正常状态标志可提供系统状态的真实指示，免去了使用外部监控器的麻烦。

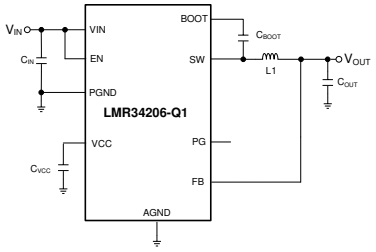
LMR34206-Q1 采用 HotRod™ 封装，实现了低 EMI、更高的效率和最小的封装裸片比率。 此器件需要极少外部组件，其引脚设计可实现简单的 PCB 布局。LMR34206-Q1 的小解决方案尺寸和功能集旨在简化各种终端设备的实施。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LMR34206-Q1	VQFN-HR (12)	2.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

图 1. 简化原理图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (May 2019) to Revision A **Page**

- 添加了 EMI 说明，目标位置：特性 ... 1
- Added 图 28 through 图 37 ... 27

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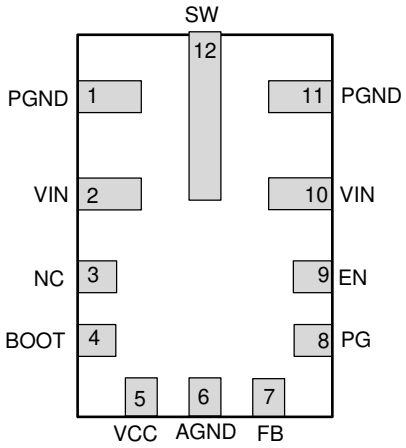
5 Device Comparison Table

ORDERABLE PART NUMBER	OUTPUT VOLTAGE	SPREAD SPECTRUM	FPWM	f_{SW}	PACKAGE QUANTITY
LMR34206FSC3RNXTQ1	3.3-V fixed	Yes	Yes	2.1 MHz	250
LMR34206FSC3RNXRQ1	3.3-V fixed	Yes	Yes	2.1 MHz	3000
LMR34206SC3QRNXTQ1	3.3-V fixed	Yes	No	2.1 MHz	250
LMR34206SC3QRNXRQ1	3.3-V fixed	Yes	No	2.1 MHz	3000
LMR34206FSC5RNXTQ1	5-V fixed	Yes	Yes	2.1 MHz	250
LMR34206FSC5RNXRQ1	5-V fixed	Yes	Yes	2.1 MHz	3000
LMR34206SC5QRNXTQ1	5-V fixed	Yes	No	2.1 MHz	250
LMR34206SC5QRNXRQ1	5-V fixed	Yes	No	2.1 MHz	3000

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6 Pin Configuration and Functions

RNX Package
12-Pin VQFN-HR
Top View



Pin Functions

NO.	NAME	TYPE	DESCRIPTION
1, 11	PGND	G	Power ground terminal. Connect to system ground and AGND. Connect to C_{IN} with short wide traces.
2, 10	VIN	P	Input supply to regulator. Connect to C_{IN} with short wide traces.
3	NC	—	Connect the SW pin to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin. This pin has no internal connection to the regulator.
4	BOOT	P	Boot-strap supply voltage for internal high-side driver. Connect a high-quality 100-nF capacitor from this pin to the SW pin. Connect the SW pin to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin.
5	VCC	P	Internal 5-V LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to GND.
6	AGND	G	Analog ground for regulator and system. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB.
7	FB	A	Feedback input to regulator. Connect to tap point of feedback voltage divider. DO NOT FLOAT. DO NOT GROUND.
8	PG	A	Open drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. Goes low when EN = Low. Can be open or grounded when not used.
9	EN	A	Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN; DO NOT FLOAT.
12	SW	P	Regulator switch node. Connect to power inductor. Connect the SW pin to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin.
A = Analog, P = Power, G = Ground			

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating junction temperature range of -40°C to 150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	–0.3	45	V
	EN to AGND	–0.3	45.3	V
	FB to AGND	–0.3	5.5	V
	PG to AGND	–0.3	22	V
	AGND to PGND	–0.3	0.3	V
Output voltage	SW to PGND	–0.3	45.3	V
	SW to PGND less than 10-ns negative transient	–3.5		V
	CBOOT to SW	–0.3	5.5	V
	VCC to AGND	–0.3	5.5	V
Junction Temperature T_J		-40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±2500	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C5	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with ANSI/ESDA/JEDEC JS-001 specification

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40 ℃ to 150 ℃ (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	4.2	42	V
	EN to PGND(2)	0	42	V
	PG to PGND(2)	0	18	V
Output current	I_{OUT}	0	0.6	A

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see *Electrical Characteristics.*
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.

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7.4 Thermal Information

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7 and simulated on a 4-Layer JEDEC board. They do not represent the performance obtained in an actual application. For design information see *Maximum Ambient Temperature* section.

THERMAL METRIC(1)(2)		LMR34206-Q1 RNX (VQFN-HR) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7 and simulated on a 4-Layer JEDEC board. They do not represent the performance obtained in an actual application. For design information see *Maximum Ambient Temperature* section.

7.5 Electrical Characteristics

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
$I_{Q\text{-}nonSW}$	Operating quiescent current (non-switching)(2)	V_{EN} = 3.3 V (PFM variant only)	14	24	35	µA
I_{SD}	Shutdown quiescent current; measured at VIN pin	V_{EN} = 0 V		3.3		µA
ENABLE (EN PIN)						
$V_{EN\text{-}VCC\text{-}H}$	Enable input high level for V_{CC} output	V_{ENABLE} rising; Internal LDO turns ON			1.14	V
$V_{EN\text{-}VCC\text{-}L}$	Enable input low level for V_{CC} output	V_{ENABLE} falling; Internal LDO turns OFF	0.3			V
$V_{EN\text{-}VOUT\text{-}H}$	Enable input high level for V_{OUT}	V_{ENABLE} rising; Switching ON	1.157	1.231	1.3	V
$V_{EN\text{-}VOUT\text{-}HYS}$	Enable input hysteresis for V_{OUT}	Hysteresis below $V_{EN\text{-}VOUT\text{-}H}$; Switching OFF	45	110	175	mV
$I_{LKG\text{-}EN}$	Enable input leakage current	V_{EN} = 3.3V		0.2	50	nA
INTERNAL LDO (VCC PIN)						
V_{CC}	Internal V_{CC} voltage	6 V ≤ V_{IN} ≤ 42 V	4.75	5	5.25	V
$V_{CC\text{-}UVLO\text{-}Rising}$	Internal V_{CC} undervoltage lockout	V_{CC} rising	3.6	3.8	4.0	V
$V_{CC\text{-}UVLO\text{-}Falling}$	Internal V_{CC} undervoltage lockout	V_{CC} falling	3.1	3.3	3.5	V
VOLTAGE REFERENCE (FB PIN)						
$V_{5v0\text{-}Fixed}$	5 V Fixed Output voltage	Fixed output voltage option	4.9	5	5.1	V
$V_{3v3\text{-}Fixed}$	3.3 V Fixed Output voltage	Fixed output voltage option	3.23	3.3	3.37	V
$I_{LKG\text{-}5v0\text{-}Fixed}$	Feedback leakage current; 5v0 Fixed	V_{OUT} = 5 V (Fixed output voltage option only)		2.5	2.9	µA
$I_{LKG\text{-}3v3V\text{-}Fixed}$	Feedback leakage current; 3v3 Fixed	V_{OUT} = 3.3 V (Fixed output voltage option only)		1.4	1.8	µA

(1) MIN and MAX limits are 100% production tested at 25℃. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.

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Electrical Characteristics (continued)

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMITS AND HICCUP						
I_{SC}	High-side current limit(3)		0.8	1	1.2	A
$I_{LS-LIMIT}$	Low-side current limit(3)		0.6	0.8	0.95	A
I_{L-ZC}	Zero cross detector threshold	PFM variants only		0.02		A
$I_{PEAK-MIN}$	Minimum inductor peak current(3)			0.18		A
I_{L-NEG}	Negative current limit(3)	FPWM variant only	-0.95	–0.6	–0.25	A
POWER GOOD (PGOOD PIN)						
$V_{PG-HIGH-UP}$	Power-Good upper threshold - rising	% of FB voltage	105%	107%	110%	
$V_{PG-LOW-DN}$	Power-Good lower threshold - falling	% of FB voltage	90%	93%	95%	
V_{PG-HYS}	Power-Good hysteresis (rising & falling)	% of FB voltage		2%		
T_{PG}	Power-Good rising/falling edge deglitch delay		80	140	200	µs
$V_{PG-VALID}$	Minimum input voltage for proper Power-Good function				2	V
R_{PG}	Power-Good on-resistance	V_{EN} = 2.5 V		80	165	Ω
R_{PG}	Power-Good on-resistance	V_{EN} = 0 V		35	90	Ω
OSCILLATOR						
F_{OSC}	Internal oscillator frequency	2.1-MHz variant	1.95	2.1	2.35	MHz
MOSFETS						
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	I_{OUT} = 0.5 A		225	435	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	I_{OUT} = 0.5 A		150	280	mΩ

(3) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.

7.6 Timing Requirements

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V.

		MIN	NOM	MAX	UNIT
t_{ON-MIN}	Minimum switch on-time		55	83	ns
$t_{OFF-MIN}$	Minimum switch off-time		53	73	ns
t_{ON-MAX}	Maximum switch on-time		7	12	µs
t_{SS}	Internal soft-start time	3	4.5	6	ms

(1) MIN and MAX limits are 100% production tested at 25℃. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

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7.7 System Characteristics

The following specifications apply to a typical application circuit with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25℃ only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40℃ to 150℃. *These specifications are not ensured by production testing.*

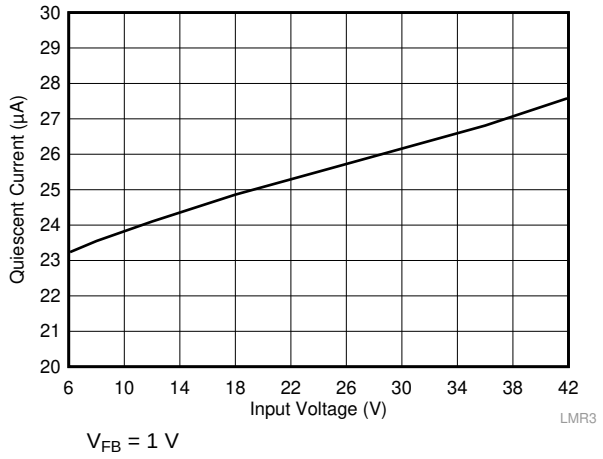
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage range		4.2		42	V
V_{OUT}	Voltage regulation for V_{OUT} = 3.3 V fixed(1)	FPWM operation	3.28	3.33	3.37	V
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 12 V, V_{OUT} = 3.3 V Fixed, PFM variant		26		µA
D_{MAX}	Maximum switch duty cycle(2)			98%		
V_{HC}	FB pin voltage required to trip short-circuit hiccup mode			0.4		V
t_{HC}	Time between current-limit hiccup burst			94		ms
t_D	Switch voltage dead time			2		ns
F_{sSS}	Frequency span of spread spectrum operation			±4		%
F_{rSS}	Triangular spread spectrum repetition frequency			16		kHz
T_{SD}	Thermal shutdown temperature	Shutdown temperature		170		°C
T_{SD}	Thermal shutdown temperature	Recovery temperature		158		°C

(1) Deviation in V_{OUT} from nominal output voltage value at V_{IN} = 24 V, I_{OUT} = 0 A to 0.6A
(2) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: $F_{MIN} = 1 / (t_{ON\text{-}MAX} + t_{OFF\text{-}MIN})$. $D_{MAX} = t_{ON\text{-}MAX} / (t_{ON\text{-}MAX} + t_{OFF\text{-}MIN})$.

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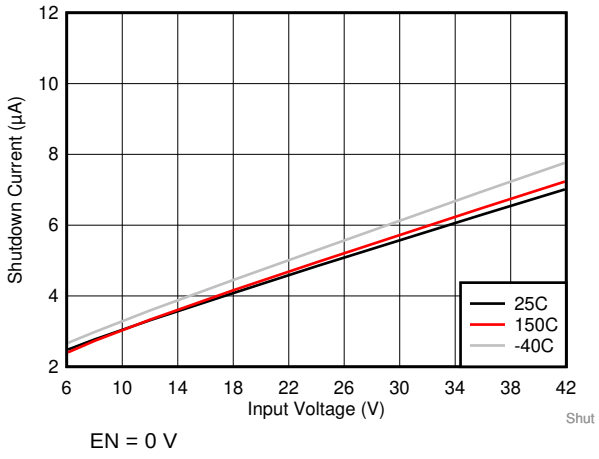
7.8 Typical Characteristics

Unless otherwise specified the following conditions apply: T_A = 25°C. V_{IN} = 24 V.



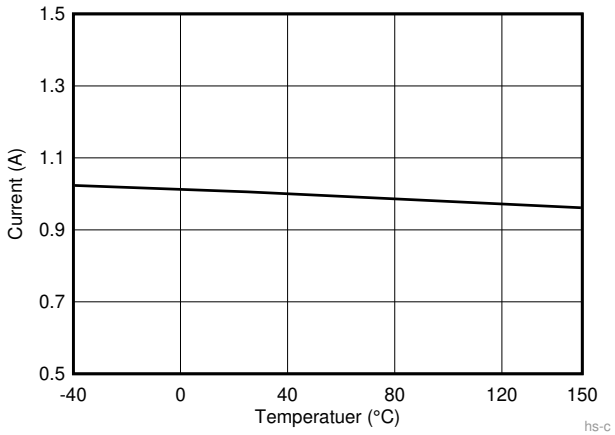
V_{FB} = 1 V

图 2. Non-Switching Input Supply Current



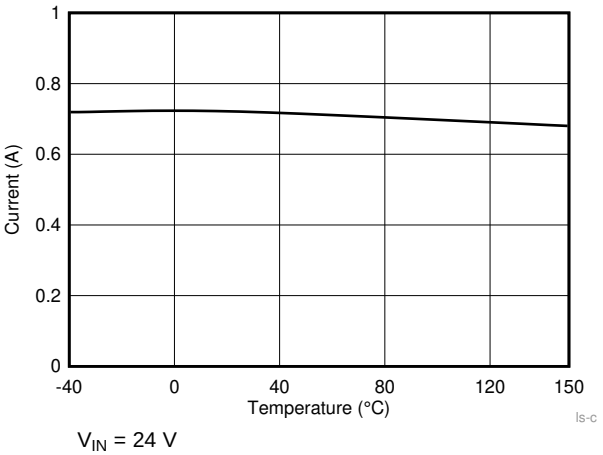
EN = 0 V

图 3. Shutdown Supply Current



V_{IN} = 24 V

图 4. High Side Current Limit



V_{IN} = 24 V

图 5. Low Side Current Limit

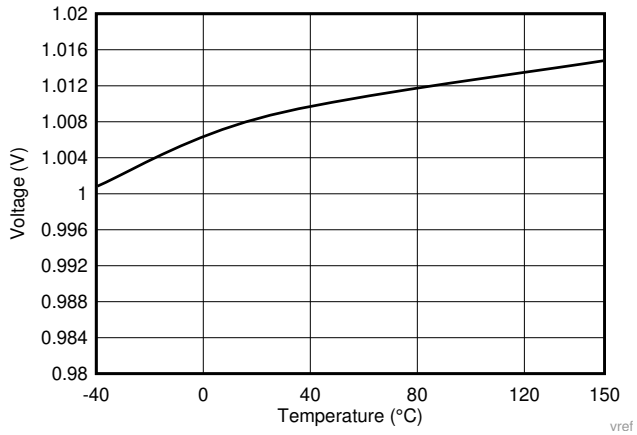
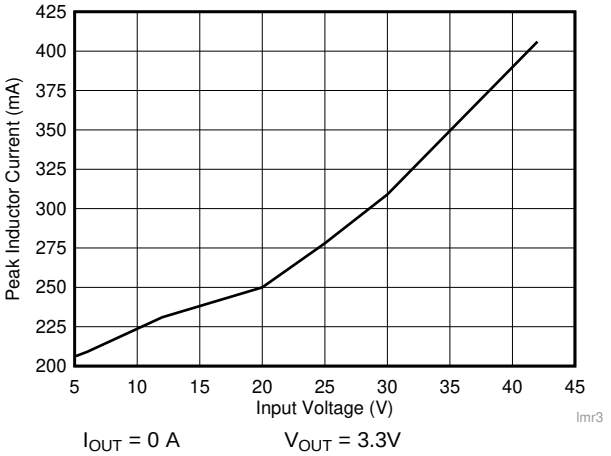


图 6. Reference Voltage Drift



I_{OUT} = 0 A V_{OUT} = 3.3V

f_{SW} = 2100 kHz

图 7. $I_{PEAK-MIN}$

8 Detailed Description

8.1 Overview

The LMR34206-Q1 is a synchronous peak-current-mode buck regulator designed for a wide variety of applications. The regulator automatically switches modes between PFM and PWM depending on load. At heavy loads, the device operates in PWM at a constant switching frequency. At light loads the mode changes to PFM, with diode emulation allowing DCM. This reduces the input supply current and keeps efficiency high. The device features internal loop compensation which reduces design time and requires fewer external components than externally compensated regulators.

The LMR34206-Q1 is designed with a flip-chip or HotRod™ technology, greatly reducing the parasitic inductance of pins. In addition, the layout of the device allows for reduction in the radiated noise generated by the switching action through partial cancellation of the current generated magnetic field. As a result the switch-node waveform exhibits less overshoot and ringing.

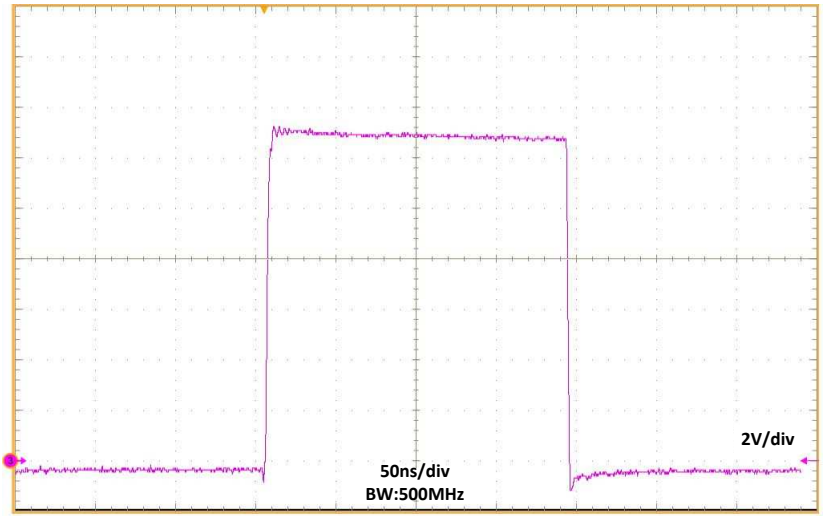
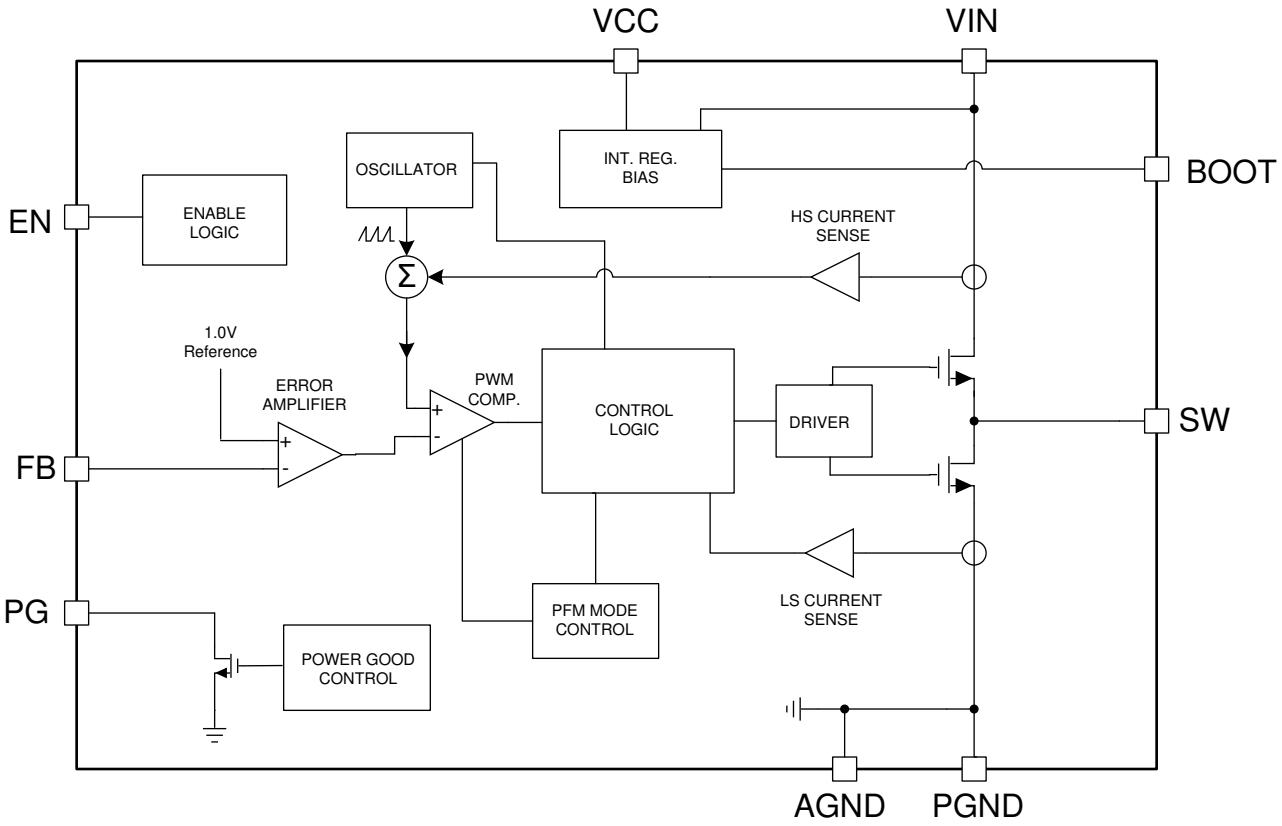


图 8. Switch Node Waveform

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8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power-Good Flag Output

The power-good flag function (PG output pin) of the LMR34206-Q1 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output goes low under fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. Output voltage excursions lasting less than t_{PG} do not trip the power-good flag. Power-good operation can best be understood by reference to 图 9 and 图 10. Note that during initial power-up a delay of about 4 ms (typical) is inserted from the time that EN is asserted to the time that the power-good flag goes high. This delay only occurs during start-up and is not encountered during normal operation of the power-good function.

The power-good output consists of an open drain NMOS; requiring an external pullup resistor to a suitable logic supply. It can also be pulled up to either VCC or V_{OUT}, through an appropriate resistor, as desired. If this function is not needed, the PG pin must be grounded. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is ≥ 2 V (typical). Limit the current into this pin to ≤ 4 mA.

Feature Description (接下页)

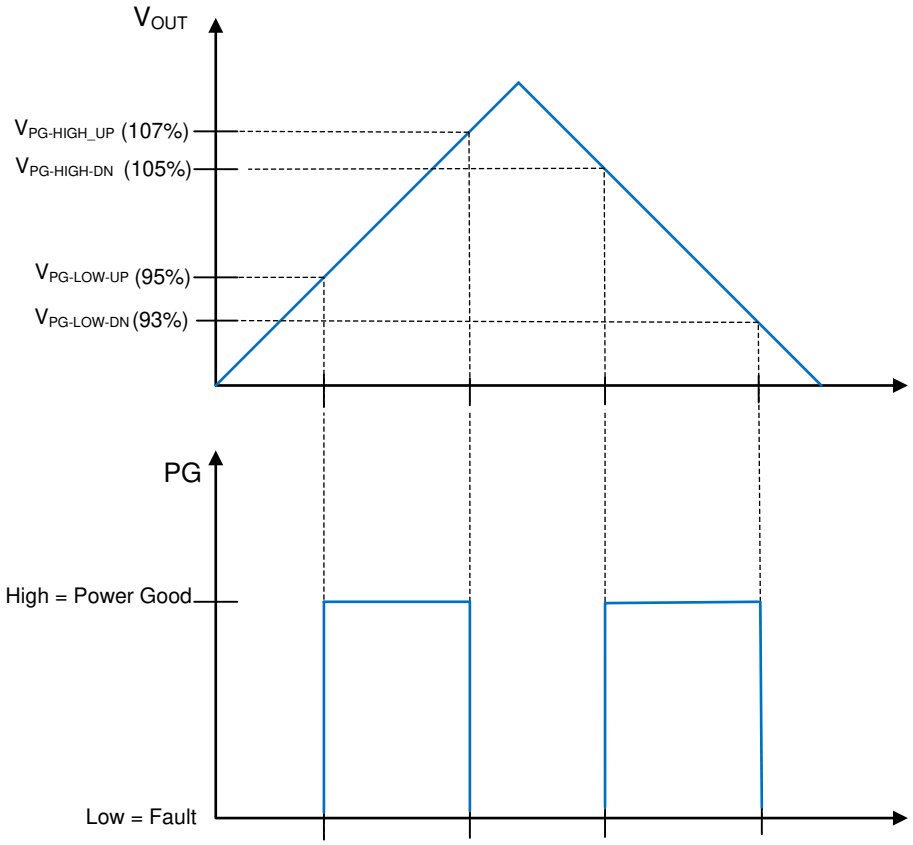


图 9. Static Power-Good Operation

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Feature Description (接下页)

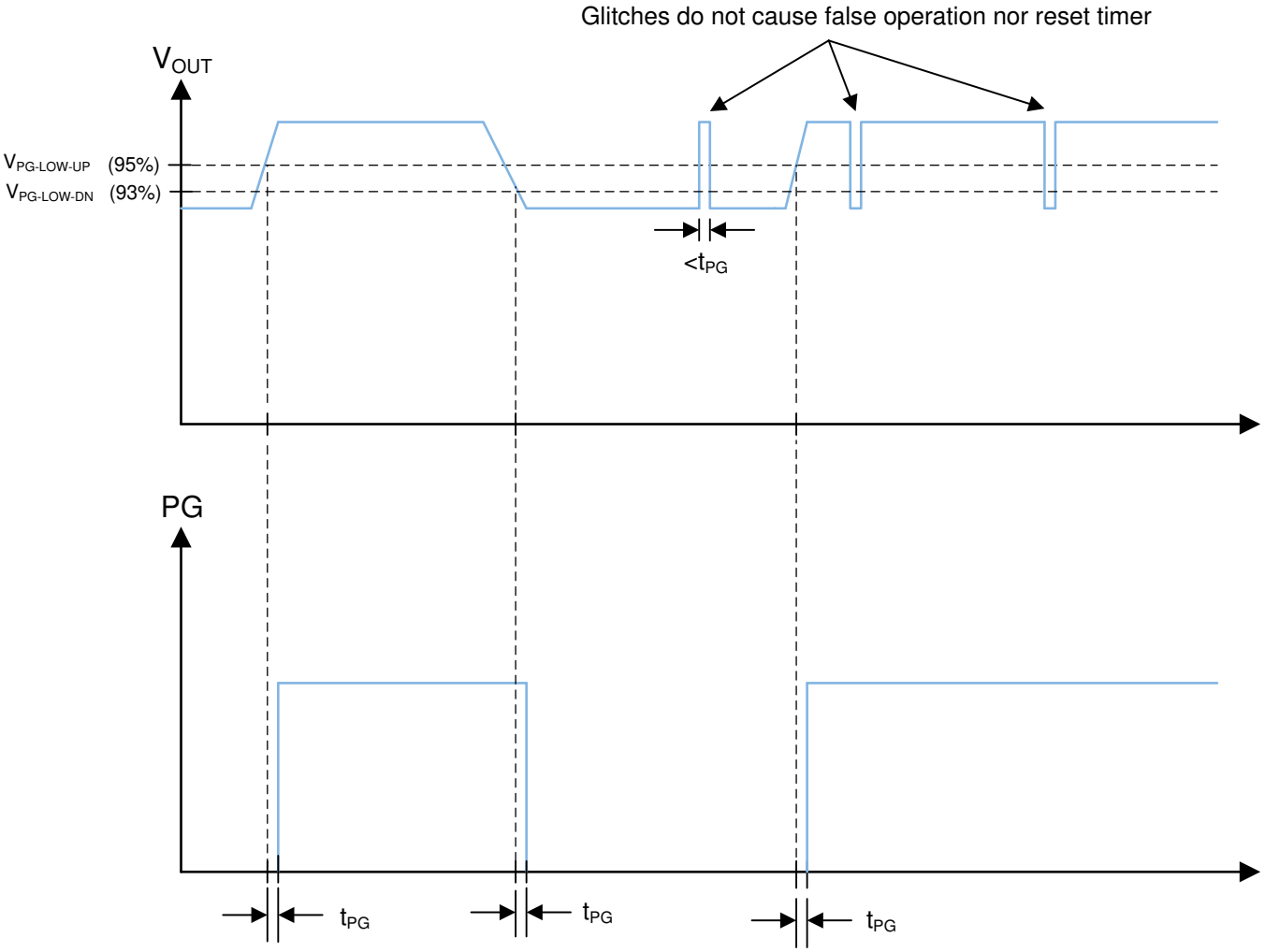


图 10. Power-Good-Timing Behavior

8.3.2 Enable and Start-up

Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input UVLO (see the *External UVLO* section). Applying a voltage of ≥ $V_{EN-VCC-H}$ causes the device to enter standby mode, powering the internal VCC, but not producing an output voltage. Increasing the EN voltage to $V_{EN-OUT-H}$ (V_{EN-H} in 图 11) fully enables the device, allowing it to enter start-up mode and beginning the soft-start period. When the EN input is brought below $V_{EN-OUT-H}$ (V_{EN-H} in 图 11) by $V_{EN-OUT-HYS}$ (V_{EN-HYS} in 图 11), the regulator stops running and enters standby mode. Further decrease in the EN voltage to below $V_{EN-VCC-L}$ completely shuts down the device. This behavior is shown in 图 11. The EN input may be connected directly to VIN if this feature is not needed. This input must not be allowed to float. The values for the various EN thresholds can be found in the table.

The LMR34206-Q1 utilizes a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up. A typical start-up waveform is shown in 图 12 along with typical timings. The rise time of the output voltage is about 4 ms.

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Feature Description (接下页)

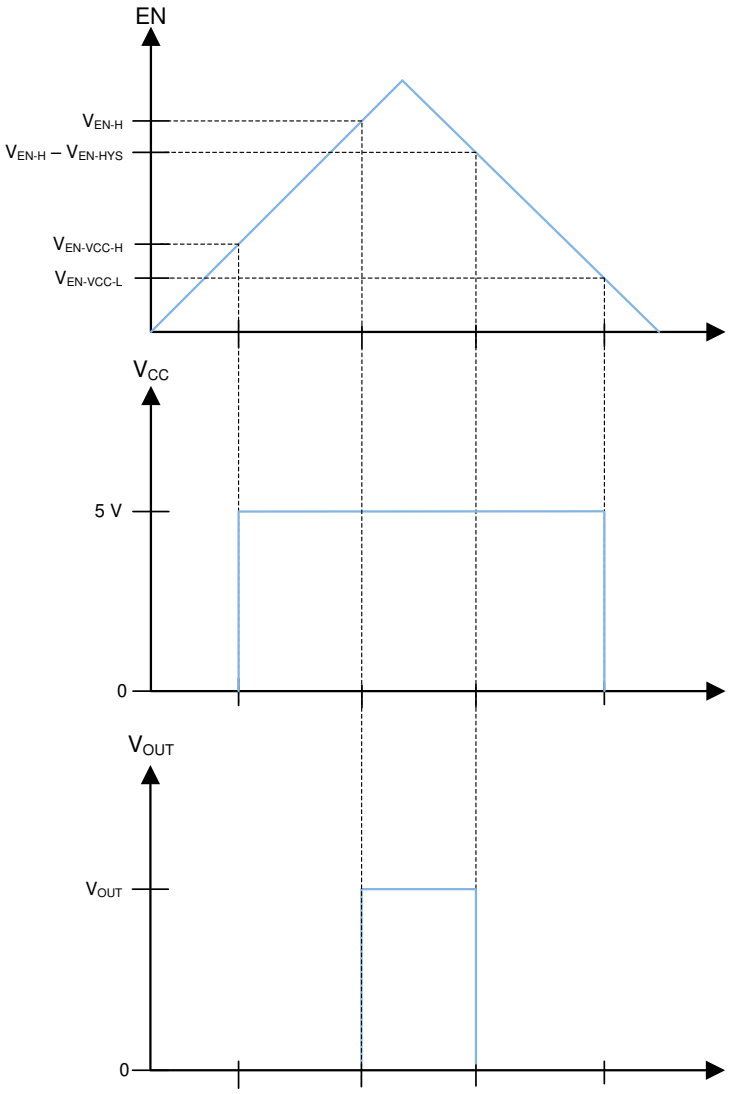


图 11. Precision Enable Behavior

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Feature Description (接下页)

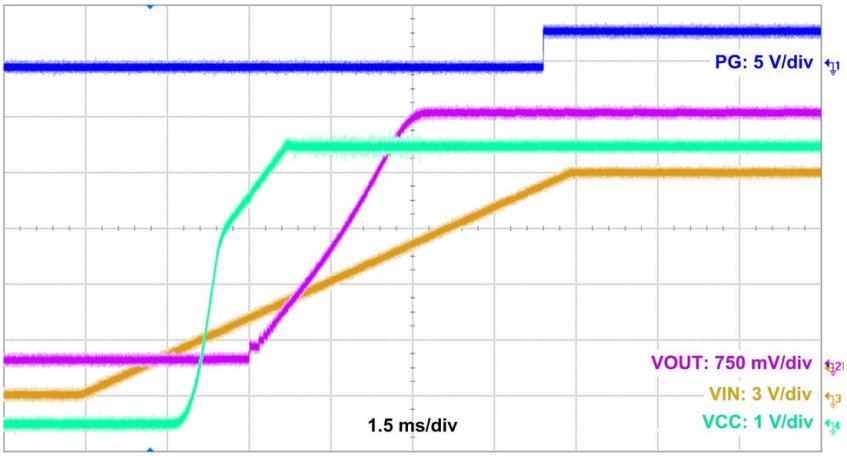


图 12. Typical Start-up Behavior
V_{IN} = 12V, V_{OUT} = 3.3 V, I_{OUT} = 0.6 A

8.3.3 Current Limit and Short Circuit

The LMR34206-Q1 incorporates valley current limit for normal overloads and for short-circuit protection. In addition the high-side power MOSFET is protected from excessive current by a peak current limit circuit. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for short circuits. Finally, a zero current detector is used on the low-side power MOSFET to implement diode emulation mode (DEM) at light loads (see *Glossary*).

During overloads the low-side current limit, I_{LIMIT}, determines the maximum load current that the LMR34206-Q1 can supply. When the low-side switch turns on, the inductor current begins to ramp down. If the current does not fall below I_{LIMIT} before the next turnon cycle, then that cycle is skipped, and the low-side MOSFET is left on until the current falls below I_{LIMIT}. This is somewhat different than the more typical peak current limit and results in 公式 1 for the maximum load current.

$$I_{OUT}\big|_{max} = I_{LIMIT} + \frac{(V_{IN} - V_{OUT})}{2 \cdot f_{SW} \cdot L} \cdot \frac{V_{OUT}}{V_{IN}} \quad (1)$$

where

- f_{SW} = switching frequency
- L = inductor value

If, during current limit, the voltage on the FB input falls below about 0.4 V due to a short circuit, the device enters into hiccup mode. In this mode the device stops switching for t_{HC} or about 94 ms, and then goes through a normal re-start with soft start. If the short-circuit condition remains, the device runs in current limit for about 20 ms (typical) and then shuts down again. This cycle repeats, as shown in as long as the short-circuit condition persists. This mode of operation helps to reduce the temperature rise of the device during a hard short on the output. Of course the output current is greatly reduced during hiccup mode. Once the output short is removed and the hiccup delay is passed, the output voltage recovers normally as shown in 图 13.

The high-side-current limit trips when the peak inductor current reaches I_{SC}. This is a cycle-by-cycle current limit and does not produce any frequency or load current fold back. It is meant to protect the high-side MOSFET from excessive current. Under some conditions, such as high input voltages, this current limit may trip before the low-side protection. Under this condition, I_{SC} determines the maximum output current. Note that I_{SC} varies with duty cycle.

Feature Description (接下页)

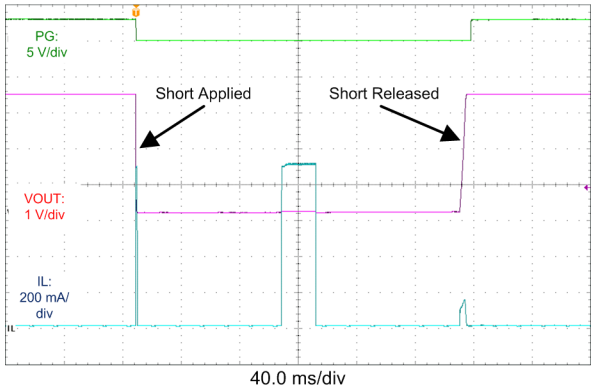


图 13. Short-Circuit Transient and Recovery

8.3.4 Undervoltage Lockout and Thermal Shutdown

The LMR34206-Q1 incorporates an undervoltage-lockout feature on the output of the internal LDO (at the VCC pin). When VCC reaches 3.8 V (typ.), the device receives the EN signal and starts switching. When VCC falls below 3.3 V (typ.), the device shuts down, regardless of EN status. Because the LDO is in dropout during these transitions, the previously mentioned values roughly represent the input voltage levels during the transitions.

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches about 170°C, the device shuts down; re-start occurs when the temperature falls to about 158°C .

8.4 Device Functional Modes

8.4.1 Auto Mode

In auto mode the device moves between PWM and PFM as the load changes. At light loads the regulator operates in PFM. At higher loads the mode changes to PWM.

In PWM the regulator operates as a constant frequency, current mode, full synchronous converter using PWM to regulate the output voltage. While operating in this mode the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple.

In PFM the high-side MOSFET is turned on in a burst of one or more pulses to provide energy to the load. The duration of the burst depends on how long it takes the inductor current to reach $I_{PEAK-MIN}$. The frequency of these bursts is adjusted to regulate the output, while diode emulation (DEM) is used to maximize efficiency (see *Glossary*). This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads. This trades off very good light-load efficiency for larger output voltage ripple and variable switching frequency. Also, a small increase in output voltage occurs at light loads. The actual switching frequency and output voltage ripple depends on the input voltage, output voltage, and load. Typical switching waveforms in PFM and PWM are shown in 图 14 and 图 15.

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Device Functional Modes (接下页)

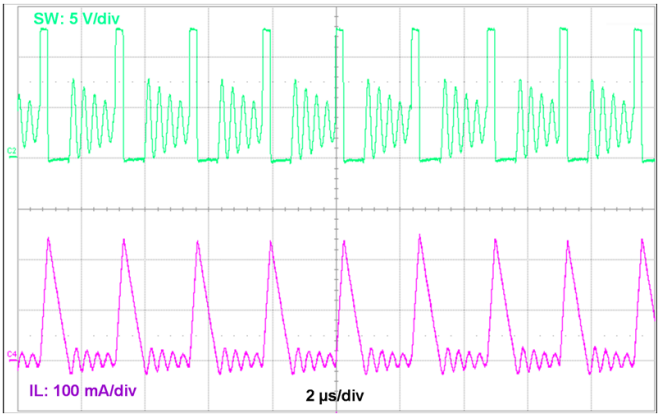


图 14. Typical PFM Switching Waveforms
V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 30 mA

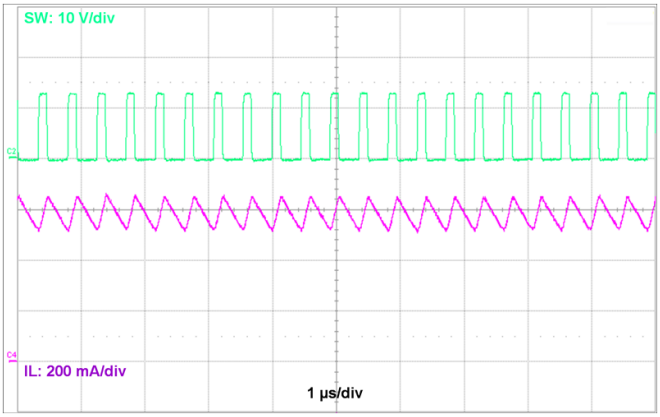


图 15. Typical PWM Switching Waveforms
V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0.6 A, f_S = 2100 kHz

8.4.2 Forced PWM Operation

The following select variant(s) is/are a factory option made available for cases when constant frequency operation is more important than light load efficiency.

表 1. LMR34206-Q1 Device Variants with Fixed Frequency Operation at No Load

ORDERABLE PART NUMBER	OUTPUT VOLTAGE	SPREAD SPECTRUM	FPWM	F_{SW}
LMR34206FSC3RNXTQ1	3.3-V fixed	Yes	Yes	2.1 MHz
LMR34206FSC3RNXRQ1	3.3-V fixed	Yes	Yes	2.1 MHz
LMR34206FSC5RNXTQ1	5-V fixed	Yes	Yes	2.1 MHz
LMR34206FSC5RNXRQ1	5-V fixed	Yes	Yes	2.1 MHz

In FPWM operation, the diode emulation feature is turned off. This means that the device remains in CCM under light loads. Under conditions where the device must reduce the on-time or off-time below the ensured minimum to maintain regulation, the frequency reduces to maintain the effective duty cycle required for regulation. This occurs for very high and very low input/output voltage ratios. When in FPWM mode, a limited reverse current is allowed through the inductor allowing power to pass from the regulator's output to its input. Note that in FPWM mode, larger currents pass through the inductor, if lightly loaded, than in auto mode. Once loads are heavy enough to necessitate CCM operation, FPWM mode has no measurable effect on regulator operation.

8.4.3 Dropout

The dropout performance of any buck regulator is affected by the R_{DSON} of the power MOSFETs, the DC resistance of the inductor, and the maximum duty cycle that the controller can achieve. As the input voltage is reduced to near the output voltage, the off-time of the high-side MOSFET starts to approach the minimum value. Beyond this point the switching may become erratic and/or the output voltage falls out of regulation. To avoid this problem the LMR34206-Q1 automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation. In this data sheet the dropout voltage is defined as the difference between the input and output voltage when the output has dropped by 1% of its nominal value. Under this condition the switching frequency has dropped to its minimum value of about 140 kHz. Note that the 0.4 V short circuit detection threshold is not activated when in dropout mode. Typical dropout characteristics can be found in 图 16 and 图 17.

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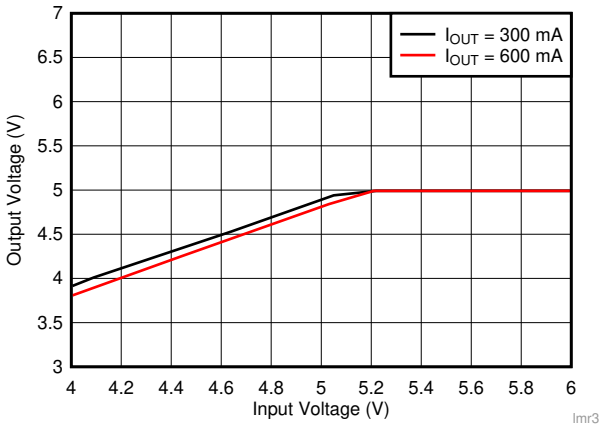


图 16. Overall Dropout Characteristic
V_{OUT} = 5 V

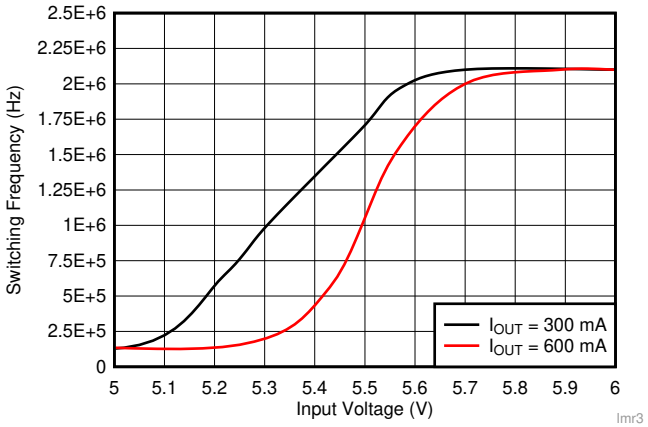


图 17. Typical f_{SW} vs Output Current
f_{SW} = 2100 kHz

8.4.4 Minimum Switch On-Time

Every switching regulator has a minimum controllable on-time dictated by the inherent delays and blanking times associated with the control circuits. This imposes a minimum switch duty cycle and therefore a minimum conversion ratio. The constraint is encountered at high input voltages and low output voltages. To help extend the minimum controllable duty cycle, the LMR34206-Q1 automatically reduces the switching frequency when the minimum on-time limit is reached. In this way the converter can regulate the lowest programmable output voltage at the maximum input voltage. An estimate for the approximate input voltage, for a given output voltage, before frequency foldback occurs is found in 公式 2. As the input voltage is increased, the switch on-time (duty cycle) reduces to regulate the output voltage. When the on-time reaches the limit, the switching frequency drops, while the on-time remains fixed.

$$V_{IN} \leq \frac{V_{OUT}}{t_{ON} \cdot f_{SW}} \tag{2}$$

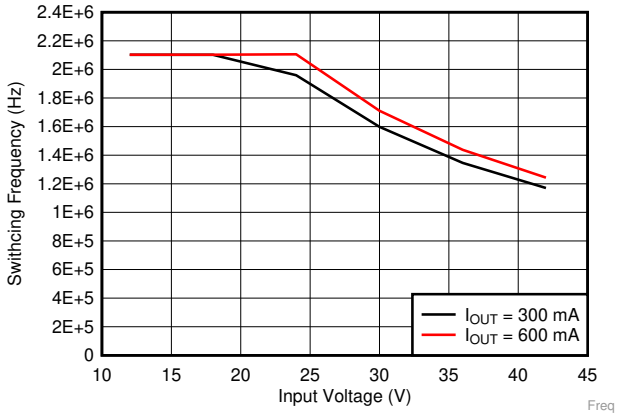


图 18. Switching Frequency vs Input Voltage
V_{OUT} = 3.3 V

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8.4.5 Spread Spectrum Operation

The spread spectrum is a factory option in the select variants.

表 2. LMR34206-Q1 Device Variant(s) with Spread Spectrum Operation

ORDERABLE PART NUMBER	OUTPUT VOLTAGE	SPREAD SPECTRUM	FPWM	f_{SW}
LMR34206FSC3RNXTQ1	3.3-V Fixed	Yes	Yes	2.1 MHz
LMR34206FSC3RNXRQ1	3.3-V Fixed	Yes	Yes	2.1 MHz
LMR34206SC3QRNXTQ1	3.3-V Fixed	Yes	No	2.1 MHz
LMR34206SC3QRNXRQ1	3.3-V Fixed	Yes	No	2.1 MHz
LMR34206FSC5RNXTQ1	5-V Fixed	Yes	Yes	2.1 MHz
LMR34206FSC5RNXRQ1	5-V Fixed	Yes	Yes	2.1 MHz
LMR34206SC5QRNXTQ1	5-V Fixed	Yes	No	2.1 MHz
LMR34206SC5QRNXRQ1	5-V Fixed	Yes	No	2.1 MHz

The purpose of the spread spectrum is to eliminate peak emissions at specific frequencies by spreading emissions across a wider range of frequencies than a part with fixed frequency operation. In most systems containing the LMR34206-Q1 low frequency conducted emissions from the first few harmonics of the switching frequency can be easily filtered. A more difficult design criterion is reduction of emissions at higher harmonics which fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node. The LMR34206-Q1 devices with a triangular spread spectrum use typically a ±4% spreading rate with the modulation rate set at 16 kHz (typical). The spread spectrum is only available while the internal clock is free running at its natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- At high input voltages/low output voltage ratio when the device operates at minimum on time the internal clock is slowed disabling spread spectrum.
- The clock is slowed during dropout.
- The internal clock is slowed at light load in the PFM variant (LMR34206SC3QRNXTQ1, LMR34206SC5QRNXRQ1). In FPWM mode, spread spectrum is active even if there is no load.

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9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMR34206-Q1 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 0.6 A. The following design procedure can be used to select components for the LMR34206-Q1. Alternately, the WEBENCH® Design Tool may be used to generate a complete design. This tool utilizes an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various options.

9.2 Typical Application

图 19 shows for the LMR34206-Q1. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick start guide, 表 3 provides typical component values for a range of the most common output voltages.

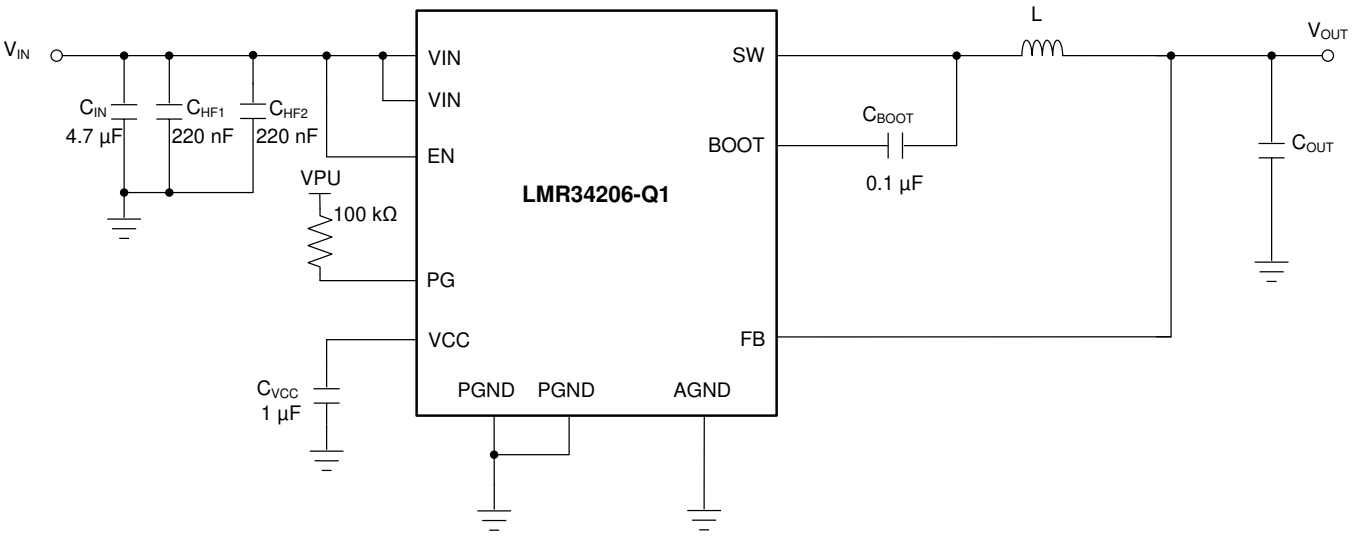


图 19. Example Applications Circuit (Fixed Output)

表 3. Typical External Component Values

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	Nominal C_{OUT} (rated capacitance) (1)	Minimum C_{OUT} (rated capacitance) (2)	C_{IN}
2100	3.3	6.8	2 × 15 µF	1 × 15 µF	4.7 µF + 2 × 220 nF
2100	5	10	2 × 15 µF	1 × 15 µF	4.7 µF + 2 × 220 nF

(1) Optimized for superior load transient performance from 0 to 100% rated load.
(2) Optimized for size constrained end applications.

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9.2.1 Design Requirements

9.2.1.1 Design Requirements

Example requirements for a typical 3.3-V application. The input voltages are here for illustration purposes only. See *Specifications* for the operating input voltage range.

表 4. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	6 V to 18 V steady state, 4.2 V to 42-V transients
Output voltage	3.3 V
Maximum output current	0 A to 0.6 A
Switching frequency	2100 kHz
Current consumption at 0-A load	Not Critical: <100 mA is acceptable
Switching frequency at 0-A load	Not critical: Need fixed frequency operation at high load only

表 5. List of Components

V_{OUT}	FREQUENCY	C_{OUT}	L	U1
3.3 V	2100 kHz	1 × 15 µF	7.8 µH, 13.6 mΩ	LMR34206FSC3RNXRQ1

9.2.2 Detailed Design Procedure

9.2.2.1 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, and hence a more compact design. For this example 2.1 MHz is used.

9.2.2.2 Setting the Output Voltage

FB is connected directly to the output voltage node. Preferably, near the top of the output capacitor. If the feedback point is located further away from the output capacitors (that is, remote sensing), then a small 100-nF capacitor may be needed at the sensing point.

9.2.2.3 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, use the the maximum device current. 公式 3 can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example K = 0.4 was chosen with an inductance 5.1 µH; the standard value of 7.8 µH was selected.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \cdot K \cdot I_{OUT\,max}} \cdot \frac{V_{OUT}}{V_{IN}} \tag{3}$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, I_{SC}. This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{LIMIT}, is designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly. This may lead to component damage; do not allow the inductor to saturate! Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies above about 1 MHz. In any case, the inductor saturation current must not be less than the device low-side current limit, I_{LIMIT}. In order to avoid sub-harmonic oscillation, the inductance value must not be less than that given in 公式 4:

$$L_{MIN} \geq 0.28 \cdot \frac{V_{OUT}}{f_{SW}} \tag{4}$$

9.2.2.4 Output Capacitor Selection

The value of the output capacitor, and its ESR, determine the output voltage ripple and load transient performance. The output capacitor bank is usually limited by the load transient requirements, rather than the output voltage ripple. 公式 5 can be used to estimate a lower bound on the total output capacitance, and an upper bound on the ESR, required to meet a specified load transient.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \cdot \Delta V_{OUT} \cdot K} \cdot \left[(1-D) \cdot (1+K) + \frac{K^2}{12} \cdot (2-D) \right]$$

$$ESR \leq \frac{(2+K) \cdot \Delta V_{OUT}}{2 \cdot \Delta I_{OUT} \left[1+K+\frac{K^2}{12} \cdot \left(1+\frac{1}{(1-D)} \right) \right]}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

where

- ΔV_{OUT} = output voltage transient
- ΔI_{OUT} = output current transient
- K = Ripple factor from

(5)

Once the output capacitor and ESR have been calculated, 公式 6 can be used to check the output voltage ripple.

$$V_r \cong \Delta I_L \cdot \sqrt{ESR^2 + \frac{1}{(8 \cdot f_{SW} \cdot C_{OUT})^2}}$$

where

- V_r = peak-to-peak output voltage ripple

(6)

The output capacitor and ESR can then be adjusted to meet both the load transient and output ripple requirements.

In practice the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help to reduce high frequency noise. Small case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing spikes on the output caused by inductor and board parasitics.

Limit the maximum value of total output capacitance to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

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9.2.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum ceramic capacitance of 4.7-µF is required on the input of the LMR34206-Q1. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and/or maintain the input voltage during load transients. In addition a small case size 220-nF ceramic capacitor must be used at the input, as close a possible to the regulator. This provides a high frequency bypass for the control circuits internal to the device. For this example a 4.7-µF, 50-V, X7R (or better) ceramic capacitor is chosen. The 220 nF must also be rated at 50-V with an X7R dielectric. The VQFN package provides two input voltage pins and two power ground pins on opposite sides of the package. This allows the input capacitors to be split, and placed optimally with respect to the internal power MOSFETs, thus improving the effectiveness of the input bypassing. In this example, place two 220-nF ceramic capacitors at each VIN-PGND location.

It is often desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads/traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor(s). The approximate RMS value of this current can be calculated from 公式 7 and should be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \tag{7}$$

9.2.2.6 C_{BOOT}

The LMR34206-Q1 requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100 nF and at least 16 V is required.

9.2.2.7 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-µF, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general this output must not be loaded with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see *Power-Good Flag Output*). A value in the range of 10 kΩ to 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 5 V.

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9.2.2.8 External UVLO

In some cases an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in 图 20 can be used. The input voltage at which the device turns on is designated V_{ON}; while the turnoff voltage is V_{OFF}. First a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ and then 公式 8 is used to calculate R_{ENT} and V_{OFF}.

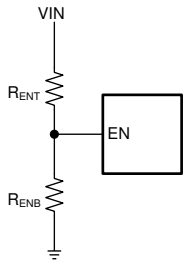


图 20. Set-up for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-H}} - 1 \right) \cdot R_{ENB}$$

$$V_{OFF} = V_{ON} \cdot \left(1 - \frac{V_{EN-HYS}}{V_{EN}} \right)$$

where

- V_{ON} = V_{IN} turnon voltage
- V_{OFF} = V_{IN} turnoff voltage

(8)

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9.2.2.9 Maximum Ambient Temperature

As with any power conversion device, the LMR34206-Q1 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss and the effective thermal resistance, $R_{\theta JA}$ of the device and PCB combination. The maximum internal die temperature for the LMR34206-Q1 must be limited to 150°C. This establishes a limit on the maximum device power dissipation and therefore the load current. 公式 9 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in *Semiconductor and IC Package Thermal Metrics*, the values given in are not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT}|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \quad (9)$$

where

- η = Efficiency

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as power dissipation, air temperature/flow, PCB area, copper heat-sink area, number of thermal vias under the package, and adjacent component placement; to mention just a few. Due to the ultra-miniature size of the VQFN (RNX) package, a DAP is not available. This means that this package exhibits a somewhat greater $R_{\theta JA}$. A typical example of $R_{\theta JA}$ vs copper board area can be found in 图 21. Note that the data given in this graph is for illustration purposes only, and the actual performance in any given application depends on all of the factors mentioned above.

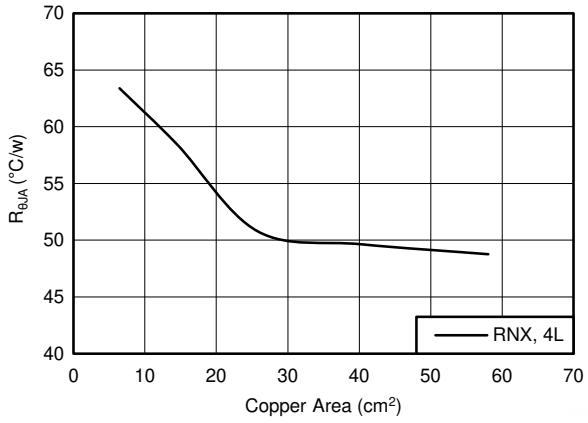


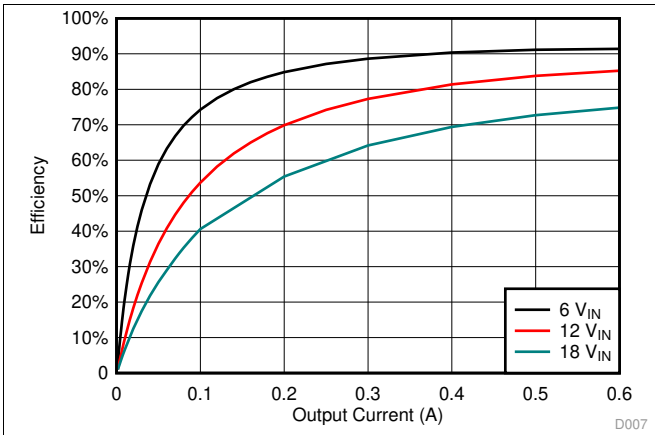
图 21. $R_{\theta JA}$ versus Copper Board Area for the VQFN (RNX) Package

Use the following resources as guides to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight*
- *Semiconductor and IC Package Thermal Metrics*
- *Thermal Design Made Simple with LM43603 and LM43602*
- *Using New Thermal Metrics*

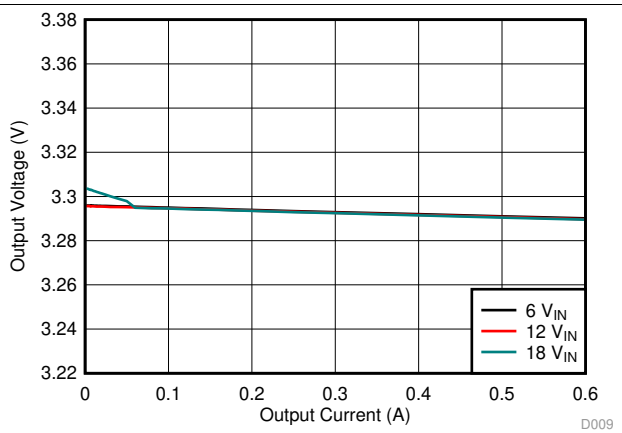
9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, T_A = 25°C. The circuit is shown in 图 19, with the BOM from 表 5. through 图 36 show the conducted and radiated emissions performance tested against the CISPR25 Class 5 limits. For the conducted EMI results the limit lines labeled "AV5" represent the average limits, and the limit lines labeled "PK5" represent the peak limits. For the radiated EMI results the blue limit lines represent the average limits, and the black limit lines represent the peak limits.



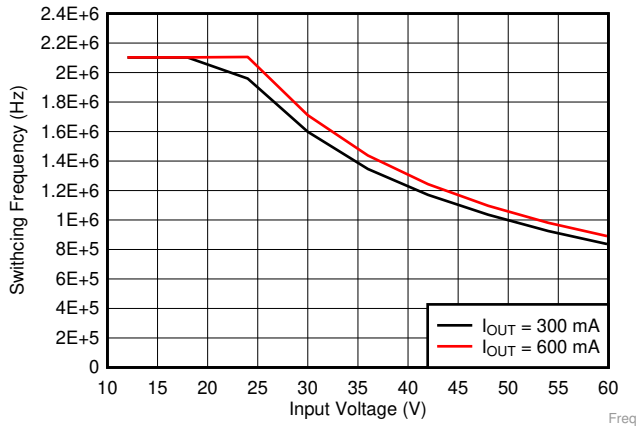
V_{OUT} = 3.3 V 2100 kHz

图 22. Efficiency



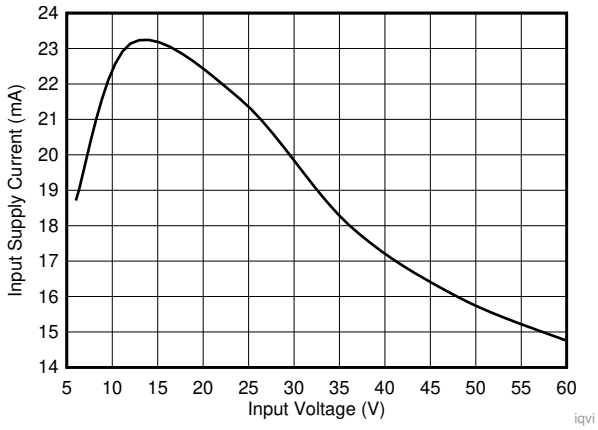
V_{OUT} = 3.3 V 2100 kHz

图 23. Load Regulation



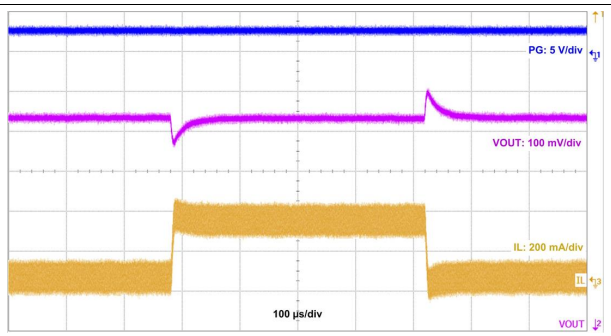
V_{OUT} = 3.3 V 2100 kHz

图 24. Switching Frequency vs Input Voltage



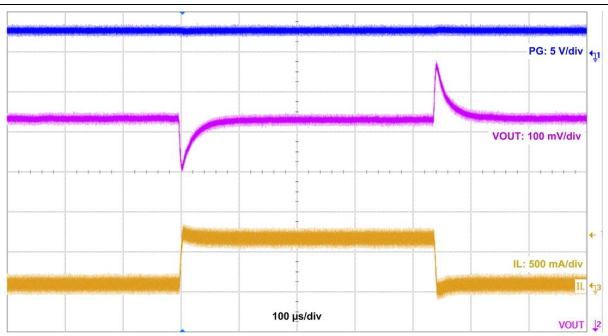
V_{OUT} = 3.3 V 2100 kHz

图 25. Input Supply Current



V_{OUT} = 3.3 V 2100 kHz I_{LOAD}= 10 mA - 0.3 A
Slew Rate = 1 A/µs

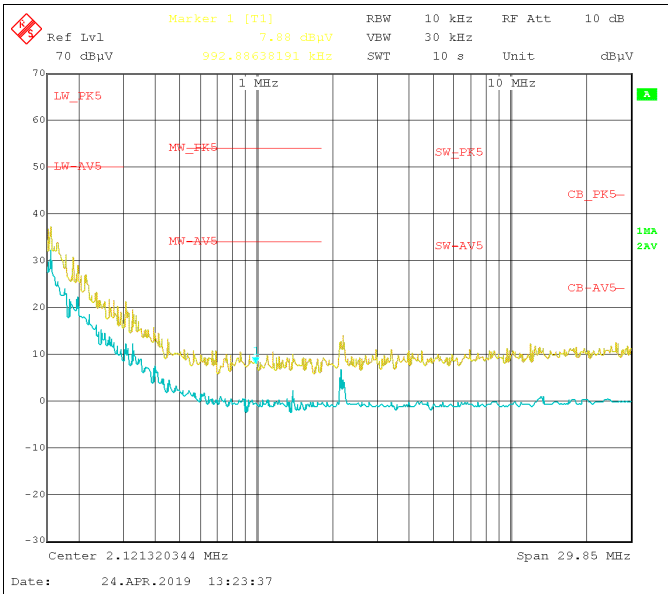
图 26. Load Transient



V_{OUT} = 3.3 V 2100 kHz I_{LOAD}= 10 mA - 0.6 A
Slew Rate = 1 A/µs

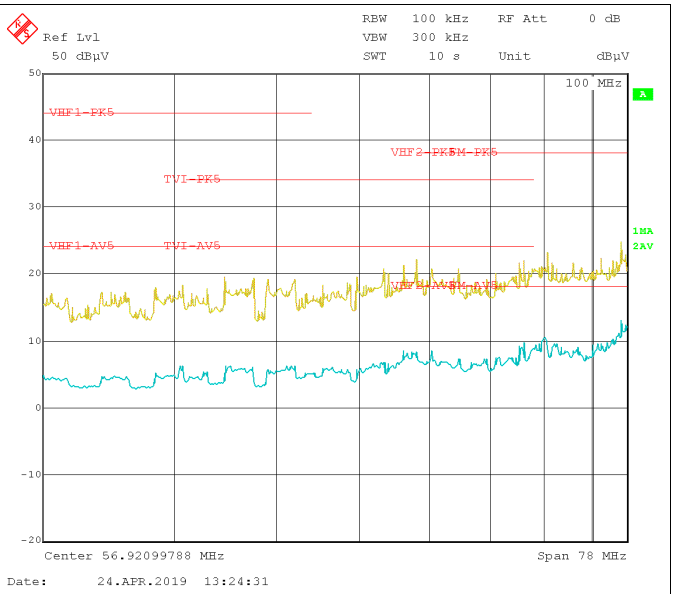
图 27. Load Transient

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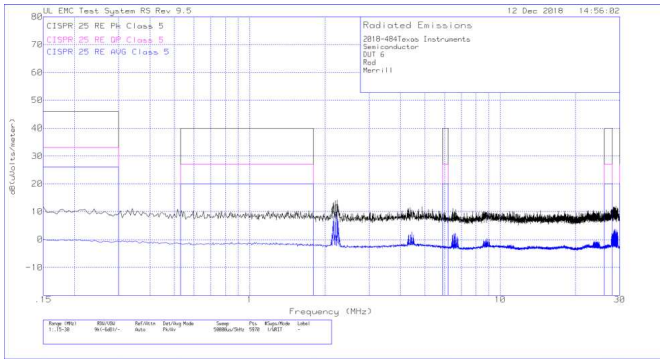
V_{IN} = 13.5 V V_{OUT} = 5 V I_{OUT} = 1.5 A
Frequency Tested: 150kHz to 30 MHz

图 28. Conducted EMI vs. CISPR25 Limits (Yellow: Peak Signal, Blue: Average Signal)



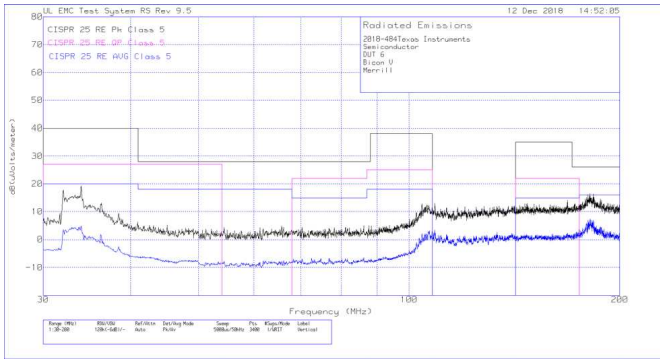
V_{IN} = 13.5 V V_{OUT} = 5 V I_{OUT} = 1.5 A
Frequency Tested: 30 MHz to 108 MHz

图 29. Conducted EMI vs. CISPR25 Limits (Yellow: Peak Signal, Blue: Average Signal)



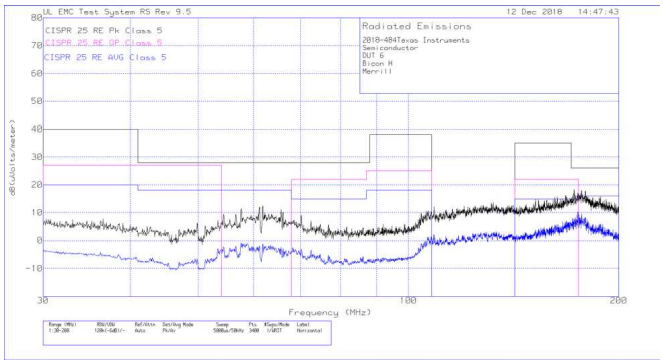
V_{IN} = 13.5 V V_{OUT} = 5 V I_{OUT} = 1.5 A
Frequency Tested: 150 kHz to 30 MHz

图 30. Radiated EMI Rod vs. CISPR25 Limits



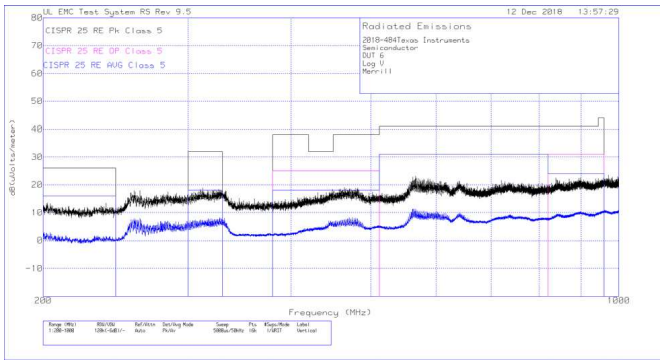
V_{IN} = 13.5 V V_{OUT} = 5 V I_{OUT} = 1.5 A
Frequency Tested: 30 MHz to 200 MHz

图 31. Radiated EMI Bicon Vertical vs. CISPR25 Limits



V_{IN} = 13.5 V V_{OUT} = 5 V I_{OUT} = 1.5 A
Frequency Tested: 30 MHz to 200 MHz

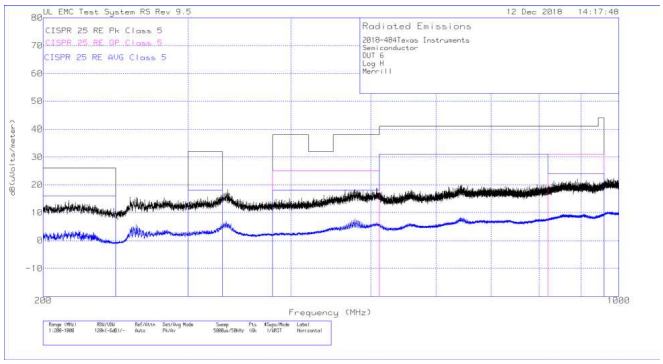
图 32. Radiated EMI Bicon Horizontal vs. CISPR25 Limits



V_{IN} = 13.5 V V_{OUT} = 5 V I_{OUT} = 1.5 A
Frequency Tested: 200 MHz to 1 GHz

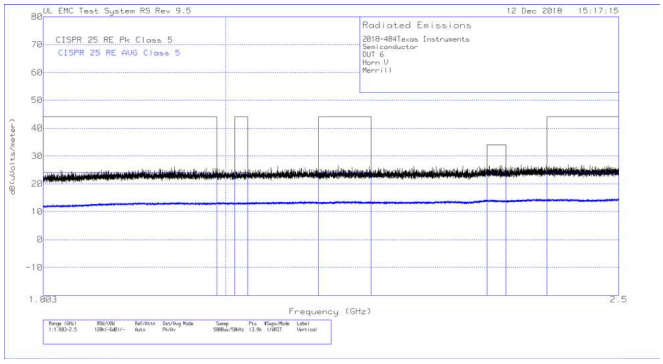
图 33. Radiated EMI Log Vertical vs. CISPR25 Limits

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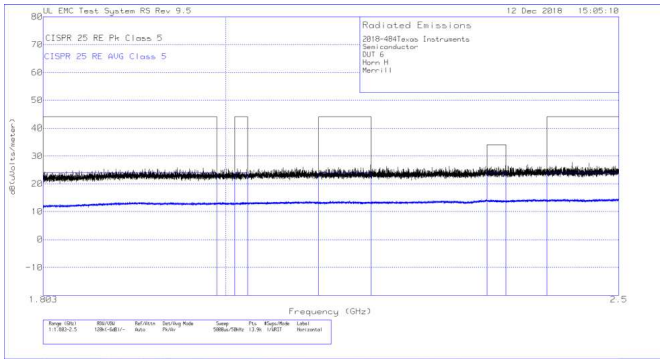
V_{IN} = 13.5 V V_{OUT} = 5 V I_{OUT} = 1.5 A
Frequency Tested: 200 MHz to 1 GHz

图 34. Radiated EMI Log Horizontal vs. CISPR25 Limits



V_{IN} = 13.5 V V_{OUT} = 5 V I_{OUT} = 1.5 A
Frequency Tested: 1.83 GHz to 2.5 GHz

图 35. Radiated EMI Horn Vertical vs. CISPR25 Limits



V_{IN} = 13.5 V V_{OUT} = 5 V I_{OUT} = 1.5 A
Frequency Tested: 1.8 GHz to 2.5 GHz

图 36. Radiated EMI Horn Horizontal vs. CISPR25 Limits

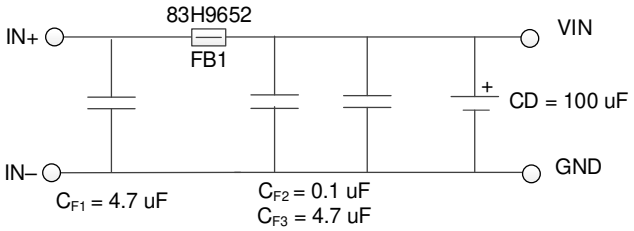


图 37. Recommended Input EMI Filter

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10 Power Supply Recommendations

The characteristics of the input supply must be compatible with the *Specifications* found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 公式 10.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \quad (10)$$

where

- η is the efficiency

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an underdamped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip may cause the regulator to momentarily shutdown and/or reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the regulator and/or use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help to damp the input resonant circuit and reduce any overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The *AN-2162 Simple Success With Conducted EMI From DCDC Converters User's Guide* provides helpful suggestions when designing an input filter for any switching regulator.

In some cases a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow may damage the device.

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11 Layout

11.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Poor PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, to a great extent the EMI performance of the regulator is dependent on the PCB layout. In a buck converter the most critical PCB feature is the loop formed by the input capacitor(s) and power ground, as shown in 图 38. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. shows a recommended layout for the critical components of the .

1. *Place the input capacitor(s) as close as possible to the VIN and GND terminals.* VIN and GND pins are adjacent, simplifying the input capacitor placement.
2. *Place bypass capacitor for VCC close to the VCC pin.* This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
3. *Use wide traces for the C_{BOOT} capacitor.* Place C_{BOOT} close to the device with short/wide traces to the BOOT and SW pins. Route the SW pin to the N/C pin and used to connect the BOOT capacitor to SW.
4. *Place the feedback divider as close as possible to the FB pin of the device.* Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
5. *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and also act as a heat dissipation path.
6. *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
7. *Provide enough PCB area for proper heat-sinking.* As stated in the section, enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers must be made with two ounce copper; and no less than one ounce. If the PCB design uses multiple copper layers (recommended), these thermal vias can also be connected to the inner layer heat-spreading ground planes.
8. *Keep switch area small.* Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies Application Report*
- *Simple Switcher PCB Layout Guidelines Application Report*
- *Construction Your Power Supply- Layout Considerations Seminar*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x Application Report*

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Layout Guidelines (接下页)

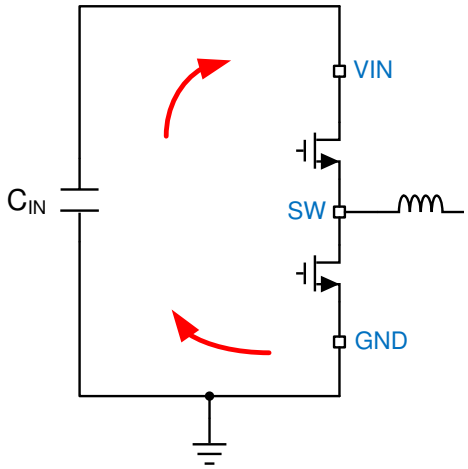


图 38. Current Loops with Fast Edges

11.1.1 Ground and Thermal Considerations

As previously mentioned, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces as well as a quiet reference potential for the control circuitry. Connect the AGND and PGND pins to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low side MOSFET switch and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and may bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise; use for sensitive routes.

Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding and lower thermal resistance.

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11.2 Layout Example

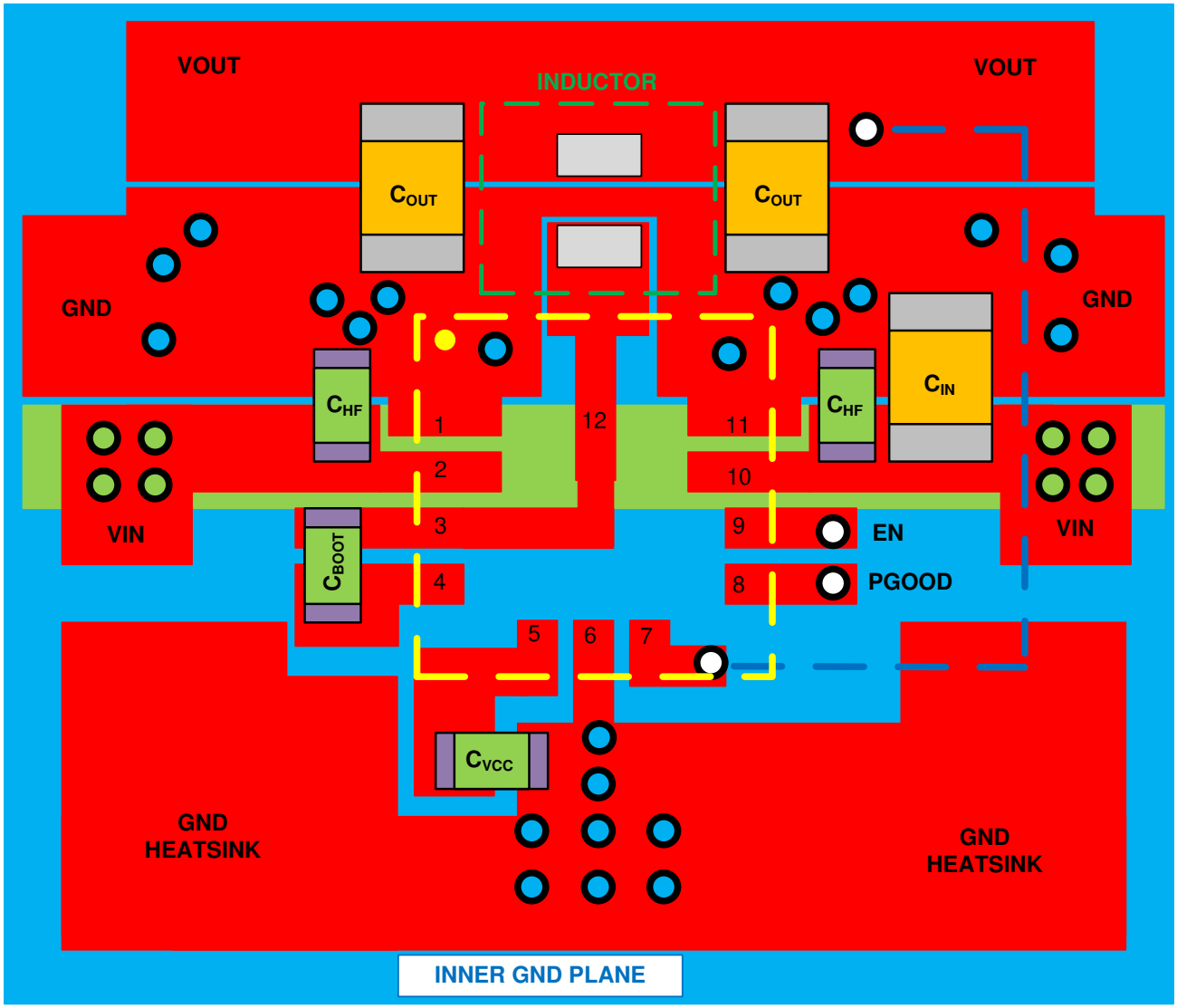


图 39. Example Layout

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12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

- *适用于现场变送器的两级电源参考设计*
- *适用于空间受限的工业传感器的宽输入电压电源参考设计*
- 针对解决方案尺寸和低噪声进行了优化的汽车 ADAS 摄像头电源参考设计
- *直流/直流转换器封装和引脚排列设计如何提高汽车 EMI 性能*
- *降压转换器简介 特性：UVLO，启用，软启动，电源正常*
- *降压转换器简介：了解模式转换*
- *降压转换器简介：最小导通时间和最小关闭时间运行*
- *降压转换器简介：了解静态电流规格*
- *直流/直流转换器的热性能与小解决方案尺寸之间的折衷*
- *利用 HotRod 封装降低 EMI 并减小解决方案尺寸*

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《设计高性能、低 EMI 的汽车电源》* 应用报告
- 德州仪器 (TI)，*《Simple Switcher PCB 布局指南》* 应用报告
- 德州仪器 (TI)，*《构建电源 - 布局注意事项》* 应用报告
- 德州仪器 (TI)，*《使用 LM4360x 与 LM4600x 简化低辐射 EMI 布局》* 应用报告
- 德州仪器 (TI)，*《半导体和 IC 封装热指标》* 应用报告
- 德州仪器 (TI)，*《通过 LM43603 和 LM43602 简化热设计》* 应用报告

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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12.4 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 商标

Hotrod, HotRod, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR34206FSC3RNXRQ1	ACTIVE	VQFN-HR	RNX	12	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	426FC3	Samples
LMR34206FSC3RNXTQ1	ACTIVE	VQFN-HR	RNX	12	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	426FC3	Samples
LMR34206FSC5RNXRQ1	ACTIVE	VQFN-HR	RNX	12	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	426FC5	Samples
LMR34206FSC5RNXTQ1	ACTIVE	VQFN-HR	RNX	12	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	426FC5	Samples
LMR34206SC3QRNXRQ1	ACTIVE	VQFN-HR	RNX	12	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	426SC3	Samples
LMR34206SC3QRNXTQ1	ACTIVE	VQFN-HR	RNX	12	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	426SC3	Samples
LMR34206SC5QRNXRQ1	ACTIVE	VQFN-HR	RNX	12	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	426SC5	Samples
LMR34206SC5QRNXTQ1	ACTIVE	VQFN-HR	RNX	12	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	426SC5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

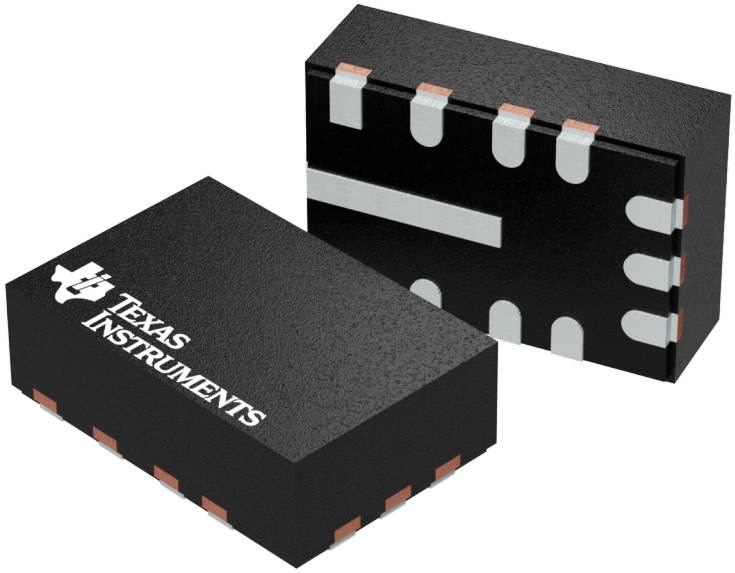
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RNX 12 VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

2 x 3 mm, 0.5 mm pitch



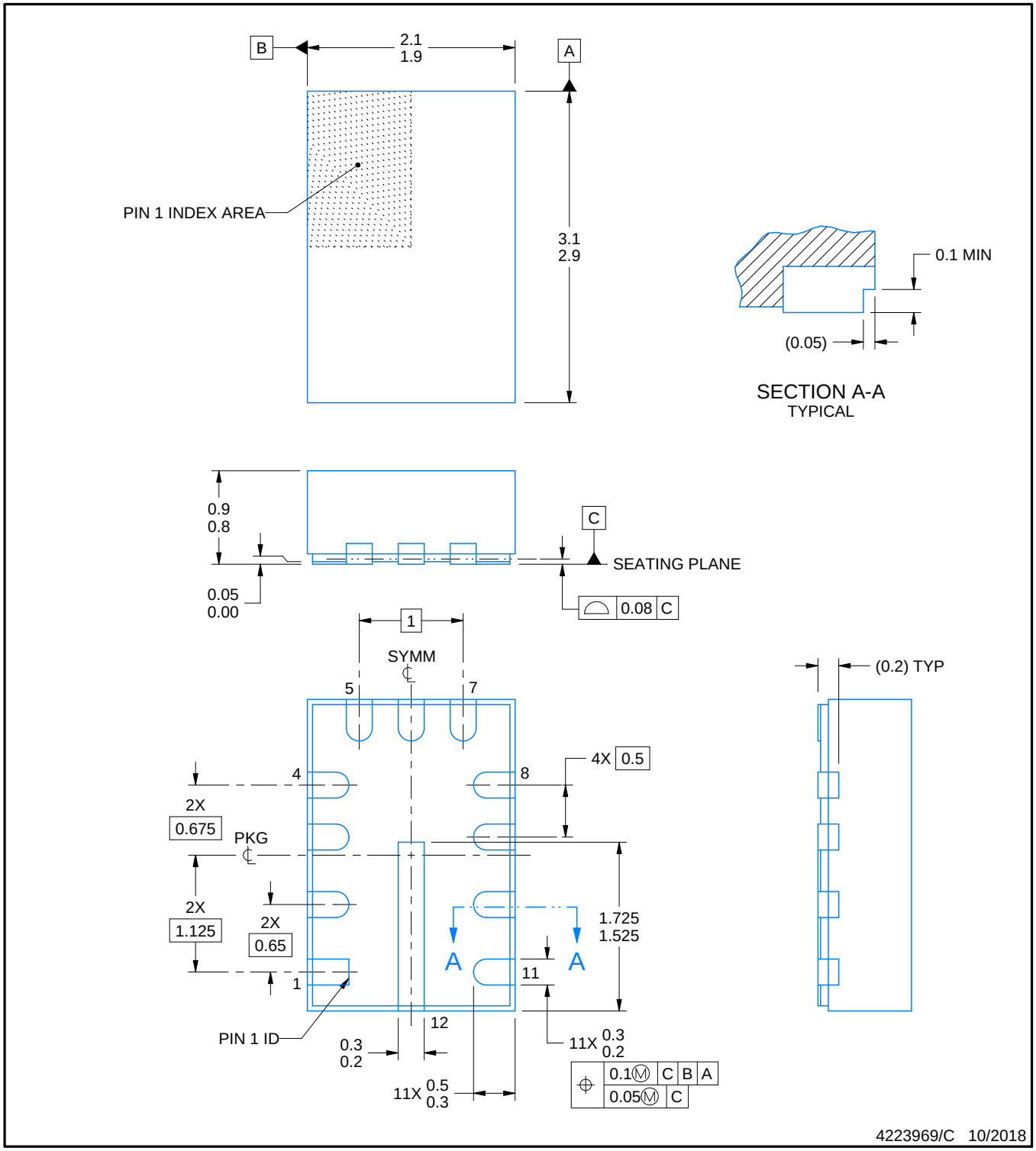
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RNX0012B

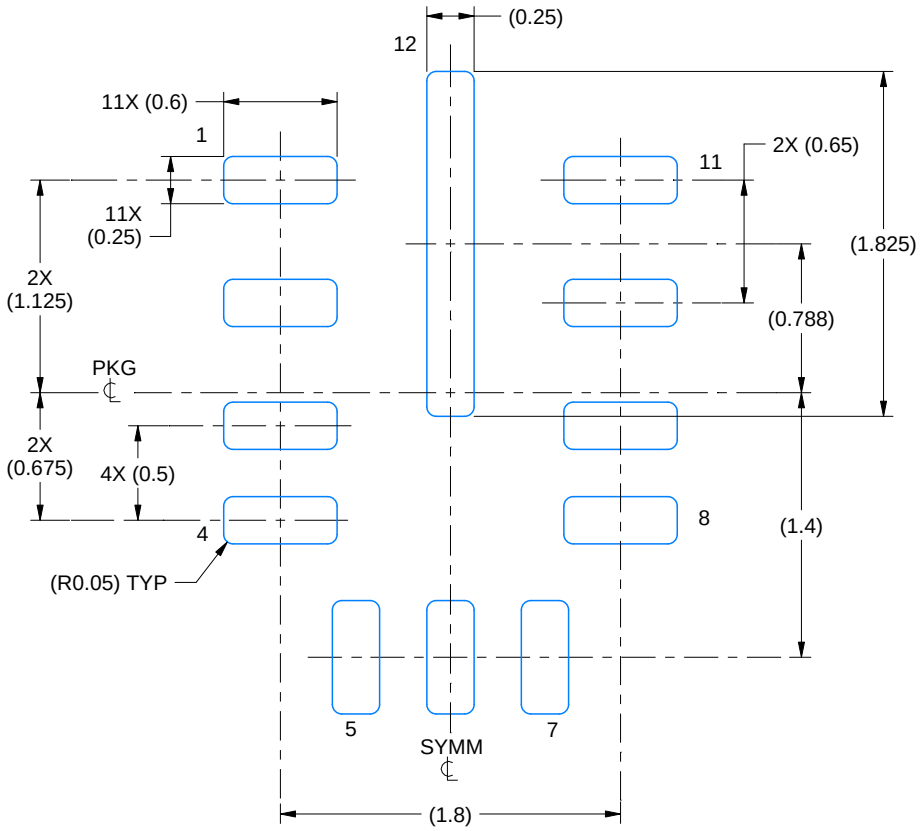
VQFN-HR - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

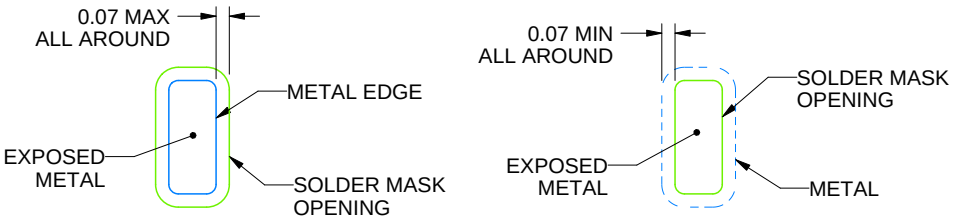


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

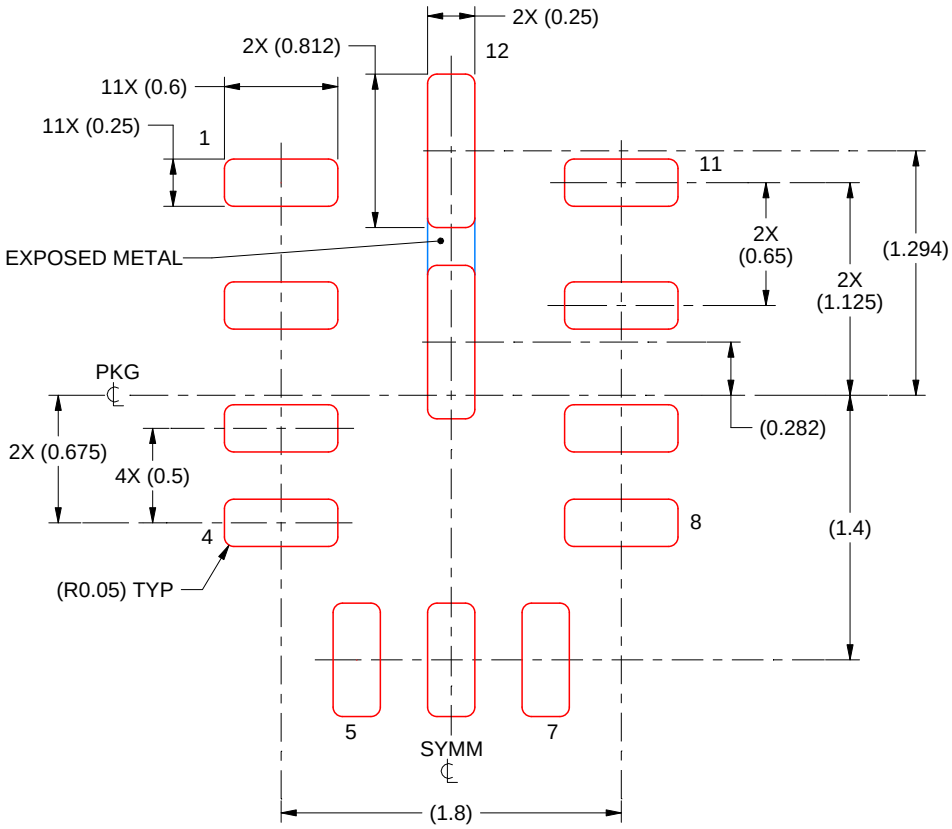


SOLDER MASK DETAILS

4223969/C 10/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



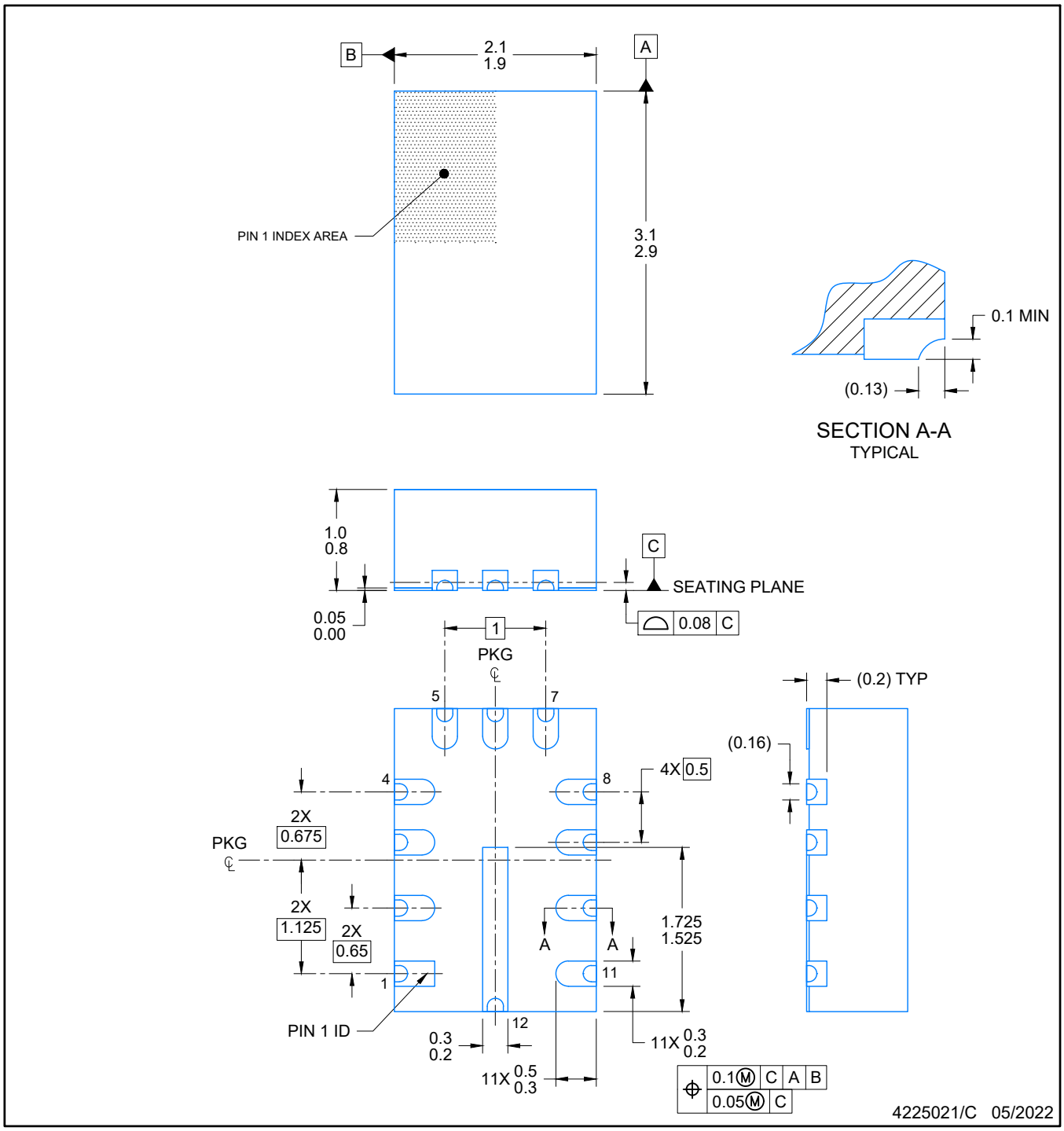
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

FOR PAD 12
87.7% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4223969/C 10/2018

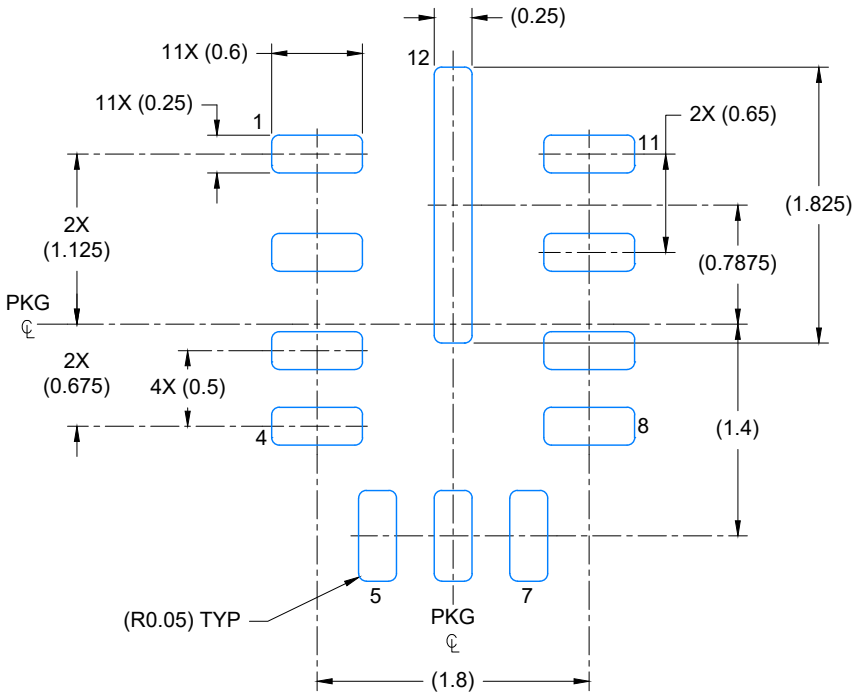
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



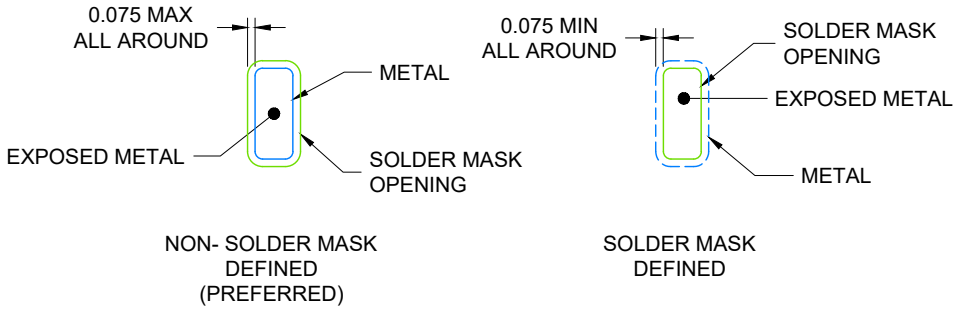
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 20X

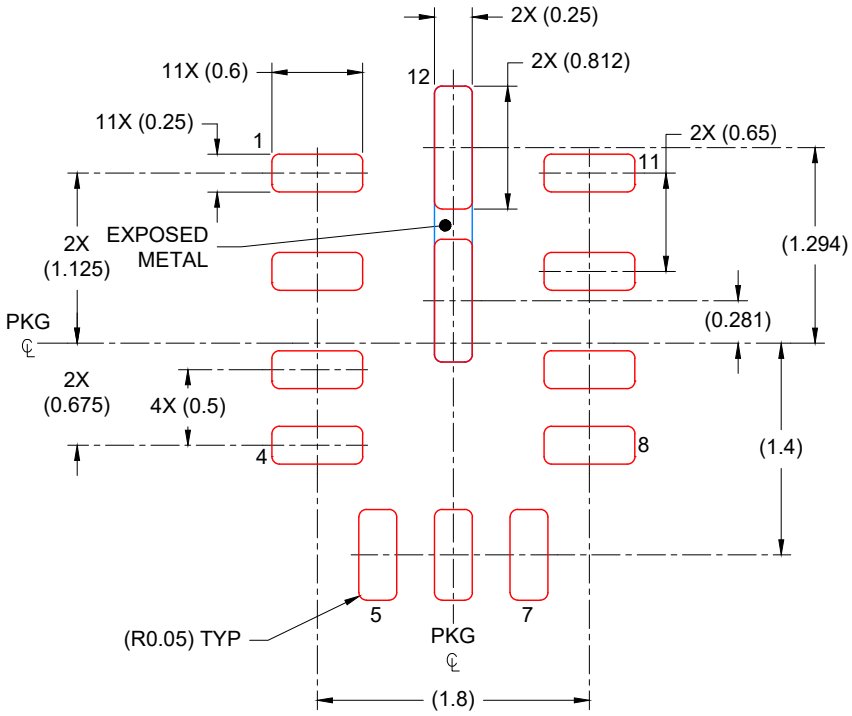


SOLDER MASK DETAILS

4225021/C 05/2022

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL

FOR PAD 12
87.7% PRINTED COVERAGE BY AREA
SCALE: 20X

4225021/C 05/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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