DATA SHEET

# GPF32512A

## 32-Channel MIDI Synthesizer with 512K x 16 ROM

NOV. 15, 2006

Version 1.1

# Table of Contents

**PAGE**

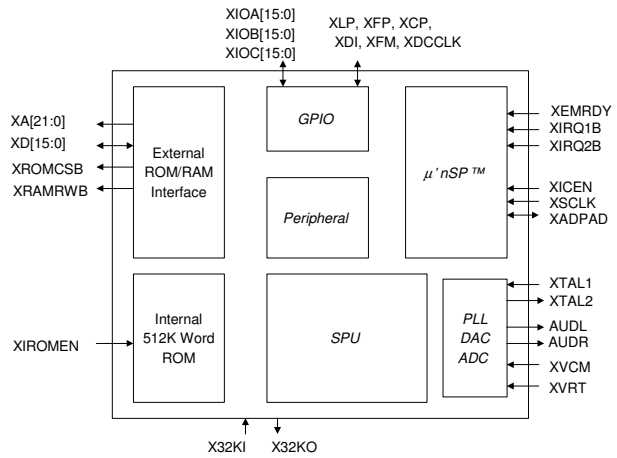
# 32-CHANNEL MIDI SYNTHESIZER WITH 512K x 16 ROM

## 1.GENERAL DESCRIPTION

GPF32512A, a single-chip integrating multi-processors, equips *μ'nSP®* (16-bit CPU developed by SUNPLUS Technology) and 32-channel Sound Processor Unit (SPU) for electronic pianos, portable Karaoke or other similar products. With the 16-bit CPU running up to 54MHz, most of the voice compression algorithms can be utilized with MIDI synthesizer applications simultaneously. In addition, it supports the interface with single color LCD panel up to 1024 x 256 dots and standard MIDI interface. Furthermore, it has up to 48 programmable I/Os and 8M bits ROM for electronic instrument applications. Its low power consumption offers the potentials to be used in battery-powered products.

The GPF32512A provides not only the high-speed performance and high quality of 32 channels synthesizer, but it also integrates several powerful tools into the development system, such as development system with C language, assembly compiler, linker, source debugger functions and project management tools.

## 2.BLOCK DIAGRAM




## 3.FEATURES

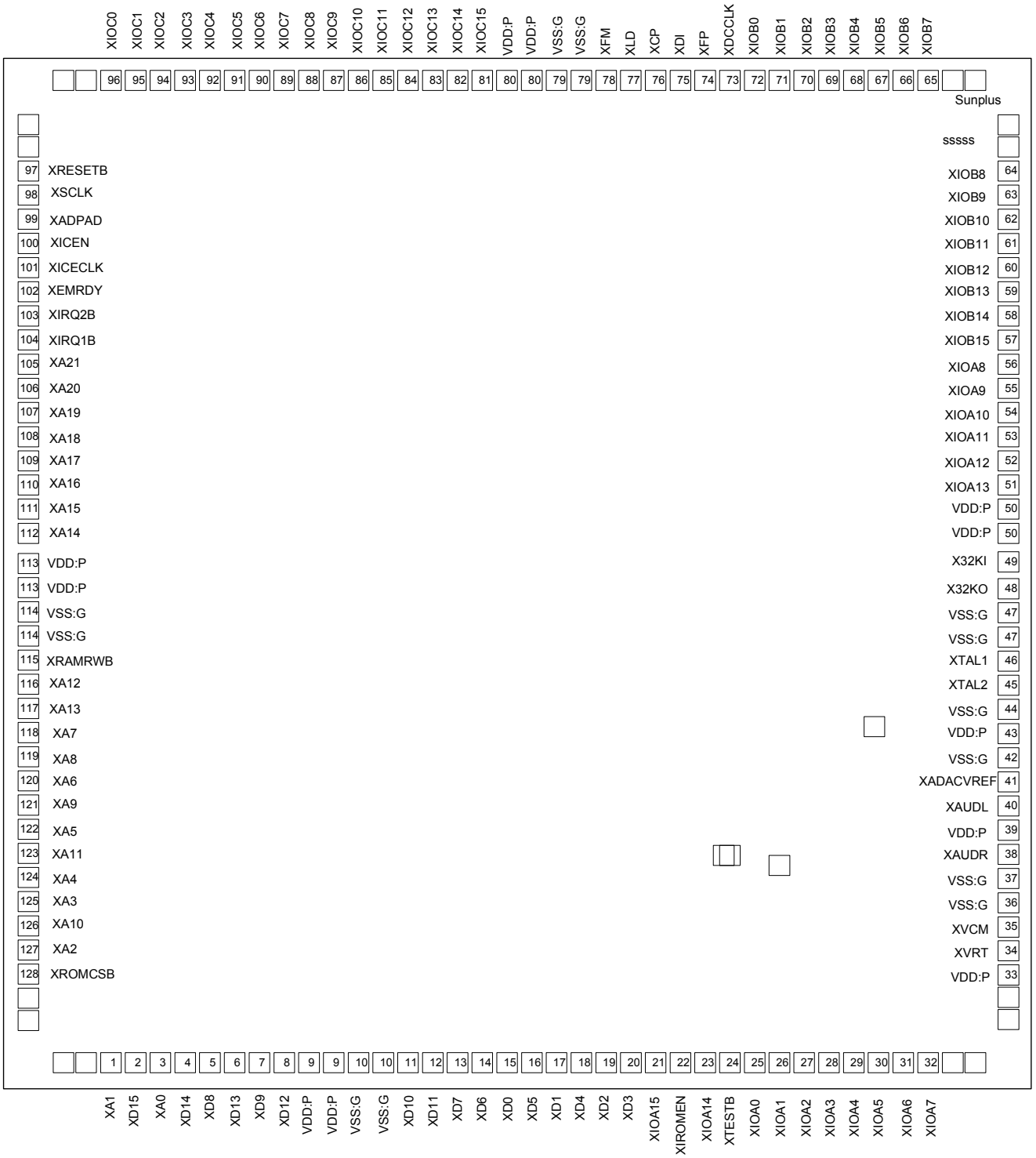
- *μ'nSP®* 16-bit CPU
- Equips 32-channel Sound Processor Unit (SPU) for MIDI synthesis applications
- 8M bits ROM for both programs and sound fonts (tone colors)
- 2048 words working RAM for programming or delay buffers
- Single color LCD interface up to 1024 x 256 dots
- 16-bit stereo DAC
- ADPCM sound fonts real-time decoding logic for each channel
- 7-bit Master volume control
- Max. 256 piece-wise slopes with repetition for envelope control
- Variable sampling rates play back for sound fonts (tone colors) wave table samples
- Beat event IRQ and Envelope IRQ for MIDI event control
- Unlimited wave table sample sizes
- Channel release control logic
- Built-in PLL to generate 54MHz internal clock with external 6.0MHz crystal
- 32768Hz real time counter
- Two 16-bit timers/counters (Programmable and Auto Reload)
- 48 general I/Os can be programmed bit by bit
- 14 interrupt sources: SPU, PPU, Timer, Timebase, External Input, Key wakeup, etc.
- Key wakeup capability
- 8 independent channels AD converters with 9-bit resolution
- UART (MIDI) Interface
- Built-in watchdog function
- SPI master interface

## 4.SIGNAL DESCRIPTIONS

| Mnemonic | PIN No. | Type | Description |
|---|---|---|---|
| DVDD | 9, 50, 80, 113 | P | Digital Power input |
| DVSS | 10, 47, 79, 114 | P | Digital Ground pin |
| AVDD1 | 33 | P | Analog power input 1 |
| AVSS1 | 36, 37 | P | Analog ground pin 1 |
| AVDD2 | 39 | P | Analog power input 2 |
| AVSS2 | 42 | P | Analog ground pin 2 |
| AVDD3 | 43 | P | Analog power input 3 |
| AVSS3 | 44 | P | Analog ground pin 3 |
| XA[21:0] | 105 - 112<br>116 - 127<br>1, 3 | I | External ROM/RAM address bus |
| XD[15:0] | 2<br>4 - 8<br>11 - 20 | I/O | External ROM/RAM data bus |
| XRAMRWB | 115 | O | External RAM write enable (Low active) |
| XROMCSB | 127 | O | External ROM/RAM chip select (Low active) |
| XIRQ1B | 104 | I | External IRQ 1 |
| XIRQ2B | 103 | I | External IRQ 2 |
| XEMRDY | 102 | I | External memory ready |
| XICEN | 100 | I | Internal ICE enable |
| XSCLK | 98 | I | ICE interface clock |
| XADPAD | 99 | I/O | ICE data bus |
| XRESETB | 97 | I | System reset (Low active) |
| XICECLK | 101 | O | System Clock output |
| XIOA[15:0] | 21, 23<br>25 - 32<br>51 - 56 | I/O | GPIO A, Bit 0-7 could be used as ADC input |
| XIOB[15:0] | 57 - 64<br>65 - 72 | I/O | GPIO B |
| XIOC[15:0] | 81 - 96 | I/O | GPIO C |
| XFP | 74 | I/O | LCD interface frame pulse, GPIO D0 |
| XLD | 77 | I/O | LCD interface latch data pulse, GPIO D1 |
| XCP | 76 | I/O | LCD interface clock signal, GPIO D2 |
| XDI | 75 | I/O | LCD interface data signal, GPIO D3 |
| XFM | 78 | I/O | LCD interface frame signal, GPIO D4 |
| XDCCLK | 73 | I/O | LCD interface DC-DC clock signal, GPIO D5 |
| XTAL1 | 46 | I | External crystal input, should be 6MHz |
| XTAL2 | 45 | O | External crystal output |
| X32KI | 49 | I | External 32768Hz crystal input |
| X32KO | 48 | O | External 32768Hz crystal output |
| XAUDL | 40 | O | Audio left channel output |
| XAUDR | 38 | O | Audio right channel output |
| XADACVREF | 41 | I | Audio DAC reference voltage |
| XVCM | 35 | O | ADC reference voltage output |

| Mnemonic | PIN No. | Type | Description |
|---|---|---|---|
| XVRT | 34 | I | ADC reference voltage input |
| XTESTB | 24 | I | Test enable, NC |
| XIROMEN | 22 | I | Internal 512K words ROM enable |

### 4.1. PIN Map



| Name | Side | Pin-Number | Name | Side | Pin-Number |
|---|---|---|---|---|---|
| XA1 | B | 1 | XADACVREF | R | 41 |
| XD15 | B | 2 | VSS:G | R | 42 |
| XA0 | B | 3 | VDD:P | B | 43 |
| XD14 | B | 4 | VSS:G | R | 44 |
| XD8 | B | 5 | XTAL2 | R | 45 |
| XD13 | B | 6 | XTAL1 | R | 46 |
| XD9 | B | 7 | VSS:G | R | 47 |
| XD12 | B | 8 | VSS:G | R | 47 |
| VDD:P | B | 9 | X32KO | R | 48 |
| VDD:P | B | 9 | X32KI | R | 49 |
| VSS:G | B | 10 | VDD:P | R | 50 |
| VSS:G | B | 10 | VDD:P | R | 50 |
| XD10 | B | 11 | XIOA13 | R | 51 |
| XD11 | B | 12 | XIOA12 | R | 52 |
| XD7 | B | 13 | XIOA11 | R | 53 |
| XD6 | B | 14 | XIOA10 | R | 54 |
| XD0 | B | 15 | XIOA9 | R | 55 |
| XD5 | B | 16 | XIOA8 | R | 56 |
| XD1 | B | 17 | XIOB15 | R | 57 |
| XD4 | B | 18 | XIOB14 | R | 58 |
| XD2 | B | 19 | XIOB13 | R | 59 |
| XD3 | B | 20 | XIOB12 | R | 60 |
| XIOA15 | B | 21 | XIOB11 | R | 61 |
| XIROMEN | B | 22 | XIOB10 | R | 62 |
| XIOA14 | B | 23 | XIOB9 | R | 63 |
| XTESTB | B | 24 | XIOB8 | R | 64 |
| XIOA0 | B | 25 | NC | R | 0 |
| XIOA1 | B | 26 | NC | R | 0 |
| XIOA2 | B | 27 | NC | T | 0 |
| XIOA3 | B | 28 | NC | T | 0 |
| XIOA4 | B | 29 | XIOB7 | T | 65 |
| XIOA5 | B | 30 | XIOB6 | T | 66 |
| XIOA6 | B | 31 | XIOB5 | T | 67 |
| XIOA7 | B | 32 | XIOB4 | T | 68 |
| NC | B | | XIOB3 | T | 69 |
| NC | B | | XIOB2 | T | 70 |
| NC | R | | XIOB1 | T | 71 |
| NC | R | | XIOB0 | T | 72 |
| VDD:P | R | 33 | XDCCLK | T | 73 |
| XVRT | R | 34 | XFP | T | 74 |
| XVCM | R | 35 | XDI | T | 75 |
| VSS:G | R | 36 | XCP | T | 76 |
| VSS:G | R | 37 | XLD | T | 77 |
| XAUDR | R | 38 | XFM | T | 78 |
| VDD:P | R | 39 | VSS:G | T | 79 |
| XAUDL | R | 40 | VSS:G | T | 79 |

| Name | Side | Pin-Number | Name | Side | Pin-Number |
|---|---|---|---|---|---|
| VDD:P | T | 80 | XA20 | L | 106 |
| VDD:P | T | 80 | XA19 | L | 107 |
| XIOC15 | T | 81 | XA18 | L | 108 |
| XIOC13 | T | 83 | XA17 | L | 109 |
| XIOC12 | T | 84 | XA16 | L | 110 |
| XIOC11 | T | 85 | XA15 | L | 111 |
| XIOC10 | T | 86 | XA14 | L | 112 |
| XIOC9 | T | 87 | VDD:P | L | 113 |
| XIOC8 | T | 88 | VDD:P | L | 113 |
| XIOC7 | T | 89 | VSS:G | L | 114 |
| XIOC6 | T | 90 | VSS:G | L | 114 |
| XIOC5 | T | 91 | XRAMRWB | L | 115 |
| XIOC4 | T | 92 | XA12 | L | 116 |
| XIOC3 | T | 93 | XA13 | L | 117 |
| XIOC2 | T | 94 | XA7 | L | 118 |
| XIOC1 | T | 95 | XA8 | L | 119 |
| XIOC0 | T | 96 | XA6 | L | 120 |
| NC | T | 0 | XA9 | L | 121 |
| NC | T | 0 | XA5 | L | 122 |
| NC | L | 0 | XA11 | L | 123 |
| NC | L | 0 | XA4 | L | 124 |
| XRESETB | L | 97 | XA3 | L | 125 |
| XSCLK | L | 98 | XA10 | L | 126 |
| XADPAD | L | 99 | XA2 | L | 127 |
| XICEN | L | 100 | XROMCSB | L | 128 |
| XICECLK | L | 101 | NC | L | 0 |
| XEMRDY | L | 102 | NC | L | 0 |
| XIRQ2B | L | 103 | NC | B | 0 |
| XIRQ1B | L | 104 | NC | B | 0 |
| XA21 | L | 105 | | | |

# 5.FUNCTIONAL DESCRIPTIONS

## 5.1. CPU

The GPF32512A is equipped with a 16-bit *μ'nSP™*, the newest 16-bit microprocessor by SUNPLUS and pronounced as *micro-n-SP*. Eight registers are involved in *μ'nSP™:* R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP) and SR (Segment Register). The interrupt include three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK.
Moreover, a high performance hardware multiplier with the Capability of FIR filter is also built in to reduce the software multiplicaton loading.

## 5.2. Memory

### 5.2.1. SRAM

The amount of SRAM is 2K-word (including Stack), ranged from $0000 through $07FF with access speed of two CPU clock cycles.

## 5.3. ROM memory

ROM memory ($004000 ~ $043FFF) is a high-speed memory with access speed of four CPU clock cycles. The address from $080000 to $3FFFFF can be used as external memory space for extension.

## 5.4. PLL, Clock, Power Mode

### 5.4.1. PLL (Phase Lock Loop)

The purpose of PLL is to provide a base frequency (6Mhz) and to pump the frequency 54MHz for system clock ($F_{OSC}$).

### 5.4.2. System clock

Basically, the system clock is provided 54Mhz by PLL and programmed by the P_WaitState_num_Ctrl (W) to determine two~six wait-state cycles to access ROM.

## 5.5. Power Savings Mode

The GPF32512A also offers a power savings mode (standby mode) for low power application needs. To enter standby mode, the desired key wakeup port (IOA [15:0], IOB [15:0], IOC [15:0]) must be configured to input first. And read the Port Latch REG to latch the GPIO state before entering the standby mode. Also remember to enable the corresponding interrupt source(s) for wakeup. After that, stop the CPU clock by writing the STOP CLOCK Register P_Sleep_Mode (W) to enter standby mode. In such mode, SRAM and I/Os remain in the previous states till CPU being awoken.

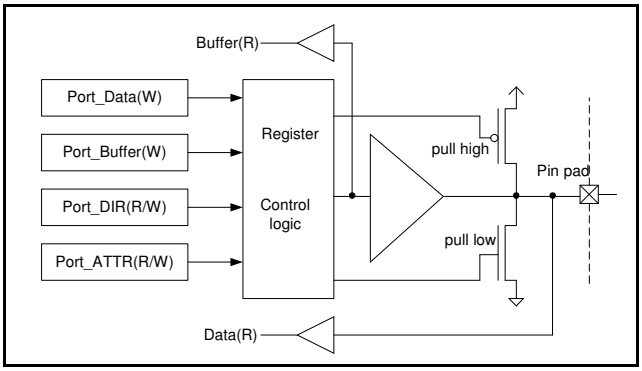
## 5.6. Interrupt

The GPF32512A has 14 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt while IRQ is the low-priority one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources.

| Interrupt Source | Interrupt Name | Priority |
|---|---|---|
| SPU Channel | FIQ / IRQ1 | High(FIQ) |
| Timer A | FIQ_TMA/ IRQ2_TMA | High(FIQ) |
| Timer B | FIQ_TMB/ IRQ2_TMB | High(FIQ) |
| UART, SPI, ADC | IRQ3 | Low |
| SPU Beat, Envelope | IRQ4 | Low |
| EXT2 | IRQ5_EXT2 | Low |
| EXT1 | IRQ5_EXT1 | Low |
| 4096Hz | IRQ6_4KHz | Low |
| 2048Hz | IRQ6_2KHZ | Low |
| 1024Hz | IRQ6_1KHz | Low |
| 4Hz | IRQ7_4Hz | Low |
| Time-base 1 | IRQ7_TMB1 | Low |
| Time-base 2 | IRQ7_TMB2 | Low |
| Key change wakeup | IRQ7_KEY | Low |

## 5.7. I/O

Two I/O ports are built in GPF32512A, PortA, PortB and PorC. The PortA, B, C is an ordinary I/O with programmable wakeup capability. In addition to the regular IO function, the PortB can also perform some special functions in certain pins.
The following diagram is an I/O schematic.



Although data can be written into the same register through Port_Data and Port_Buffer, they can be read from different places, Buffer (R) and Data (R). The GPIO is the key wakeup port. To activate key wakeup function, latch data on PORT Latch and enable the key wakeup function. Wakeup is triggered when the GPIO state is different from at the time latched. In addition to an ordinary I/O port, PortB carries some special functions. A summary of PortB special functions is listed as follows:

**Special function in PortB**

| PortB | Special Function | Function Description | Note |
|---|---|---|---|
| IOB2 | TMB2 | Timebase output 2 | Output |
| IOB3 | TMB1 | Timebase output 1 | Output |
| IOB4 | TBPWM | TimeB, Pulse Width Modulation | Output |
| IOB5 | TAPWM | TimeA, Pulse Width Modulation | Output |
| IOB6 | Ext1 | External clock source of timer | Input |
| IOB7 | Ext2 | Extternal clock source of timer | Input |

Default state: Pull Low

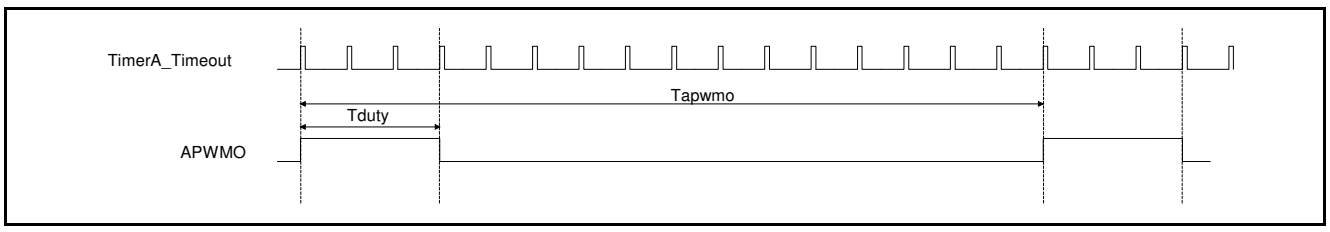
### 5.8. Timer / Counter

The GPF32512A provides two 16-bit timers/counters, TimerA and TimerB. The TimerA is called a universal counter. TimerB is a general-purpose counter. The clock source of TimerA comes from the combination of clock source A and clock source B. In TimerB, the clock source is given from source C. When timer overflows, an INT signal is sent to CPU to generate a time-out signal.

| Clock of Source A | Clock of Source B | Clock of Source C |
|---|---|---|
| Fosc/2 | 2048Hz | Fosc/2 |
| -- | 1024Hz | -- |
| 32768Hz | 256Hz | 32768Hz |
| 8192Hz | TMB1 | 8192Hz |
| 4096Hz | 4Hz | 4096Hz |
| 1 | 2Hz | 1 |
| 0 | 1 | 0 |
| EXT1 | EXT2 | EXT1 |

Initially, write a value of N into a timer and select a desired clock source, timer will start counting from N, N+1, N+2 ... through FFFF. An INT (TimerA/TimerB) signal is generated at the next clock after reaching “FFFF” and the INT signal is transmitted to INT controller for further processing. At the same time, N will be reloaded into timer and start all over again. The clock source A is a high frequency source and clock source B is a low frequency source. The combination of clock source A and B provides a variety of speeds to TimerA. A “1” represents pass signal and not gating. In contrast, “0” indicates deactivating timer. The EXT1 and EXT2 are the external clock sources. Moreover, counter can generate time-out signal for input clock source to a four bits (16 levels) PWM pulse width counter. A variety of clock duration can be generated and exported from IOB5 (APWMO) and IOB4 (BPWMO).

The following example is a 3/16-duration cycle. The APWMO waveform is made by selecting a pulse width through Port_TimerA_Ctrl (W) [9:6]. As a result, each 16 cycles will generate a pulse width defined in control port. These PWM signals can be applied for controlling the speed of motor or other devices.



Generally speaking, the clock source A and C are fast clock sources and source B comes from RTC system (32768Hz). Therefore, clock source B can be utilized as a precise counter for time counting, e.g., the 4Hz clock can be used for real time counting.

### 5.8.1. Timebase

Timebase, generated by 32768Hz, is a combination of frequency selections. The outputs of timebase block are named to TMB1 and TMB2. TMB1 is frequency for TimerA (Clock source B). The TMB1 and TMB2 are the sources for Interrupt (IRQ7). Furthermore, timebases generates additional 4Hz to 4096Hz interrupt sources (IRQ6 and IRQ7) for Real-Time-Clock (RTC).

| TMB2 | TMB1 |
|---|---|
| 128Hz | 8Hz |
| 256Hz | 16Hz |
| 512Hz | 32Hz |
| 1024Hz | 64Hz |
| Default: 128Hz | Default: 8Hz |

## 5.9. Sleep, Wakeup and Watchdog

### 5.9.1. Wakeup and sleep

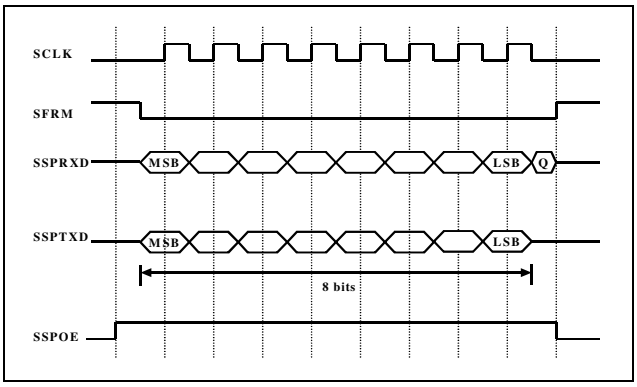
1) Sleep: After power-on reset, IC starts running until a sleep command occurs. When a sleep command is accepted, IC will turn the system clock (PLL) off. After all, it enters sleep mode.
2) Wakeup: CPU waking up from sleep mode requires a wakeup signal to turn the system clock (PLL) on. The IRQ signal makes CPU to complete the wakeup process and initialization.

### 5.9.2. Watchdog

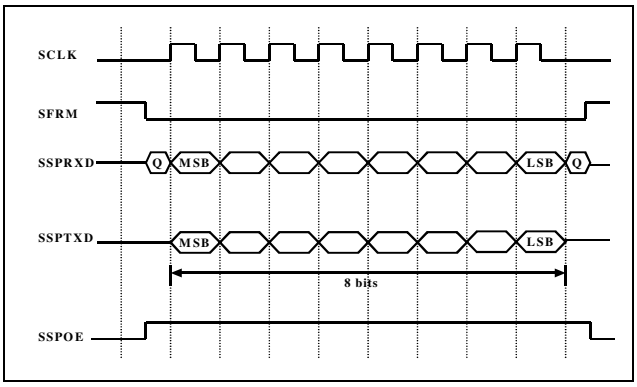
The purpose of watchdog is to monitor if the system operates normally. Within a certain period, watchdog must be cleared. If watchdog is not cleared, CPU assumes the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again. In GPF32512A, the clear period is 0.75 seconds. If watchdog is cleared within each 0.75 seconds, the system will not be reset. The watchdog function remains enabled during standby mode if the 32768Hz.

## 5.10. Serial Peripheral Interface (SPI)

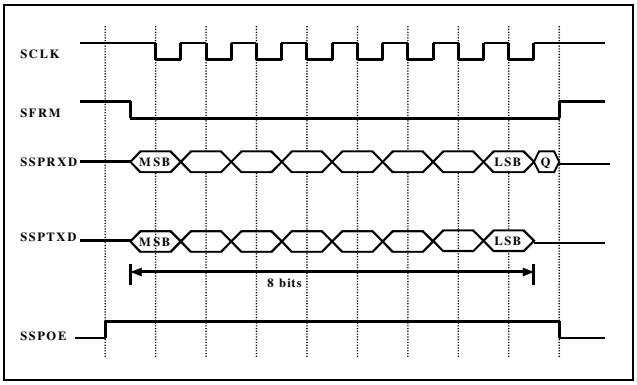
The SPI interface is a master-only interface that enables synchronous serial communication with slave peripherals.



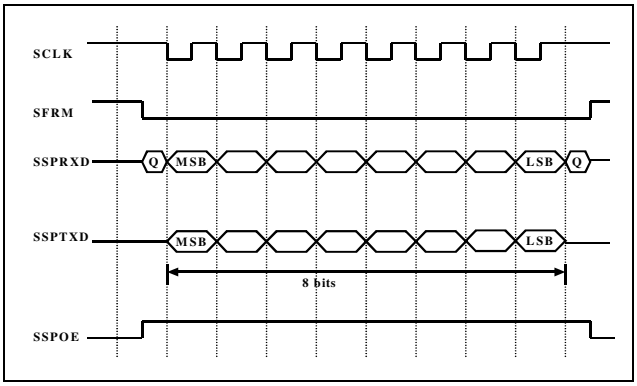

Single transfer Data Change at Falling, Latch at Rising.




Continuous transfer




Single transfer




Continuous transfer

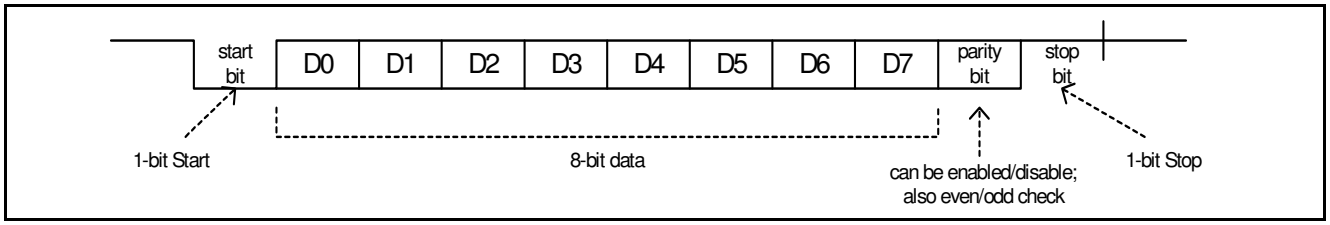
### 5.11. IDE Tools Function

The functions of IDE include the follows:

1). C compiler, Assembly, and Linker.
2). Single step trace
3). Break point (break point for debugging)
4). Run (execute)

### 5.12. UART Function

UART block provides a full-duplex standard interface that facilitates the communication with other devices. With this interface, GPF32512A can transmit and receive simultaneously. The maximum baud-rate can be up to 115200bps. The Rx and Tx of UART are shared with IOA14 and IOA15.



## 6.ELECTRICAL SPECIFICATIONS

### 6.1. Absolute Maximum Rating

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | VDD | 0 to 3.6 | V |
| Input Voltage | $V_{IN}$ | -0.3 to VDD +0.3 | V |
| Operating Temperature | $T_A$ | 0 to 85 | ℃ |
| Storage Temperature | $T_{STG}$ | -55 to +125 | ℃ |

### 6.2. DC Characteristics

| Characteristic | Symbol | Limits | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operating Voltage | VDD | 3.0 | 3.3 | 3.6 | V | @ 54MHz |
| Operating Current | $I_{OP}$ | 63.563 | 72.750 | 81.170 | mA | @ 54MHz with IROMON |
| Power Down Current | $I_{STBY}$ | -30 | - | 30.0 | μA | Sleep Mode |
| High Input Voltage | $V_{IH}$ | 0.7VDD | - | VDD | V | |
| Low Input Voltage | $V_{IL}$ | VSS | - | 0.8 | V | |
| Crystal Frequency | $F_{CRYSTAL}$ | - | - | 6.0 | MHz | |
| System Clock | $F_{SYS}$ | 27 (Note 1) | 54 | 54 | MHz | |

**Note 1:** By setting internal register.

### 6.3. DAC Characteristics

| Characteristic | Limits | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Resolution | - | 16 | - | Bit | |
| Full Scale Output Voltage | - | 1.2 | - | Vp-p | |
| THD+N (f = 1kHz) | - | 0.094 | - | % | |
| Noise at No Signal | - | -102 | -98 | dBv | |
| Frequency Response (f = 50Hz to 20 kHz) | -0.04 | - | 0.01 | dB | |

### 6.4. ADC Characteristics (VDD = 3.3V, $T_A$ = 25℃)

| Characteristics | Symbol | Unit | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| ADC Power Dissipation | IADC | - | 1.8 | - | mA |
| ADC Input Voltage Range | VINL (Note 1) | VSS-0.3 | - | VDD+0.3 | V |
| Resolution of ADC | RESO | - | - | 10 | bits |
| Signal-to-Noise Plus Distortion of ADC from Line In | SINAD (Note 3) | - | 56 | - | dB |
| Effective Number of Bit | ENOB (Note 4) | 8.0 | 9.0 | - | bits |
| Integral Non-Linearity of ADC | INL | - | ±4.0 | - | LSB (Note 2) |
| Differential Non-Linearity of ADC | DNL (Note 5) | - | ±0.5 | - | LSB |
| AD Conversion Rate | $F_{CONV}$ | Fcpu/2048 | - | Fcpu/256 | Hz |

**Note1:** Internal protection diodes clamp the analog input to VDD and VSS. These diodes allow the analog input to swing from (VSS-0.3V) to (VDD+0.3V) without causing damage to the devices.

**Note2:** LSB means Least Significant Bit. With VINL = 2.0V, 1LSB = 2.0V/2^10 = 1.953mV.

**Note3:** The SINAD testing condition at VINLp-p = 0.8*VDD, $F_{CONV}$ = Fcpu/512 = 54MHz/256 = 211KHz, Fin=1.0KHz Sine waves at VDD = 3.0V from the ADC input.

**Note4:** ENOB = (SINAD-1.76)/6.02.

**Note5:** This ADC can guarantee no missing code.

## 7.RESET AND POWER DOWN

### 7.1. Reset

During power-up, the RESET input should be held low until the crystal oscillator and PLL are stabilized, which can take about 20 ms. A typical RC/diode power-up network can be used.

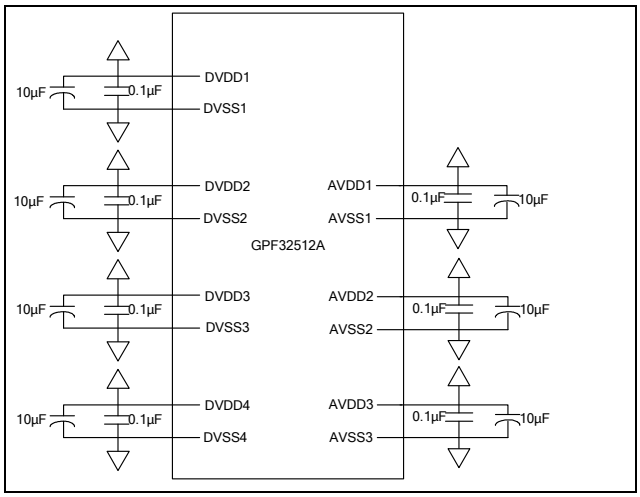
### 7.2. Power Down

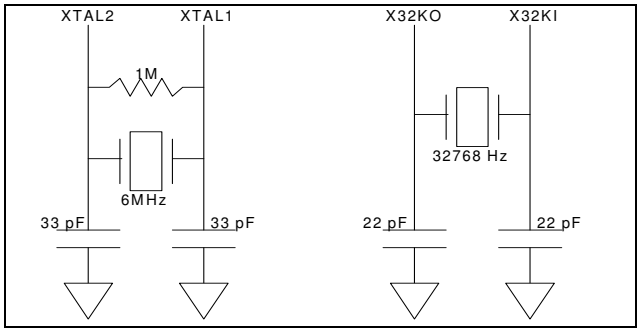
Sleep mode can be entered by write the control register. But system can wake up only when 32768Hz is existed. In order to minimize the power consumption during sleep mode, the program counter should stay in internal SRAM and the pin XIROMEN can be switch to low after sleep.

# 8. RECOMMENDED BOARD LAYOUT

## 8.1. Digital Section

All digital VDD VSS should be connected. The decoupling capacitor of 0.1µF and 10µF should be connected to each power pin of the IC as the following diagram.



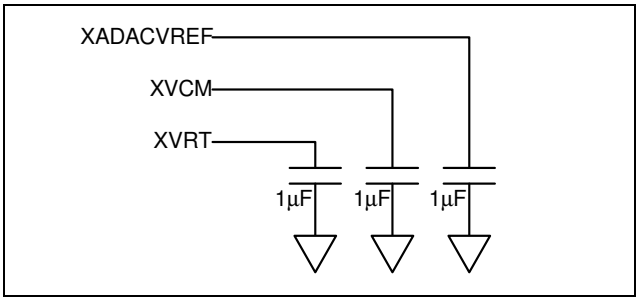

**Note:** These capacitor values are for design guidance only. Different capacitor values may be needed for different crystal used.

## 8.2. Crystal

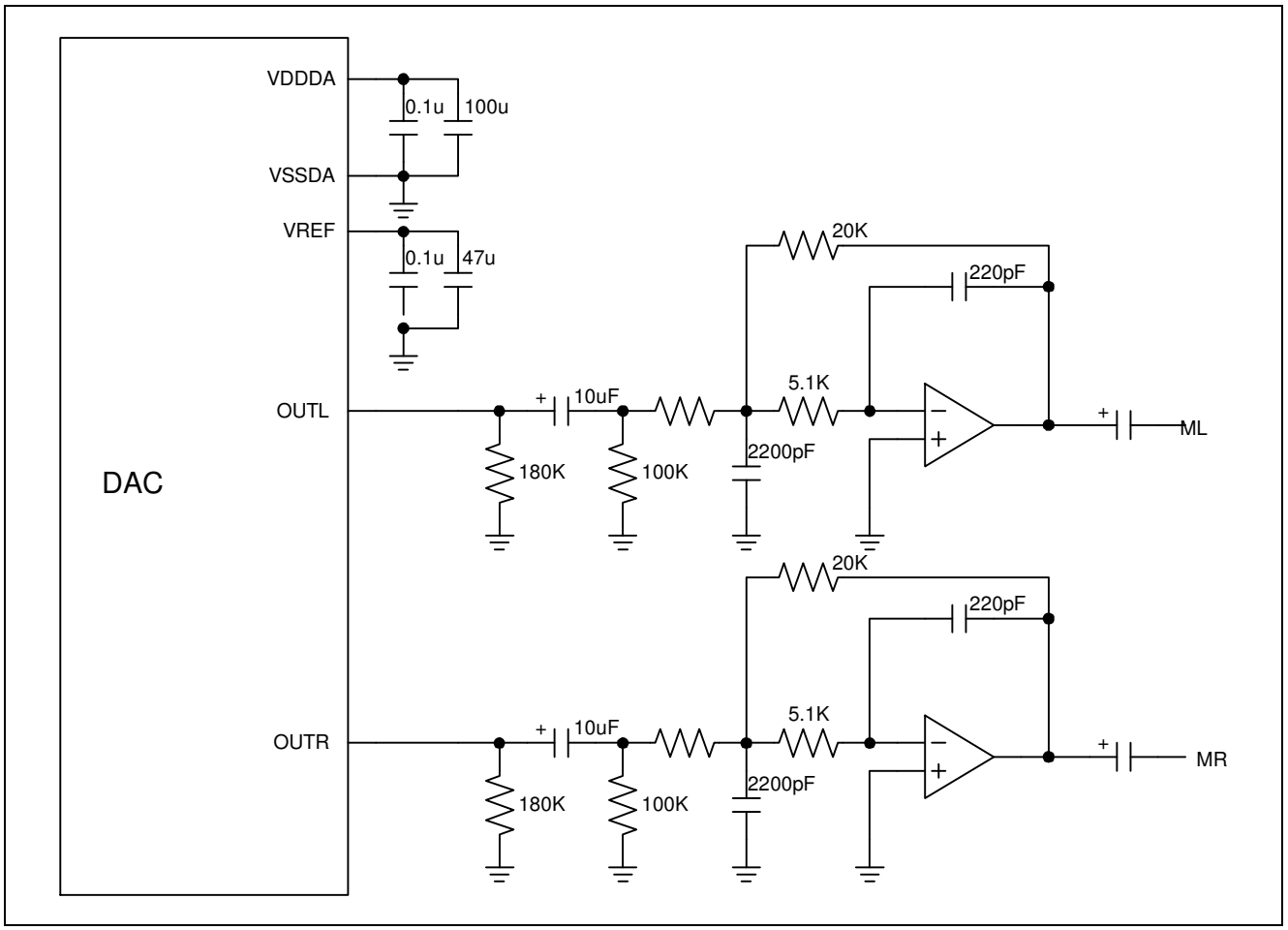
Please refer to following diagram to connect the crystal circuit.

## 8.3. Analog Section

A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. Each of XADACVREF, XVCM, and XVRT should be connected to a 1uF capacitor as the following diagram.



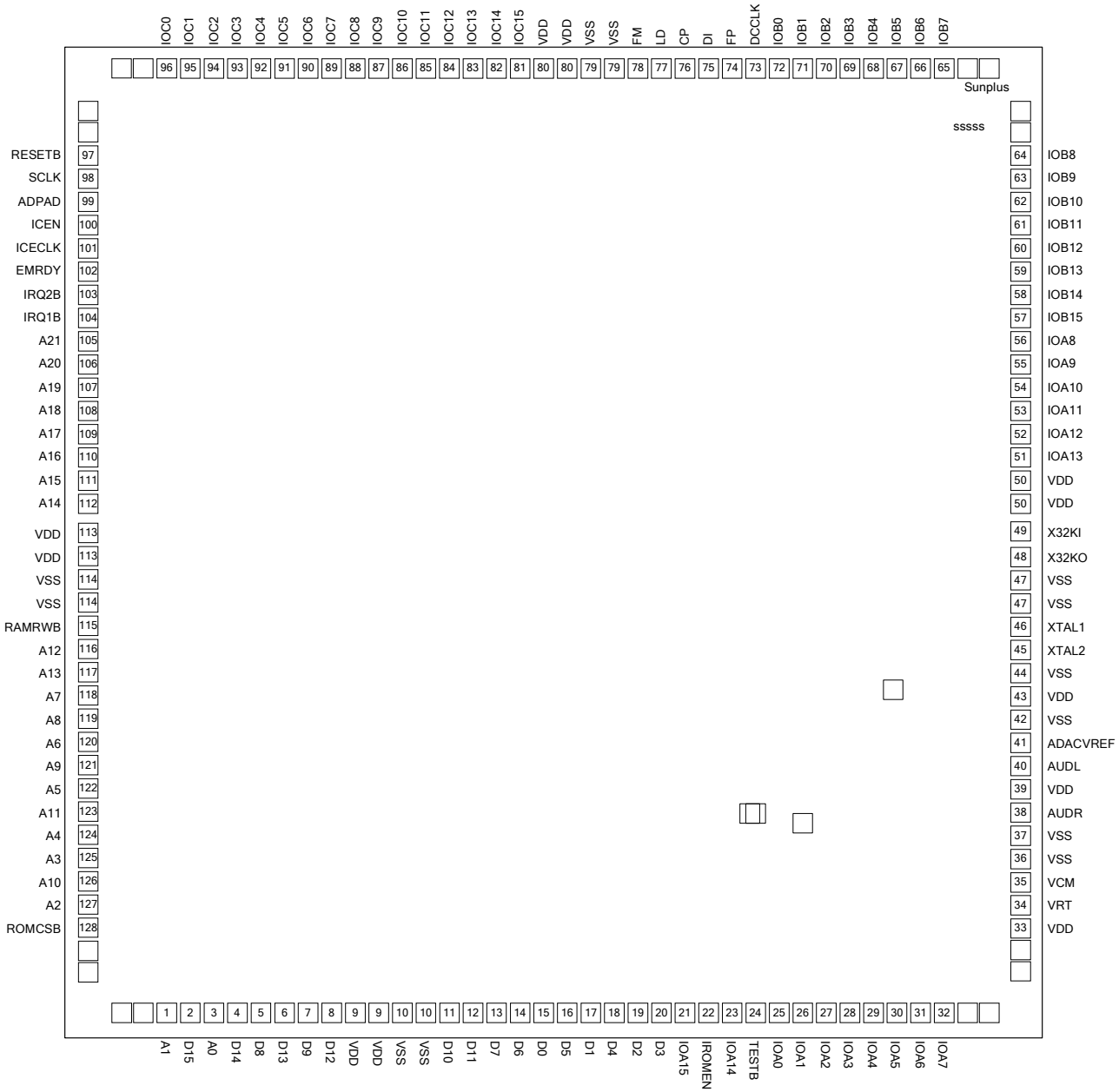
## 9. APPLICATION CIRCUIT




Audio Application Circuit

## 10. PACKAGE/PAD LOCATIONS

### 10.1. PAD Assignment and Locations




This IC substrate should be connected to VSS

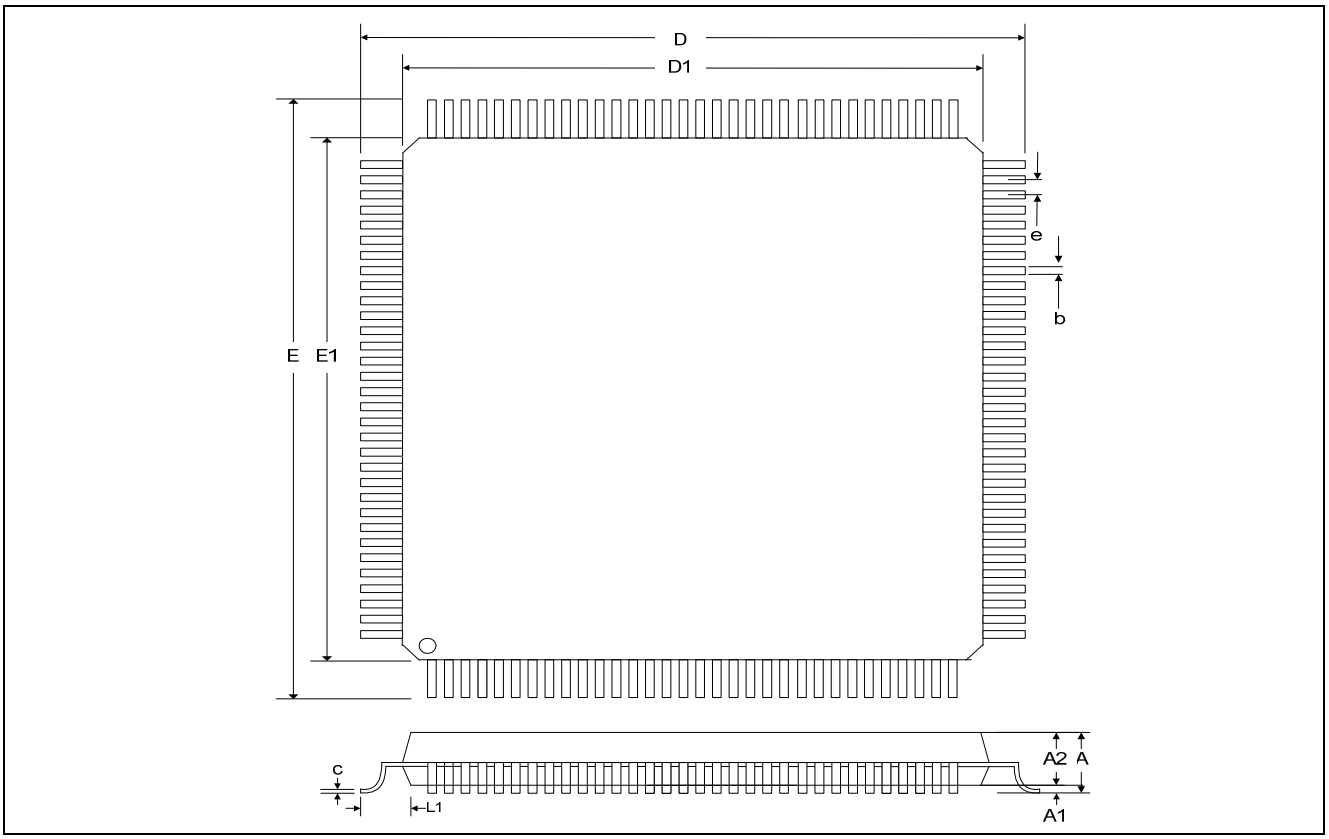
**Note1:** To ensure that the IC functions properly, please bond all of VDD and VSS pins.
**Note2:** The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

### 10.2. Ordering Information

| Product Number | Package Type |
|---|---|
| GPF32512A - NnnV - C | Chip form |
| GPF32512A - NnnV - HL09x | Green Package form - LQFP 128 |

**Note1:** Code number is assigned for customer.
**Note2:** Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).
**Note3:** Package form number (x = 0 - 9, serial number).
**Note4:** Please reference section 10.4 Storage Condition and Period for Package.

### 10.3. Package Information




(Dimension in mm)

| Symbol | Min. | Nom. | Max. |
|---|---|---|---|
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| D | | 16.00 BSC. | |
| D1 | | 14.00 BSC. | |
| E | | 16.00 BSC. | |
| E1 | | 14.00 BSC. | |
| e | | 0.40 BSC. | |
| b | 0.13 | 0.16 | 0.23 |
| c | 0.09 | - | 0.20 |
| L1 | | 1.00 REF | |

### 10.4. Storage Condition and Period for Package

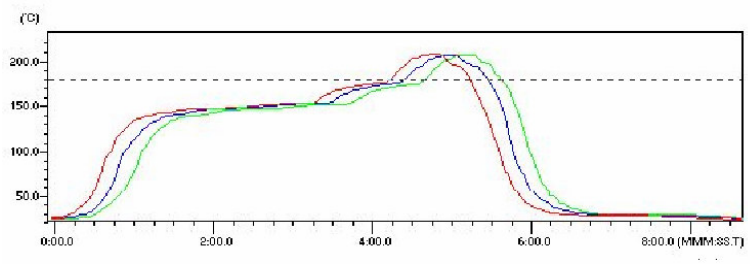
| Package | Moisture sensitivity level | Max. Reflow temperature | Floor life storage condition | Dry pack |
|---|---|---|---|---|
| LQFP | LEVEL 3 | 220 +5/-0℃ | 168Hrs @ ≦30℃/ 60% R.H. | Yes |

**Note1:** Please refer to IPC/JEDEC standard J-STD-020A and EIA JEDEC stand JFSD22-A112.
**Note2:** or refer to the "CAUTION Note" on dry pack bag.

### 10.5. Recommended SMT Temperature Profile

This "Recommended" temperature profile is a rough guideline for SMT process reference. Most of GENERALPLUS leadframe base product choice Matte Tin and Sn/Bi for plating recipe. For PPF(Pre-Plated Frame) product with 63/37 solder paste, we recommend 240℃~245℃ for peak temperature.

**Recommended Reflow Profile for 63/37 Solder Paste or Cu lead frame**




*This profile is designed for use with Sn63 or Sn62 and can serve as a general guideline in establishing a reflow profile.*

**Reflow Profile:**

- Heating-up @1~3°C per sec to 140°C
- Preheat @ 140-150°C for 120 ~ 160 sec
- Ramp @ 2~3 °C per sec to peak temperature (220 ~ 225 °C), Temperature over 183°C for 45~ 75 sec
- Cooling down to room temperature @4~2°C per sec to avoid undesired intermatalic compound layer.

## 11. DISCLAIMER

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## 12. REVISION HISTORY

| Date | Revision # | Description | Page |
|---|---|---|---|
| NOV. 15, 2006 | 1.1 | 1. Modify the “Pin Map” in section 4.1.<br>2. Add Note in section 8.1.Digital Section.<br>3. Modify the “Pad Assignment and Locations” in section 10.1<br>4. Modify the “Ordering Information” in section 10.2. | 5<br>14<br>16<br>16 |
| JAN. 18, 2006 | 1.0 | Original<br>Note: The GPF32512A data sheet v1.0 is a continued version of SPF32512A data sheet v0.4. | 20 |