DUAL-OUTPUT, LOW DROPOUT VOLTAGE REGULATORS WITH INTEGRATED SVS FOR SPLIT VOLTAGE SYSTEMS

Check for Samples: TPS70345, TPS70348, TPS70351, TPS70358, TPS70302

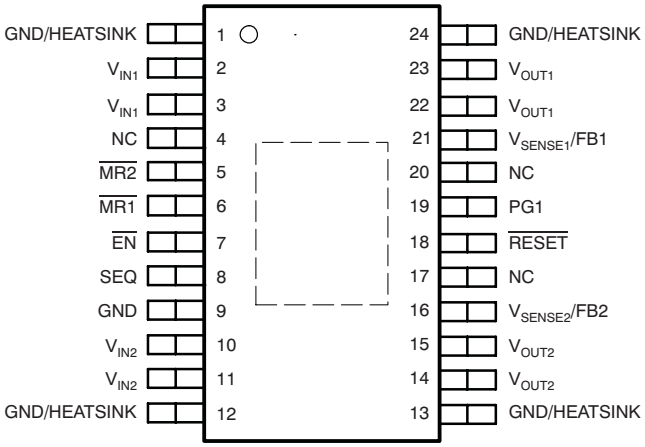
FEATURES

- **Dual Output Voltages for Split-Supply Applications**
- **Independent Enable Functions (See Part Number TPS704xx for Independent Enabling of Each Output)**
- **Output Current Range of 1 A on Regulator 1 and 2A on Regulator 2**
- **Fast Transient Response**
- **Voltage Options: 3.3 V/2.5 V, 3.3 V/1.8 V, 3.3 V/1.5 V, 3.3 V/1.2 V, and Dual Adjustable Outputs**
- **Open Drain Power-On Reset with 120 ms Delay**
- **Open Drain Power Good for Regulator 1**
- **Ultralow 185 μA (typ) Quiescent Current**
- **2 μA Input Current During Standby**
- **Low Noise: 78 μV_{RMS} Without Bypass Capacitor**
- **Quick Output Capacitor Discharge Feature**
- **Two Manual Reset Inputs**
- **2% Accuracy Over Load and Temperature**
- **Undervoltage Lockout (UVLO) Feature**
- **24-Pin PowerPAD™ TSSOP Package**
- **Thermal Shutdown Protection**

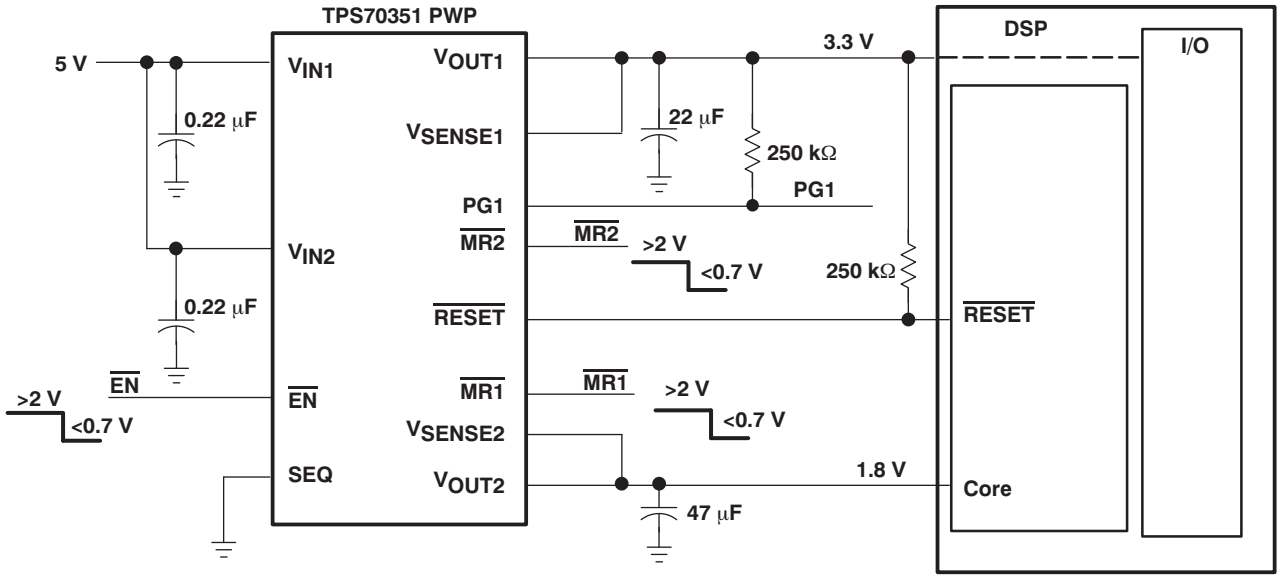
DESCRIPTION

The TPS703xx family of devices is designed to provide a complete power management solution for TI DSP, processor power, ASIC, FPGA, and digital applications where dual output voltage regulators are required. Easy programmability of the sequencing function makes this family ideal for any TI DSP application with power sequencing requirements. Differentiated features, such as accuracy, fast transient response, SVS supervisory circuit (power-on reset), manual reset inputs, and enable function, provide a complete system solution.

PWP PACKAGE
(TOP VIEW)



NC = No internal connection



The TPS703xx family of voltage regulators offers very low dropout voltage and dual outputs with power up sequence control, designed primarily for DSP applications. These devices have low noise output performance without using any added filter bypass capacitors, and are designed to have a fast transient response and be stable with 47 μF low ESR capacitors.

These devices have fixed 3.3 V/2.5 V, 3.3 V/1.8 V, 3.3 V/1.5 V, 3.3 V/1.2 V, and adjustable voltage options. Regulator 1 can support up to 1 A, and regulator 2 can support up to 2 A. Separate voltage inputs allow the designer to configure the source power.

Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low (typically 160mV on regulator 1) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (maximum of 250 μA over the full range of output current). This LDO family also features a sleep mode; applying a high signal to $\overline{EN}$ (enable) shuts down both regulators, reducing the input current to 1 μA at T_J = +25°C.

The device is enabled when the $\overline{EN}$ pin is connected to a low-level input voltage. The output voltages of the two regulators are sensed at the V_{SENSE1} and V_{SENSE2} pins respectively.

The input signal at the SEQ pin controls the power-up sequence of the two regulators. When the device is enabled and the SEQ terminal is pulled high or left open, V_{OUT2} turns on first and V_{OUT1} remains off until V_{OUT2} reaches approximately 83% of its regulated output voltage. At that time V_{OUT1} is turned on. If V_{OUT2} is pulled below 83% (that is, in an overload condition) of its regulated voltage, V_{OUT1} is turned off. Pulling the SEQ terminal low reverses the power-up order and V_{OUT1} is turned on first. The SEQ pin is connected to an internal pull-up current source.

For each regulator, there is an internal discharge transistor to discharge the output capacitor when the regulator is turned off (disabled).

The PG1 pin reports the voltage condition at V_{OUT1}. The PG1 pin can be used to implement an SVS (POR, or power-on reset) for the circuitry supplied by regulator 1.

The TPS703xx features a $\overline{RESET}$ (SVS, POR, or power-on reset). $\overline{RESET}$ is an active low, open drain output and requires a pull-up resistor for normal operation. When pulled up, $\overline{RESET}$ goes to a high impedance state (that is, logic high) after a 120 ms delay when all three of the following conditions are met. First, V_{IN1} must be above the undervoltage condition. Second, the manual reset ($\overline{MR}$) pin must be in a high impedance state. Third, V_{OUT2} must be above approximately 95% of its regulated voltage. To monitor V_{OUT1}, the PG1 output pin can be connected to $\overline{MR1}$ or $\overline{MR2}$. $\overline{RESET}$ can be used to drive power-on reset or a low-battery indicator. If $\overline{RESET}$ is not used, it can be left floating.

Internal bias voltages are powered by V_{IN1} and require 2.7V for full functionality. Each regulator input has an undervoltage lockout circuit that prevents each output from turning on until the respective input reaches 2.5 V.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	VOLTAGE (V)(2) V_{OUT1}	VOLTAGE (V)(2) V_{OUT2}	PACKAGE-LEAD (DESIGNATOR)	SPECIFIED TEMPERATURE RANGE (T_J)	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TPS70302	Adjustable	Adjustable	HTSSOP-24 (PWP)	-40°C to +125°C	TPS70302PWP	Tube, 60
					TPS70302PWPR	Tape and Reel, 2000
TPS70345	3.3 V	1.2 V	HTSSOP-24 (PWP)	-40°C to +125°C	TPS70345PWP	Tube, 60
					TPS70345PWPR	Tape and Reel, 2000
TPS70348	3.3 V	1.5 V	HTSSOP-24 (PWP)	-40°C to +125°C	TPS70348PWP	Tube, 60
					TPS70348PWPR	Tape and Reel, 2000
TPS70351	3.3 V	1.8 V	HTSSOP-24 (PWP)	-40°C to +125°C	TPS70351PWP	Tube, 60
					TPS70351PWPR	Tape and Reel, 2000
TPS70358	3.3 V	2.5 V	HTSSOP-24 (PWP)	-40°C to +125°C	TPS70358PWP	Tube, 60
					TPS70358PWPR	Tape and Reel, 2000

(1) For the most current package and ordering information see the Package Option Addendum located at the end of this document, or see the TI web site at www.ti.com.
(2) For fixed 1.20V operation, tie FB to OUT.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

	TPS703xx	UNIT
Input voltage range: V_{IN1}, V_{IN2}(2)	–0.3 to +7	V
Voltage range at $\overline{EN}$	–0.3 to +7	V
Output voltage range (V_{OUT1}, V_{SENSE1})	5.5	V
Output voltage range (V_{OUT2}, V_{SENSE2})	5.5	V
Maximum $\overline{RESET}$, PG1 voltage	7	V
Maximum $\overline{MR1}$, $\overline{MR2}$, and SEQ voltage	V_{IN1}	V
Peak output current	Internally limited	—
Continuous total power dissipation	See Dissipation Ratings Table	—
Operating virtual junction temperature range, T_J	–40 to +150	°C
Storage temperature range, T_{STG}	–65 to +150	°C
ESD rating, HBM	2	kV

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are tied to network ground.

DISSIPATION RATINGS

PACKAGE	AIR FLOW (CFM)	$T_A \leq +25°C$	DERATING FACTOR	$T_A = +70°C$	$T_A = +85°C$
PWP (1)	0	3.067 W	30.67 mW/°C	1.687 W	1.227 W
	250	4.115 W	41.15 mW/°C	2.265 W	1.646 W

(1) This parameter is measured with the recommended copper heat sink pattern on a 4-layer PCB, 1 oz. copper on a 4-in by 4-in ground layer. For more information, refer to TI technical brief SLMA002.

RECOMMENDED OPERATING CONDITIONS

Over operating temperature range (unless otherwise noted).

	MIN	MAX	UNIT
Input voltage, V_I (1) (regulator 1 and 2)	2.7	6	V
Output current, I_O (regulator 1)	0	1	A
Output current, I_O (regulator 2)	0	2	A
Output voltage range (for adjustable option)	1.22	5.5	V
Operating virtual junction temperature, T_J	–40	+125	°C

(1) To calculate the minimum input voltage for maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.

ELECTRICAL CHARACTERISTICS

Over recommended operating junction temperature range (T_J = –40°C to +125°C), V_{IN1} or V_{IN2} = $V_{OUTX(nom)}$ + 1V, I_{OUTX} = 1mA, $\overline{EN}$ = 0V, C_{OUT1} = 22μF, and C_{OUT2} = 47μF (unless otherwise noted).

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage (1)(2)	Reference voltage	2.7 V < V_{IN} < 6 V, T_J = +25°C	FB connected to V_O		1.224		V
			2.7 V < V_{IN} < 6 V,	FB connected to V_O	1.196		1.248	
		1.2 V output (V_{OUT2})	2.7 V < V_{IN} < 6 V,	T_J = +25°C		1.2		
			2.7 V < V_{IN} < 6 V,		1.176		1.224	
		1.5 V output (V_{OUT2})	2.7 V < V_{IN} < 6 V,	T_J = +25°C		1.5		
			2.7 V < V_{IN} < 6 V,		1.47		1.53	
		1.8 V output (V_{OUT2})	2.8 V < V_{IN} < 6 V,	T_J = +25°C		1.8		
			2.8 V < V_{IN} < 6 V,		1.764		1.836	
		2.5 V output (V_{OUT2})	3.5 V < V_{IN} < 6 V,	T_J = +25°C		2.5		
			3.5 V < V_{IN} < 6 V,		2.45		2.55	
		3.3 V output (V_{OUT1})	4.3 V < V_{IN} < 6 V,	T_J = +25°C		3.3		
			4.3 V < V_{IN} < 6 V,		3.234		3.366	
Quiescent current (GND current) for regulator 1 and regulator 2, $\overline{EN}$ = 0 V (1)			See (2)	T_J = +25°C		185		μA
			See (2)				250	
Output voltage line regulation ($\Delta V_O/V_O$) for regulator 1 and regulator 2 (3)			V_O + 1 V < V_{IN} ≤ 6 V,	T_J = +25°C (1)		0.01		%V
			V_O + 1 V < V_{IN} ≤ 6 V	(1)			0.1	
Load regulation for $V_{OUT\ 1}$ and V_{OUT2}			T_J = +25°C			1		mV
V_n	Output noise voltage (TPS70351)	Regulator 1	BW = 300 Hz to 50 kHz,	C_O = 33 μF, T_J = +25°C		79		μV_{RMS}
		Regulator 2				77		
Output current limit		Regulator 1	V_{OUT} = 0 V			1.75	2.2	A
		Regulator 2				3.8	4.5	
Thermal shutdown junction temperature						+150		°C
I_I (standby)	Standby current		$\overline{EN1}$ = V_{IN}, $\overline{EN2}$ = V_I	T_J = +25°C		1	2	μA
			$\overline{EN1}$ = V_{IN}, $\overline{EN2}$ = V_I				10	
PSRR	Power-supply ripple rejection (TPS70351)	Regulator 1	f = 1 kHz,	T_J = +25°C (1)		65		dB
		Regulator 2	f = 1 kHz,	T_J = +25°C (1)		60		
RESET Terminal								
Minimum input voltage for valid $\overline{RESET}$			I_{RESET} = 300 μA,	$V_{(RESET)}$ ≤ 0.8 V		1.0	1.3	V
Trip threshold voltage			V_O decreasing		92	95	98	$\%V_{OUT}$
Hysteresis voltage			Measured at V_O			0.5		$\%V_{OUT}$
$t_{\overline{(RESET)}}$			$\overline{RESET}$ pulse duration		80	120	160	ms
$t_{r\ \overline{(RESET)}}$			Rising edge deglitch			30		μs
Output low voltage			V_{IN} = 3.5 V,	$I_{(RESET)}$ = 1 mA		0.15	0.4	V
Leakage current			$V_{(RESET)}$ = 6 V				1	μA

(1) Minimum input operating voltage is 2.7 V or $V_{O(typ)}$ + 1V, whichever is greater. Maximum input voltage = 6V, minimum output current = 1 mA.

(2) I_O = 1 mA to 1 A for Regulator 1 and 1mA to 2A for Regulator 2.

(3) If V_O < 1.8 V then V_{Imax} = 6 V, V_{Imin} = 2.7 V: $$\text{Line regulation (mV)} = (\%/V) \times V_o \frac{(V_{Imax} - 2.7)}{100} \times 1000$$

If V_O > 2.5 V then V_{Imax} = 6 V, V_{Imin} = V_O + 1 V: $$\text{Line regulation (mV)} = (\%/V) \times V_o \frac{[V_{Imax} - (V_o + 1)]}{100} \times 1000$$

ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating junction temperature range (T_J = –40°C to +125°C), V_{IN1} or V_{IN2} = $V_{OUTX(nom)}$ + 1V, I_{OUTX} = 1mA, $\overline{EN}$ = 0V, C_{OUT1} = 22μF, and C_{OUT2} = 47μF (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PG Terminal					
Minimum input voltage for valid PG	$I_{(PG)}$ = 300 μA, $V_{(PG1)}$ ≤ 0.8 V		1.0	1.3	V
Trip threshold voltage	V_O decreasing	92	95	98	%V_{OUT}
Hysteresis voltage	Measured at V_O		0.5		%V_{OUT}
$t_{r(PG1)}$	Rising edge deglitch		30		μs
Output low voltage	V_{IN} = 2.7 V, $I_{(PG)}$ = 1 mA		0.15	0.4	V
Leakage current	$V_{(PG1)}$ = 6 V			1	μA
EN Terminal					
High-level $\overline{EN}$ input voltage		2			V
Low-level $\overline{EN}$ input voltage				0.7	V
Input current ($\overline{EN}$)		–1		1	μA
SEQ Terminal					
High-level SEQ input voltage		2			V
Low-level SEQ input voltage				0.7	V
SEQ pull-up current source			6		μA
MR1/MR2 Terminal					
High-level input voltage		2			V
Low-level input voltage				0.7	V
Pull-up current source			6		μA
V_{OUT2} Terminal					
V_{OUT2} UV comparator: positive-going input threshold voltage at V_{OUT1} UV comparator		80	83	86	%V_{OUT}
V_{OUT2} UV comparator: hysteresis			3		%V_{OUT}, mV
V_{OUT2} UV comparator: falling edge deglitch	V_{SENSE2} decreasing below threshold		140		μs
Peak output current	2 ms pulse width		3		A
Discharge transistor current	V_{OUT2} = 1.5 V		7.5		mA

ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating junction temperature range (T_J = –40°C to +125°C), V_{IN1} or V_{IN2} = $V_{OUTX(nom)}$ + 1V, I_{OUTX} = 1mA, $\overline{EN}$ = 0V, C_{OUT1} = 22μF, and C_{OUT2} = 47μF (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT1} Terminal					
V_{OUT1} UV comparator: positive-going input threshold voltage at V_{OUT2} UV comparator		80	83	86	%V_{OUT}
V_{OUT1} UV comparator: hysteresis			3		%V_{OUT}, mV
V_{OUT1} UV comparator: falling edge deglitch	V_{SENSE1} decreasing below threshold		140		μs
Dropout voltage(4)	I_O = 1 A, V_{IN1} = 3.2 V T_J = +25°C		160		mV
	I_O = 1 A, V_{IN1} = 3.2 V			250	
Peak output current	2ms pulse width		1.2		A
Discharge transistor current	V_{OUT1} = 1.5 V		7.5		mA
V_{IN1}/V_{IN2} Terminal					
UVLO threshold		2.3		2.65	V
UVLO hysteresis			110		mV
FB Terminal					
Input current: TPS70302	FB = 1.8 V		1		μA

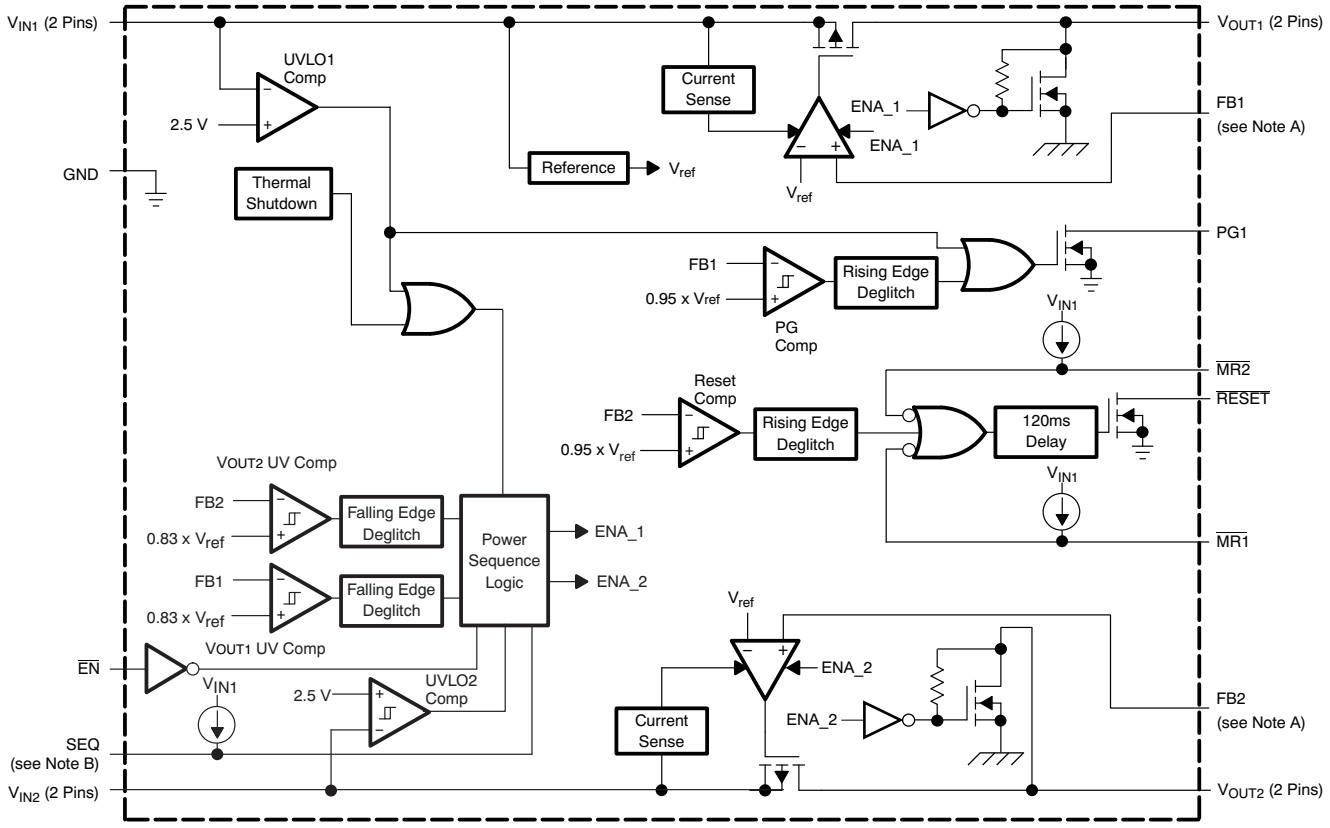
(4) Input voltage (V_{IN1} or V_{IN2}) = $V_{O(typ)}$ – 100mV. For 1.5 V, 1.8 V and 2.5 V regulators, the dropout voltage is limited by input voltage range. The 3.3 V regulator input is set to 3.2 V to perform this test.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN}$	7	I	Active low enable
GND	9	—	Regulator ground
GND/HEATSINK	1, 12, 13, 24	—	Ground/heatsink
$\overline{MR1}$	6	I	Manual reset input 1, active low, pulled up internally
$\overline{MR2}$	5	I	Manual reset input 2, active low, pulled up internally
NC	4, 17, 20	—	No connection
PG1	19	O	Open drain output, low when V_{OUT1} voltage is less than 95% of the nominal regulated voltage
$\overline{RESET}$	18	O	Open drain output, SVS (power-on reset) signal, active low
SEQ	8	I	Power-up sequence control: SEQ = High, V_{OUT2} powers up first; SEQ = Low, V_{OUT1} powers up first. SEQ terminal pulled up internally.
V_{IN1}	2, 3	I	Input voltage of regulator 1
V_{IN2}	10, 11	I	Input voltage of regulator 2
V_{OUT1}	22, 23	O	Output voltage of regulator 1
V_{OUT2}	14, 15	O	Output voltage of regulator 2
V_{SENSE2}/FB2	16	I	Regulator 2 output voltage sense/regulator 2 feedback for adjustable
V_{SENSE1}/FB1	21	I	Regulator 1 output voltage sense/regulator 1 feedback for adjustable

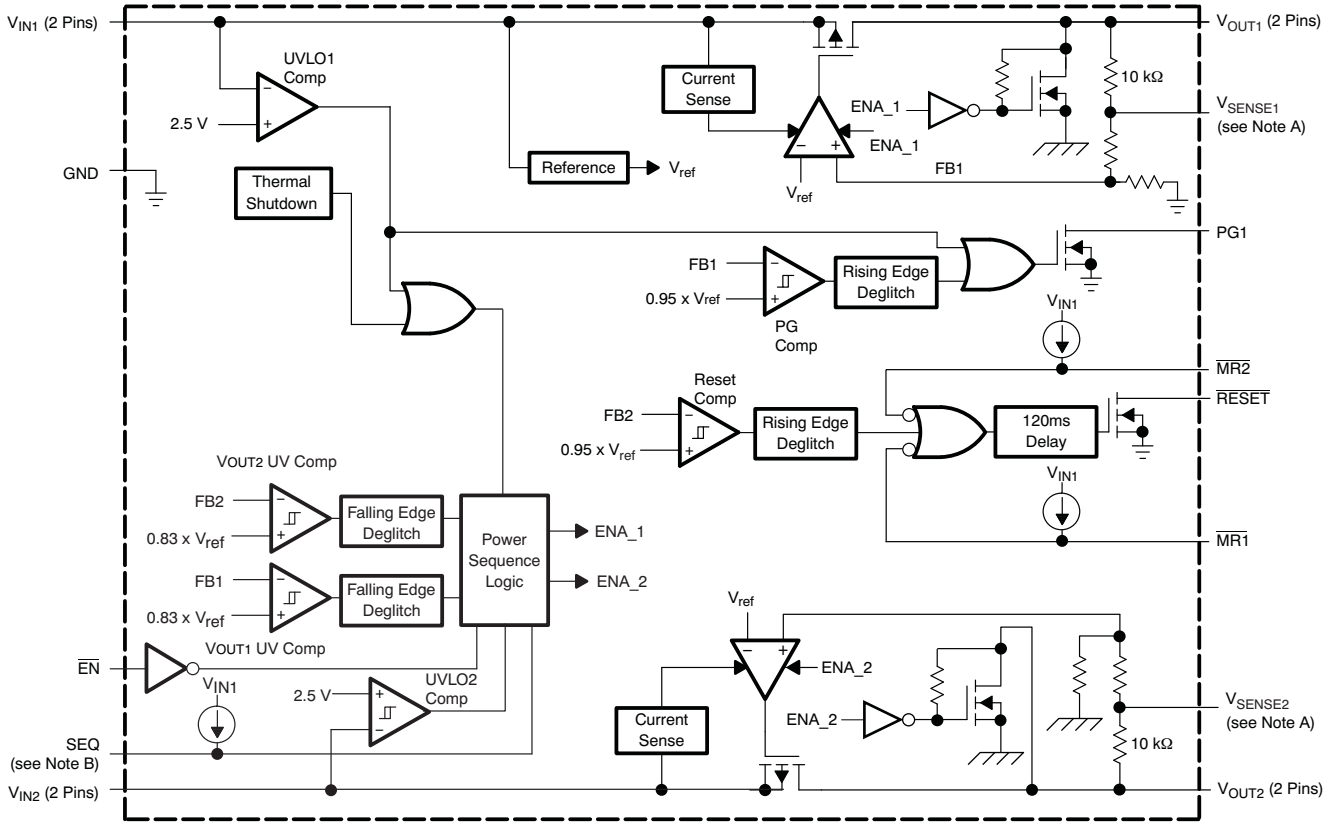
DEVICE INFORMATION

Adjustable Voltage Version



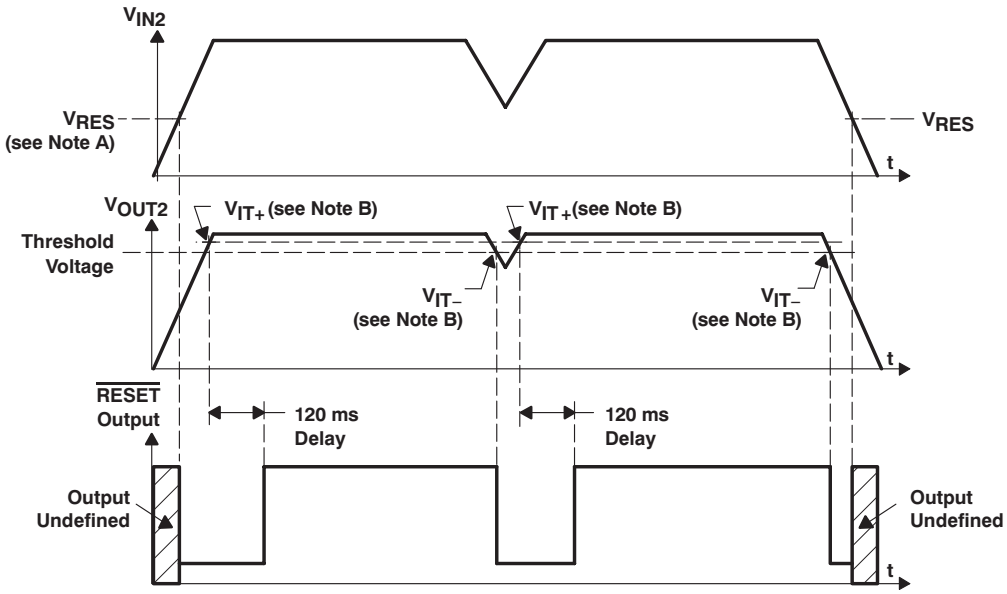
A. For most applications, V_{SENSE1} and V_{SENSE2} should be externally connected to V_{OUT1} and V_{OUT2}, respectively, as close as possible to the device. For other implementations, refer to SENSE terminal connection discussion in the ***Application Information*** section.

Fixed Voltage Version



A. For most applications, FB1 and FB2 should be externally connected to resistor dividers as close as possible to the device. For other implementations, refer to FB terminals connection discussion in the ***Application Information*** section.

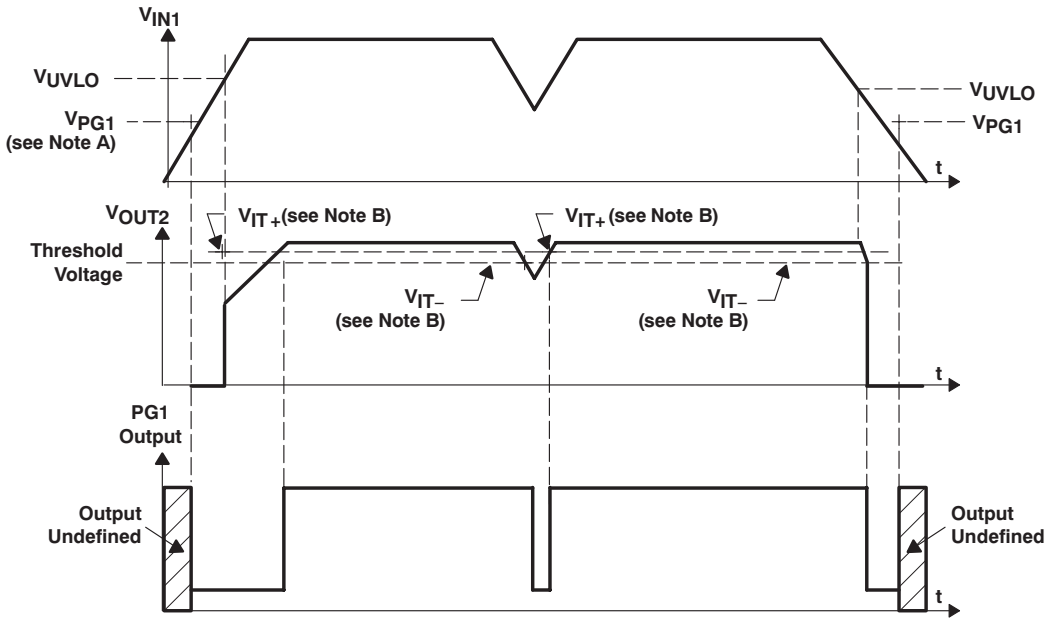
$\overline{\text{RESET}}$ Timing Diagram with V_{IN1} Powered Up, $\overline{\text{MR1}}$ and $\overline{\text{MR2}}$ at Logic High



NOTES: A. V_{RES} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{RES} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. V_{IT-} trip voltage is typically 5% lower than the output voltage (95%V_O). V_{IT-} to V_{IT+} is the hysteresis voltage.

PG1 Timing Diagram



NOTES: A. V_{PG1} is the minimum input voltage for a valid PG1. The symbol V_{PG1} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. V_{IT-} trip voltage is typically 5% lower than the output voltage (95%V_O). V_{IT-} to V_{IT+} is the hysteresis voltage.

Detailed Description

The TPS703xx low dropout regulator family provides dual regulated output voltages for DSP applications that require a high-performance power management solution. These devices provide fast transient response and high accuracy, while drawing low quiescent current. Programmable sequencing provides a power solution for DSPs without any external component requirements. This reduces the component cost and board space while increasing total system reliability. The TPS703xx family has an enable feature that puts the device into sleep mode, reducing the input current to 1 μA. Other features are the integrated SVS (power-on reset, $\overline{\text{RESET}}$) and power good (PG1). These differential features monitor output voltages and provide logic output to the system, and provide a complete DSP power solution.

The TPS703xx, unlike many other LDOs, features very low quiescent current that remains virtually constant even with varying loads. Conventional LDO regulators use a PNP pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS703xx uses a PMOS transistor to pass current. Because the gate of the PMOS is voltage driven, operating current is low and stable over the full load range.

Pin Functions

Enable ($\overline{\text{EN}}$)

The $\overline{\text{EN}}$ terminal is an input that enables or shuts down the device. If $\overline{\text{EN}}$ is at a logic high signal, the device is in shutdown mode. When $\overline{\text{EN}}$ goes to voltage low, then the device is enabled.

Sequence (SEQ)

The SEQ terminal is an input that programs the output voltage (V_{OUT1} or V_{OUT2}) that turns on first. When the device is enabled and the SEQ terminal is pulled high or left open, V_{OUT2} turns on first and V_{OUT1} remains off until V_{OUT2} reaches approximately 83% of its regulated output voltage. If V_{OUT2} is pulled below 83% (that is, goes to an overload) V_{OUT1} is turned off. This terminal has a 6 μA pull-up current to V_{IN1}.

Pulling the SEQ terminal low reverses the power-up order and V_{OUT1} turns on first. For detailed timing diagrams, see Figure 33 through Figure 39.

Power-Good (PG1)

The PG1 terminal is an open drain, active high output terminal that indicates the status of the V_{OUT1} regulator. When V_{OUT1} reaches 95% of its regulated voltage, PG1 goes to a high impedance state. PG1 goes to a low impedance state when V_{OUT1} is pulled below 95% (that is, goes to an overload condition) of its regulated voltage. The open drain output of the PG1 terminal requires a pull-up resistor.

Manual Reset Pins ($\overline{\text{MR1}}$ and $\overline{\text{MR2}}$)

$\overline{\text{MR1}}$ and $\overline{\text{MR2}}$ are active low input terminals used to trigger a reset condition. When either $\overline{\text{MR1}}$ or $\overline{\text{MR2}}$ is pulled to logic low, a POR ($\overline{\text{RESET}}$) occurs. These terminals have a 6μA pull-up current to V_{IN1}. It is recommended that these pins be pulled high to V_{IN} when they are not used..

Sense (V_{SENSE1} and V_{SENSE2})

The sense terminals of fixed-output options must be connected to the regulator output, and the connection should be as short as possible. Internally, the sense terminals connect to high-impedance wide-bandwidth amplifiers through resistor-divider networks and noise pickup feeds through to the regulator output. It is essential to route the sense connections in such a way to minimize or avoid noise pickup. Adding RC networks between the V_{SENSE} terminals and V_{OUT} terminals to filter noise is not recommended because these networks can cause the regulators to oscillate.

FB1 and FB2

FB1 and FB2 are input terminals used for adjustable-output devices and must be connected to the external feedback resistor divider. FB1 and FB2 connections should be as short as possible. It is essential to route them in such a way as to minimize or avoid noise pickup. Adding RC networks between the FB terminals and the V_{OUT} terminals to filter noise is not recommended because these networks can cause the regulators to oscillate.

$\overline{\text{RESET}}$ Indicator

$\overline{\text{RESET}}$ is an active low, open drain output that requires a pull-up resistor for normal operation. When pulled up, $\overline{\text{RESET}}$ goes to a high impedance state (that is, logic high) after a 120 ms delay when all three of the following conditions are met. First, V_{IN1} must be above the undervoltage condition. Second, the manual reset ($\overline{\text{MR}}$) pin must be in a high impedance state. Third, V_{OUT2} must be above approximately 95% of its regulated voltage. To monitor V_{OUT1}, the PG1 output pin can be connected to $\overline{\text{MR1}}$ or $\overline{\text{MR2}}$.

V_{IN1} and V_{IN2}

V_{IN1} and V_{IN2} are inputs to each regulator. **Internal bias voltages are powered by V_{IN1}.**

V_{OUT1} and V_{OUT2}

V_{OUT1} and V_{OUT2} are output terminals of each regulator.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	Figure 1, Figure 2
		vs Junction temperature	Figure 3, Figure 4
	Ground current	vs Junction temperature	Figure 5
PSRR	Power-supply rejection ratio	vs Frequency	Figure 6 to Figure 9
	Output spectral noise density	vs Frequency	Figure 10 to Figure 13
Z_O	Output impedance	vs Frequency	Figure 14 to Figure 17
	Dropout voltage	vs Temperature	Figure 18, Figure 19
		vs Input voltage	Figure 20, Figure 21
	Load transient response		Figure 22, Figure 23
	Line transient response (V_{OUT1})		Figure 24
	Line transient response (V_{OUT2})		Figure 25
V_O	Output voltage	vs Time (start-up)	Figure 26, Figure 27
	Equivalent series resistance (ESR)	vs Output current	Figure 29 to Figure 32

TPS70351
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

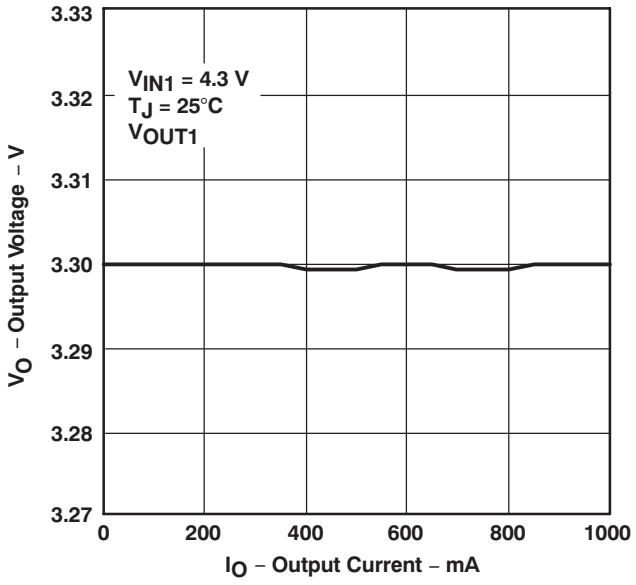


Figure 1.

TPS70351
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

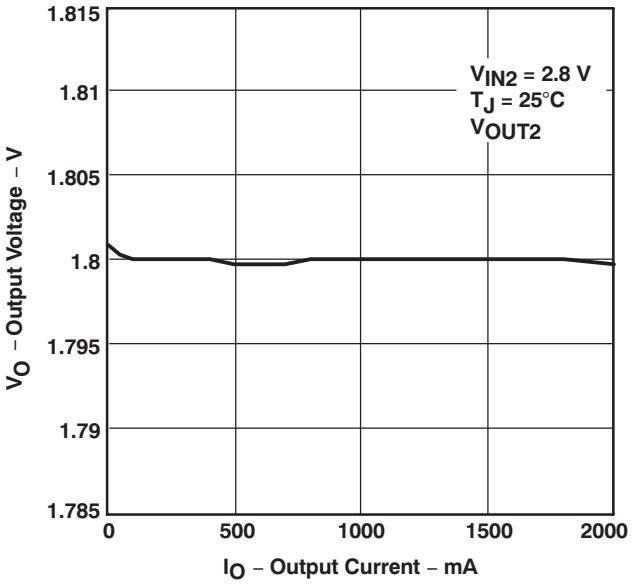


Figure 2.

TYPICAL CHARACTERISTICS (continued)

TPS70351
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

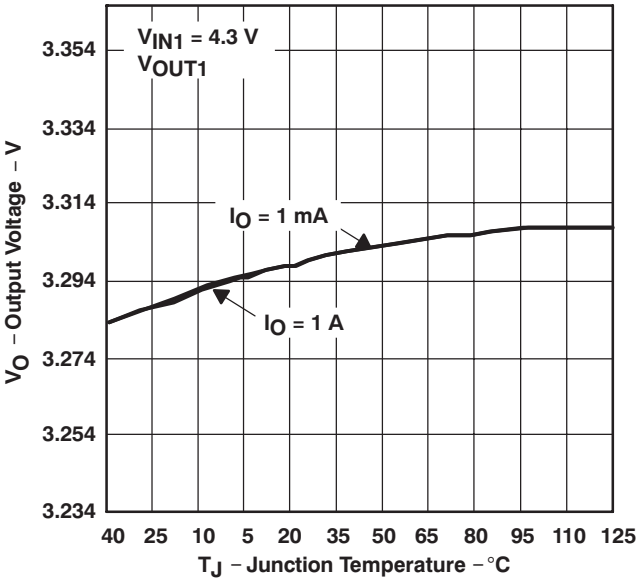


Figure 3.

TPS70351
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

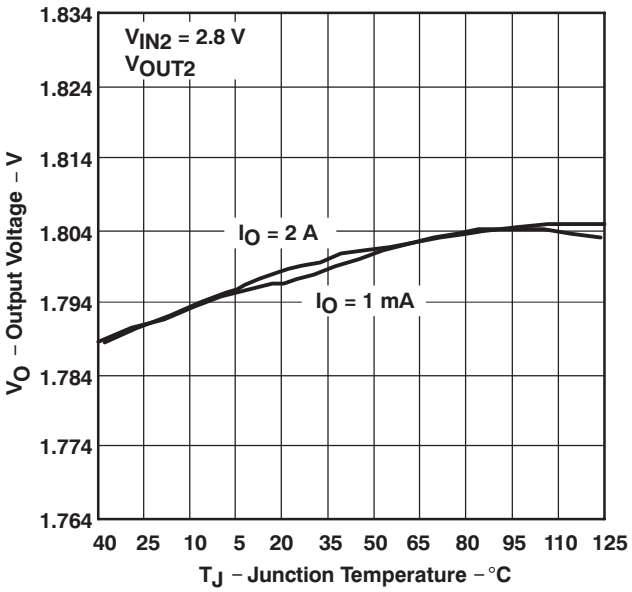


Figure 4.

TPS70351
GROUND CURRENT
vs
JUNCTION TEMPERATURE

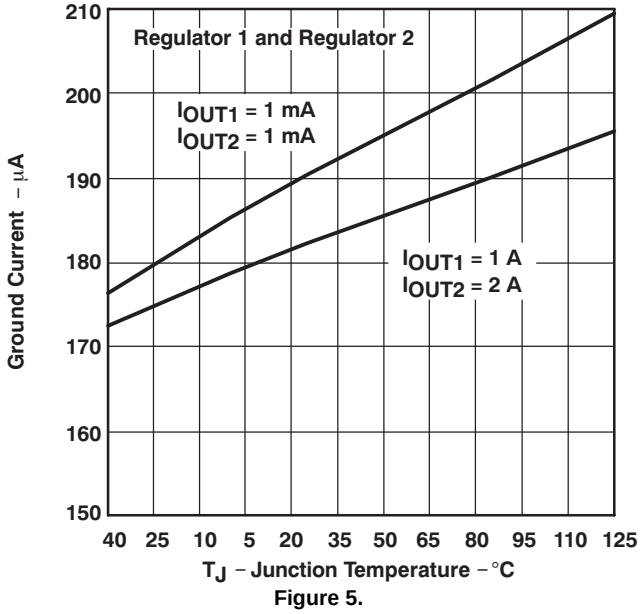


Figure 5.

TYPICAL CHARACTERISTICS (continued)

TPS70351
POWER-SUPPLY REJECTION RATIO
vs
FREQUENCY

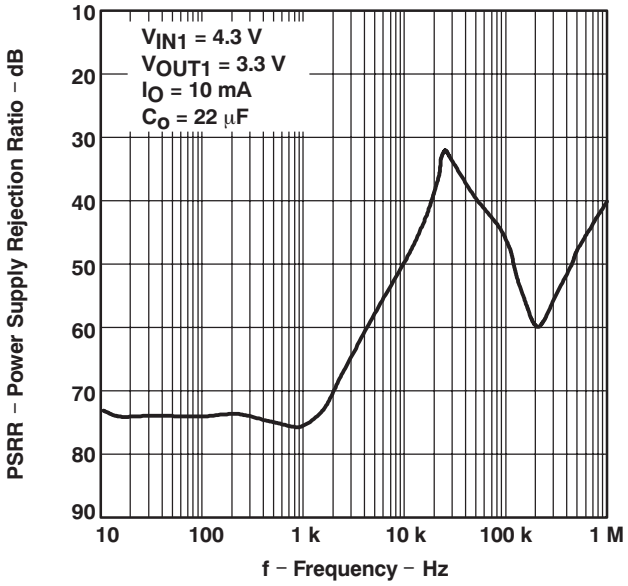


Figure 6.

TPS70351
POWER-SUPPLY REJECTION RATIO
vs
FREQUENCY

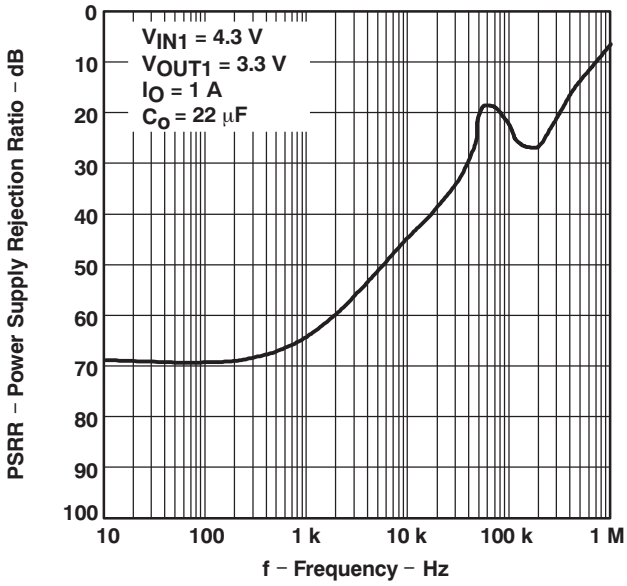


Figure 7.

TPS70351
POWER-SUPPLY REJECTION RATIO
vs
FREQUENCY

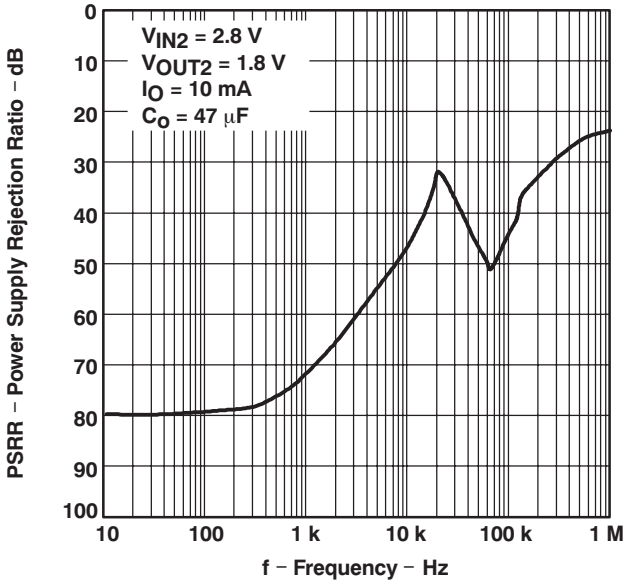


Figure 8.

TPS70351
POWER-SUPPLY REJECTION RATIO
vs
FREQUENCY

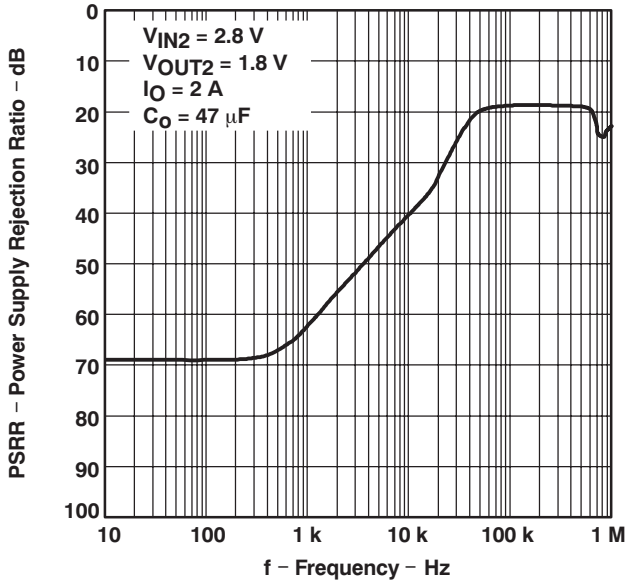


Figure 9.

TYPICAL CHARACTERISTICS (continued)

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

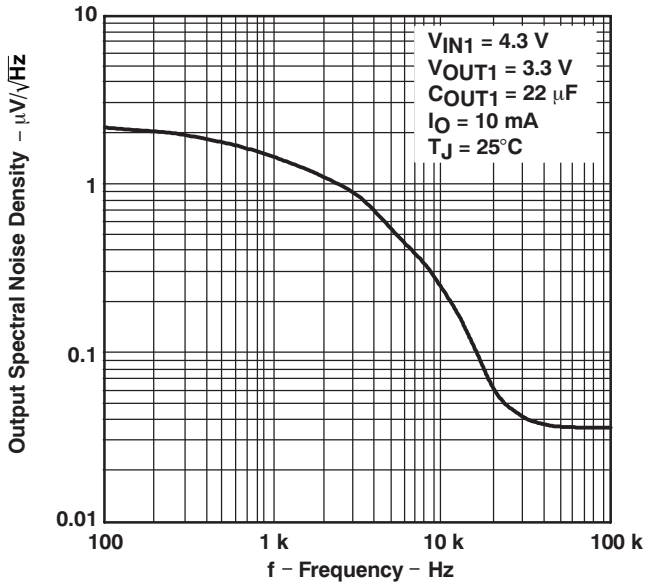


Figure 10.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

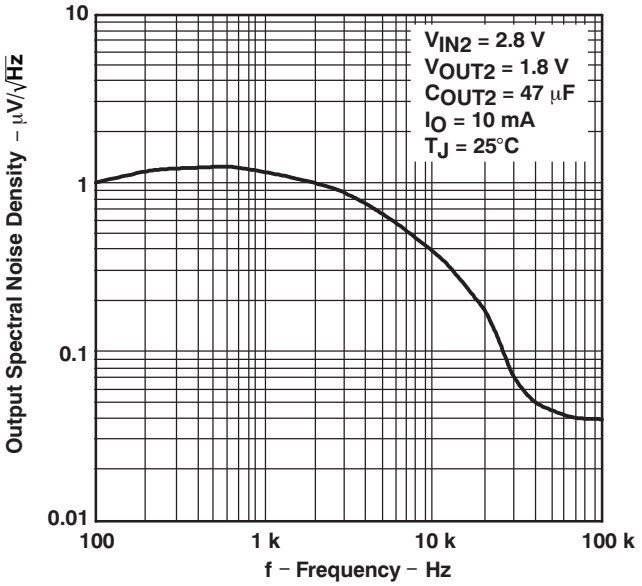


Figure 11.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

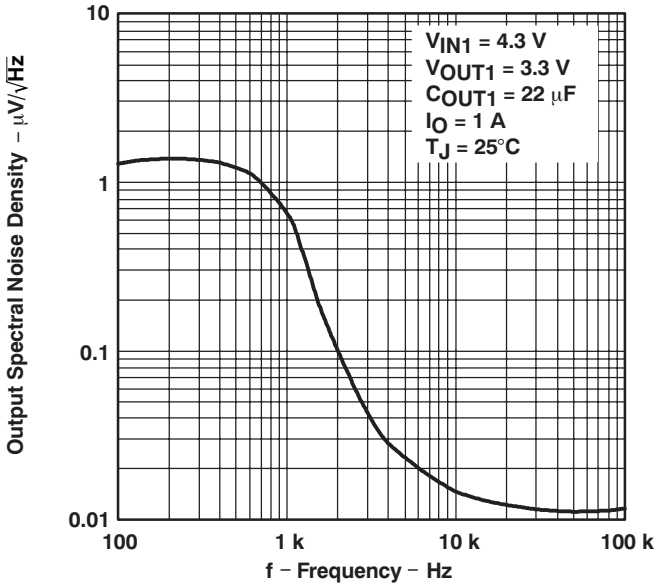


Figure 12.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

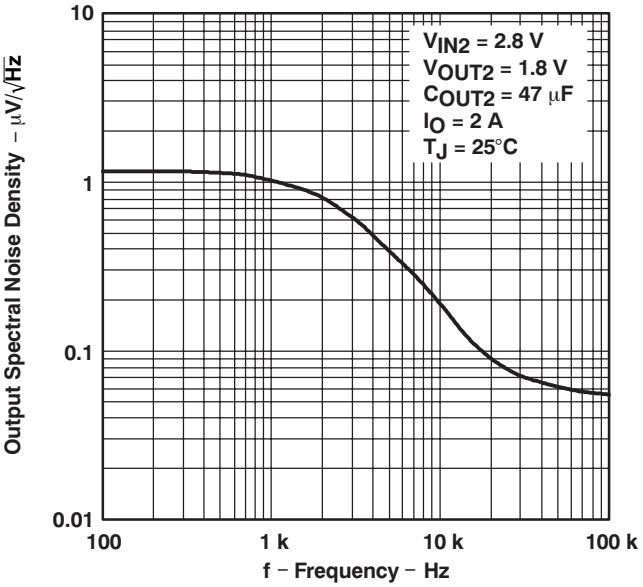


Figure 13.

TYPICAL CHARACTERISTICS (continued)

OUTPUT IMPEDANCE vs FREQUENCY

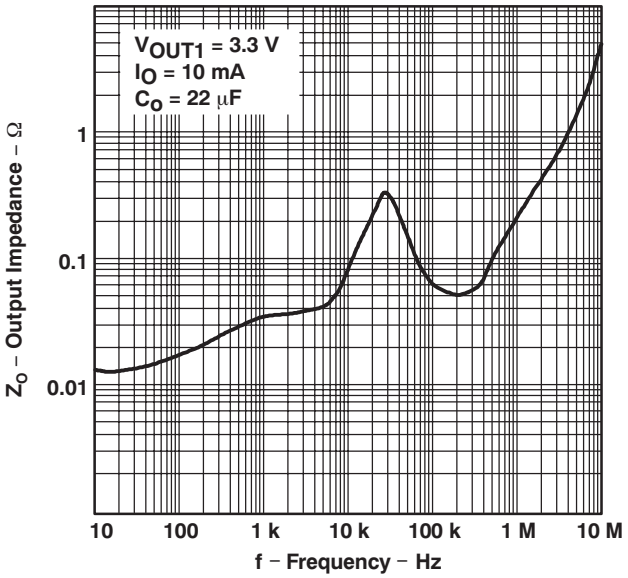


Figure 14.

OUTPUT IMPEDANCE vs FREQUENCY

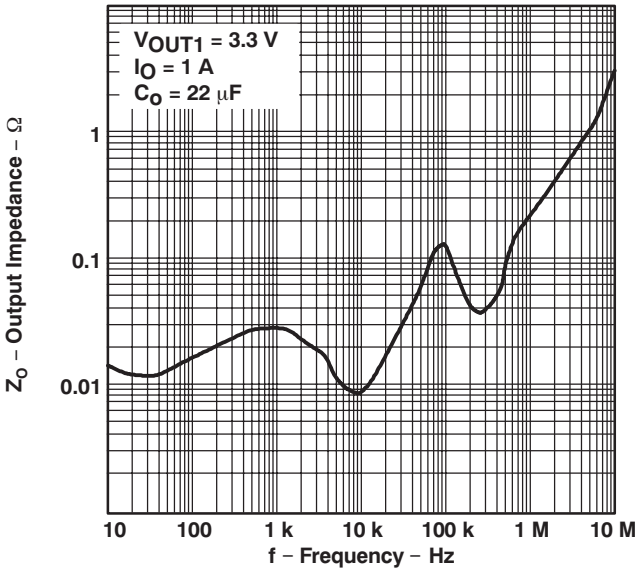


Figure 15.

OUTPUT IMPEDANCE vs FREQUENCY

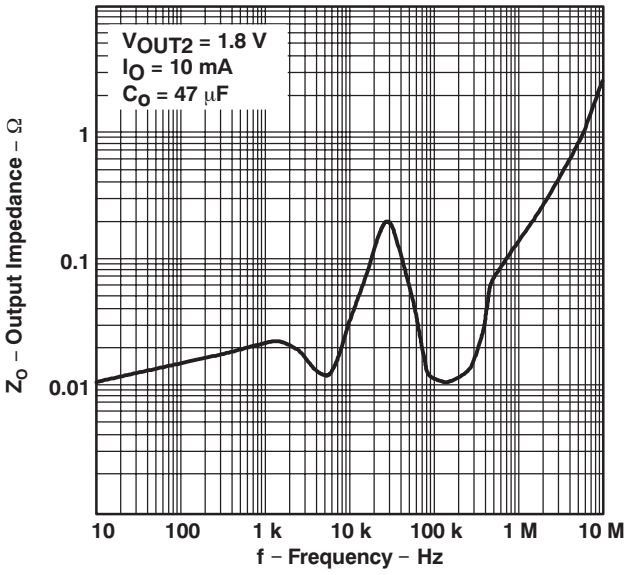


Figure 16.

OUTPUT IMPEDANCE vs FREQUENCY

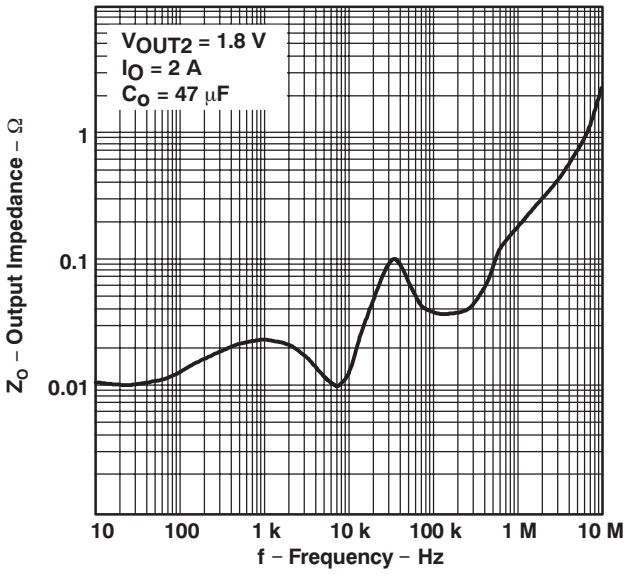


Figure 17.

TYPICAL CHARACTERISTICS (continued)

DROPOUT VOLTAGE vs TEMPERATURE

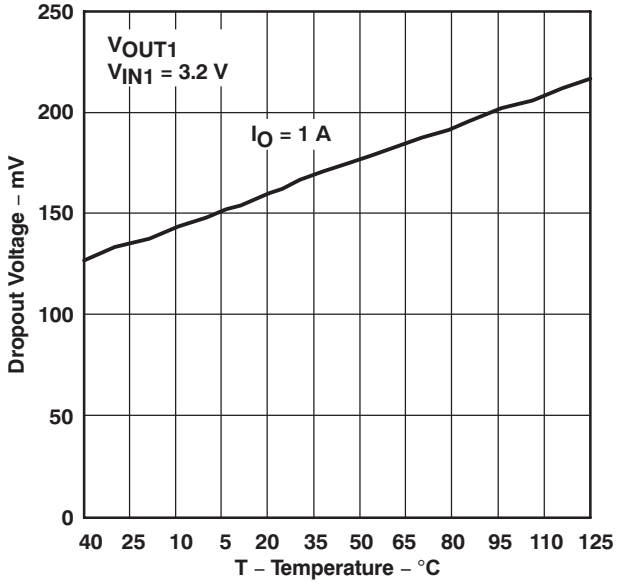


Figure 18.

DROPOUT VOLTAGE vs TEMPERATURE

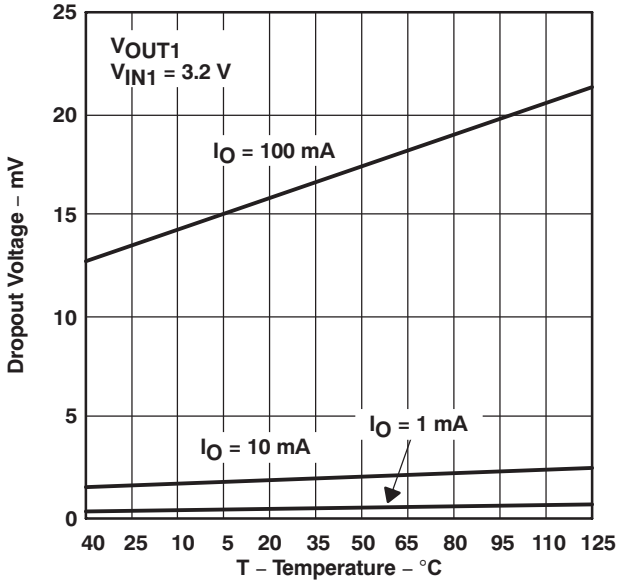


Figure 19.

TPS70302 DROPOUT VOLTAGE vs INPUT VOLTAGE

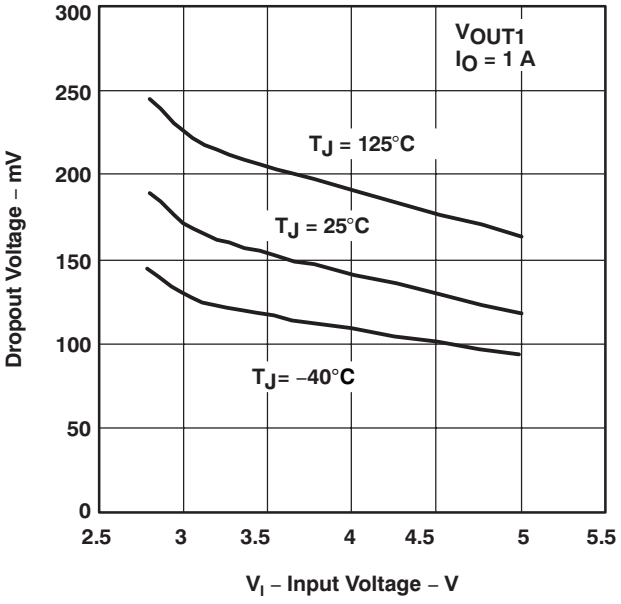


Figure 20.

TPS70302 DROPOUT VOLTAGE vs INPUT VOLTAGE

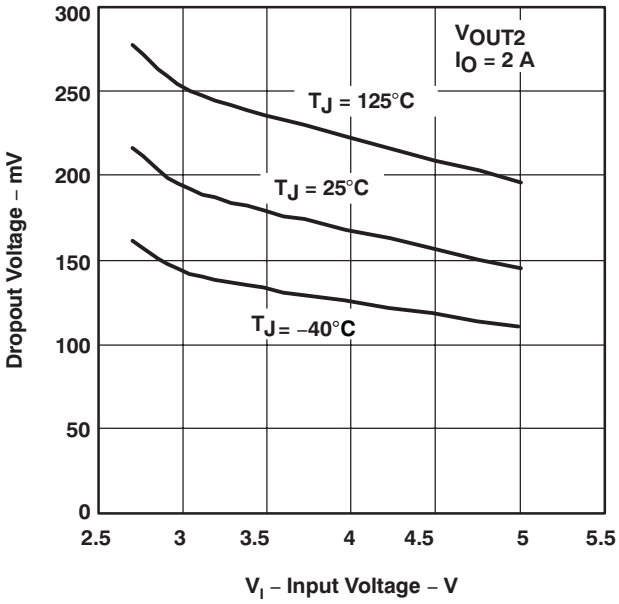


Figure 21.

TYPICAL CHARACTERISTICS (continued)

LOAD TRANSIENT RESPONSE

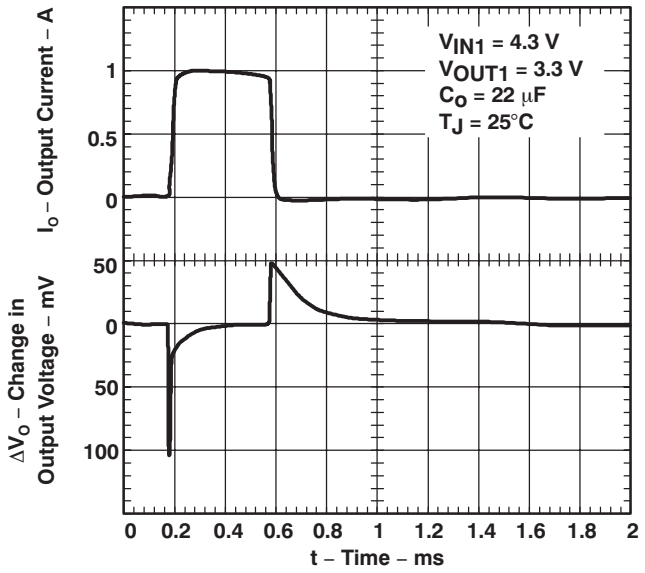


Figure 22.

LOAD TRANSIENT RESPONSE

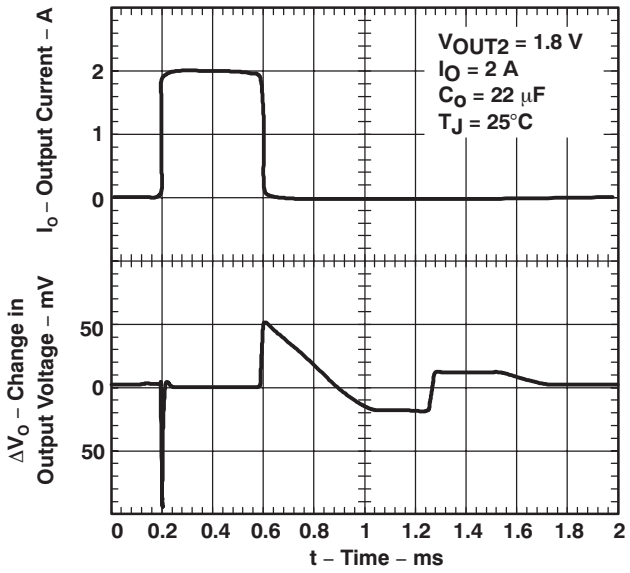


Figure 23.

LINE TRANSIENT RESPONSE

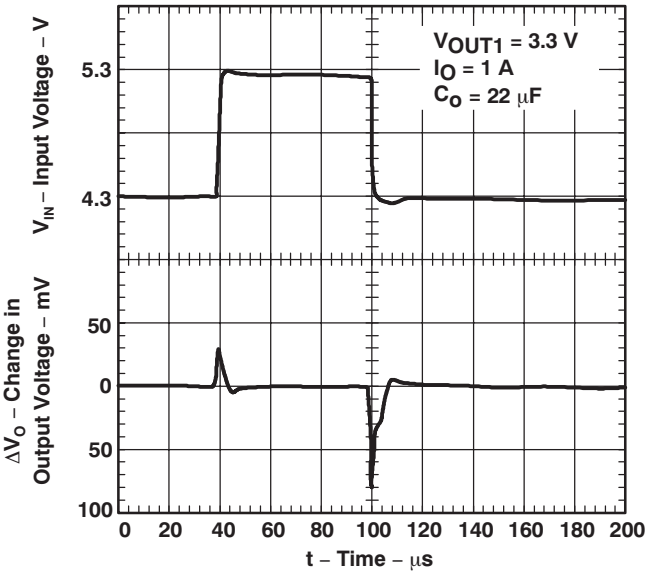


Figure 24.

LINE TRANSIENT RESPONSE

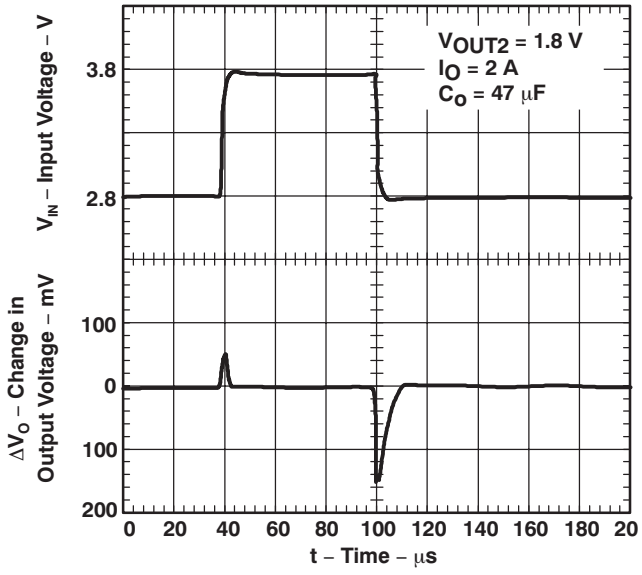


Figure 25.

TYPICAL CHARACTERISTICS (continued)

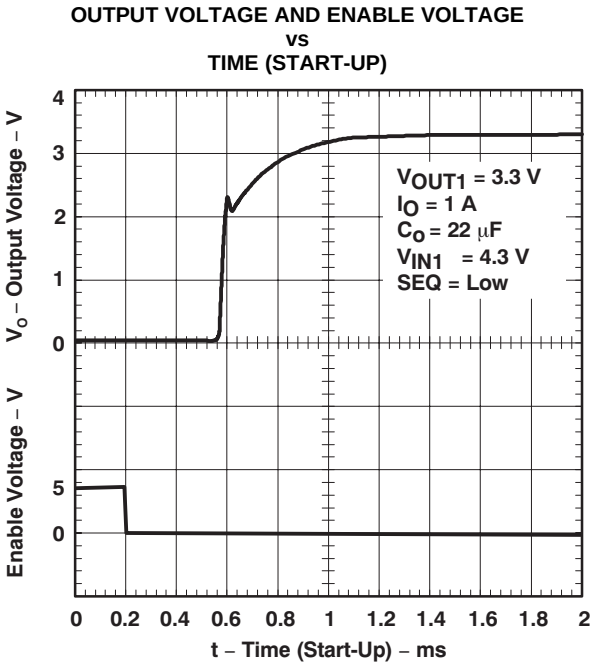


Figure 26.

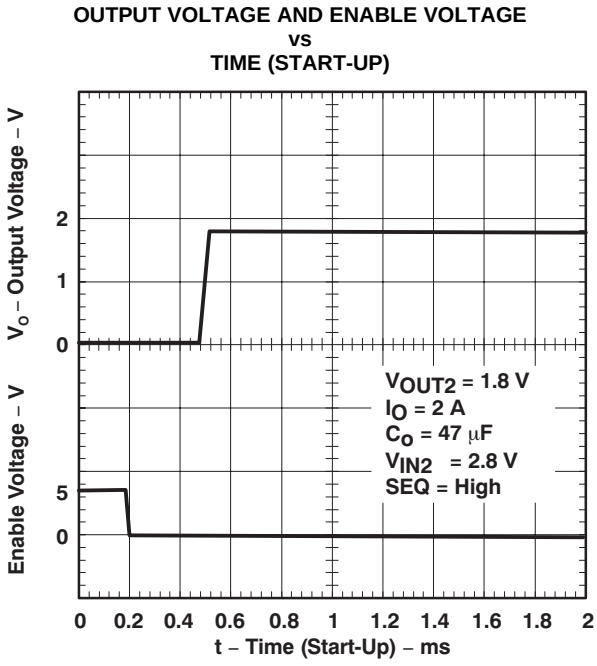


Figure 27.

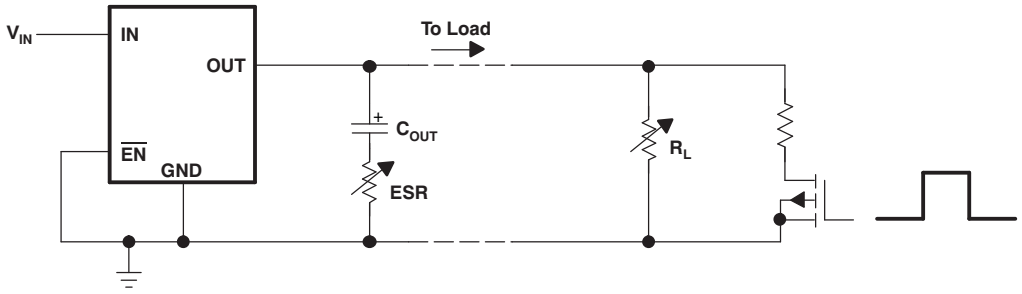


Figure 28. Test Circuit for Typical Regions of Stability

TYPICAL CHARACTERISTICS (continued)

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT**

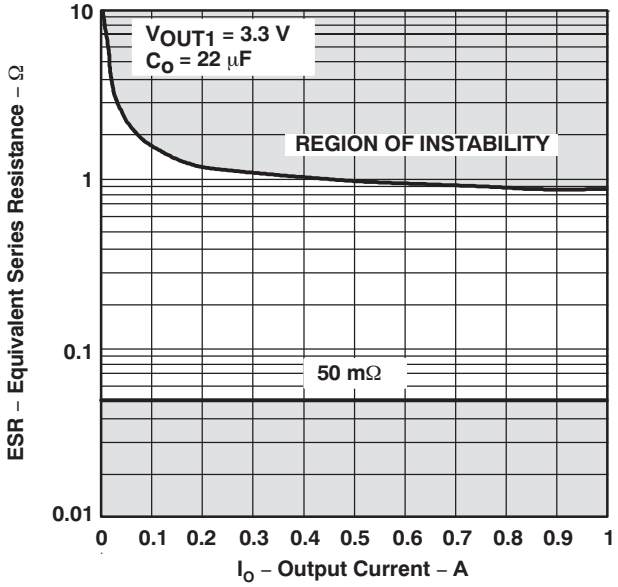


Figure 29.

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT**

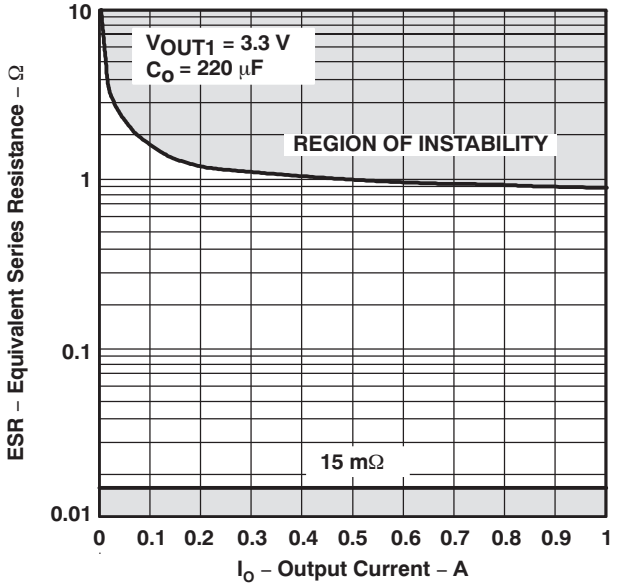


Figure 30.

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT**

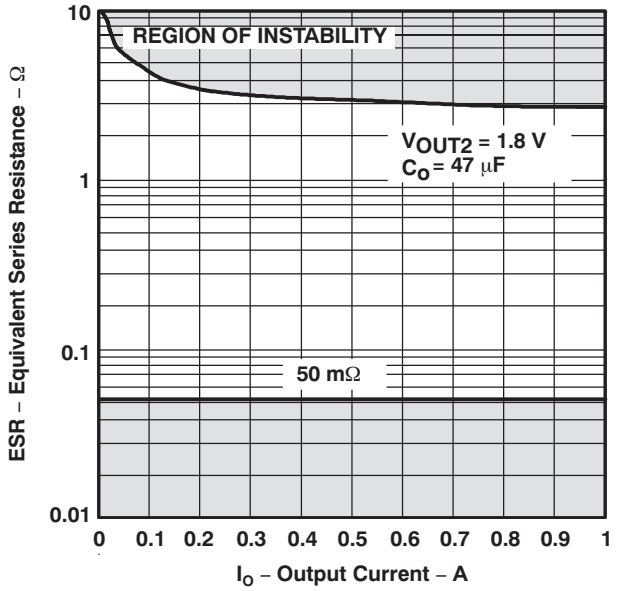


Figure 31.

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT**

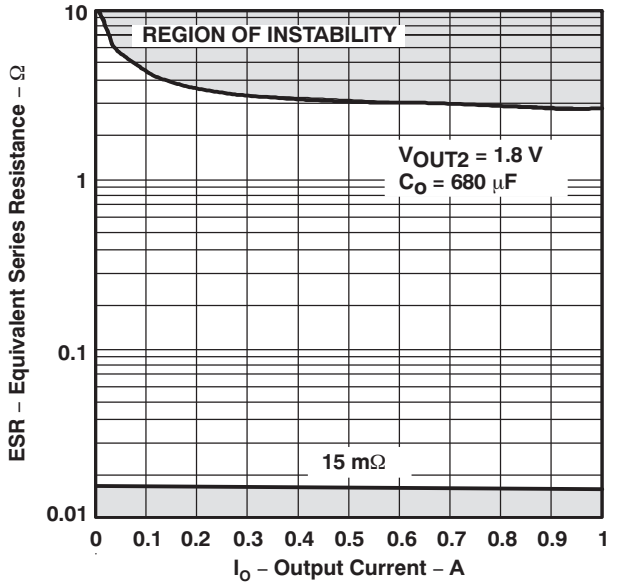


Figure 32.

(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

THERMAL INFORMATION

Thermally-Enhanced TSSOP-24 (PWP— PowerPAD™)

The thermally-enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad [see Figure 33(c)] to provide an effective thermal contact between the IC and the printed wiring board (PWB).

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally-enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

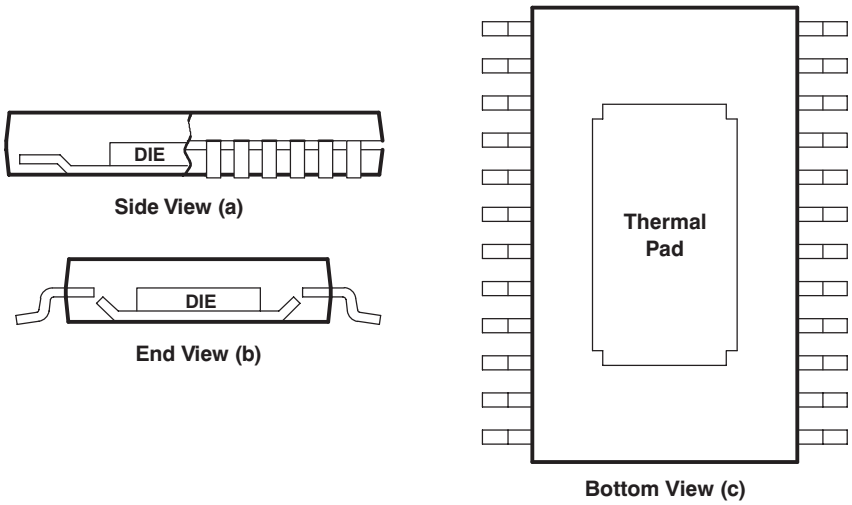


Figure 33. Views of Thermally-Enhanced PWP Package

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heat-sink surface), which is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air (reference Figure 35(a), 8 cm^2 of copper heat sink and natural convection). Increasing the heat-sink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly (see Figure 34 and Figure 35). The line drawn at 0.3 cm^2 in Figure 34 and Figure 35 indicates performance at the minimum recommended heat-sink size, illustrated in Figure 36.

The thermal pad is directly connected to the substrate of the IC, which for the TPS703xx series is a secondary electrical connection to device ground. The heat-sink surface that is added to the PWP can be a ground plane or left electrically isolated. In TO220-type surface-mount packages, the thermal connection is also the primary electrical connection for a given terminal which is not always ground. The PWP package provides up to 24 independent leads that can be used as inputs and outputs (**Note:** leads 1, 12, 13, and 24 are internally connected to the thermal pad and the IC substrate).

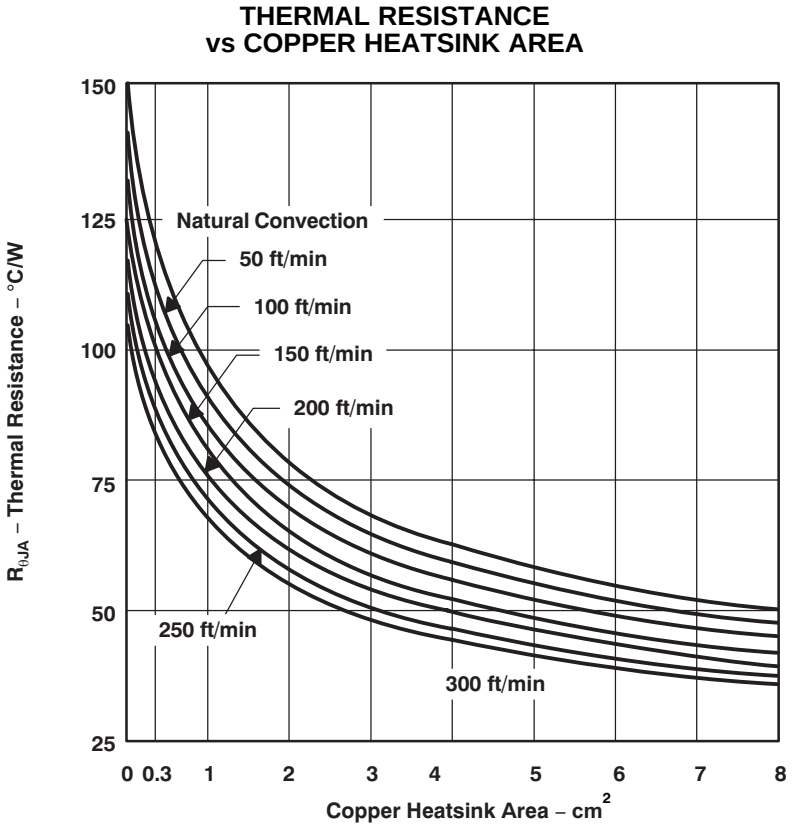


Figure 34.

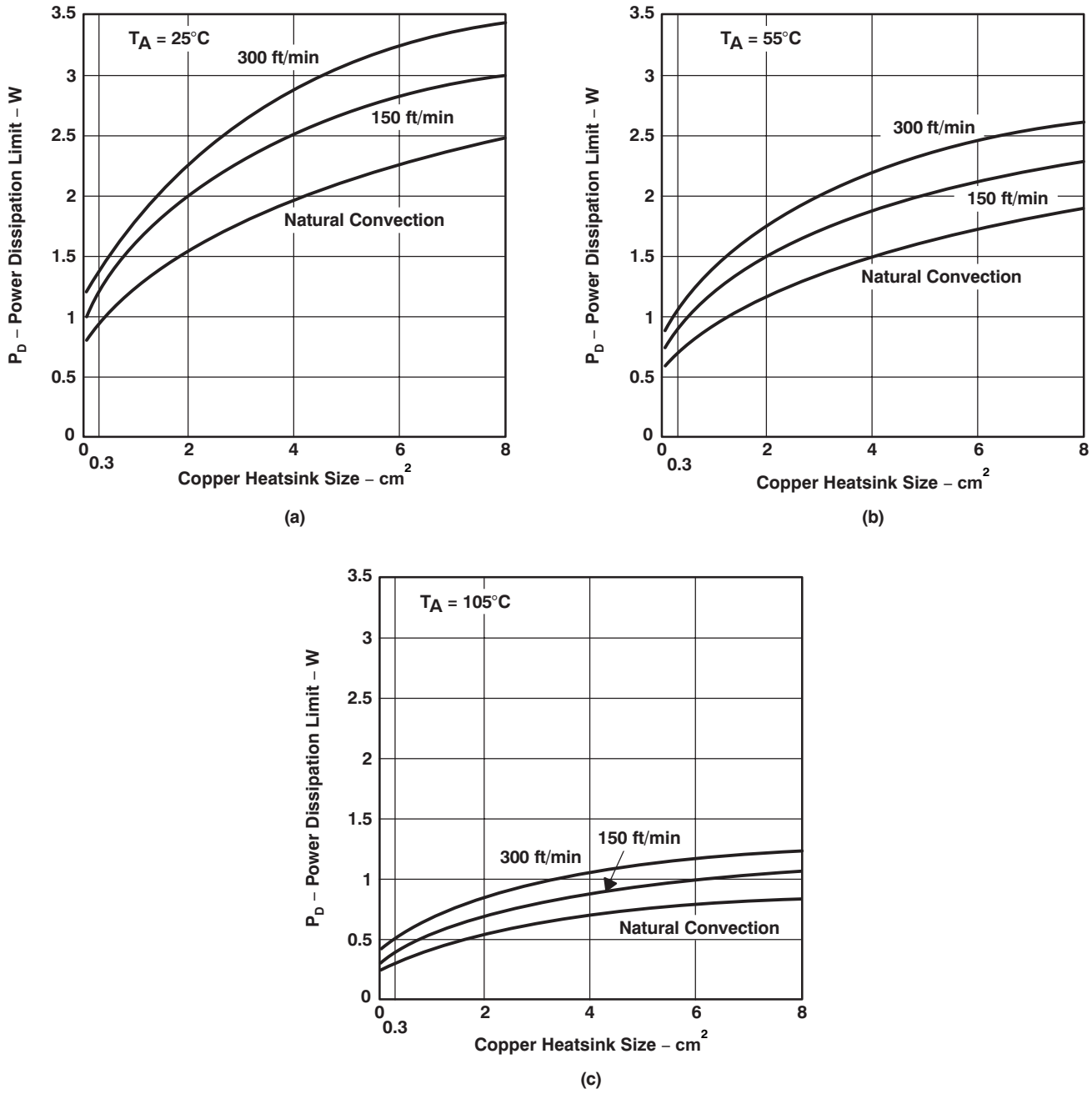
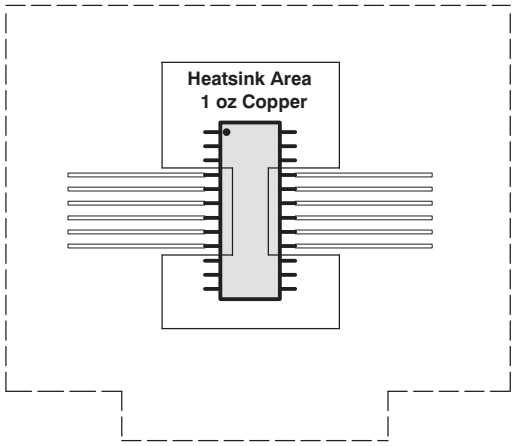


Figure 35. Power Ratings of the PWP Package at Ambient Temperatures of +25°C, +55°C, and +105°C

Figure 36 is an example of a thermally-enhanced PWB layout for use with the new PWP package. This board configuration was used in the thermal experiments that generated the power ratings shown in Figure 34 and Figure 35. As discussed earlier, copper has been added on the PWB to conduct heat away from the device. $R_{\theta JA}$ for this assembly is illustrated in Figure 34 as a function of heat-sink area. A family of curves is included to illustrate the effect of airflow introduced into the system.



Board thickness	62 mils
Board size	3.2 in × 3.2 in
Board material	FR4
Copper trace/heat sink	1 oz
Exposed pad mounting	63/67 tin/lead solder

Figure 36. PWB Layout (Including Copper Heatsink Area) for Thermally-Enhanced PWP Package

From Figure 34, $R_{\theta JA}$ for a PWB assembly can be determined and used to calculate the maximum power-dissipation limit for the component/PWB assembly, with the equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA(system)}}$$

where:

- T_{Jmax} is the maximum specified junction temperature (+150°C absolute maximum limit, +125°C recommended operating limit) and T_A is the ambient temperature. (1)

$P_{D(max)}$ should then be applied to the internal power dissipated by the TPS703xx regulator. The equation for calculating total internal power dissipation of the TPS703xx is:

$$P_{D(total)} = \left(V_{IN1} - V_{OUT1}\right) \times I_{OUT1} + V_{IN1} \times \frac{I_Q}{2} + \left(V_{IN2} - V_{OUT2}\right) \times I_{OUT2} + V_{IN2} \times \frac{I_Q}{2} \quad (2)$$

Since the quiescent current of the TPS703xx is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = \left(V_{IN1} - V_{OUT1}\right) \times I_{OUT1} + \left(V_{IN2} - V_{OUT2}\right) \times I_{OUT2} \quad (3)$$

For the case where T_A = +55°C, airflow = 200 ft/min, copper heat-sink area = 4 cm^2, the maximum power-dissipation limit can be calculated. First, from Figure 34, we find the system $R_{\theta JA}$ is +50°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA(system)}} = \frac{+125°C - 55°C}{+50°C/W} = 1.4\ W \quad (4)$$

If the system implements a TPS703xx regulator, where V_{IN1} = 5.0V, V_{IN2} = 2.8 V, I_{OUT1} = 500 mA, and I_{OUT2} = 800 mA, the internal power dissipation is:

$$P_{D(total)} = \left(V_{IN1} - V_{OUT1}\right) \times I_{OUT1} + \left(V_{IN2} - V_{OUT2}\right) \times I_{OUT2}$$
$$= (5.0 - 3.3) \times 0.5 + (2.8 - 1.8) \times 0.8 = 1.65\ W \quad (5)$$

Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the calculated limit. When it does, one of two corrective actions should be made: raising the power-dissipation limit by increasing the airflow or the heat-sink area, or lowering the internal power dissipation of the regulator by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters. This parameter is measured with the recommended copper heat sink pattern on a 4-layer PWB, 2 oz. copper traces on 4-in × 4-in ground layer. Simultaneous and continuous operation of both regulator outputs at full load may exceed the power dissipation rating of the PWP package.

Mounting Information

The primary requirement is to complete the thermal contact between the thermal pad and the PWB metal. The thermal pad is a solderable surface and is fully intended to be soldered at the time the component is mounted. Although voiding in the thermal-pad solder-connection is not desirable, up to 50% voiding is acceptable. The data included in Figure 34 and Figure 36 are for soldered connections with voiding between 20% and 50%. The thermal analysis shows no significant difference resulting from the variation in voiding percentage.

Figure 37 shows the solder-mask land pattern for the PWP package. The minimum recommended heat-sink area is also illustrated. This is simply a copper plane under the body extent of the package, including metal routed under terminals 1, 12, 13, and 24.

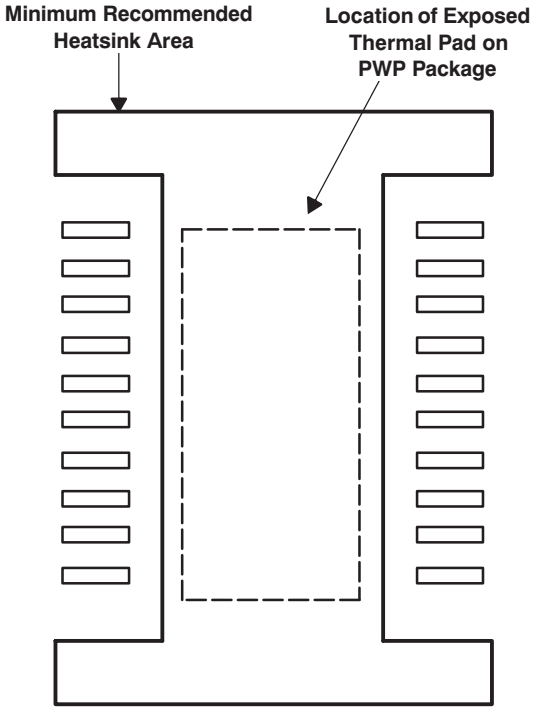


Figure 37. PWP Package Land Pattern

APPLICATION INFORMATION

Sequencing Timing Diagrams

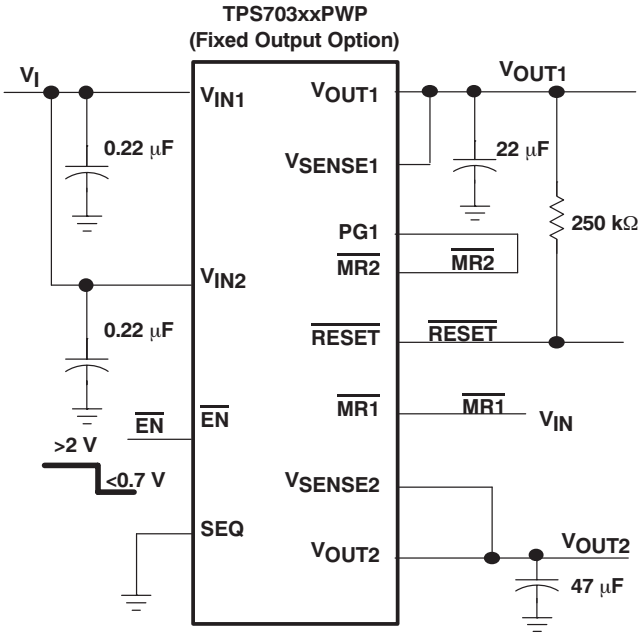
This section provides a number of timing diagrams showing how this device functions in different configurations.

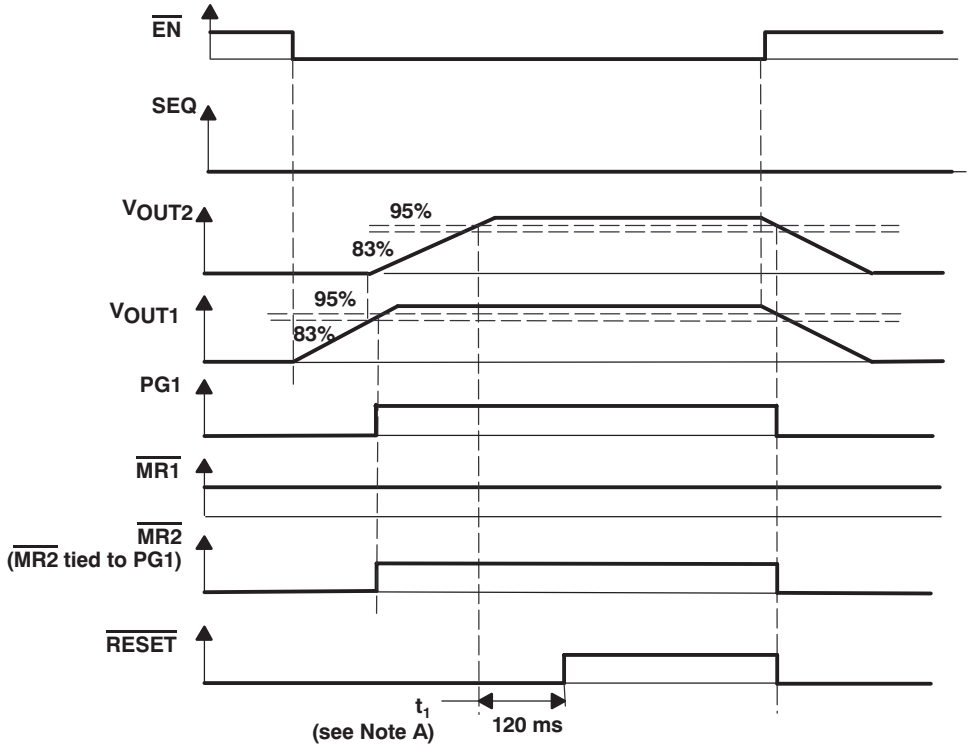
Application conditions not shown in block diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than V_{UVLO}; SEQ is tied to logic low; PG1 is tied to $\overline{MR2}$; $\overline{MR1}$ is not used and is connected to V_{IN}.

Explanation of timing diagrams:

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic low, when $\overline{EN}$ is taken to logic low, V_{OUT1} turns on. V_{OUT2} turns on after V_{OUT1} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay. When $\overline{EN}$ returns to a logic high, both devices power down and both PG1 (tied to $\overline{MR2}$) and $\overline{RESET}$ return to logic low.





NOTE A: t_1: Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

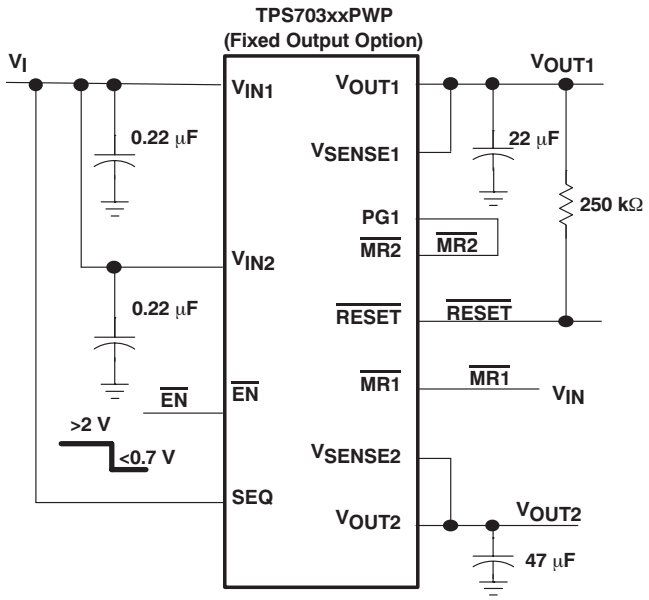
Figure 38. Timing When SEQ = Low

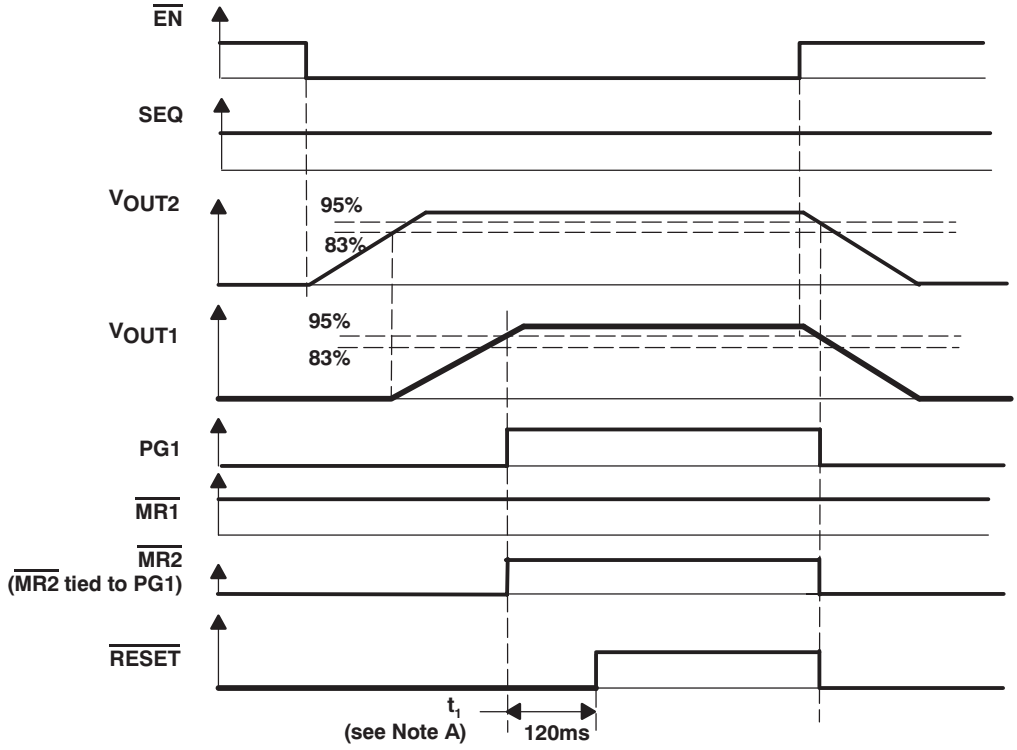
Application conditions not shown in block diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than V_{UVLO}; SEQ is tied to logic high; PG1 is tied to $\overline{MR2}$; $\overline{MR1}$ is not used and is connected to V_{IN}.

Explanation of timing diagrams:

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken to logic low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay. When $\overline{EN}$ returns to logic high, both devices turn off and both PG1 (tied to $\overline{MR2}$) and $\overline{RESET}$ return to logic low.



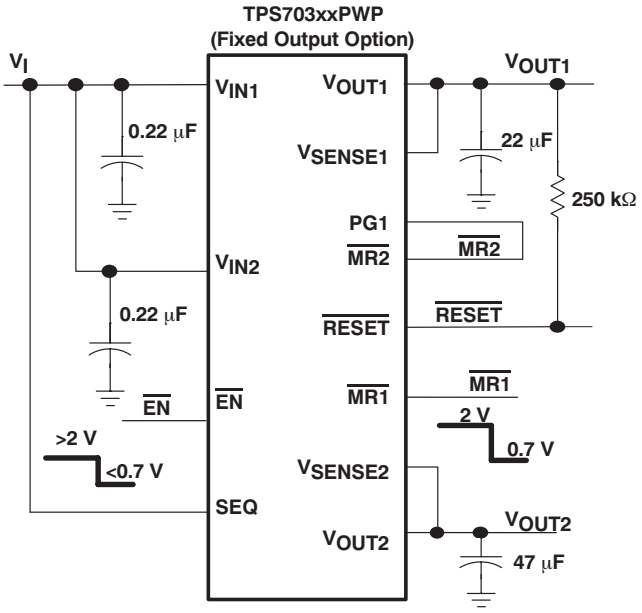


NOTE A: t_1: Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 39. Timing When SEQ = High

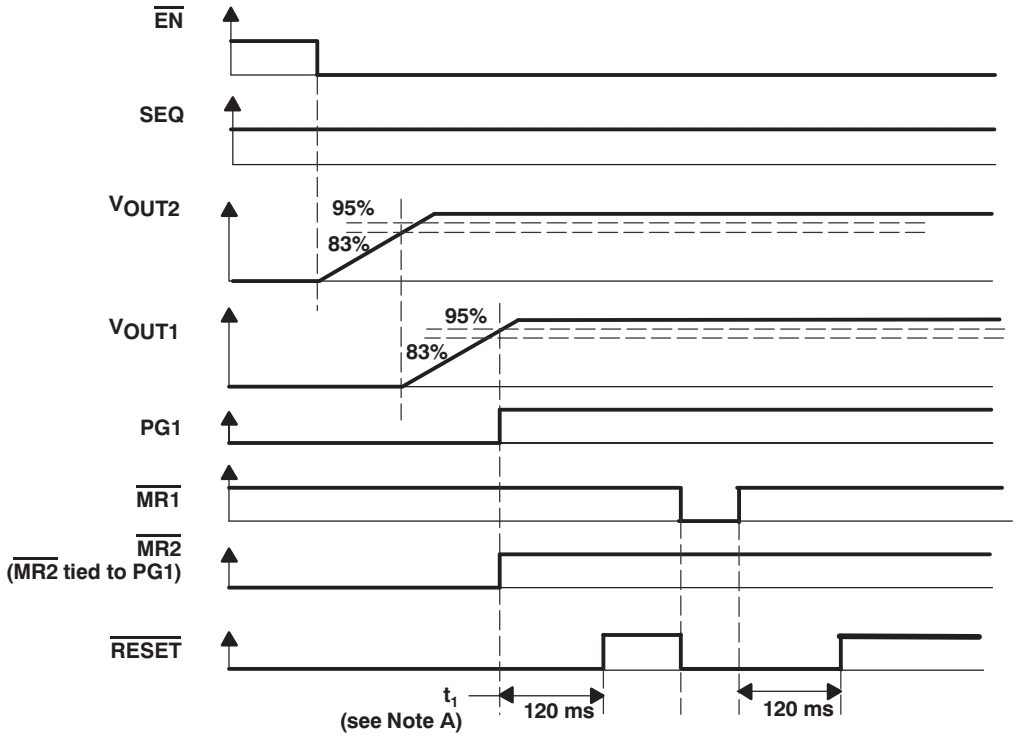
Application conditions not shown in block diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than V_{UVLO}; SEQ is tied to logic high; PG1 is tied to $\overline{MR2}$; $\overline{MR1}$ is initially at logic high but is eventually toggled.



Explanation of timing diagrams:

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay. When $\overline{MR1}$ is taken low, $\overline{RESET}$ returns to logic low but the outputs remain in regulation. When $\overline{MR1}$ returns to logic high, because both V_{OUT1} and V_{OUT2} remain above 95% of their respective regulated output voltages and $\overline{MR2}$ (tied to PG1) remains at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay.



NOTE A: t_1: Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

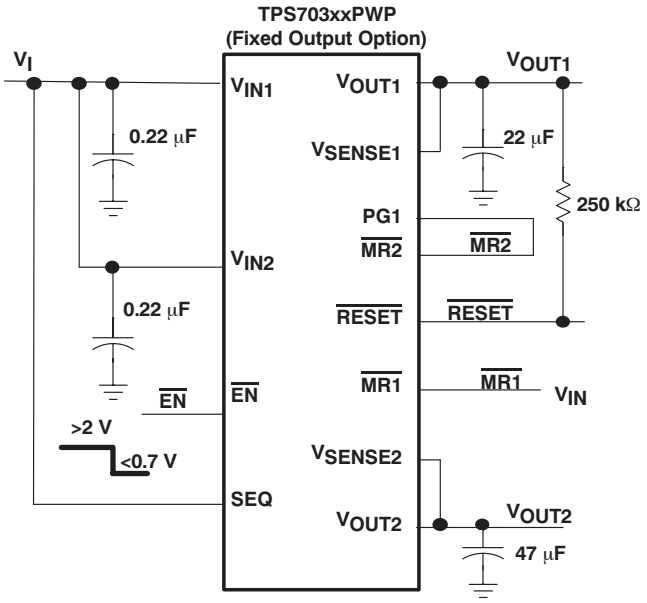
Figure 40. Timing When $\overline{MR1}$ is Toggled

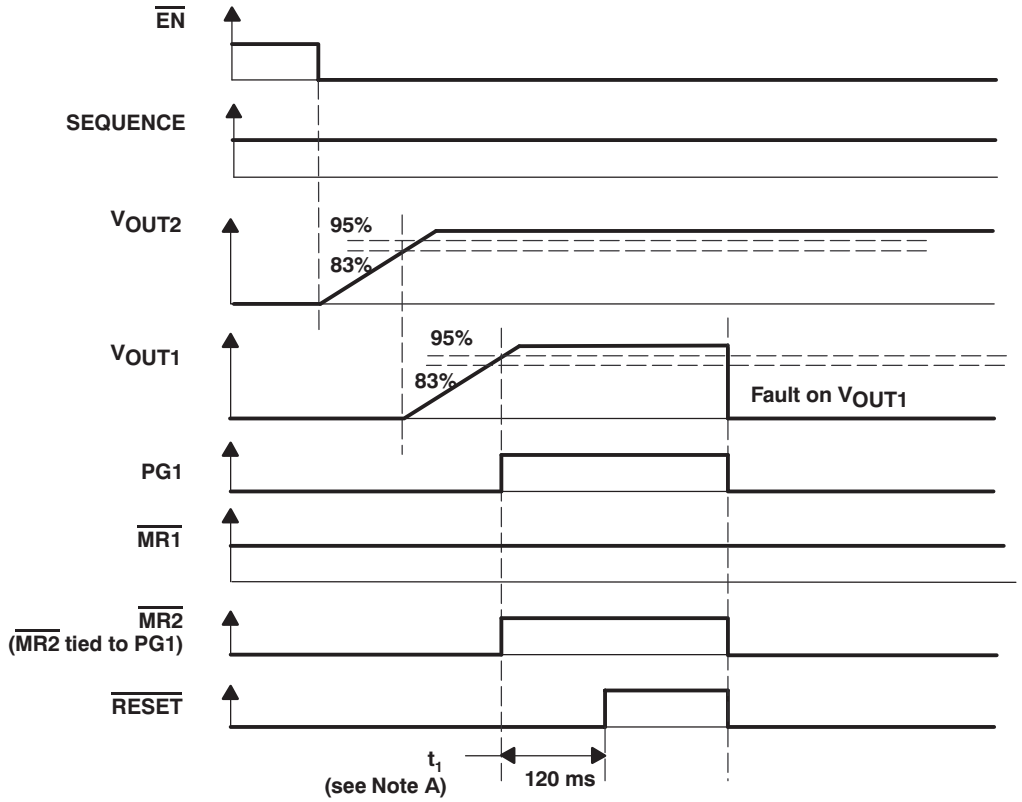
Application conditions not shown in block diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than V_{UVLO}; SEQ is tied to logic high; PG1 is tied to $\overline{MR2}$; $\overline{MR1}$ is not used and is connected to V_{IN}.

Explanation of timing diagrams:

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay. When a fault on V_{OUT1} causes it to fall below 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic low.





NOTE A: t_1: Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

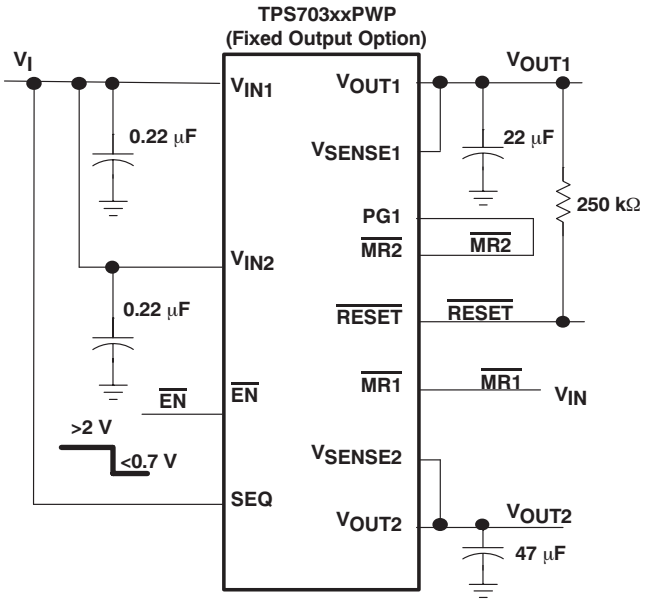
Figure 41. Timing When a Fault Occurs on V_{OUT1}

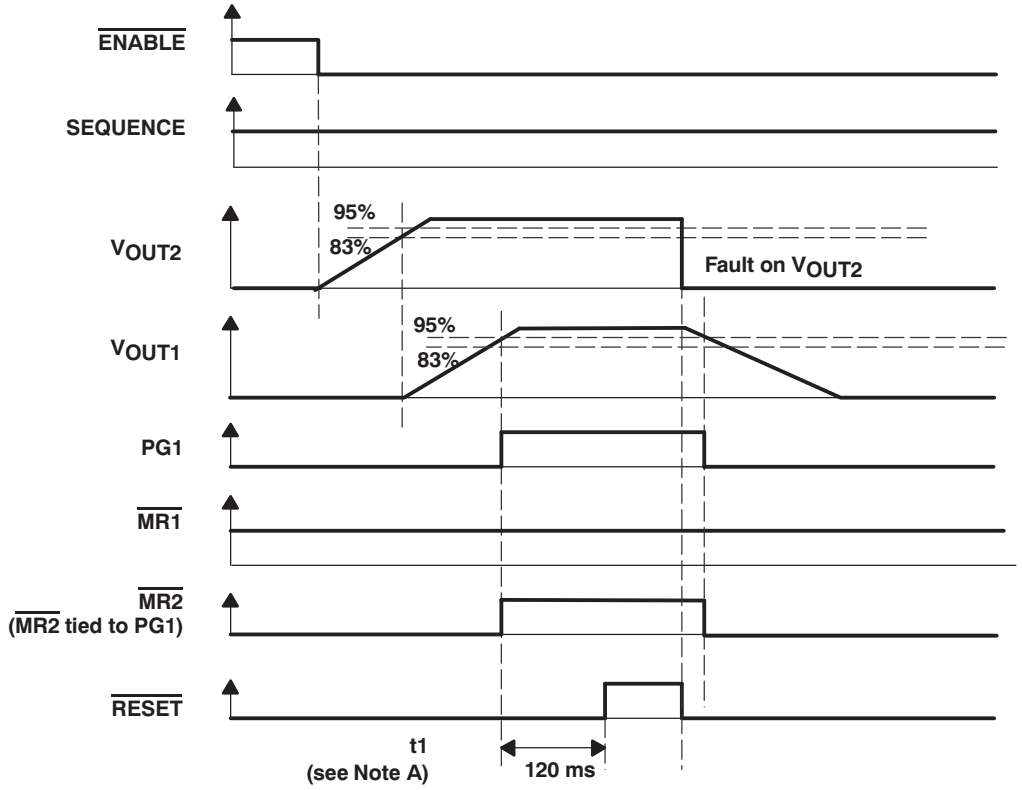
Application conditions not shown in block diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than V_{UVLO}; SEQ is tied to logic high; PG1 is tied to $\overline{MR2}$; $\overline{MR1}$ is not used and is connected to V_{IN}.

Explanation of timing diagrams:

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken low, V_{OUT2}turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay. When a fault on V_{OUT2} causes it to fall below 95% of its regulated output voltage, $\overline{RESET}$ returns to logic low and V_{OUT1} begins to power down because SEQ is high. When V_{OUT1} falls below 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) returns to logic low.





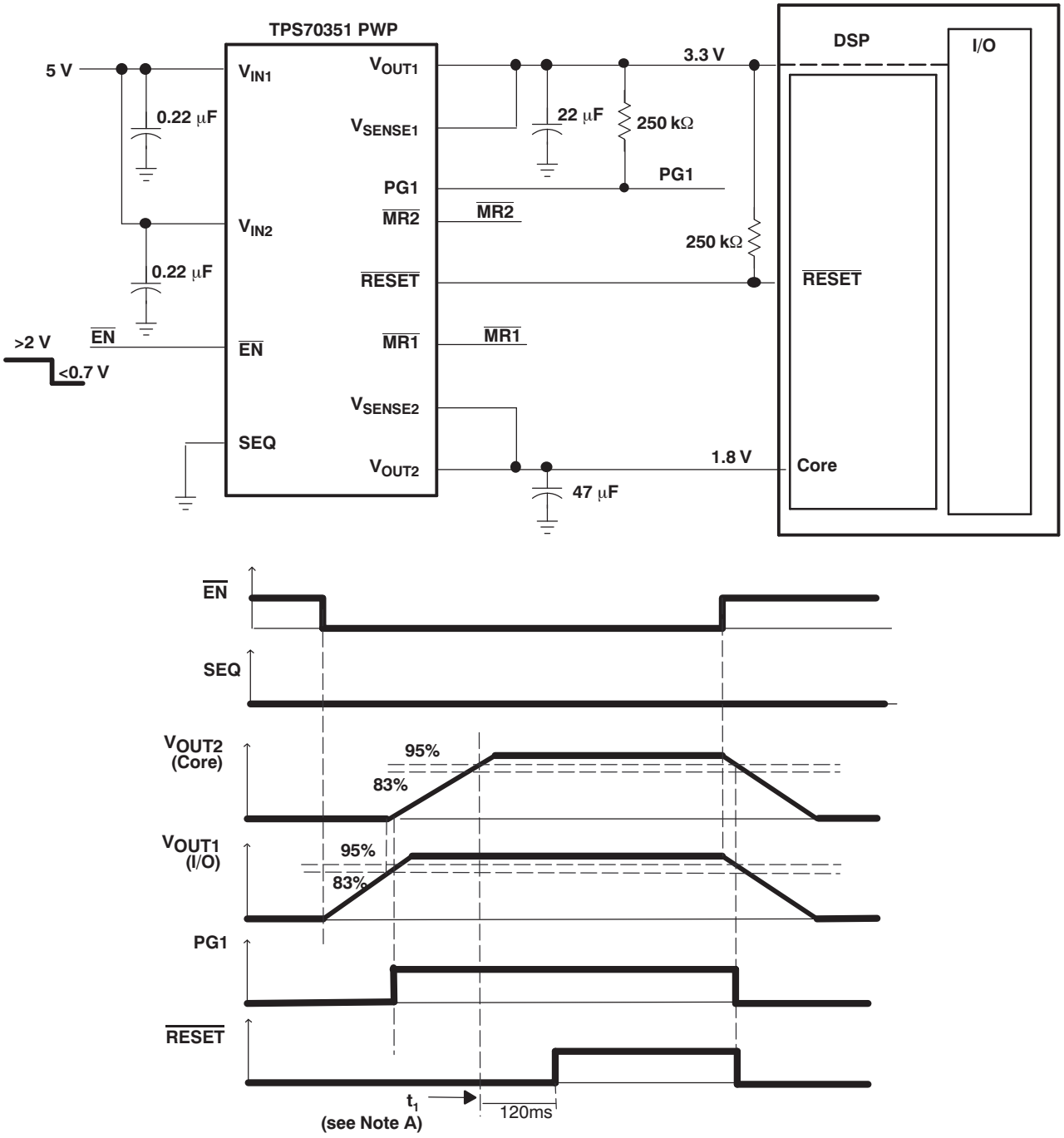
NOTE A: t_1: Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 42. Timing When a Fault Occurs on V_{OUT2}

APPLICATION INFORMATION

Split Voltage DSP Application

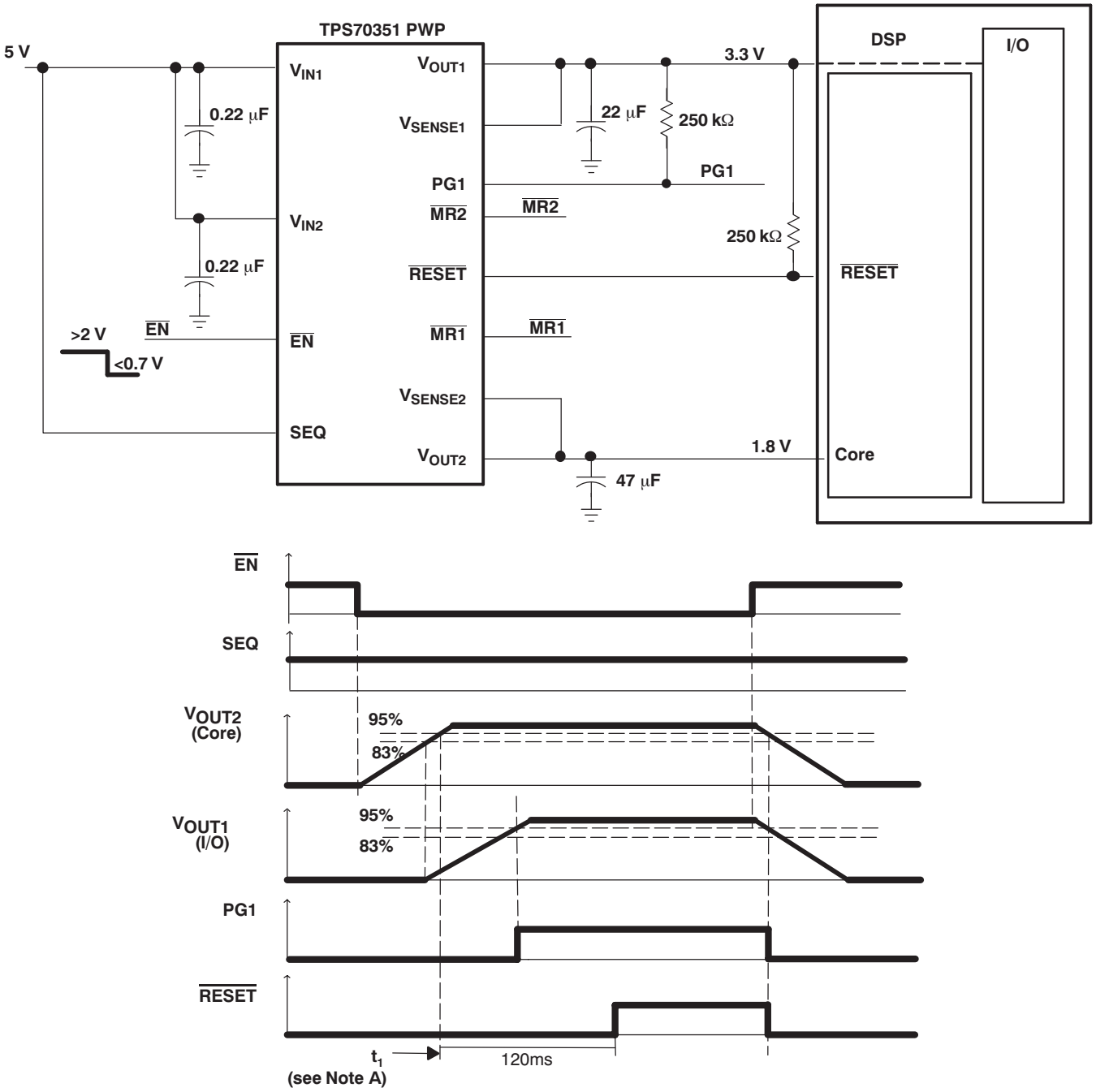
Figure 43 shows a typical application where the TPS70351 is powering up a DSP. In this application, by grounding the SEQ pin, V_{OUT1} (I/O) powers up first, and then V_{OUT2} (core).



NOTE A: t_1: Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 43. Application Timing Diagram (SEQ = Low)

Figure 44 shows a typical application where the TPS70351 is powering up a DSP. In this application, by pulling up the SEQ pin, V_{OUT2} (core) powers up first, and then V_{OUT1} (I/O).



NOTE A: t_1: Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 44. Application Timing Diagram (SEQ = High)

Input Capacitor

For a typical application, a ceramic input bypass capacitor (0.22 μF to 1 μF) is recommended to ensure device stability. This capacitor should be as close as possible to the input pin. Because of the impedance of the input supply, large transient currents cause the input voltage to droop. If this droop causes the input voltage to drop below the UVLO threshold, the device turns off. Therefore, it is recommended that a larger capacitor be placed in parallel with the ceramic bypass capacitor at the regulator input. The size of this capacitor depends on the output current, response time of the main power supply, and the main power supply distance to the regulator. At a minimum, the capacitor should be sized to ensure that the input voltage does not drop below the minimum UVLO threshold voltage during normal operating conditions.

Output Capacitor

As with most LDO regulators, the TPS703xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value for V_{OUT1} is 22 μF and the ESR (equivalent series resistance) must be between 50 mΩ and 800 mΩ. The minimum recommended capacitance value for V_{OUT2} is 47μF and the ESR must be between 50 mΩ and 2 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Larger capacitors provide a wider range of stability and better load transient response. Table 1 gives a partial listing of surface-mount capacitors suitable for use with the TPS703xx for fast transient response applications.

This information, along with the ESR graphs, is included to assist in selection of suitable capacitance for user applications. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

Table 1. Partial Listing of TPS703xx-Compatible Surface-Mount Capacitors

VALUE	MANUFACTURER	MFR PART NO.
680 μF	Kemet	T510X6871004AS
470 μF	Sanyo	4TPB470M
150 μF	Sanyo	4TPC150M
220 μF	Sanyo	2R5TPC220M
100 μF	Sanyo	6TPC100M
68 μF	Sanyo	10TPC68M
68 μF	Kemet	T495D6861006AS
47 μF	Kemet	T495D4761010AS
33 μF	Kemet	T495C3361016AS
22 μF	Kemet	T495C2261010AS

Programming the TPS70302 Adjustable LDO Regulator

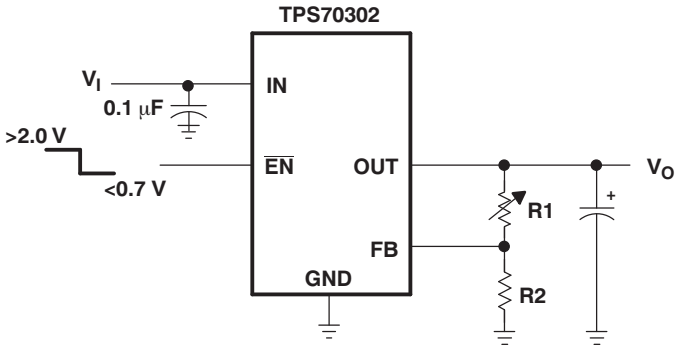
The output voltage of the TPS70302 adjustable regulators is programmed using external resistor dividers as shown in Figure 45.

Resistors R1 and R2 should be chosen for approximately a 50 μA divider current. Lower value resistors can be used, but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at the sense terminal increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at approximately 50 μA, and then calculate R1 using Equation 6:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (6)$$

where:

- V_{REF} = 1.224 V typ (the internal reference voltage)



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	31.6	30.1	kΩ
3.3 V	51.1	30.1	kΩ
3.6 V	59.0	30.1	kΩ

Figure 45. TPS70302 Adjustable LDO Regulator Programming

Regulator Protection

Both TPS703xx PMOS-pass transistors have built-in back diodes that conduct reverse currents when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS703xx also features internal current limiting and thermal protection. During normal operation, the TPS703xx regulator 1 limits output current to approximately 1.75 A (typ) and regulator 2 limits output current to approximately 3.8 A (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds +150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below +130°C (typ), regulator operation resumes.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (December 2009) to Revision H	Page
• Changed *Tube* transport media, quantity value from *70* to *60* in Ordering Information table	3

Changes from Revision F (September 2009) to Revision G	Page
• Changed *Dissipation Ratings* table	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS70302PWP	ACTIVE	HTSSOP	PWP	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70302	Samples
TPS70302PWPG4	ACTIVE	HTSSOP	PWP	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70302	Samples
TPS70302PWPR	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70302	Samples
TPS70345PWP	ACTIVE	HTSSOP	PWP	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70345	Samples
TPS70345PWPG4	ACTIVE	HTSSOP	PWP	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70345	Samples
TPS70345PWPR	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70345	Samples
TPS70348PWP	ACTIVE	HTSSOP	PWP	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70348	Samples
TPS70348PWPR	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70348	Samples
TPS70351PWP	ACTIVE	HTSSOP	PWP	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70351	Samples
TPS70351PWPG4	ACTIVE	HTSSOP	PWP	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70351	Samples
TPS70351PWPR	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70351	Samples
TPS70358PWP	ACTIVE	HTSSOP	PWP	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70358	Samples
TPS70358PWPR	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70358	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

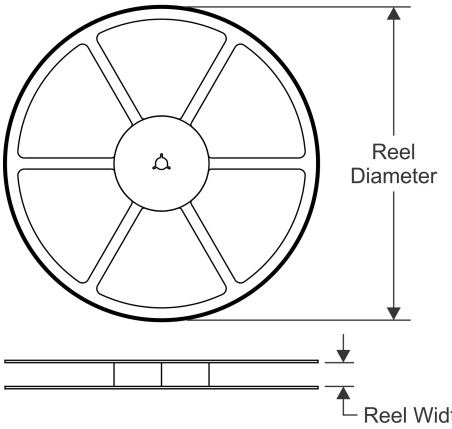
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

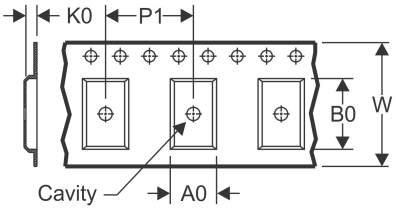
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

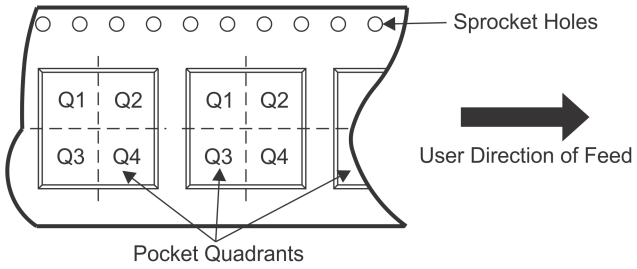


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

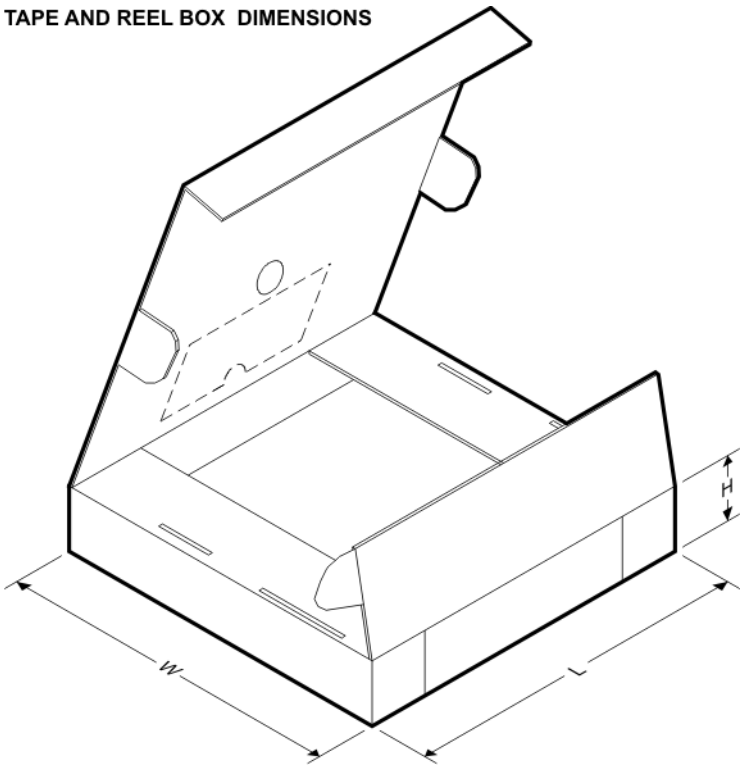
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70302PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS70345PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS70348PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS70351PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS70358PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

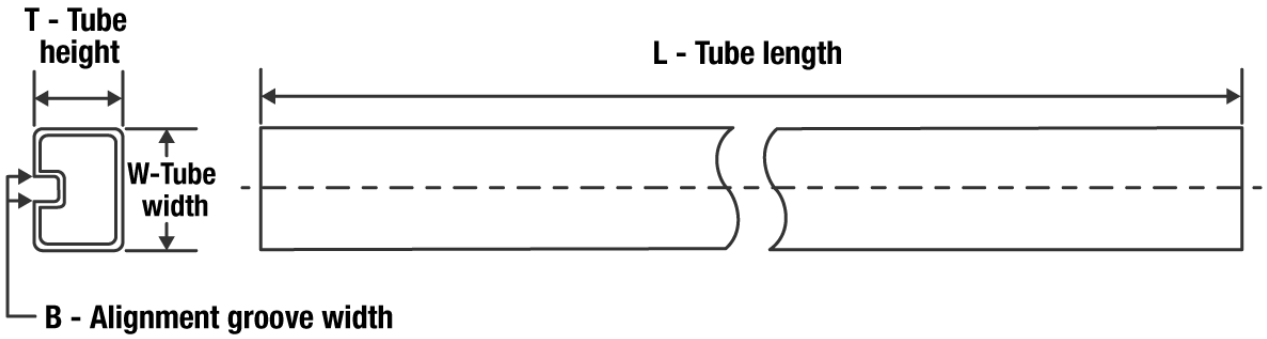
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70302PWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0
TPS70345PWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0
TPS70348PWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0
TPS70351PWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0
TPS70358PWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS70302PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5
TPS70302PWPG4	PWP	HTSSOP	24	60	530	10.2	3600	3.5
TPS70345PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5
TPS70345PWPG4	PWP	HTSSOP	24	60	530	10.2	3600	3.5
TPS70348PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5
TPS70351PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5
TPS70351PWPG4	PWP	HTSSOP	24	60	530	10.2	3600	3.5
TPS70358PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

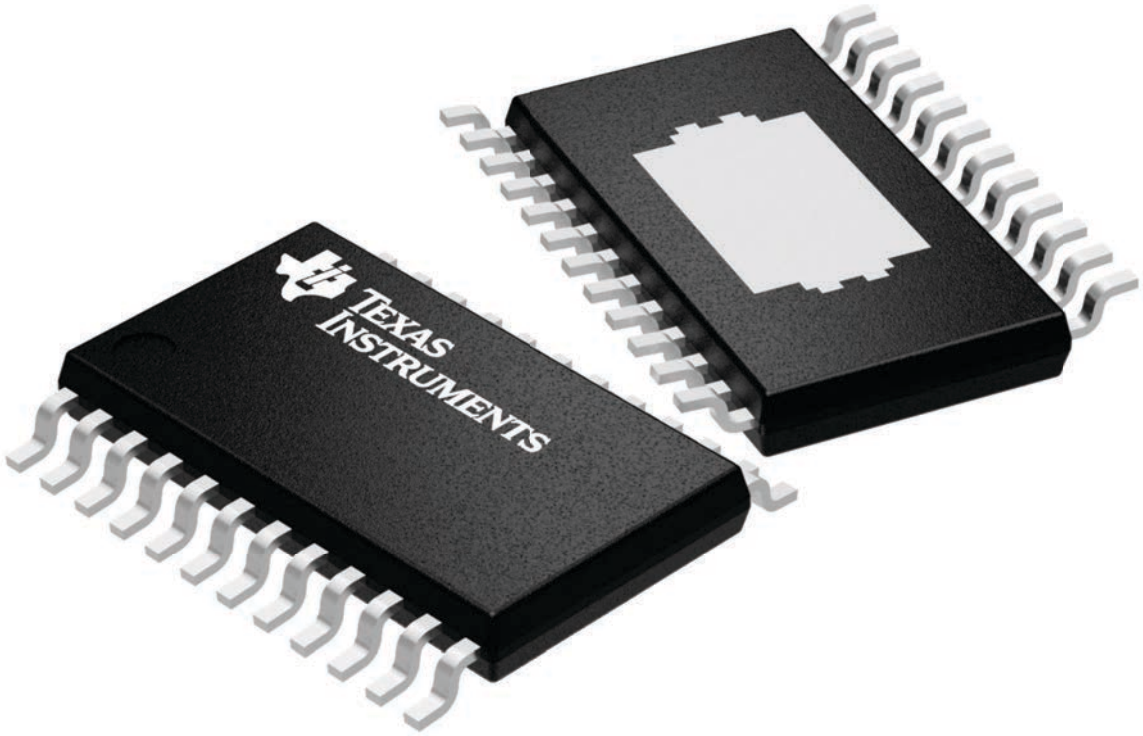
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

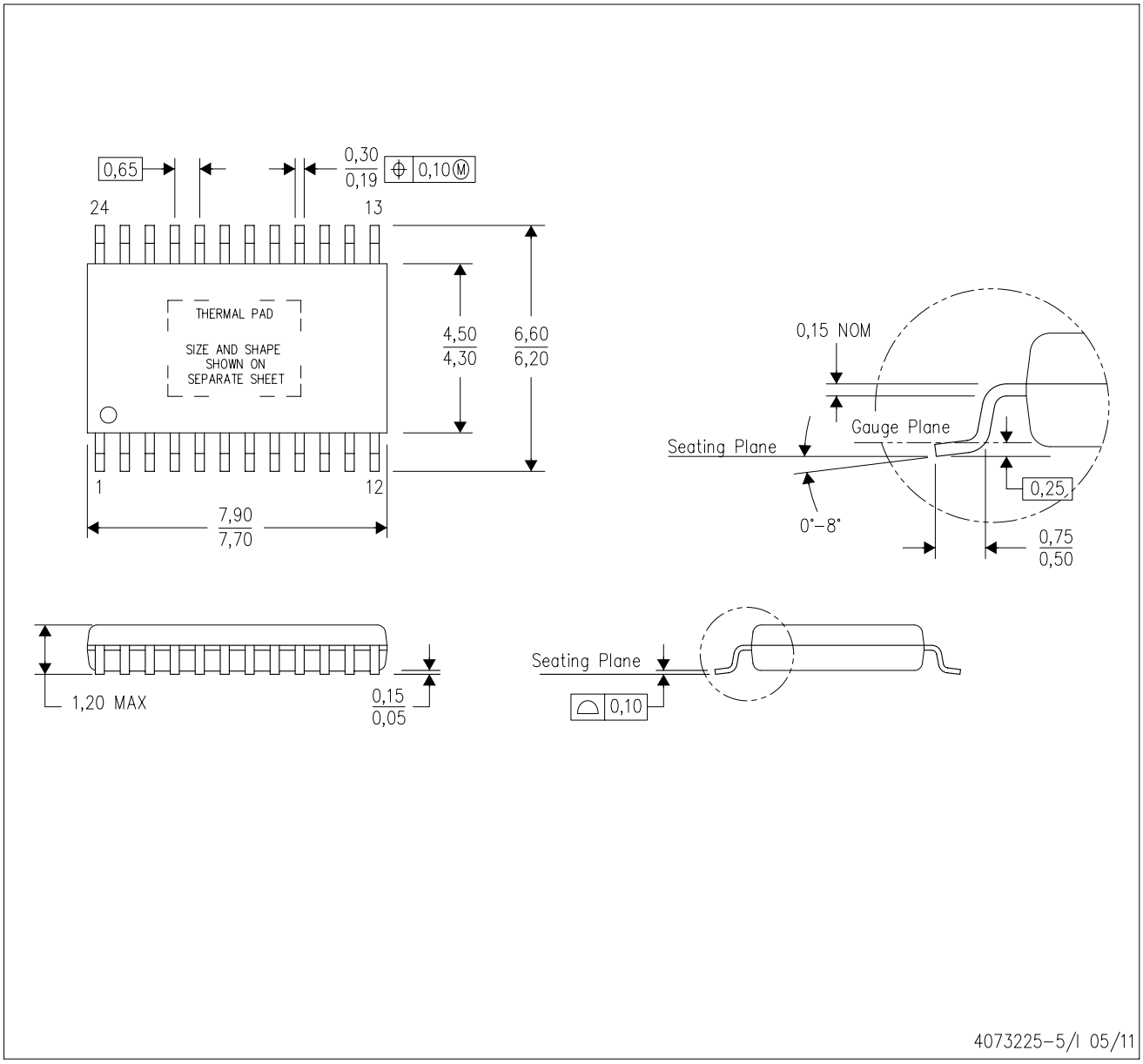
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

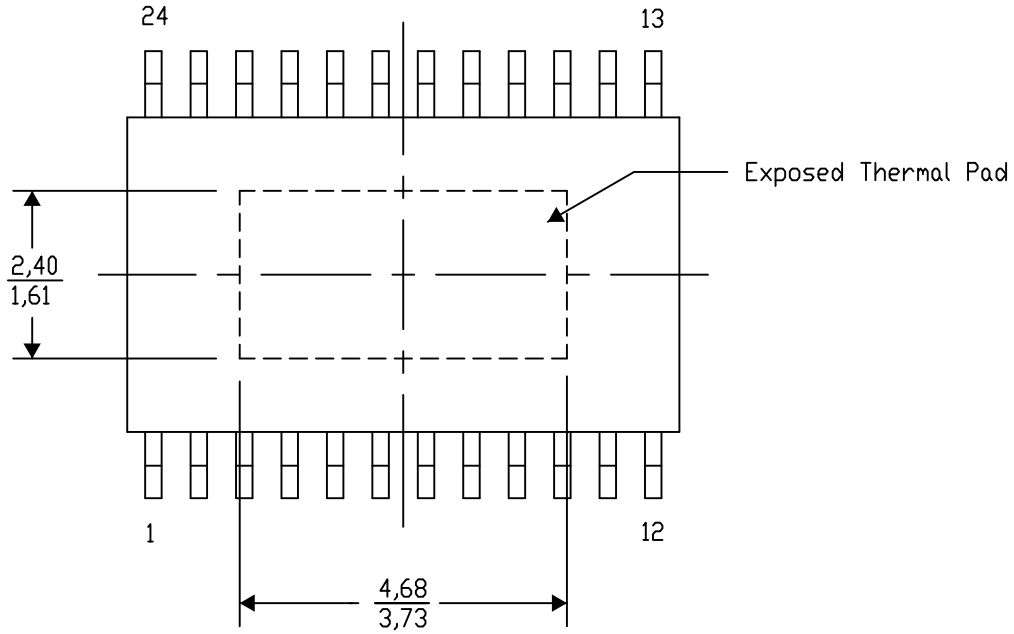
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

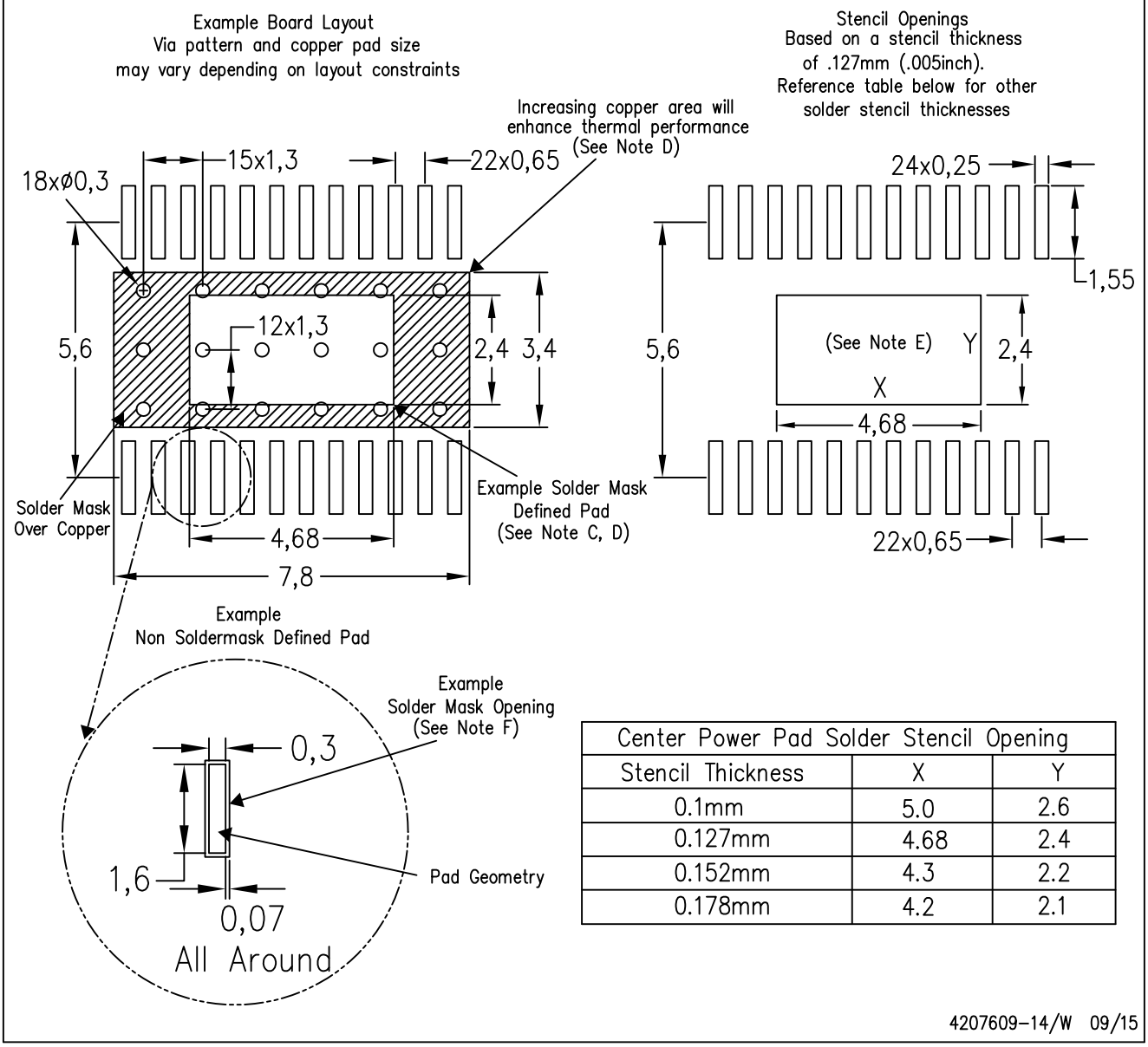
Exposed Thermal Pad Dimensions

4206332–27/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE

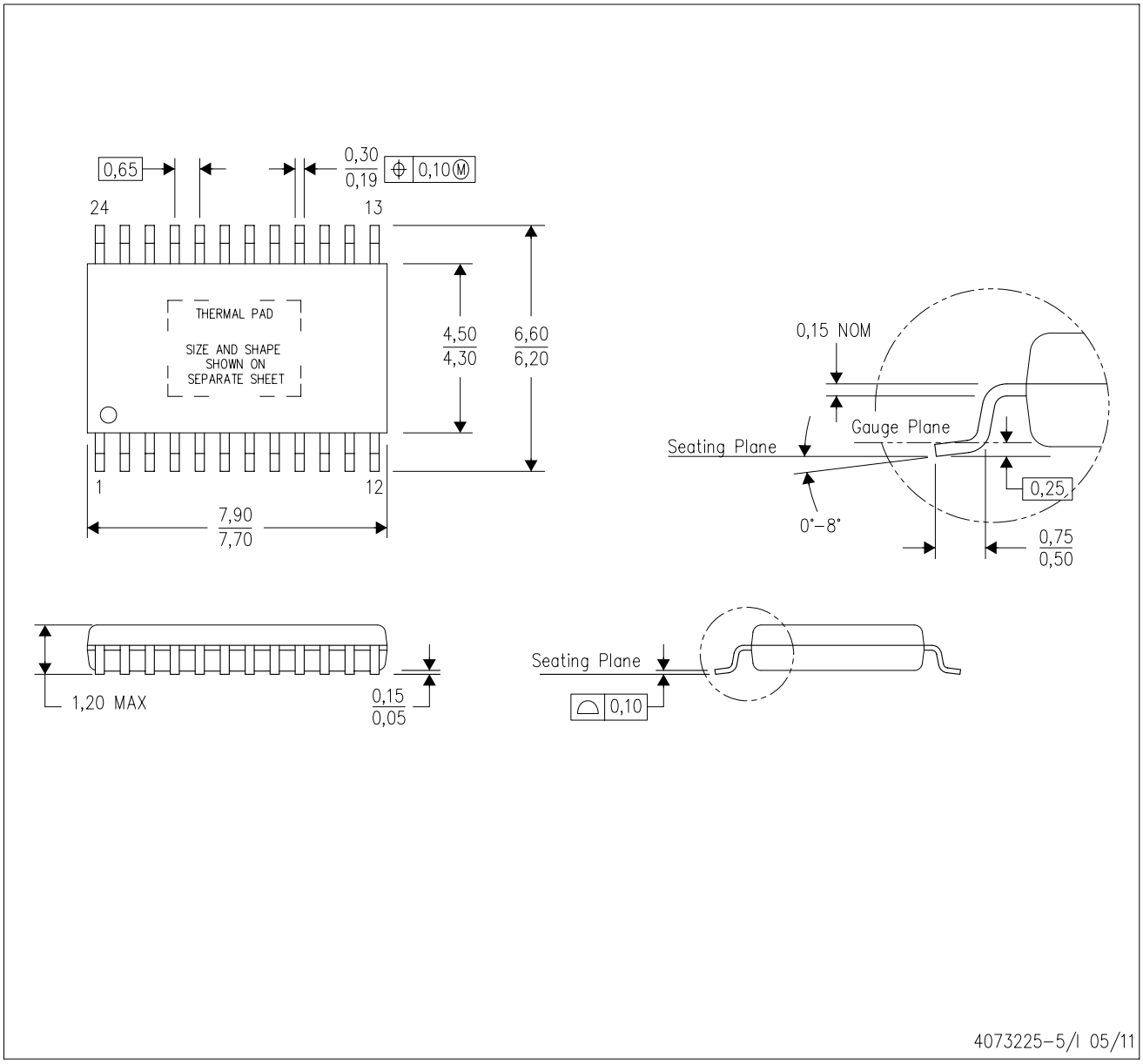


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.0	2.6
0.127mm	4.68	2.4
0.152mm	4.3	2.2
0.178mm	4.2	2.1

4207609–14/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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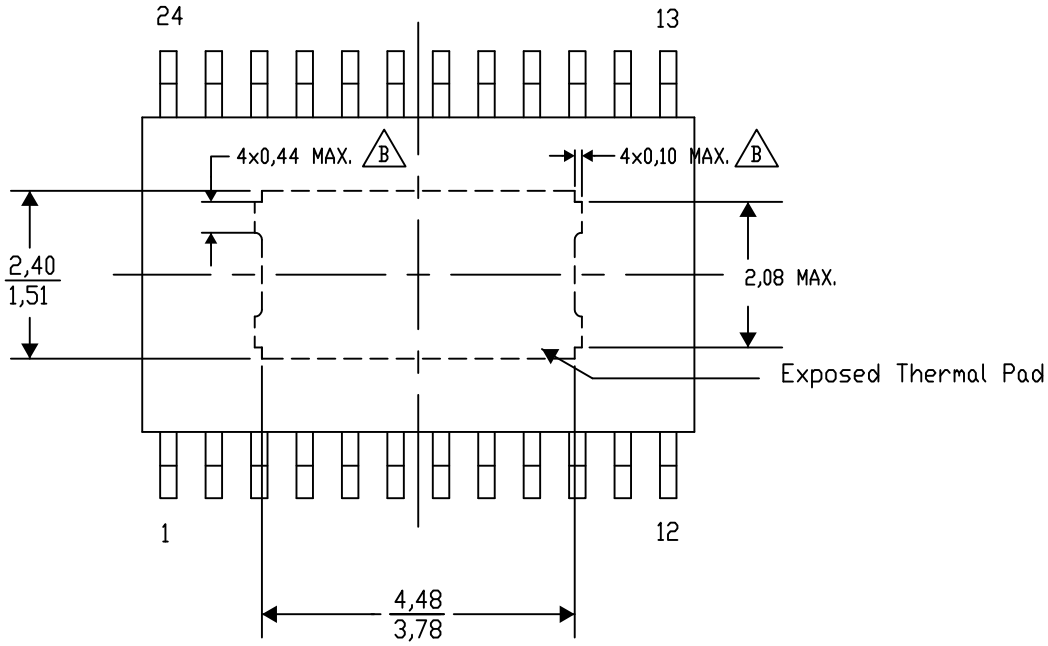
The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–42/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265