4 Megabyte Sync/Sync Burst, Dual Key DIMM

FEATURES

- 4x128Kx72 Synchronous, Synchronous Burst
- Flow-Through Architecture
- Linear and Sequential Burst Support via MODE pin
- Clock Controlled Registered Module Enable (EM#)
- Clock Controlled Registered Bank Enables (E1#, E2#, E3#, E4#)
- Clock Controlled Byte Write Mode Enable (BWE#)
- Clock Controlled Byte Write Enables (BW1# - BW8#)
- Clock Controlled Registered Address
- Clock Controlled Registered Global Write (GW#)
- Aysnchronous Output Enable (G#)
- Internally Self-timed Write
- Individual Bank Sleep Mode enables (ZZ_1, ZZ_2, ZZ_3, ZZ_4)
- Gold Lead Finish
- 3.3V $\pm$10% Operation
- Access Speed(s): TKHQV=8.5, 10, 12, 15ns
- Common Data I/O
- High Capacitance (30pf) drive, at rated Access Speed
- Single Total Array Clock
- Multiple Vcc and Gnd

DESCRIPTION

The EDI2CG472128VxxD2 is a Synchronous/Synchronous Burst SRAM, 84 position Dual Key; Double High DIMM (168 contacts) Module, organized as 4x128Kx72. The Module contains eight (8) Synchronous Burst Ram Devices, packaged in the industry standard JEDEC 14mmx20mm TQFP placed on a Multilayer FR4 Substrate. The module architecture is defined as a Sync/Sync Burst, Flow-Through, with support for either linear or sequential burst. This module provides High Performance, 2-1-1-1 accesses when used in Burst Mode, and used as a Synchronous Only Mode, provides a high performance cost advantage over BiCMOS aysnchronous device architectures.

Synchronous Only operations are performed via strapping ADSC# Low, and ADSP# / ADV# High, which provides for Ultra Fast Accesses in Read Mode while providing for internally self-timed Early Writes.

Synchronous/Synchronous Burst operations are in relation to an externally supplied clock, Registered Address, Registered Global Write, Registered Enables as well as an Asynchronous Output enable. This Module has been defined with full flexibility, which allows individual control of each of the eight bytes, as well as Quad Words in both Read and Write Operations.

*This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

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PIN CONFIGURATION

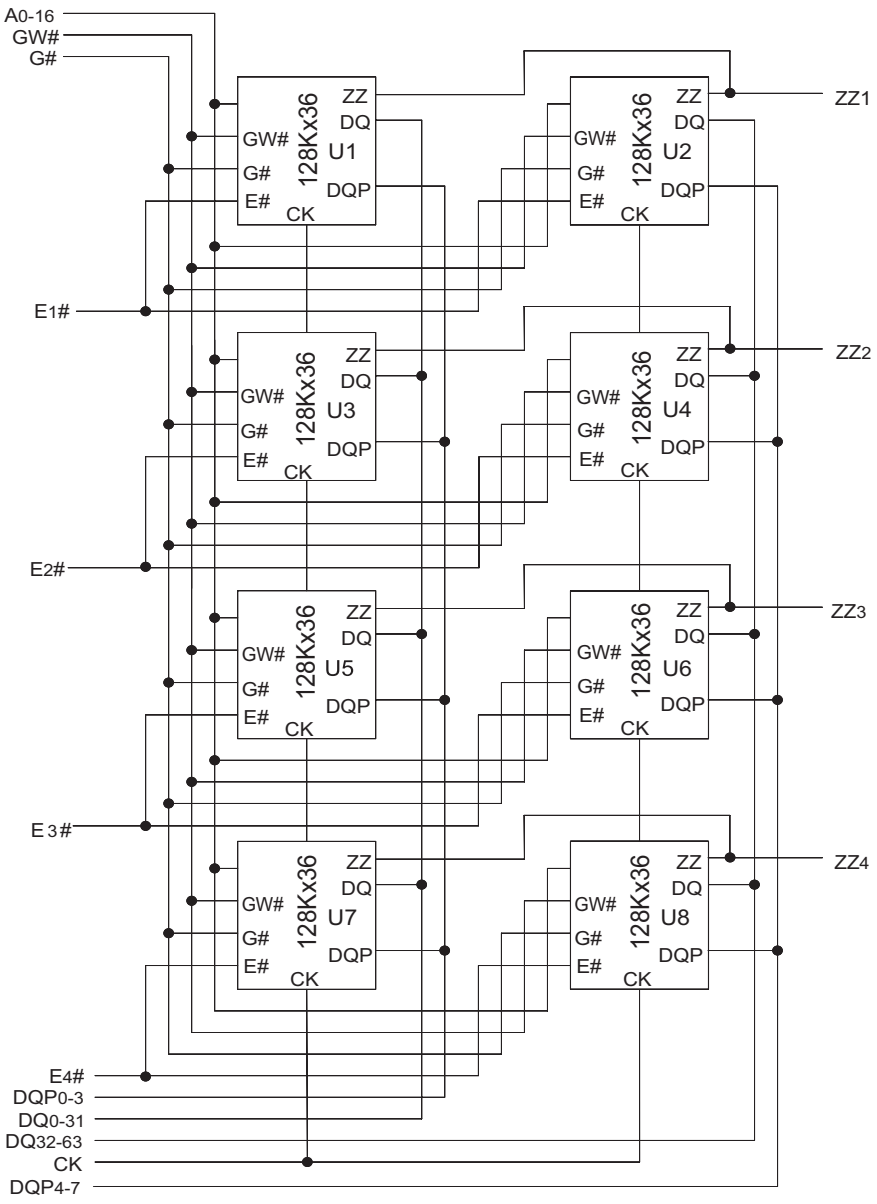
PIN	FRONT	PIN	BACK
1	V_{SS}	85	V_{SS}
2	A0	86	A_{17}
3	A_{16}	87	A_1
4	A_2	88	A_{15}
5	A_{14}	89	A_3
6	V_{CC}	90	V_{CC}
7	A_4	91	A_{13}
8	A_{12}	92	A_5
9	A_6	93	A_{11}
10	A_{10}	94	A_7
11	V_{SS}	95	V_{SS}
12	A_8	96	A_9
13	NC	97	NC_3
14	E_4#	98	E_1#
15	E_2#	99	E_3#
16	V_{SS}	100	V_{SS}
17	MODE	101	CK
18	EM#	102	V_{SS}
19	GW#	103	G#
20	NC_1	104	BWE#
21	V_{CC}	105	V_{CC}
22	BW_4#	106	BW_2#
23	BW_3#	107	BW_1#
24	BW_8#	108	BW_6#
25	BW_7#	109	BW_5#
26	ADSC#	110	V_{SS}
27	ADSP#	111	ADV#
28	V_{SS}	112	V_{SS}
29	NC	113	DQP_0
30	V_{CC}	114	V_{CC}
31	DQ_0	115	DQ_7
32	DQ_1	116	DQ_6
33	DQ_2	117	DQ_5
34	DQ_3	118	DQ_4
35	V_{SS}	119	V_{SS}
36	ZZ_1	120	DQP_1
37	V_{CC}	121	V_{CC}
38	DQ_8	122	DQ_{15}
39	DQ_9	123	DQ_{14}
40	DQ_{10}	124	DQ_{13}
41	DQ_{11}	125	DQ_{12}
42	V_{SS}	126	V_{SS}

PIN	FRONT	PIN	BACK
43	NC	127	CRFU
44	V_{CC}	128	V_{CC}
45	DQ_{16}	129	DQ_{23}
46	DQ_{17}	130	DQ_{22}
47	DQ_{18}	131	DQ_{21}
48	DQ_{19}	132	DQ_{20}
49	V_{SS}	133	V_{SS}
50	ZZ_2	134	DQP_3
51	V_{CC}	135	V_{CC}
52	DQ_{24}	136	DQ_{31}
53	DQ_{25}	137	DQ_{30}
54	DQ_{26}	138	DQ_{29}
55	DQ_{27}	139	DQ_{28}
56	V_{SS}	140	V_{SS}
57	NC_5	141	DQP_4
58	V_{CC}	142	V_{CC}
59	DQ_{32}	143	DQ_{39}
60	DQ_{33}	144	DQ_{38}
61	DQ_{34}	145	DQ_{37}
62	DQ_{35}	146	DQ_{36}
63	V_{SS}	147	V_{SS}
64	ZZ_3	148	DQP_5
65	V_{CC}	149	V_{CC}
66	DQ_{40}	150	DQ_{47}
67	DQ_{41}	151	DQ_{46}
68	DQ_{42}	152	DQ_{45}
69	DQ_{43}	153	DQ_{44}
70	V_{SS}	154	V_{SS}
71	NC	155	DQP_6
72	V_{CC}	156	V_{CC}
73	DQ_{48}	157	DQ_{55}
74	DQ_{49}	158	DQ_{54}
75	DQ_{50}	159	DQ_{53}
76	DQ_{51}	160	DQ_{52}
77	V_{SS}	161	V_{SS}
78	ZZ_4	162	DQP_7
79	V_{CC}	163	V_{CC}
80	DQ_{56}	164	DQ_{63}
81	DQ_{57}	165	DQ_{62}
82	DQ_{58}	166	DQ_{61}
83	DQ_{59}	167	DQ_{60}
84	V_{SS}	168	V_{SS}

PIN NAMES

DQ0-DQ63	Input/Output Bus
DQP0-DQP7	Parity Bits
A0-A6	Address Bus
EM#	Module Enable
E1#, E2#, E3#, E4#	Synchronous Bank Enables
BWE#	Byte Write Mode Enable
BWE1#-BW8#	Byte Write Enables
CK	Array Clock
GW#	Synchronous Global Write Enable
G#	Asynchronous Output Enable
ZZ_1, ZZ_2, ZZ_3, ZZ_4	Blank Sleep Mode Enables
Vcc	3.3V Power Supply
Vss	Ground

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

DIMM Pins	Symbol	Type	Description
2, 87, 4, 89, 7, 92, 9, 94, 12, 96, 10, 93, 8, 91, 5, 88, 3	A0-A16	Input Synchronous	Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CK. The burst counter generates internal addresses associated with A0 and A1, during burst and wait cycle.
107, 106, 23, 22, 109, 108, 25, 24	BW1#, BW2#, BW3#, BW4#, BW5#, BW6#, BW7#, BW8#	Input Synchronous	Byte Write: A byte write is LOW for a WRITE cycle and HIGH for a READ cycle. BW0/ controls DQ0-7 and DQP0, BW1# controls DQ8-15 and DQP1. BW2# controls DQ16-23 and DQP2. BW3# controls DQ24-31 and DQP3. BW4# controls DQ32-39 and DQP4. BW5# controls DQ40-47 and DQP5. BW6# controls DQ48-55 and DQP6. BW7# controls DQ56-64 and DQP7.
104	BWE#	Input Synchronous	Write Enable: This active LOW input gates byte write operations and must meet the setup and hold times around the rising edge of CK.
19	GW#	Input Synchronous	Global Write: This active LOW input allows a full 72-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CK.
101	CK	Input Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98, 15, 99, 14	E1#, E2#, E3#, E4#	Input Synchronous	Bank Enables: These active LOW inputs are used to enable each individual bank and to gate ADSP#.
103	G#	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
111	ADV#	Input Synchronous	Address Status Processor: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
27	ADSP#	Input Synchronous	Address Status Processor: This active LOW input, along with EL# and EH# being LOW, causes a new external address to be registered and a READ cycle is initiated using the new address.
26	ADSC#	Input Synchronous	Address Status Controller: This active LOW input causes device to be de-selected or selected along with new external address to be registered. A READ or WRITE cycle is initiated depending upon write control inputs.
17	MODE	Input Static	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST.
36, 50, 64, 78	ZZ_1, ZZ_2, ZZ_3, ZZ_4	Input Asynchronous	Snooze: These active HIGH inputs put the individual banks in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (no connect).
Various	DQ0-63	Input/Output	Data Inputs/Outputs: First byte is DQ0-7, second byte is DQ8-15, third byte is DQ16-23, fourth byte is DQ24-31, fifth byte is DQ32-39, sixth byte is DQ40-47, seventh byte is DQ48-55 and the eight byte is DQ56-64.
113, 120, 127, 134, 141, 148, 155, 162	DQP0-7	Input/Output	Parity Inputs/Outputs: DQP0 is parity bit for DQ0-7. DQP1 is parity bit for DQ8-15. DQP2 is parity bit for DQ16-23. DQP3 is parity bit for DQ24-31. DQP4# is parity bit for DQ-32-39. DQP5 is parity bit for DQ40-47. DQP6# is parity bit for DQ48-55. DQP7 is parity bit for DQ56-64 and DQP7. In order to use the device configured as a 128K x 64, the parity bits need to be tied to V_{SS} through a 10K ohm resistor.
Various	Vcc	Supply	Core Power supply: +3.3V -5%/+10%
Various	Vss	Ground	Ground

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SYNCHRONOUS BURST - TRUTH TABLE

Operation	E1#	E2#	E3#	E4#	ADSP#	ADSC#	ADV#	GW#	G#	CK	DQ	Addr. Used
Deselected Cycle, Power Down; Bank 1	H	X	*	*	X	L	X	X	X	L-H	High-Z	None
Deselected Cycle, Power Down; Bank 2	X	H	*	*	X	L	X	X	X	L-H	High-Z	None
Read Cycle, Begin Burst; Bank 1	L	H	*	*	L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H	*	*	L	X	X	X	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	L	X	X	X	H	L-H	High-Z	External
Write Cycle, Begin Burst; Bank 1	L	H	*	*	H	L	X	L	X	L-H	D	External
Write Cycle, Begin Burst; Bank 2	H	L	*	*	H	L	X	L	X	L-H	D	External
Read Cycle, Begin Burst; Bank 1	L	H	*	*	H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H	*	*	H	L	X	H	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	H	L	X	H	H	L-H	High-Z	External
Read Cycle, Continue Burst; Bank 1	X	H	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	X	H	*	*	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	X	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	X	*	*	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 1	H	H	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	H	H	*	*	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	H	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	H	*	*	X	H	L	H	H	L-H	High-Z	Next
Write Cycle, Continue Burst; Bank 1	X	H	*	*	H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 1	H	H	*	*	X	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	X	*	*	H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	H	*	*	X	H	L	L	X	L-H	D	Next
Read Cycle, Suspend Burst; Bank 1	X	H	*	*	H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	X	H	*	*	H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	X	*	*	H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	X	*	*	H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 1	H	H	*	*	X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	H	H	*	*	X	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	H	*	*	X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	H	*	*	X	H	H	H	H	L-H	High-Z	Current
Write Cycle, Suspend Burst; Bank 1	X	H	*	*	H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 1	H	H	*	*	X	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	X	*	*	H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	H	*	*	X	H	H	L	X	L-H	D	Current

*All Truth Table Functions Repeat for Bank 3 (E3#) and Bank 4 (E4#)

SYNCHRONOUS ONLY - TRUTH TABLE

Operation	E1#	E2#	E3#	E4#	GW#	G#	ZZ	CK	DQ
Synchronous Write-Bank 1	L	H	H	H	L	H	L	↑	High-Z
Synchronous Read-Bank 1	L	H	H	H	H	L	L	↑	
Synchronous Write-Bank 2	H	L	H	H	L	H	L	↑	High-Z
Synchronous Read-Bank 2	H	L	H	H	H	L	L	↑	
Synchronous Write-Bank 3	H	H	L	H	L	H	L	↑	High-Z
Synchronous Read-Bank 3	H	H	L	H	H	L	L	↑	
Synchronous Write-Bank 4	H	H	H	L	L	H	L	↑	High-Z
Synchronous Read-Bank 4	H	H	H	L	H	L	L	↑	
Snooze Mode	X	X	X	X	X	X	H	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Relative to V_{SS}	-0.5V to +4.6V
V_{IN}	-0.5V to V_{CC} +0.5V
Storage Temperature	-55°C to +125°C
Operating Temperature (Commercial)	0°C to +70°C
Operating Temperature (Industrial)	-40°C to +85°C
Short Circuit Output Current	10 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.14	3.3	3.6	V
Supply Voltage	V_{SS}	0.0	0.0	0.0	V
Input High	V_{IH}	1.1	3.0	V_{CC}+0.3	V
Input Low	V_{IL}	-0.3	0.0	0.3	V
Input Leakage	I_{LI}	-2	1	2	µA
Output Leakage	I_{LO}	-2	1	2	µA

DC ELECTRICAL CHARACTERISTICS - READ CYCLE

Description	SYM	Typ	8.5	10	12	15	Units
Power Supply Current	Icc1	2.0	2.9	2.7	2.7	2.5	A
Power Supply Current Device Selected, No Operation	Icc	875	1.8	1.8	1.3	1.3	A
Snooze Mode	IccZZ	500	700	700	700	700	mA
CMOS Standby	Icc3	270	350	350	350	350	mA
Clock Running-Deselect	IccK	900	1.1	1.1	1.0	1.0	A

AC TEST CONDITIONS

Input Pulse Levels	Vss to 3.0V
Input and Output Timing Ref.	1.25V
Output Test equivalencies	

AC TEST LOAD

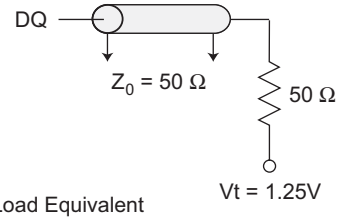


Fig. 1 Output Load Equivalent

BURST ADDRESS TABLE (MODE=NC/Vcc)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A-A00	A-A01	A-A10	A-A11
A-A01	A-A00	A-A11	A-A10
A-A10	A-A11	A-A00	A-A01
A-A11	A-A10	A-A01	A-A00

BURST ADDRESS TABLE (MODE=GND)

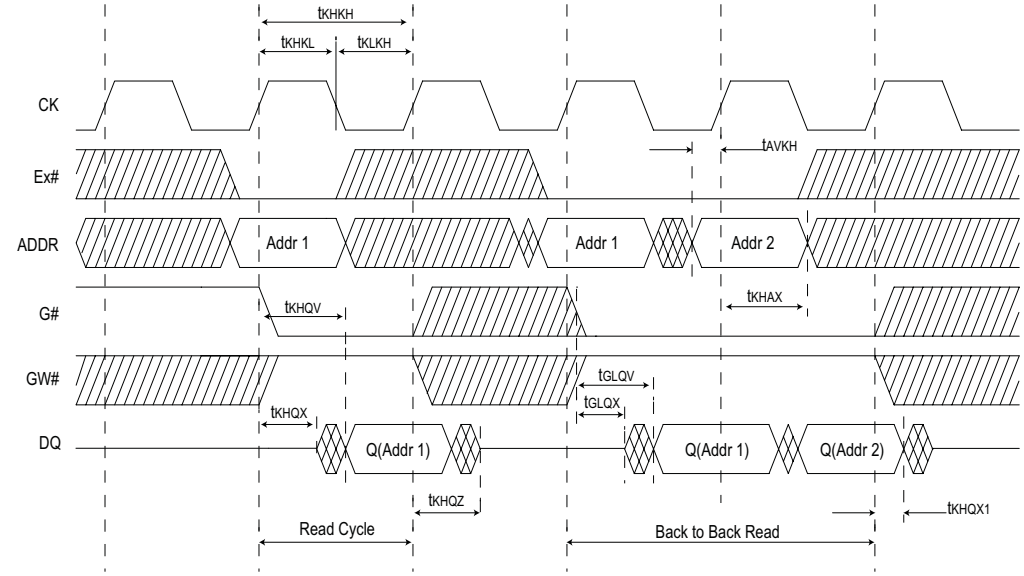
First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A-A00	A-A01	A-A10	A-A11
A-A01	A-A10	A-A11	A-A00
A-A10	A-A11	A-A00	A-A01
A-A11	A-A00	A-A01	A-A10

READ CYCLE TIMING PARAMETERS

		8.5ns		10ns		12ns		15ns		
Description	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Clock Cycle Time	t_{KHKH}	*	*	15		15		20		ns
Clock High Time	t_{KHKL}	*	*	5		5		6		ns
Clock Low Time	t_{KLKH}	*	*	5		5		6		ns
Clock to Output Valid	t_{KHQV}	*	*		10		12		15	ns
Clock to Output Invalid	t_{KHQX1}	*	*	3		3		3		ns
Clock to Output Low-Z	t_{KHQX}	*	*	4		4		4		ns
Output Enable to Output Valid	t_{GLQV}	*	*		5		5		6	ns
Output Enable to Output Low-Z	t_{GLQX}	*	*	0		0		0		ns
Output Enable to Output High-Z	t_{GHQZ}	*	*		5		5		5	ns
Address Setup	t_{AVKH}	*	*	2.5		2.5		2.5		ns
Bank Enable Setup	t_{EVKH}	*	*	2.5		2.5		2.5		ns
Address Hold	t_{KHAX}	*	*	1.0		1.0		1.0		ns
Bank Enable Hold	t_{KHEX}	*	*	1.0		1.0		1.0		ns

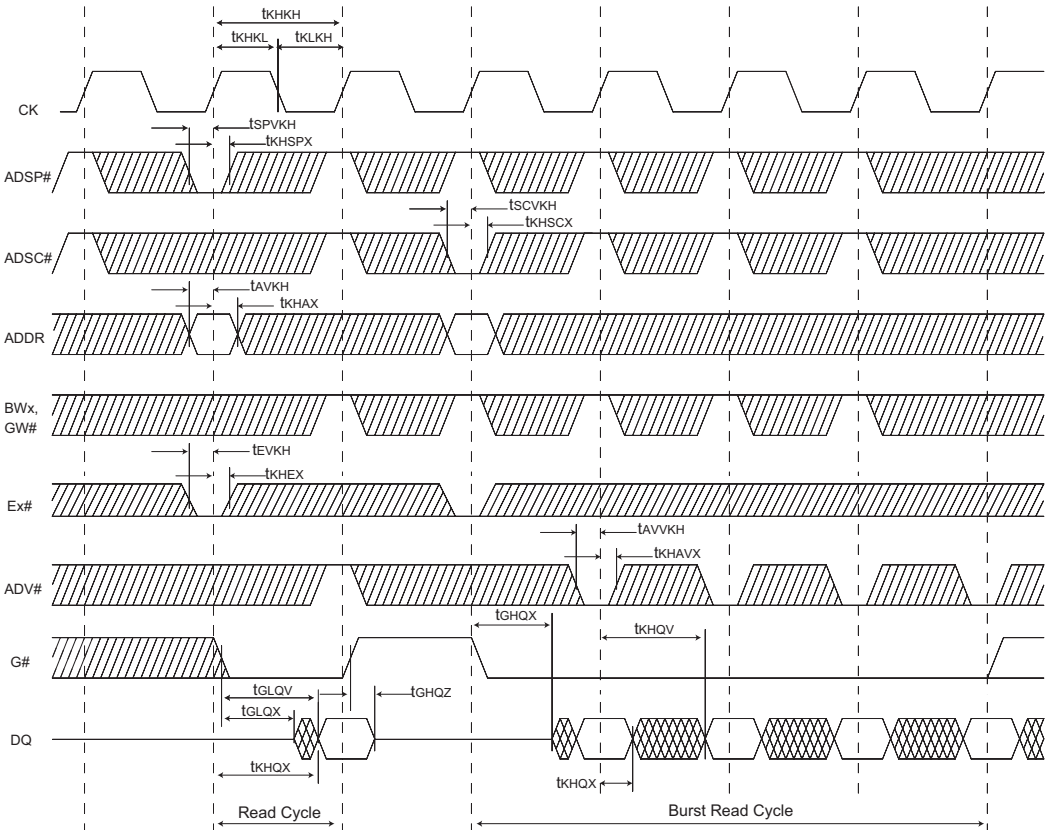
*TBD

SYNCHRONOUS ONLY READ CYCLE



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SYNC-BURST READ CYCLE

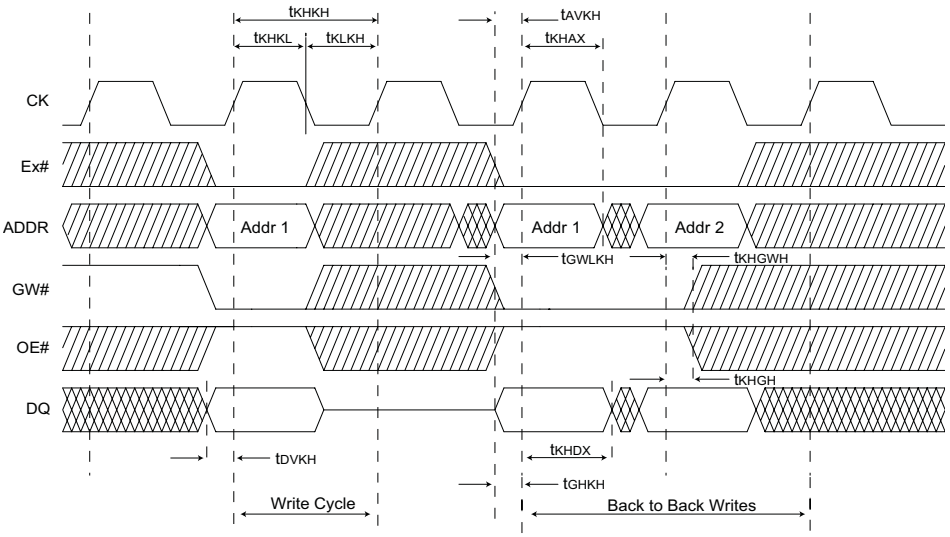


WRITE CYCLE TIMING PARAMETERS

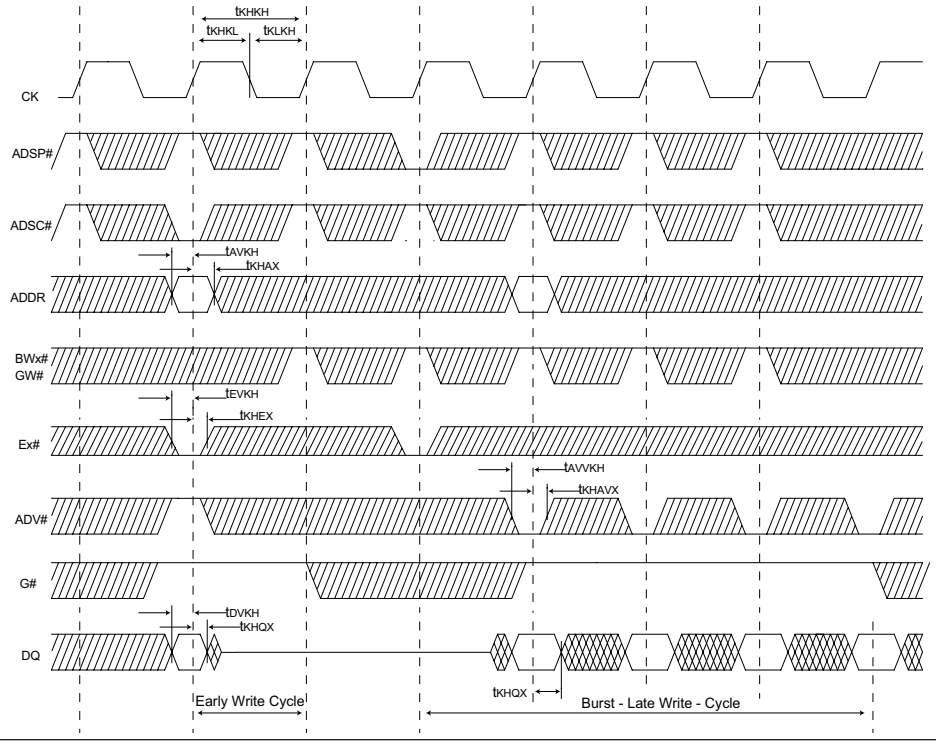
		8.5ns		10ns		12ns		15ns		
Description	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Clock Cycle Time	t_{KHKH}	*	*	15		15		20		ns
Clock High Time	t_{KHKL}	*	*	5		5		6		ns
Clock Low Time	t_{KLKH}	*	*	5		5		6		ns
Address Setup	t_{AVKH}	*	*	2.5		2.5		2.5		ns
Address Hold	t_{KHAX}	*	*	1.0		1.0		1.0		ns
Bank Enable Setup	t_{EVKH}	*	*	2.5		2.5		2.5		ns
Bank Enable Hold	t_{KHEX}	*	*	1.0		1.0		1.0		ns
Global Write Enable Setup	t_{WVKH}	*	*	2.5		2.5		2.5		ns
Global Write Enable Hold	t_{KHWX}	*	*	1.0		1.0		1.0		ns
Data Setup	t_{DVKH}	*	*	2.5		2.5		2.5		ns
Data Hold	t_{KHDX}	*	*	1.0		1.0		1.0		ns

**TBD*

SYNC (NON-BURST) WRITE CYCLE

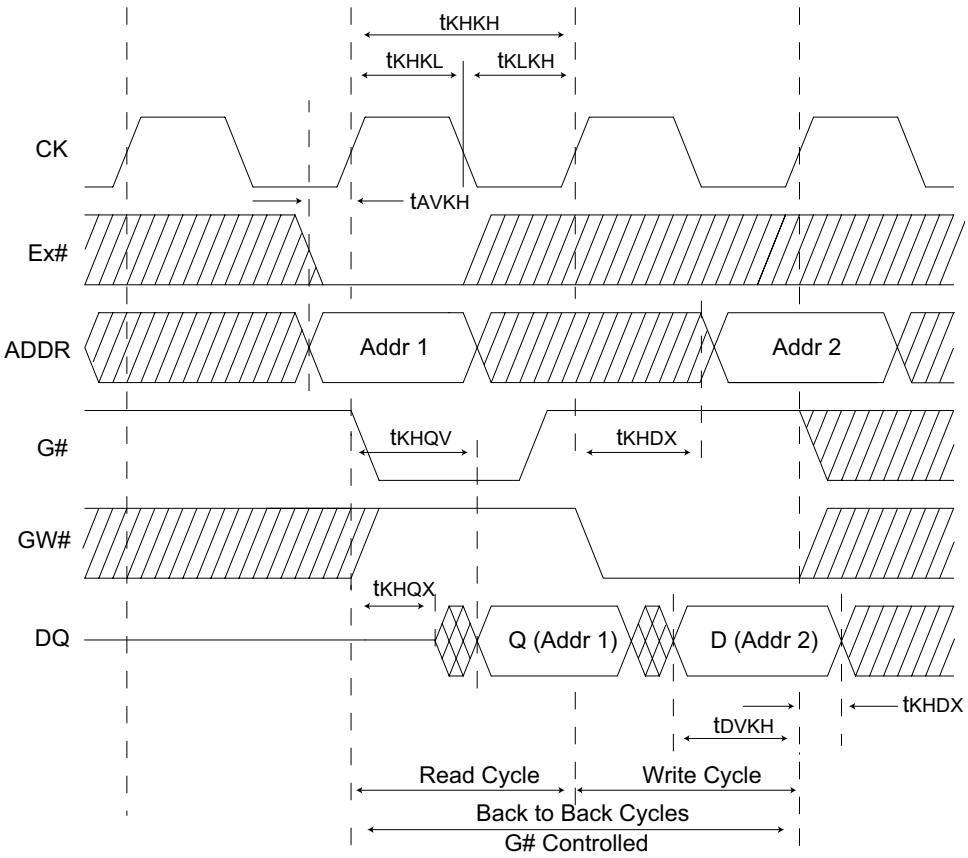


SYNCBURST WRITE CYCLE



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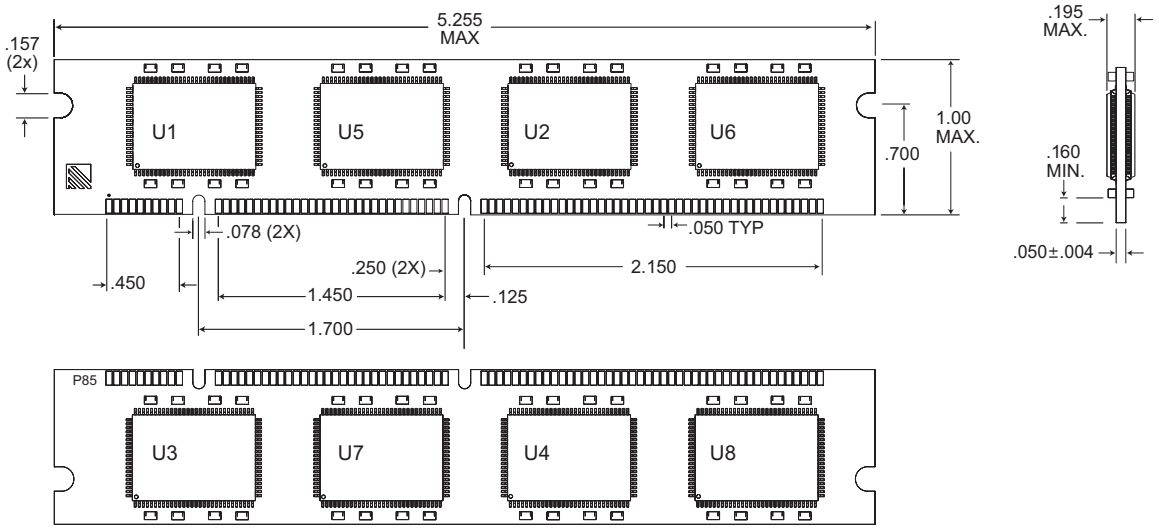
SYNC (NON-BURST) READ/WRITE CYCLE



PACKAGE DESCRIPTION

Package No. 410

168 Lead
Dual Key DIMM



ORDERING INFORMATION

Part Number	Organization	Voltage	Speed (ns)	Package
EDI2CG472128V85D2*	4x128Kx72	3.3	8.5	168 Gold Lead DIMM
EDI2CG472128V10D2*	4x128Kx72	3.3	10	168 Gold Lead DIMM
EDI2CG472128V12D2	4x128Kx72	3.3	12	168 Gold Lead DIMM
EDI2CG472128V15D2	4x128Kx72	3.3	15	168 Gold Lead DIMM

**Consult Factory for Availability*