TOSHIBA PHOTOCOUPLER GaAℓAs IRED & PHOTO-IC

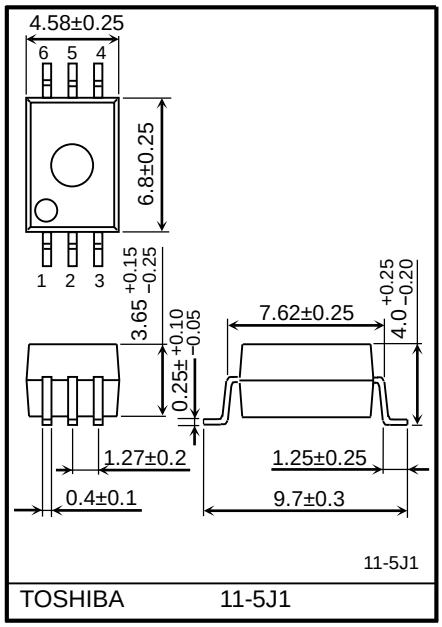
TLP718

Isolated Bus Drivers

High Speed Line Receivers

Microprocessor System Interfaces

Unit: mm



Weight: 0.26 g (typ.)

The Toshiba TLP718 consists of a GaAℓAs light-emitting diode and an integrated high-gain, high-speed photodetector. This unit is a 6-pin SDIP. The TLP718 is 50% smaller than the 8-PIN DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification.

The detector has a totem pole output stage to provide both source and sink driving. The detector IC has an internal shield that provides a guaranteed common-mode transient immunity of 10 kV/μs.

The TLP718 is inverter logic type. For buffer logic type, the TLP715 is in line-up.

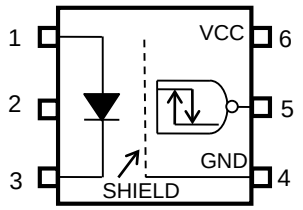
- Inverter logic type (totem pole output)
- Guaranteed performance over temperature : −40 to 100°C
- Power supply voltage : 4.5 to 20 V
- Input current: I_{FHL} = 3 mA (max)
- Switching time (t_{pHL} / t_{pLH}) : 250 ns (max)
- Common-mode transient immunity : ±10 kV/μs (min)
- Isolation voltage : 5000 Vrms (min)
- UL recognized
  UL1577, File No.E67349
- c-UL recognized
  CSA Component Acceptance Service No. 5A, File No.E67349
- Option (D4) VDE approved : DIN EN60747-5-5

Note : When a EN60747-5-5 approved type is needed, Please designate "Option(D4)"

- Construction Mechanical Rating

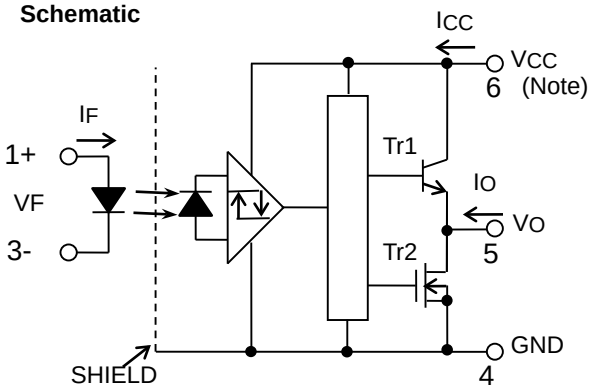
	7.62 mm pitch standard type	10.16 mm pitch TLPXXXF type
Creepage Distance	7.0 mm (min)	8.0 mm (min)
Clearance	7.0 mm (min)	8.0 mm (min)
Insulation Thickness	0.4 mm (min)	0.4 mm (min)

Pin Configuration (Top View)



1: ANODE
2: N.C.
3: CATHODE
4: GND
5: V_O (Output)
6: V_{CC}

Schematic



Note: 0.1 μF bypass capacitor must be connected between pins 6 and 4.

Truth Table

Input	LED	Tr1	Tr2	Output
H	ON	OFF	ON	L
L	OFF	ON	OFF	H

Start of commercial production
2008/12

Absolute Maximum Ratings (Ta = 25°C)

CHARACTERISTIC			SYMBOL	RATING	UNIT
LED	Forward Current (Ta ≤ 83°C)		I_F	20	mA
	Forward Current Derating (Ta ≥ 83°C)		$\Delta I_F/\Delta Ta$	−0.48	mA/°C
	Peak Transient Forward Current	(Note 1)	I_{FPT}	1	A
	Reverse Voltage		V_R	5	V
	Input power dissipation		PD	40	mW
	Junction Temperature		Tj	125	°C
DETECTOR	Output Current 1 (Ta ≤ 25°C)		I_{O1}	25 / −15	mA
	Output Current 2 (Ta ≤ 100°C)		I_{O2}	13 / −13	mA
	Output Voltage		V_O	−0.5 to 20	V
	Supply Voltage		V_{CC}	−0.5 to 20	V
	Output power dissipation		PO	75	mW
	Output power dissipation derating（Ta ≥ 25°C）		$\Delta P_O/\Delta T_a$	0.75	mW / °C
	Junction Temperature		Tj	125	°C
Operating Temperature Range			Topr	−40 to 100	°C
Storage Temperature Range			Tstg	−55 to 125	°C
Lead Solder Temperature (10 s)			Tsol	260	°C
Isolation Voltage (AC, 60 s, R.H. ≤ 60%, Ta = 25°C)		(Note 2)	BV_S	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width PW ≤ 1 μs, 300 pps.

Note 2: Device Considered a two terminal device: pins 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.

Recommended Operating Conditions

CHARACTERISTIC		SYMBOL	MIN	TYP.	MAX	UNIT
Input Current, ON		$I_{F\ (ON)}$	4.5	−	10	mA
Input Voltage, OFF		$V_{F\ (OFF)}$	0	−	0.8	V
Supply Voltage	(Note 1)	V_{CC}	4.5	−	20	V
Operating Temperature		T_{opr}	-40	−	100	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 1: This item denotes operating ranges, not meaning of recommended operating conditions.

Electrical Characteristics
(Unless otherwise specified, Ta = −40 to 100°C, V_{CC} = 4.5 to 20 V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION		MIN	TYP.	MAX	UNIT
Input forward voltage	V_F	—	I_F = 5 mA, Ta = 25°C		1.4	1.6	1.7	V
Temperature coefficient of forward voltage	$\Delta V_F/\Delta Ta$	—	I_F = 5 mA		—	−2.0	—	mV/°C
Input reverse current	I_R	—	V_R = 5 V, Ta = 25°C		—	—	10	μA
Input capacitance	C_T	—	V = 0 V, f = 1 MHz, Ta = 25°C		—	45	—	pF
Logic LOW output voltage	V_{OL}	Figure 1	I_{OL} = 3.5 mA , I_F = 5 mA		—	0.2	0.6	V
Logic HIGH output voltage (Note 1)	V_{OH}	Figure 2	I_{OH} = −2.6 mA, V_F = 0.8 V	V_{CC} = 4.5 V	2.7	3.5	—	V
				V_{CC} = 20 V	17.4	19	—	
Logic LOW supply current	I_{CCL}	Figure 3	I_F = 5 mA		—	—	3.0	mA
Logic HIGH supply current	I_{CCH}	Figure 4	V_F=0 V		—	—	3.0	mA
Logic LOW short circuit output current (Note 2)	I_{OSL}	Figure 5	I_F = 5 mA	V_{CC} = V_O = 5.5 V	15	80	—	mA
				V_{CC} = V_O = 20 V	20	90	—	
Logic HIGH short circuit output current (Note 3)	I_{OSH}	Figure 6	V_F = 0 V, V_O = GND	V_{CC} = 5.5 V	−5	-15	—	mA
				V_{CC} = 20 V	−10	−20	—	
Input current logic LOW output	I_{FHL}	—	I_O = 3.5 mA, V_O < 0.6 V		—	0.4	3	mA
Input voltage logic HIGH output	V_{FLH}	—	I_O = −2.6 mA, V_O > 2.4 V		0.8	—	—	V
Input current hysteresis	I_{HYS}	—	V_{CC} = 5 V		—	0.05	—	mA

Note**:** All typical values are at Ta = 25°C, V_{CC} = 5 V unless otherwise specified.

Note 1**:** $V_{OH} = V_{CC} - V_O$ [V]

Note 2**:** Duration of output short circuit time should not exceed 10 ms.

Note 3**:** A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Isolation Characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Capacitance input to output	C_S (Note 1)	V_S = 0V, f = 1 MHz	—	1.0	—	pF
Isolation resistance	R_S (Note 1)	R.H. ≤ 60%, V_S = 500 V	1×10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S (Note 1)	AC, 60 s	5000	—	—	V_{rms}
		AC, 1 s, in oil	—	10000	—	
		DC, 60 s, in oil	—	10000	—	Vdc

Note 1**:** This device is considered as a two-terminal device**:** Pins 1, 2 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

Switching Characteristics

(Unless otherwise specified, Ta = −40 to 100°C, V_{CC} = 4.5 to 20 V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP.	MAX	UNIT
Propagation delay time to logic HIGH output	t_{pLH}	Figure 7, Figure 8	I_F = 3 → 0 mA	30	120	250	ns
Propagation delay time to logic LOW output	t_{pHL}		I_F = 0 → 3 mA	30	120	250	ns
Switching time dispersion between ON and OFF	$\lvert t_{pHL} - t_{pLH} \rvert$		—	—	—	220	ns
Rise Time (10 – 90 %)	t_r		I_F = 3 → 0 mA, V_{CC} = 5 V	—	30	—	ns
Fall Time (90 – 10 %)	t_f		I_F = 0 → 3 mA, V_{CC} = 5 V	—	30	—	ns
Common-mode transient Immunity at HIGH level output	CM_H	Figure 9	V_{CM} = 1000 V_{p-p}, I_F = 0 mA, V_{CC} = 20 V, Ta = 25°C	10000	—	—	V/μs
Common-mode transient Immunity at LOW level output	CM_L		V_{CM} = 1000 V_{p-p}, I_F = 5 mA, V_{CC} = 20 V, Ta = 25°C	−10000	—	—	V/μs

Note**:** All typical values are at Ta = 25°C.

Figure 1: V_{OL} TEST CIRCUIT

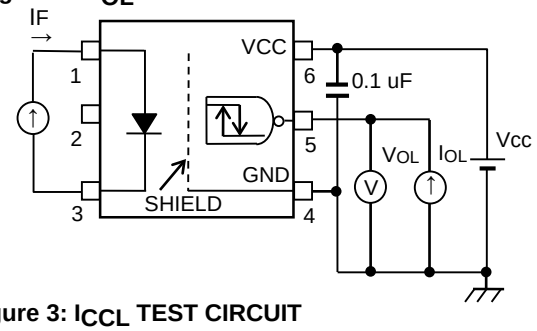
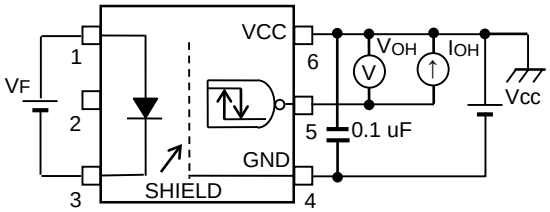


Figure 2: V_{OH} TEST CIRCUIT



$V_{OH} = V_{CC} - V_O$ [V]

Figure 3: I_{CCL} TEST CIRCUIT

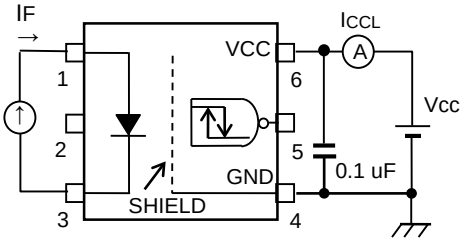


Figure 4: I_{CCH} TEST CIRCUIT

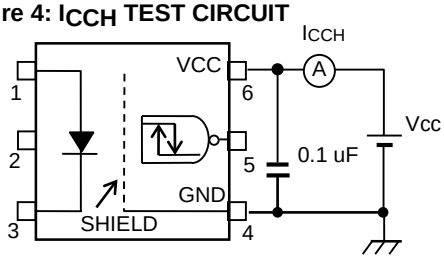


Figure 5: I_{OSL} TEST CIRCUIT

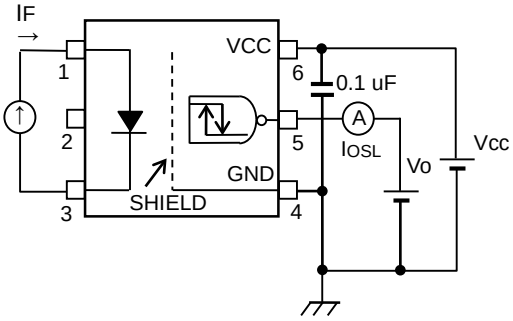


Figure 6: I_{OSH} TEST CIRCUIT

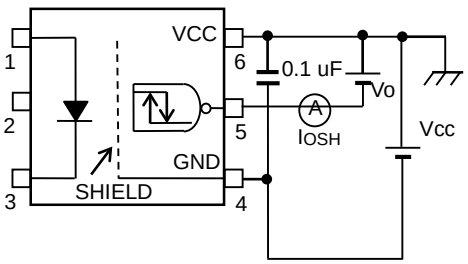
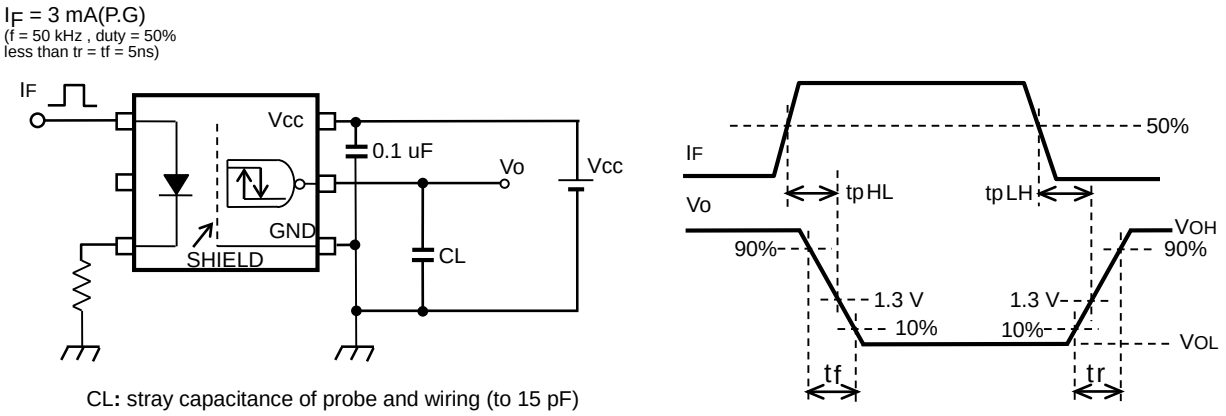
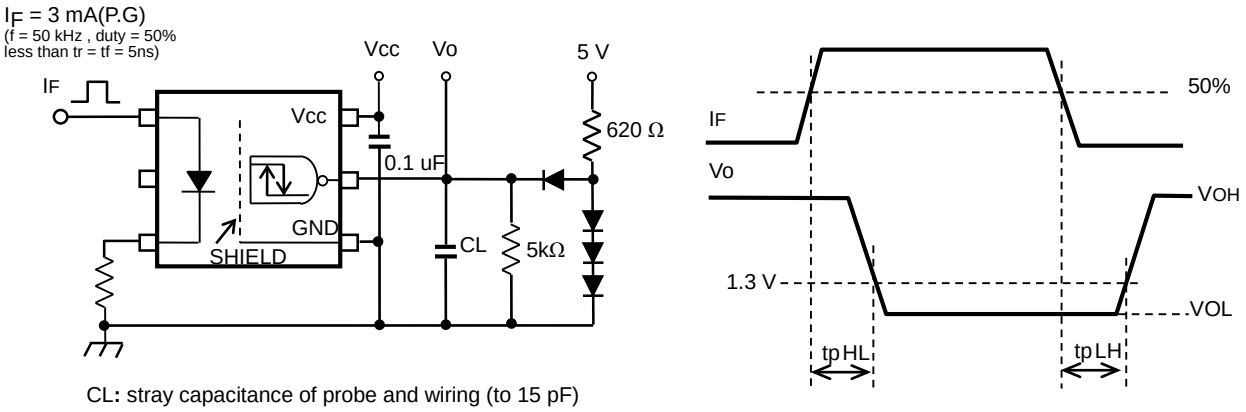


Figure 7: Switching Time Test Circuit



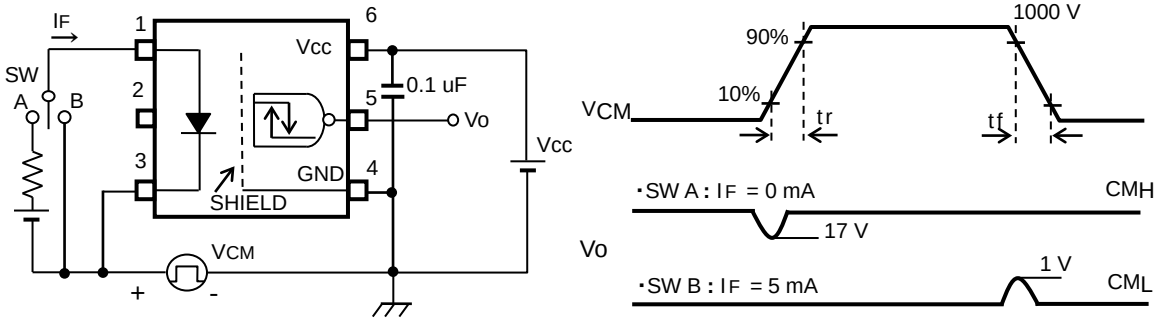
CL: stray capacitance of probe and wiring (to 15 pF)

Figure 8: Switching Time Test Circuit



CL: stray capacitance of probe and wiring (to 15 pF)

Figure 9: Common-Mode Transient Immunity Test Circuit



$$CM_H = \frac{800(V)}{t_r(\mu s)} \qquad CM_L = -\frac{800(V)}{t_f(\mu s)}$$

CM_H (CM_L) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the high (low) state.

EN60747-5-5 Option:(D4)

Types : TLP718, TLP718F

Type designations for “option: (D4)”, which are tested under EN60747 requirements.

Ex.: TLP718 (D4-TP,F)

D4 : EN60747 option
TP : Standard tape & reel type
F : [[G]]/RoHS COMPATIBLE (Note 1)

Note: Use TOSHIBA standard type number for safety standard application.
Ex.: TLP718 (D4-TP,F) → TLP718

Note 1 : Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.
The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronics equipment.

EN60747 Isolation Characteristics

Description		Symbol	Rating	Unit
Application classification for rated mains voltage ≤ 300 V_{rms} for rated mains voltage ≤ 600 V_{rms}			 I-IV I-III	—
Climatic classification			40 / 100 / 21	—
Pollution degree			2	—
Maximum operating insulation voltage	TLPxxx type	V_{IORM}	890	Vpk
	TLPxxxF type		1140	
Input to output test voltage, method A Vpr = 1.6×V_{IORM}, type and sample test tp = 10 s, partial discharge < 5 pC	TLPxxx type	Vpr	1424	Vpk
	TLPxxxF type		1824	
Input to output test voltage, method B Vpr = 1.875×V_{IORM}, 100% production test t_p = 1 s, partial discharge < 5 pC	TLPxxx type	Vpr	1670	Vpk
	TLPxxxF type		2140	
Highest permissible overvoltage (transient overvoltage, t_{pr} = 60 s)		V_{TR}	8000	Vpk
Safety limiting values (max permissible ratings in case of fault, also refer to thermal derating curve) current (input current I_F, P_{si} = 0) power (output or total power dissipation) temperature		 Isi Psi Tsi	 300 700 150	 mA mW °C
Insulation resistance,	V_{IO} = 500 V, Ta = 25°C	Rsi	$\geq 10^{12}$	Ω
	V_{IO} = 500 V, Ta = 100°C		$\geq 10^{11}$	
	V_{IO} = 500 V, Ta = Tsi		$\geq 10^{9}$	

Insulation Related Specifications

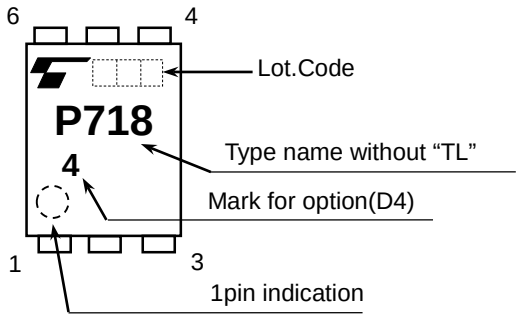
		 7.62 mm pitch TLPxxx type	 10.16 mm pitch TLPxxxF type
Minimum creepage distance	Cr	7.0 mm	8.0 mm
Minimum clearance	Cl	7.0 mm	8.0 mm
Minimum insulation thickness	ti	0.4 mm	
Comperative tracking index	CTI	175	

Note**:** If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value. (e.g.at a standard distance between soldering eye centres of 7.5mm). If this is not permissible, the user shall take suitable measures.

Note**:** This photocoupler is suitable for 'safe electrical isolation' only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Marking on product for EN60747 **:** 4

Marking Example**:**



Note: The above marking is applied to the photocouplers that have been qualified according to option (D4) of EN60747.

Figure 1 Partial discharge measurement procedure according to EN60747
Destructive test for qualification and sampling tests.

Method A

(for type and sampling tests, destructive tests)

t_1, t_2	= 1 to 10 s
t_3, t_4	= 1 s
t_p(Measuring time for partial discharge)	= 10 s
t_b	= 12 s
t_{ini}	= 60 s

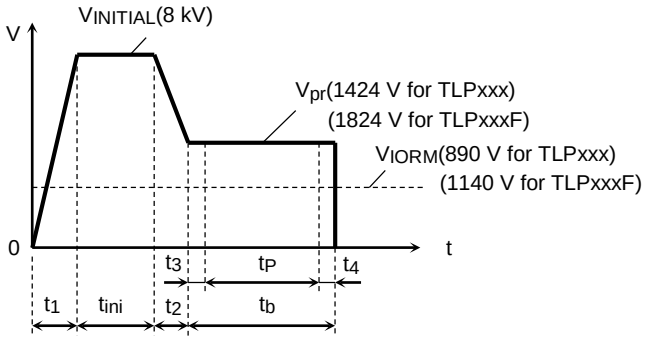


Figure 2 Partial discharge measurement procedure according to EN60747
Non-destructive test for100% inspection.

Method B

(for sample test,non-destructive test)

t_3, t_4	= 0.1 s
t_p(Measuring time for partial discharge)	= 1 s
t_b	= 1.2 s

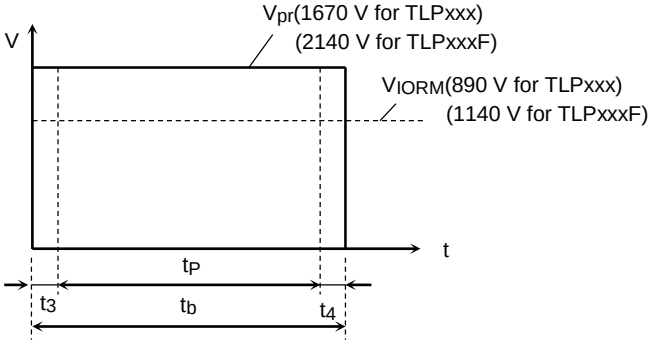
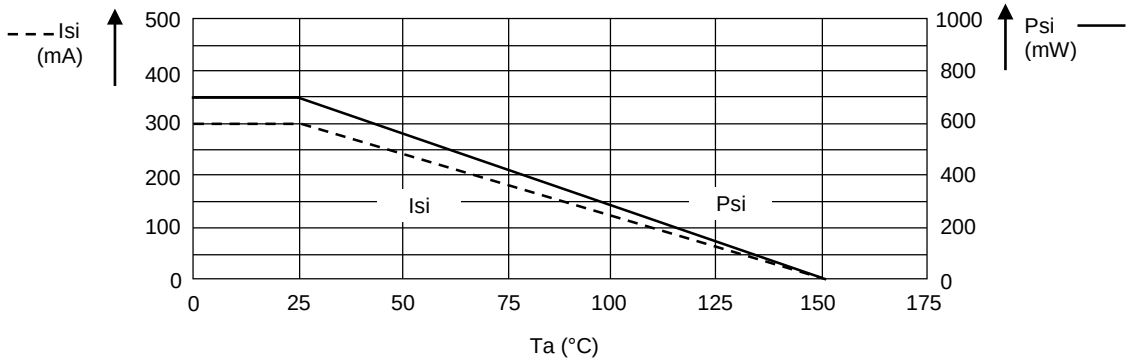


Figure 3 Dependency of maximum safety ratings on ambient temperature



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