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ISL6328

Dual PWM Controller For Powering AMD SVI Split-Plane Processors

FN7621
Rev 1.00
June 7, 2011

The ISL6328 dual PWM controller delivers high efficiency and tight regulation from two synchronous buck DC/DC converters. The ISL6328 supports power control of AMD processors, which operate from a serial VID interface (SVI). The dual output ISL6328 features a multi-phase controller to support the Core voltage (VDD) and a single phase controller to power the Northbridge (VDDNB).

A precision core voltage regulation system is provided by a one-to-four-phase PWM voltage regulator (VR) controller. The integration of two power MOSFET drivers adds flexibility in layout and reduces the number of external components in the multi-phase section. A single phase PWM controller with integrated driver provides a second precision voltage regulation system for the Northbridge portion of the processor. This monolithic, dual controller with an integrated driver solution provides a cost and space saving power management solution.

For applications that benefit from load line programming to reduce bulk output capacitors, the ISL6328 features temperature compensated output voltage droop. The multi-phase portion also includes advanced control loop features for optimal transient response to load application and removal. One of these features is highly accurate, fully differential, continuous DCR current sensing for load line programming and channel current balance. Dual edge modulation is another unique feature, allowing for quicker initial response to high di/dt load transients.

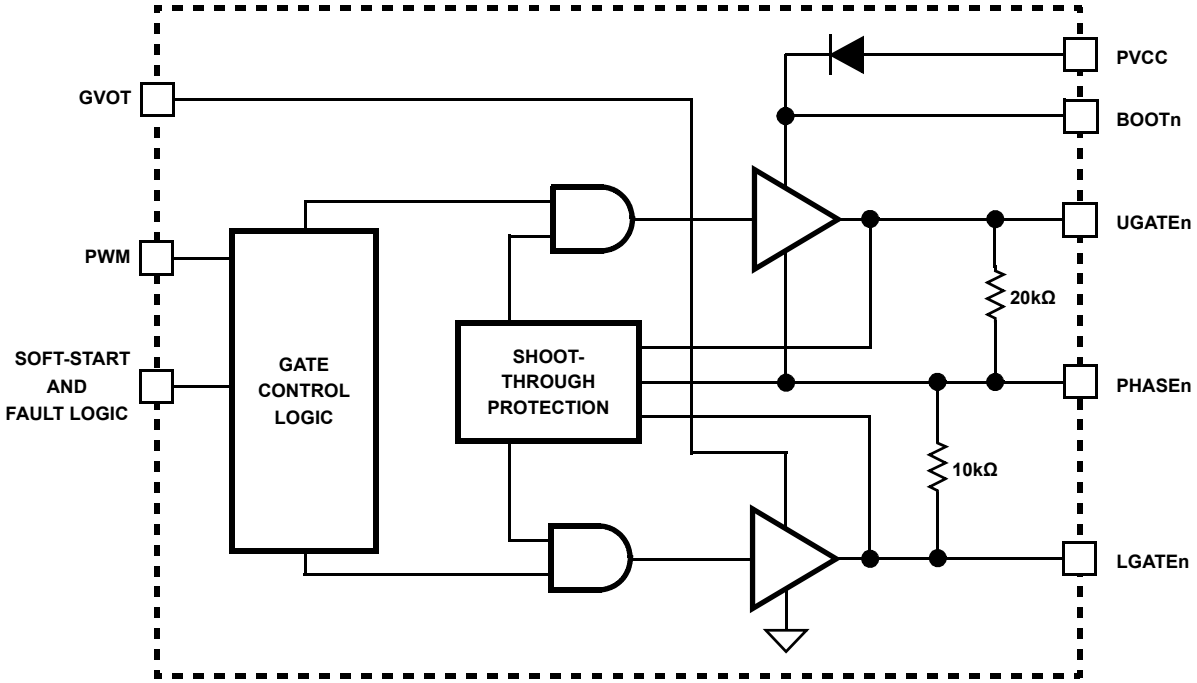
The ISL6328 supports Power Savings Mode by dropping the number of phases when the PSI_L bit is set.

Features

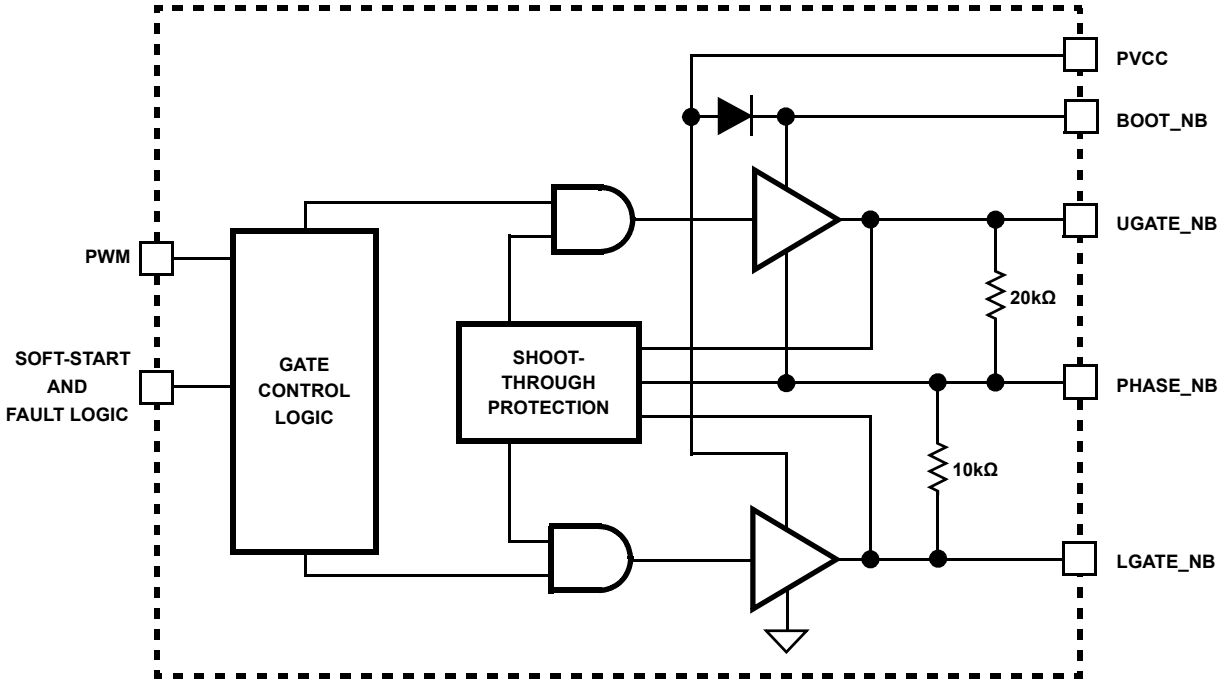
- Processor Core Voltage Via Integrated Multi-Phase Power Conversion
- Configuration Flexibility
  - 1 or 2-Phase Operation with Internal Drivers
  - 3 or 4-Phase Operation with External PWM Drivers
- PSI_L Support
  - Phase Shedding for Improved Efficiency at Light Load
  - Diode Emulation in PSI mode
  - Gate Voltage Optimization
- Precision Core Voltage Regulation
  - Differential Remote Voltage Sensing
  - ±0.6% System Accuracy Over-Temperature
- Optimal Processor Core Voltage Transient Response
  - Adaptive Phase Alignment (APA)
  - Active Pulse Positioning Modulation
- Fully Differential, Continuous DCR Current Sensing
  - Accurate Load Line Programming
  - Precision Channel Current Balancing
  - Temperature Compensated
- Serial VID interface Handles up to 3.4MHz Clock Rates
- Two Level Overcurrent Protection Allows for High Current Throttling (I_{DD_SPIKE})
- Multi-tiered Overvoltage Protection
- Selectable Switching Frequency up to 1MHz
- Simultaneous Digital Soft-Start of Both Outputs

Integrated Driver Block Diagram

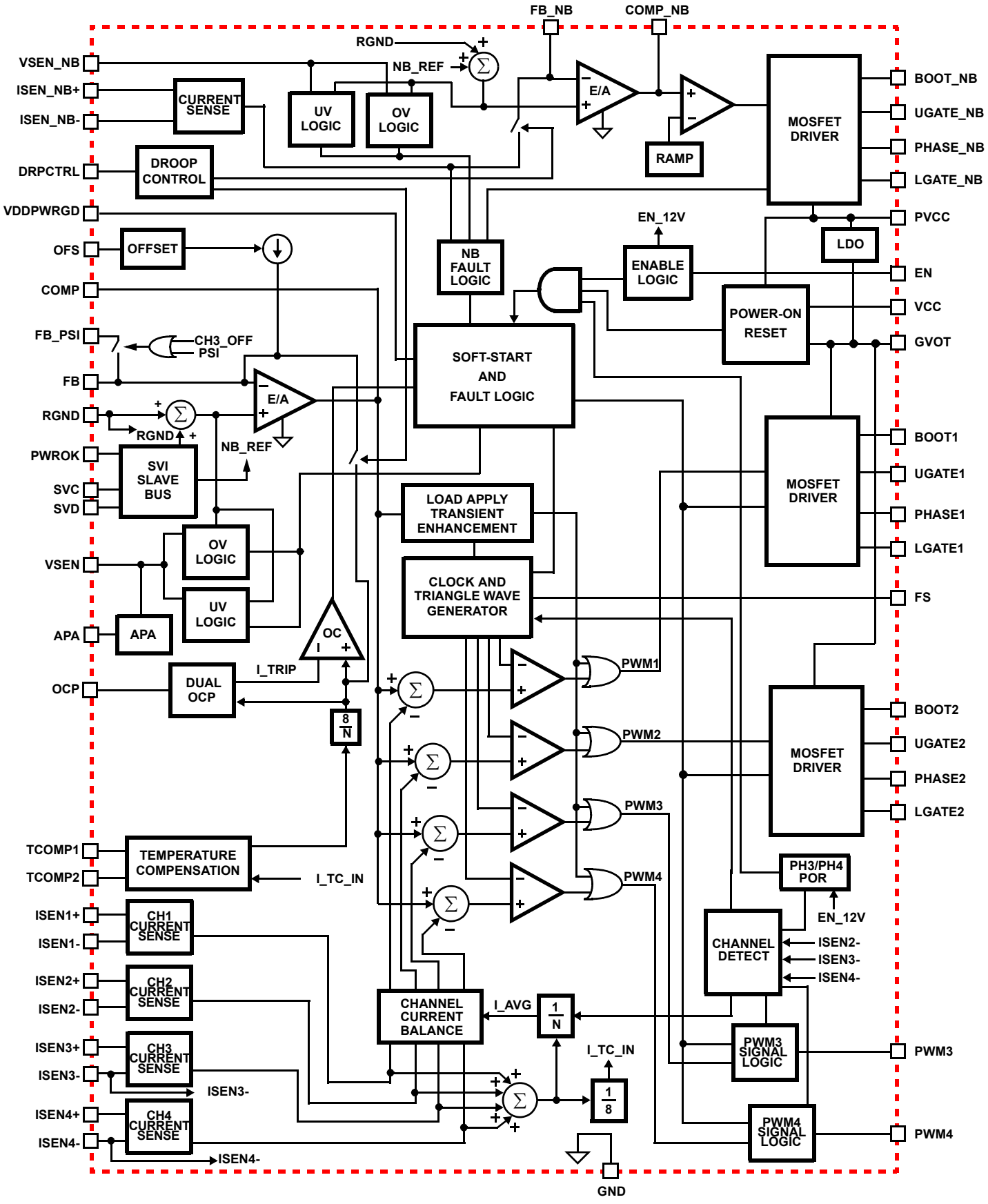
Channels 1 and 2 Gate Drive



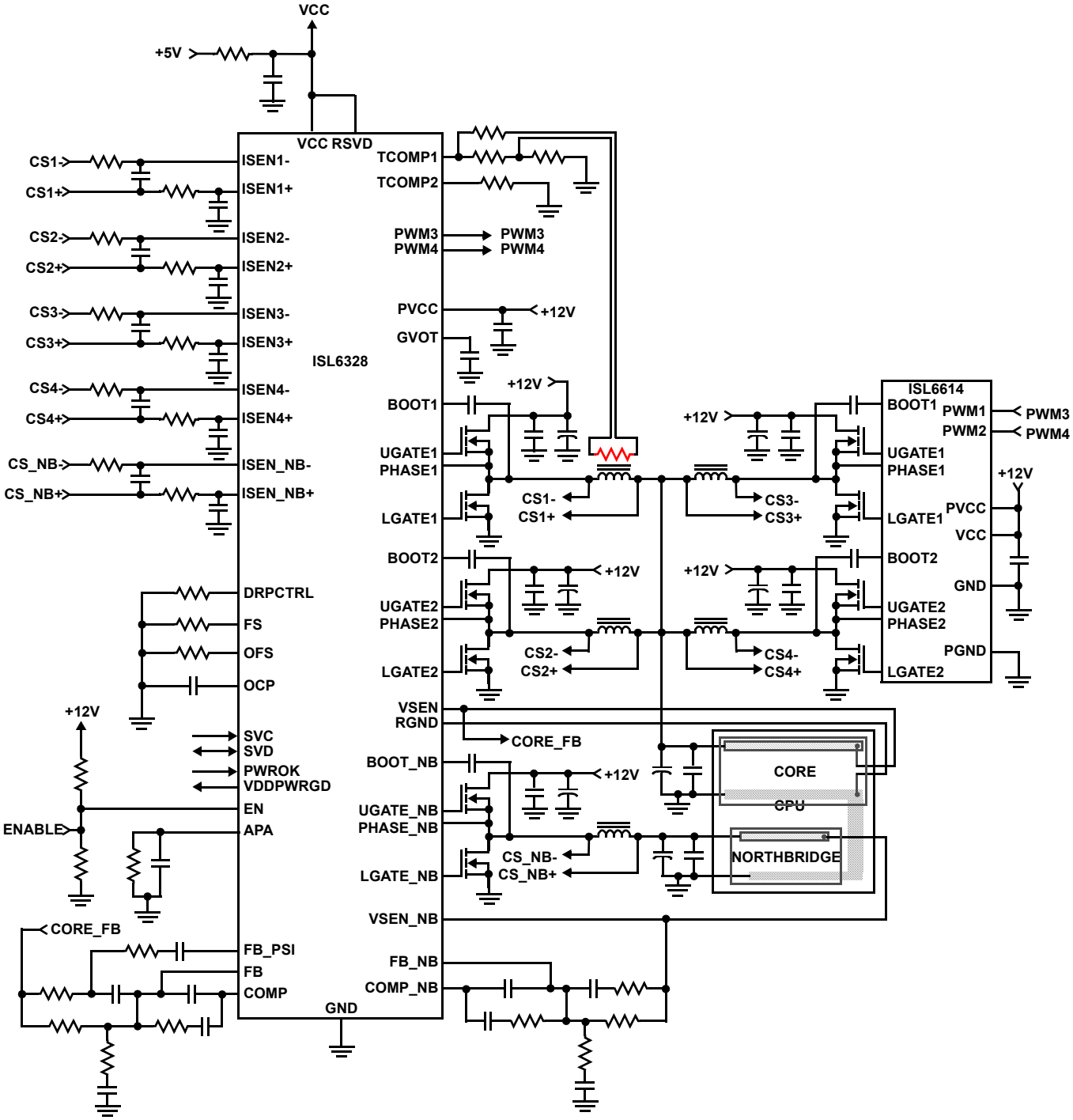
Northbridge Gate Drive



Controller Block Diagram

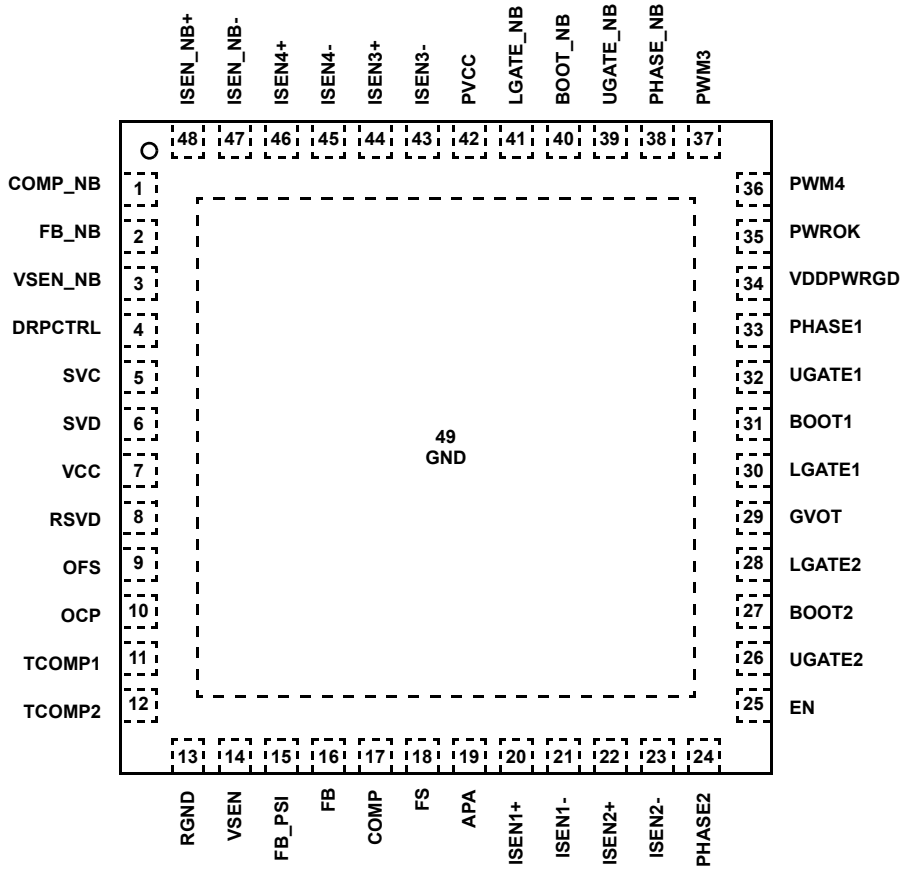


Typical Application



Pin Configuration

ISL6328
(48 LD QFN)
TOP VIEW



Functional Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
COMP_NB	1	Output of the internal error amplifier for the Northbridge regulator.
FB_NB	2	Inverting input to the internal error amplifier for the Northbridge regulator.
VSEN_NB	3	Non-inverting input to the Northbridge regulator precision differential remote-sense amplifier. This pin should be connected to the remote Northbridge sense pin of the processor, VDDNB_SENSE.
DRPCTRL	4	Droop Control for Core and Northbridge. This pin is used to set up one of four user programmable selections via a resistor: Core Droop On and Northbridge Droop On; Core Droop Off and Northbridge Droop On, Core Droop On and Northbridge Droop Off; Core Droop Off and Northbridge Droop Off. If the resistor is tied to ground, the number of active phases in PSI mode is 1. If the resistor is tied to VCC, the number of active phases in PSI mode is 2.
SVC	5	Serial VID clock input from the AMD processor.
SVD	6	Serial VID data bi-directional signal to and from the master device on AMD processor.
VCC	7	VCC is the bias supply for the ICs small-signal circuitry. Connect this pin to a +5V supply and decouple using a quality 0.1µF ceramic capacitor.
RSVD	8	RESERVED. Connect this pin directly to the VCC pin.
OFS	9	The OFS pin provides a means to program a DC current for generating an offset voltage across the resistor between FB and VSEN. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFS pin should be left unconnected.

Functional Pin Descriptions (Continued)

PIN NAME	PIN NUMBER	DESCRIPTION
OCP	10	A capacitor from this pin to ground determines the time that the regulator is allowed to service a load current spike that exceeds the internal OCP trip point.
TCOMP1, TCOMP2	11, 12	These two pins are used to compensate the inductor current sensing for fluctuations due to temperature.
RGND	13	Inverting input to the Core and Northbridge regulator precision differential remote-sense amplifiers. This pin should be connected to the remote ground sense pin of the processor core, VSS_SENSE.
VSEN	14	Non-inverting input to the Core regulator precision differential remote-sense amplifier. This pin should be connected to the remote Core sense pin of the processor, VDD_SENSE.
FB_PSI	15	In PSI mode this pin is internally shorted to the FB pin to augment the feedback compensation network for the lower phase count.
FB	16	Inverting input to the internal error amplifier for the Core regulator.
COMP	17	Output of the internal error amplifier for the Core regulator.
FS	18	This is a dual function pin. A resistor, placed from FS to either Ground or VCC sets the switching frequency of both controllers. Refer to Equation 1 for proper resistor calculation. $R_T = 10^{[10.61 - 1.035\log(f_s)]}$ (EQ. 1) This pin also controls the SVID high and low trip thresholds.
APA	19	Allows for programming of the Auto Phase Alignment threshold. A resistor in parallel with a capacitor to ground is used to set this threshold.
ISENn+, ISENn-, ISEN_NB+, ISEN_NB-	20, 21, 22, 23, 43, 44, 45, 46, 47, 48	These pins are used for differentially sensing the corresponding channel output currents. The sensed currents are used for channel balancing, protection, and core load line regulation. Connect ISEN- to the node between the RC sense elements surrounding the inductor of the respective channel. Tie the ISEN+ pin to the other end of the sense capacitor through a resistor, R_{ISEN}. The voltage across the sense capacitor is proportional to the inductor current. The sense current, therefore, is proportional to the inductor current and scaled by the DCR of the inductor and R_{ISEN}.
PHASE1, PHASE2	33, 24	Connect these pins to the sources of the corresponding upper MOSFETs. These pins are the return path for the upper MOSFET drives.
GND	49	Bias and reference ground for the IC. The GND connection for the ISL6328 is made with three pins and through the thermal pad on the bottom of the package.
EN	25	This pin is a threshold-sensitive (approximately 0.85V) system enable input for the controller. Held low, this pin disables both CORE and NB controller operation. Pulled high, the pin enables both controllers for operation. A second function of this pin is to provide driver bias monitor for external drivers. A resistor divider with the center tap connected to this pin from the drive bias supply prevents enabling the controller before insufficient bias is provided to external driver. The resistors should be selected such that when the POR-trip point of the external driver is reached, the voltage at this pin meets the above mentioned threshold level.
UGATE1, UGATE2	32, 26	Connect this pin to the corresponding upper MOSFET gate. This pin provides the PWM-controlled gate drive for the upper MOSFET and is monitored for shoot-through prevention purposes.
BOOT1, BOOT2	31, 27	This pin provides the bias voltage for the corresponding upper MOSFET drive. Connect this pin to appropriately-chosen external bootstrap capacitor. The internal bootstrap diode connected to the PVCC pin provides the necessary bootstrap charge.
LGATE1, LGATE2	30, 28	Connect this pin to the corresponding MOSFET's gate. This pin provides the PWM-controlled gate drive for the lower MOSFET. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
GVOT	29	The power supply pin for the multi-phase internal MOSFET drivers. In normal operation, this pin is shorted to the PVCC pin. While in PSI mode, this pin is tied to the output of the internal LDO for Gate Drive Voltage Optimization. Decouple this pin with a quality 2.2µF ceramic capacitor.
VDDPWRGD	34	During normal operation this pin indicates whether both output voltages are within specified overvoltage and undervoltage limits. If either output voltage exceeds these limits or a reset event occurs (such as an overcurrent event), the pin is pulled low. This pin is always low prior to the end of soft-start.

Functional Pin Descriptions (Continued)

PIN NAME	PIN NUMBER	DESCRIPTION
PWROK	35	System wide Power Good input signal. If this pin is low, the two SVI bits are decoded to determine the “metal VID”. When pin is high, the SVI is actively running its protocol.
PWM3, PWM4	37, 36	Pulse-width modulation outputs. Connect these pins to the PWM input pins of an Intersil driver IC if 3- or 4-phase operation is desired. Connect the ISEN- pins of the channels not desired to +5V to disable them. Channels must be disabled in decremental order.
PHASE_NB	38	Connect this pin to the source of the corresponding upper MOSFET. This pin is the return path for the upper MOSFET drive. This pin is used to monitor the voltage drop across the upper MOSFET for overcurrent protection.
UGATE_NB	39	Connect this pin to the corresponding upper MOSFET gate. This pin provides the PWM-controlled gate drive for the upper MOSFET and is monitored for shoot-through prevention purposes.
BOOT_NB	40	This pin provides the bias voltage for the corresponding upper MOSFET drive. Connect this pin to appropriately-chosen external bootstrap capacitor. The internal bootstrap diode connected to the PVCC pin provides the necessary bootstrap charge.
LGATE_NB	41	Connect this pin to the corresponding MOSFET’s gate. This pin provides the PWM-controlled gate drive for the lower MOSFET. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
PVCC	42	The power supply pin for the internal MOSFET drivers. Connect this pin to +12V. This pin is the input to the internal LDO for GVOT. Decouple this pin with a quality 1.0µF ceramic capacitor.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6328CRZ	ISL6328 CRZ	0 to +70	48 Ld 6x6 QFN	L48.6x6B
ISL6328IRZ	ISL6328 IRZ	-40 to +85	48 Ld 6x6 QFN	L48.6x6B

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6328. For more information on MSL please see techbrief TB363.

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Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.3V to +6V
Supply Voltage (PVCC) . . . . . -0.3V to +15V
Absolute Boot Voltage (V_{BOOT}) . . . . . GND - 0.3V to GND + 36V
Phase Voltage (V_{PHASE}) . . . . . GND - 0.3V to 24V
(PVCC = 12V) GND - 8V (<400ns, 20µJ) to 31V (<200ns, 20µJ, $V_{BOOT-PHASE}$ = 5V)
Upper Gate Voltage (V_{UGATE}) . . . . . V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
V_{PHASE} - 3.5V (<100ns Pulse Width, 2µJ) to V_{BOOT} + 0.3V
Lower Gate Voltage (V_{LGATE}) . . . . . GND - 0.3V to PVCC + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to PVCC+ 0.3V
Input, Output, or I/O Voltage . . . . . GND - 0.3V to VCC + 0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114F) 2000V
Machine Model (Tested per JESD22-A115C) 200V
Charge Device Model (Tested per JESD22-C101D) 2000V
Latch Up (Tested per JESD78C; Class II, Level A) 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 4, 5)	27	1

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

VCC Supply Voltage . . . . . +5V ±5%
PVCC Supply Voltage . . . . . +5V to 12V ±5%
Ambient Temperature
ISL6328CRZ . . . . . 0°C to +70°C
ISL6328IRZ . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Boldface limits apply over the operating temperature range.

PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
BIAS SUPPLIES					
Input Bias Supply Current	I_{VCC}; EN = high		26	**35**	mA
Gate Drive Bias Current - PVCC Pin	I_{PVCC}; EN = high		4	**8**	mA
VCC POR (Power-On Reset) Threshold	VCC Rising		4.35	**4.7**	V
	VCC Falling	**3.6**	3.85		V
PVCC POR (Power-On Reset) Threshold	PVCC Rising		4.45	**4.7**	V
	PVCC Falling	**3.6**	3.95		V
GVOT POR (Power-On Reset) Threshold	GVOT Rising		4.45	**4.7**	V
	GVOT Falling	**3.6**	3.95		V
PWM MODULATOR					
Oscillator Frequency Accuracy, F_{SW}	R_T = 100kΩ to Ground	230	250	265	kHz
Oscillator Frequency Accuracy, F_{SW}	R_T = 100kΩ to VCC	225	255	287	kHz
Typical Adjustment Range of Switching Frequency	(Note 7)	**0.150**		**1.5**	MHz
Oscillator Ramp Amplitude, V_{PP}	(Note 7)		1.5		V
CONTROL THRESHOLDS					
EN Rising Threshold		**0.8**	0.87	**0.92**	V
EN Hysteresis		**70**	100	**190**	mV
PWROK Input HIGH Threshold		**0.9**	1.05	**1.2**	V
PWROK Input LOW Threshold		**0.8**	0.95	**1.1**	V
VDDPWRGD	Open drain, VDDPWRGD = 1.24kΩ to 5V			**0.5**	V
PWM Channel Disable Threshold	V_{ISEN2-}, V_{ISEN3-}, V_{ISEN4-}			**4.4**	V

Electrical Specifications Boldface limits apply over the operating temperature range. (Continued)

PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
PIN ADJUSTABLE OFFSET					
OFS Source Current Accuracy (Positive Offset)		**0.29**		**0.32**	V
OFS Sink Current Accuracy (Negative Offset)		**VCC-1.7**		**VCC-1.56**	V
REFERENCE AND DAC					
System Accuracy (VDAC > 1.000V)		**-0.6**		**+0.6**	%
System Accuracy (0.600V < VDAC < 1.000V)		**-1.0**		**+1.0**	%
System Accuracy (VDAC < 0.600V)		**-2.0**		**+2.0**	%
GATE VOLTAGE OPTIMIZATION					
GVOT Voltage	PVCC = 12V, I_{GVOT} = 50mA		5.75		V
ERROR AMPLIFIER					
DC Gain	R_L = 10k to ground, (Note 7)		96		dB
Gain-Bandwidth Product (Note 7)	C_L = 100pF, R_L = 10k to ground, (Note 7)		20		MHz
Slew Rate (Note 7)	C_L = 100pF, Load = ±400µA, (Note 7)		8		V/µs
Maximum Output Voltage	Load = 500µA	**3.8**	4.2		V
Minimum Output Voltage	Load = -500µA		1.4	**1.65**	V
FB_PSI Impedance	Impedance Between FB and FB_PSI		60		Ω
SOFT-START RAMP					
Soft-Start Slew Rate (SR_{SS}) and VID-On-The-Fly Slew Rate (SR_{VOF})		**2.5**	3	**3.8**	mV/µs
PWM OUTPUTS					
PWM Output Voltage LOW	I_{LOAD} = ±500µA			**0.35**	V
PWM Output Voltage HIGH	I_{LOAD} = ±500µA	**4.0**			V
PWM Tri-State Output Voltage	I_{LOAD} = 100µA	**1.5**	2	**2.7**	V
DROOP CURRENT					
Core Tolerance	4 Phases Active, R_{ISENn} = 100Ω, ISENn = 80µA	**67**	75	**85**	µA
North Bridge Tolerance	R_{ISEN_NB} = 100Ω, I_{ISEN_NB} = 100µA	**67**	75	**83**	µA
CORE OVERCURRENT PROTECTION					
Instant Overcurrent Trip Level - I_{DROOP}		**115**	141	**166**	µA
Instant Overcurrent Trip Level - I_{SEN_AVG}		**131**	150	**178**	µA
Delayed Overcurrent Trip Level - I_{SEN_AVG}	(Note 7)		100		µA
Overcurrent Trip Level - Individual Channel	(Note 7)		170		µA
OCP Pin Current	Delayed OCP Level Tripped		20		µA
OCP Pin Voltage Trip	Delayed OCP Level Tripped	**1.95**	2.05	**2.15**	V
NORTH BRIDGE OVERCURRENT PROTECTION					
Overcurrent Trip Level - I_{SEN_NB}		**82**		**141**	µA
Overcurrent Trip Level - I_{DROOP_NB}	ISL6328CRZ	**80**		**128**	µA
Overcurrent Trip Level - I_{DROOP_NB}	ISL6328IRZ	**76**		**128**	µA

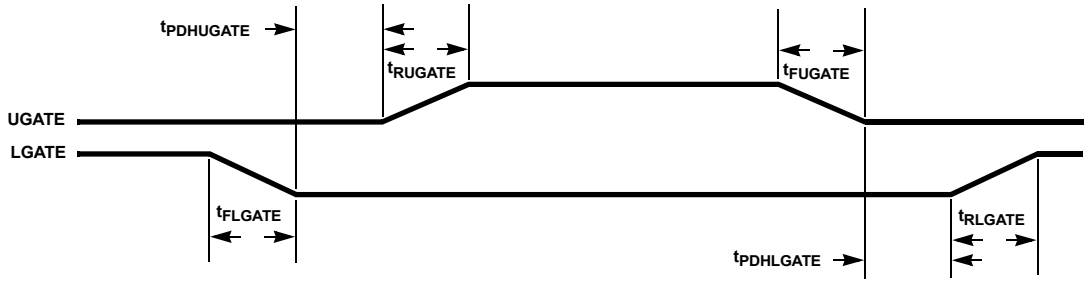
Electrical Specifications Boldface limits apply over the operating temperature range. (Continued)

PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
POWER GOOD					
Overvoltage Threshold	VSEN Rising	VDAC + 220mV		VDAC + 325mV	V
Undervoltage Threshold	VSEN Falling	VDAC - 345mV		VDAC - 190mV	mV
Power-Good Hysteresis			50		mV
OVERVOLTAGE PROTECTION					
OVP Trip Level	V_{DAC} = 1.1V	1.75	1.79	1.85	V
OVP Lower Gate Release Threshold		0.35			V
SWITCHING TIME (Note 7) [See "Timing Diagram" on page 12]					
UGATE Rise Time	t_{RUGATE}; V_{PVCC} = 8V, 3nF Load, 10% to 90%		26		ns
LGATE Rise Time	t_{RLGATE}; V_{PVCC} = 8V, 3nF Load, 10% to 90%		18		ns
UGATE Fall Time	t_{FUGATE}; V_{PVCC} = 12V, 3nF Load, 90% to 10%		18		ns
LGATE Fall Time	t_{FLGATE}; V_{PVCC} = 12V, 3nF Load, 90% to 10%		12		ns
UGATE Turn-On Non-overlap	$t_{PDHUGATE}$; V_{PVCC} = 12V, 3nF Load, Adaptive		10		ns
LGATE Turn-On Non-overlap	$t_{PDHLGATE}$; V_{PVCC} = 12V, 3nF Load, Adaptive		10		ns
GATE DRIVE RESISTANCE					
Upper Drive Source Resistance	V_{PVCC} = 12V, 15mA Source Current		2.5		Ω
Upper Drive Sink Resistance	V_{PVCC} = 12V, 15mA Sink Current		2.0		Ω
Lower Drive Source Resistance	V_{PVCC} = 12V, 15mA Source Current		1.6		Ω
Lower Drive Sink Resistance	V_{PVCC} = 12V, 15mA Sink Current		1.1		Ω
SVI INTERFACE					
SVC, SVD Input HIGH (VIH)	FS resistor tied to GND	0.85			V
SVC, SVD Input LOW (VIL)	FS resistor tied to GND			0.45	V
SVC, SVD Input HIGH (VIH)	FS resistor tied to VCC	1.05			V
SVC, SVD Input LOW (VIL)	FS resistor tied to VCC			0.55	V
SVD Low Level Output Voltage	510Ω Resistor to 1.8V			0.4	V
SVC, SVD Leakage (Note 7)				±5	µA

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Limits should be considered typical and are not production tested.

Timing Diagram



Operation

The ISL6328 utilizes a multi-phase architecture to provide a low cost, space saving power conversion solution for the processor core voltage. The controller also implements a simple single phase architecture to provide the Northbridge voltage on the same chip.

NOTE: All references to VCC refer to the VCC pin or the node that is tied to the VCC pin. This should not be confused with the bias voltage as the bias rail can be separated from the VCC node by an RC filter resistor.

Multi-phase Power Conversion

Microprocessor load current profiles have changed to the point that the advantages of multi-phase power conversion are impossible to ignore. The technical challenges associated with producing a single-phase converter that is both cost-effective and thermally viable have forced a change to the cost-saving approach of multi-phase. The ISL6328 controller helps simplify implementation by integrating vital functions and requiring minimal external components. The “Controller Block Diagram” on page 3 provides a top level view of the multi-phase power conversion using the ISL6328 controller.

Interleaving

The switching of each channel in a multi-phase converter is timed to be symmetrically out-of-phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the three-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 2 and 3). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

Figure 1 illustrates the multiplicative effect on output ripple frequency. The three channel currents (IL1, IL2, and IL3) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The peak-to-peak current for each phase is about 7A, and the DC components of the inductor currents combine to feed the load.

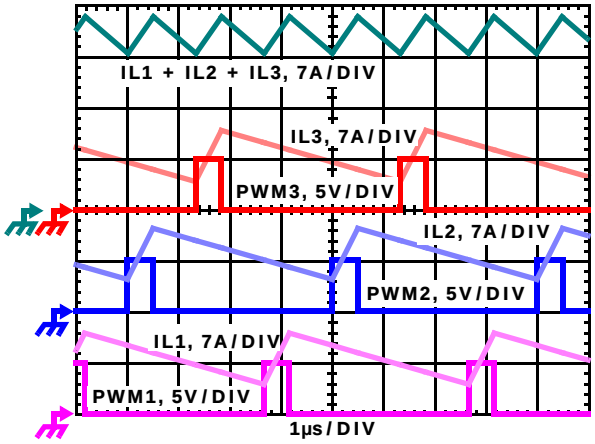


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

To understand the reduction of ripple current amplitude in the multi-phase circuit, examine Equation 2, which represents an individual channel peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{Lf_S V_{IN}} \quad \text{(EQ. 2)}$$

In Equation 2, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multi-phase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 2 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 3. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output-voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C,PP} = \frac{(V_{IN} - N\,V_{OUT})V_{OUT}}{Lf_S V_{IN}} \quad \text{(EQ. 3)}$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multi-phase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 2 illustrates input currents from a 3-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 2 delivers 1.5V to a 36A load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has $11.9A_{RMS}$ input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

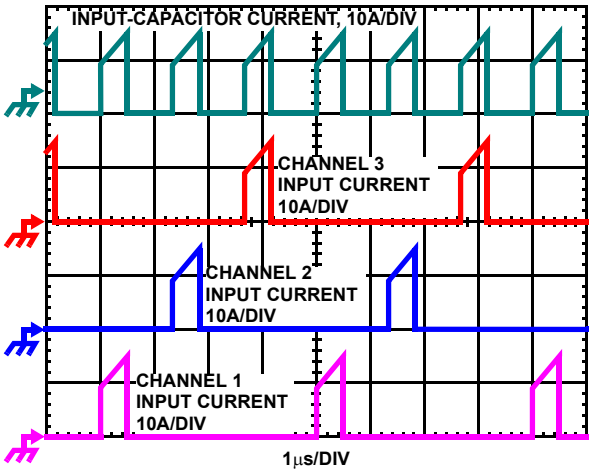


FIGURE 2. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

Figures 23, 24 and 25 in the section entitled “Input Capacitor Selection” on page 28 can be used to determine the input-capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution.

Active Pulse Positioning Modulated PWM Operation

The ISL6328 uses a proprietary Active Pulse Positioning (APP) modulation scheme to control the internal PWM signals that command each channel’s driver to turn their upper and lower MOSFETs on and off. The time interval in which a PWM signal can occur is generated by an internal clock, whose cycle time is the inverse of the switching frequency set by the resistor between the FS pin and ground. The advantage of Intersil’s proprietary Active Pulse Positioning (APP) modulator is that the PWM signal has the ability to turn on at any point during this PWM time interval, and turn off immediately after the PWM signal has transitioned high. This is important because it allows the controller to quickly respond to output voltage drops associated with current load spikes, while avoiding the ring back affects associated with other modulation schemes.

The PWM output state is driven by the position of the error amplifier output signal, V_{COMP}, minus the current correction signal relative to the proprietary modulator ramp waveform as illustrated in Figure 3. At the beginning of each PWM time interval, this modified V_{COMP} signal is compared to the internal modulator waveform. As long as the modified V_{COMP} voltage is lower then the modulator waveform voltage, the PWM signal is commanded low. The internal MOSFET driver detects the low state of the PWM signal and turns off the upper MOSFET and turns on the lower synchronous MOSFET. When the modified V_{COMP} voltage crosses the modulator ramp, the PWM output transitions high, turning off the synchronous MOSFET and turning on the upper MOSFET. The PWM signal will remain high until the modified V_{COMP} voltage crosses the modulator ramp again. When this occurs the PWM signal will transition low again.

During each PWM time interval, the PWM signal can only transition high once. Once PWM transitions high, it can not transition high again until the beginning of the next PWM time interval. This prevents the occurrence of double PWM pulses occurring during a single period.

To further improve the transient response, ISL6328 also implements Intersil’s proprietary Adaptive Phase Alignment (APA) technique, which turns on all phases together under transient events with large step current. With both APP and APA control, ISL6328 can achieve excellent transient performance and reduce the demand on the output capacitors.

Adaptive Phase Alignment (APA)

When a load is applied, the output will fall in direct relation to the amount of load being applied and the speed at which the load is being applied. The ISL6329 monitors the output differentially through the VSEN pin. If the sensed voltage drops quickly by a user programmable magnitude ($V_{APATRIP}$), all of the upper MOSFETs will immediately be turned on simultaneously. The trip level is relative, not absolute, and can be programmed through a resistor and capacitor tied in parallel from the APA pin to ground.

$$R_{APA} = \frac{V_{APATRIP}}{1.75\mu A} \quad \text{(EQ. 4)}$$

A 3900pF, X7R capacitor is required to be placed in parallel to the APA resistor.

PWM Operation

The timing of each core channel is set by the number of active channels. Channel detection on the ISEN2-, ISEN3- and ISEN4-, pins selects 1-channel to 4-channel operation for the ISL6328. The switching cycle is defined as the time between PWM pulse termination signals of each channel. The cycle time of the pulse signal is the inverse of the switching frequency set by the resistor between the FS pin and ground (or VCC). The PWM signals command the MOSFET driver to turn on/off the channel MOSFETs.

The channel firing order for 4-channel operation, the channel firing order is 1-2-3-4. For 3-channel operation, the channel firing order is 1-2-3.

Connecting ISEN4- to VCC selects three channel operation. To set 2-channel operation, both ISEN4- and ISEN3- must be tied to VCC. Similarly, to set single channel operation, ISEN4-, ISEN3- and ISEN2- must be tied to VCC.

Continuous Current Sampling

In order to realize proper current-balance, the currents in each channel are sampled continuously every switching cycle. During this time, the current-sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L. This sensed current, I_{SEN}, is simply a scaled version of the inductor current.

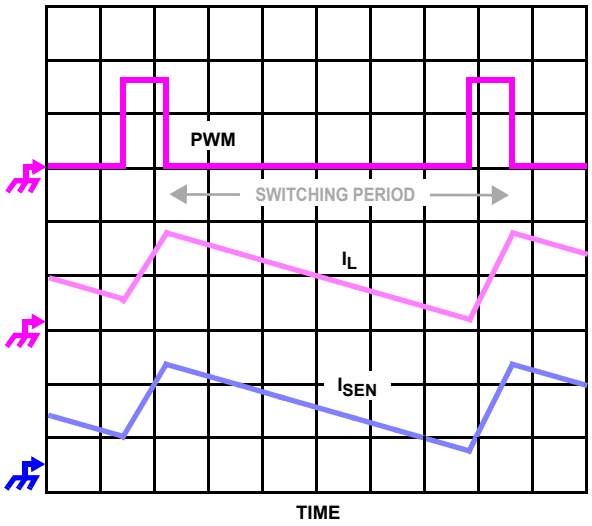


FIGURE 3. CONTINUOUS CURRENT SAMPLING

The ISL6328 supports Inductor DCR current sensing to continuously sample each channel's current for channel-current balance. The internal circuitry shown in Figure 4 represents Channel n of an n-Channel converter. This circuitry is repeated for each channel in the converter, but may not be active depending on how many channels are operating.

Inductor windings have a characteristic distributed resistance or DCR (Direct Current Resistance). For simplicity, the inductor DCR is considered as a separate lumped quantity, as shown in Figure 4. The channel current I_{Ln}, flowing through the inductor, passes through the DCR. Equation 5 shows the S-domain equivalent voltage, V_L, across the inductor.

$$V_L(s) = I_{L_n} \cdot (s \cdot L + DCR) \quad \text{(EQ. 5)}$$

A simple R-C network across the inductor (R_1, R_2 and C) extracts the DCR voltage, as shown in Figure 6. The voltage across the sense capacitor, V_C, can be shown to be proportional to the channel current I_{Ln}, shown in Equation 6.

$$V_C(s) = \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{\left(s \cdot \frac{(R_1 \cdot R_2)}{R_1 + R_2} \cdot C + 1\right)} \cdot K \cdot DCR \cdot I_{L_n} \quad \text{(EQ. 6)}$$

Where:

$$K = \frac{R_2}{R_2 + R_1} \quad \text{(EQ. 7)}$$

If the R-C network components are selected such that the RC time constant matches the inductor L/DCR time constant (see Equation 8), then V_C is equal to the voltage drop across the DCR

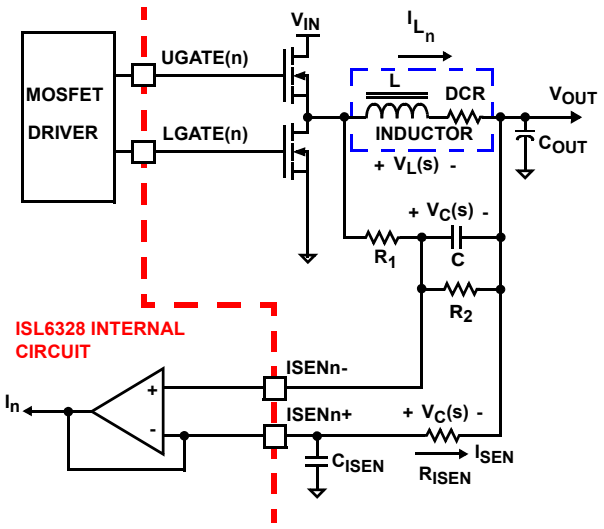


FIGURE 4. INDUCTOR DCR CURRENT SENSING CONFIGURATION

multiplied by the ratio of the resistor divider, K. If a resistor divider is not being used, the value for K is 1.

$$\frac{L}{DCR} = \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C \quad \text{(EQ. 8)}$$

The capacitor voltage V_C, is then replicated across the effective internal sense resistor, R_{ISEN}. This develops a current through R_{ISEN} which is proportional to the inductor current. This current, I_{SEN}, is continuously sensed and is then used by the controller for load-line regulation, channel-current balancing, and overcurrent detection and limiting. Equation 9 shows that the proportion between the channel current, I_L, and the sensed current, I_{SEN}, is driven by the value of the effective sense resistance, R_{ISEN}, and the DCR of the inductor.

$$I_{SEN} = I_L \cdot \frac{DCR}{R_{ISEN}} \quad \text{(EQ. 9)}$$

The Northbridge regulator samples the load current in the same manner as the Core regulator does.

The sampled currents, I_n, from each active channel are summed together and divided by the number of active channels. this current is then gained by 30%. The resulting cycle average current, I_{AVG}, provides a measure of the total load-current demand on the converter during each switching cycle. Assuming that the current in all the active channels is balanced, the average sensed current can be calculated from Equation 10.

$$I_{AVG} = \frac{I_{Load}}{N} \cdot \frac{DCR}{R_{ISEN}} \quad \text{(EQ. 10)}$$

In the ISL6328, the average scaled version of the load current, I_{AVG}, has a 100µA range. At 100µA, the Overcurrent Protection circuitry is enabled (refer to the "Overvoltage Protection" on page 21 for detailed information). It is recommended that the maximum load current correlate to an average sensed current, I_{AVG}, of 80µA.

A capacitor, C_{ISEN}, should be placed between the ISENn+ pin and ground. The value of the capacitor can be calculated using Equation 11.

$$C_{ISEN} = \frac{9.5ns}{R_{ISEN}} \quad \text{(EQ. 11)}$$

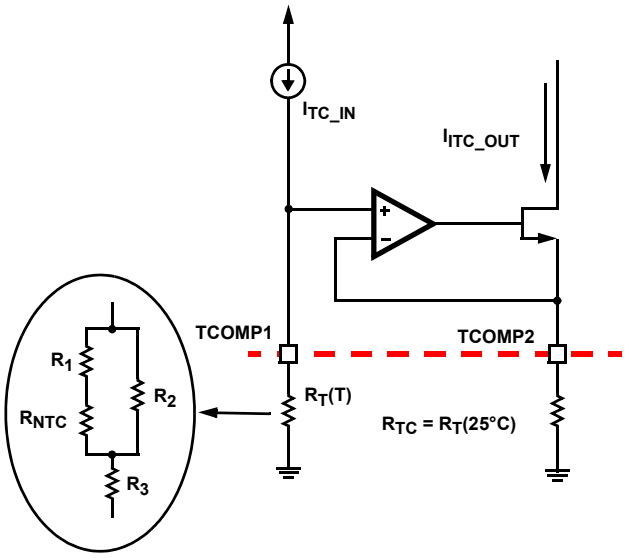


FIGURE 5. AVERAGE CURRENT TEMPERATURE COMPENSATION

Temperature Compensated Current Sensing

As the load increases, the conduction losses in the output inductors will cause the temperature of the inductors to rise. As the inductor temperature rises, the DCR of the output inductors will also rise. An increase in the DCR will result in an increase in the sensed current even if the load current remains constant. To counteract this error in the sensed current, the ISL6328 features a temperature compensating circuit that utilizes an NTC resistor to adjust the average current as inductor temperature increases. Figure 5 shows the implementation of the ISL6328 average current temperature compensation. The temperature dependent resistor, $R_T(T)$, is a combination of resistors and an NTC which create an approximate linearization of the NTC resistor (refer to Equation 12). Resistors R_1, R_2 and R_3 should be adjusted so that Equation 13 is satisfied.

$$R_T(T) = R_3 + \frac{1}{\frac{1}{R_1 + R_{NTC}} + \frac{1}{R_2}} \quad \text{(EQ. 12)}$$

$$R_T(T) = \frac{DCR(+25^\circ C)}{DCR(T)} \cdot R_{TC} \quad \text{(EQ. 13)}$$

Where $R_{TC} = R_T$ (+25°C)

LOAD MONITORING

The TCOMP2 pin can be utilized to monitor the load current. The voltage across the R_{TC} resistor is a temperature compensated representation of the load current. The load current is given by Equation 14.

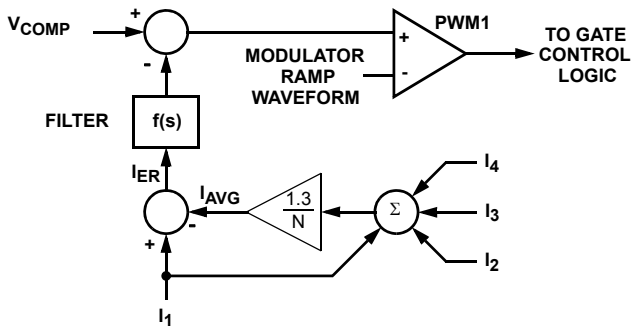
$$I_{LOAD} = 8 \cdot \frac{V_{TCOMP2}}{R_{TC}} \cdot \frac{R_{ISEN}}{DCR} \quad \text{(EQ. 14)}$$

Where R_{ISEN} is the current sense resistor value and DCR is the DC resistance of the output inductors. It is recommended that a high impedance buffer be used when monitoring the voltage on the TCOMP2 pin.

Channel-Current Balance

One important benefit of multi-phase operation is the thermal advantage gained by distributing the dissipated heat over multiple devices and greater area. By doing this the designer avoids the complexity of driving parallel MOSFETs and the expense of using expensive heat sinks and exotic magnetic materials.

In order to realize the thermal advantage, it is important that each channel in a multi-phase converter be controlled to carry about the same amount of current at any load level. To achieve this, the currents through each channel must be sampled every switching cycle. The sampled currents, I_n, from each active channel are summed together and divided by the number of active channels. The resulting cycle average current, I_{AVG}, provides a measure of the total load-current demand on the converter during each switching cycle. Channel-current balance is achieved by comparing the sampled current of each channel to the cycle average current, and making the proper adjustment to each channel pulse width based on the error. Intersil's patented current-balance method is illustrated in Figure 6, with error correction for Channel 1 represented. In the figure, the cycle average current, I_{AVG}, is compared with the Channel 1 sample, I_1, to create an error signal I_{ER}.



NOTE: CHANNELS 2, 3 AND 4 ARE OPTIONAL.

FIGURE 6. CHANNEL-1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

The filtered error signal modifies the pulse width commanded by V_{COMP} to correct any unbalance and force I_{ER} toward zero. The same method for error signal correction is applied to each active channel.

Serial VID Interface (SVI)

The on-board Serial VID interface (SVI) circuitry allows the processor to directly drive the core voltage and Northbridge voltage reference level within the ISL6328. The SVC and SVD

states are decoded with direction from the PWROK input as described in the sections that follow. The ISL6328 uses a digital to analog converter (DAC) to generate a reference voltage based on the decoded SVI value. See Figure 7 for a simple SVI interface timing diagram.

The upper and lower threshold levels for the SVI inputs are programmable through the FS pin. The FS resistor can be tied to either ground or to VCC. This option allows for selection of the SVID threshold levels.

TABLE 1. SVID THRESHOLDS

FS RESISTOR TIED TO	SVI VIL (V)	SVI VIH (V)
VCC	0.55	1.05
Ground	0.45	0.85

Pre-PWROK METAL VID

At start-up, the controller decodes the SVC and SVD inputs to determine the Pre-PWROK metal VID setting. Once the POR circuitry is satisfied, the ISL6328 begins decoding the inputs per Table 2. Once the EN input exceeds the rising enable threshold, the ISL6328 saves the Pre-PWROK metal VID value in an on-board holding register and passes this target to the internal DAC circuitry.

TABLE 2. PRE-PWROK METAL VID CODES

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

The Pre-PWROK metal VID code is decoded and latched on the rising edge of the enable signal. Once enabled, the ISL6328 passes the Pre-PWROK metal VID code on to internal DAC circuitry. The internal DAC circuitry begins to ramp both the VDD and VDDNB planes to the decoded Pre-PWROK metal VID output level. The digital soft-start circuitry actually stair steps the internal reference to the target gradually over a fixed interval. The controlled ramp of both output voltage planes reduces in-rush current during the soft-start interval. At the end of the soft-start interval, the VDDPWRGD output transitions high indicating both output planes are within regulation limits.

SVI Mode

Once the controller has successfully soft-started and VDDPWRGD transitions high, the Northbridge SVI interface can assert PWROK to signal the ISL6328 to prepare for SVI commands. The controller actively monitors the SVI interface for set VID commands to move the plane voltages to start-up VID values. Details of the SVI Bus protocol are provided in the AMD Design Guide for Voltage Regulator Controllers Accepting Serial VID Codes specification.

Once the set VID command is received, the ISL6328 decodes the information to determine which plane and the VID target required. See Table 3. The internal DAC circuitry steps the required output plane voltage to the new VID level. During this time one or both of the planes could be targeted. In the event the core voltage plane, VDD, is commanded to power off by serial VID commands, the VDDPWRGD signal remains asserted. The Northbridge voltage plane must remain active during this time.

If the PWROK input is de-asserted, then the controller steps both VDD and VDDNB planes back to the stored Pre-PWROK metal VID level in the holding register from initial soft-start. No attempt is made to read the SVC and SVD inputs during this time. If PWROK is reasserted, then the on-board SVI interface waits for a set VID command.

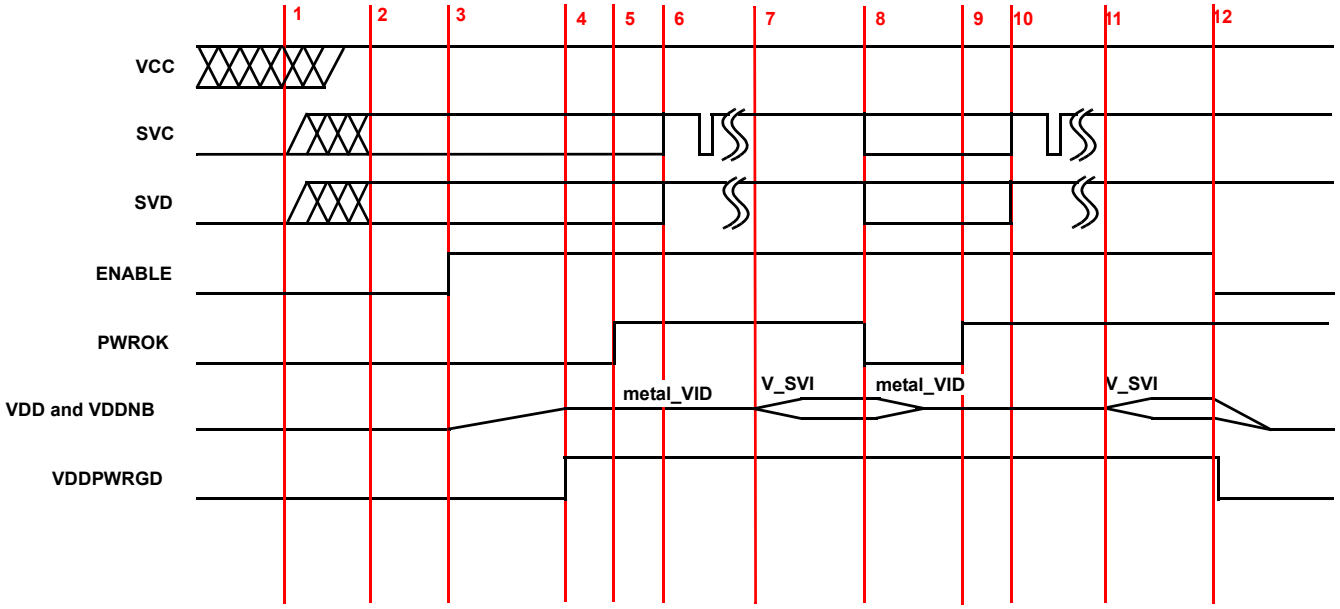


FIGURE 7. SVI INTERFACE TIMING DIAGRAM: TYPICAL PRE-PWROK METAL VID START-UP

TABLE 3. SERIAL VID CODES

SVID[6:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)
000_0000b	1.5500	010_0000b	1.1500	100_0000b	0.7500	110_0000b	0.3500*
000_0001b	1.5375	010_0001b	1.1375	100_0001b	0.7375	110_0001b	0.3375*
000_0010b	1.5250	010_0010b	1.1250	100_0010b	0.7250	110_0010b	0.3250*
000_0011b	1.5125	010_0011b	1.1125	100_0011b	0.7125	110_0011b	0.3125*
000_0100b	1.5000	010_0100b	1.1000	100_0100b	0.7000	110_0100b	0.3000*
000_0101b	1.4875	010_0101b	1.0875	100_0101b	0.6875	110_0101b	0.2875*
000_0110b	1.4750	010_0110b	1.0750	100_0110b	0.6750	110_0110b	0.2750*
000_0111b	1.4625	010_0111b	1.0625	100_0111b	0.6625	110_0111b	0.2625*
000_1000b	1.4500	010_1000b	1.0500	100_1000b	0.6500	110_1000b	0.2500*
000_1001b	1.4375	010_1001b	1.0375	100_1001b	0.6375	110_1001b	0.2375*
000_1010b	1.4250	010_1010b	1.0250	100_1010b	0.6250	110_1010b	0.2250*
000_1011b	1.4125	010_1011b	1.0125	100_1011b	0.6125	110_1011b	0.2125*
000_1100b	1.4000	010_1100b	1.0000	100_1100b	0.6000	110_1100b	0.2000*
000_1101b	1.3875	010_1101b	0.9875	100_1101b	0.5875	110_1101b	0.1875*
000_1110b	1.3750	010_1110b	0.9750	100_1110b	0.5750	110_1110b	0.1750*
000_1111b	1.3625	010_1111b	0.9625	100_1111b	0.5625	110_1111b	0.1625*
001_0000b	1.3500	011_0000b	0.9500	101_0000b	0.5500	111_0000b	0.1500*
001_0001b	1.3375	011_0001b	0.9375	101_0001b	0.5375	111_0001b	0.1375*
001_0010b	1.3250	011_0010b	0.9250	101_0010b	0.5250	111_0010b	0.1250*
001_0011b	1.3125	011_0011b	0.9125	101_0011b	0.5125	111_0011b	0.1125*
001_0100b	1.3000	011_0100b	0.9000	101_0100b	0.5000	111_0100b	0.1000*
001_0101b	1.2875	011_0101b	0.8875	101_0101b	0.4875*	111_0101b	0.0875*
001_0110b	1.2750	011_0110b	0.8750	101_0110b	0.4750*	111_0110b	0.0750*
001_0111b	1.2625	011_0111b	0.8625	101_0111b	0.4625*	111_0111b	0.0625*
001_1000b	1.2500	011_1000b	0.8500	101_1000b	0.4500*	111_1000b	0.0500*
001_1001b	1.2375	011_1001b	0.8375	101_1001b	0.4375*	111_1001b	0.0375*
001_1010b	1.2250	011_1010b	0.8250	101_1010b	0.4250*	111_1010b	0.0250*
001_1011b	1.2125	011_1011b	0.8125	101_1011b	0.4125*	111_1011b	0.0125*
001_1100b	1.2000	011_1100b	0.8000	101_1100b	0.4000*	111_1100b	OFF
001_1101b	1.1875	011_1101b	0.7875	101_1101b	0.3875*	111_1101b	OFF
001_1110b	1.1750	011_1110b	0.7750	101_1110b	0.3750*	111_1110b	OFF
001_1111b	1.1625	011_1111b	0.7625	101_1111b	0.3625*	111_1111b	OFF

NOTE: * Indicates a VID not required for AMD Family 10h processors.

Power Savings Mode: PSI_L

Bit 7 of the Serial VID codes transmitted as part of the 8-bit data stream over the SVI bus is allocated for the PSI_L. If bit 7 is 0, then the processor is at an optimal load for the regulator to enter power savings mode. If bit 7 is 1, then the regulator should not be in power savings mode.

With the ISL6328, Power Savings mode is realized through phase shedding, Gate Voltage Optimization and Diode Emulation. Once a Serial VID command with Bit 7 set to 0 is received, the ISL6328 will shed phases in a sequential manner until then minimum phase count for PSI is reached. The minimum phase count for PSI can be programmed via the DRPCTRL pin to be either 1 phase or 2 phases. If the DRPCTRL resistor is tied to ground, then the minimum phase count in PSI is 1 phase. If the DRPCTRL resistor is tied to VCC then the minimum phase count in PSI is 2 phases. Channels are shed in reverse sequential order so that the highest numbered channel that is active will be shed first. When a phase is shed, that phase will not go into a tri-state mode until that phase would have had its PWM go HIGH.

When leaving Power Savings Mode, through the reception of a Serial VID command with Bit 7 set to 1, the ISL6328 will sequentially turn on phases starting with lowest numbered inactive channel. When a phase is being reactivated, it will not leave a tri-state until the PWM of that phase goes HIGH.

If, while in Power Savings Mode, a Serial VID command is received that forces a VID level change while maintaining Bit 7 at 0, the ISL6328 will first exit the Power Savings Mode state as

described previously. The output voltage will then be stepped up or down to the appropriate VID level. Finally, the ISL6328 will then re-enter Power Savings Mode.

While in Power Savings Mode, the ISL6328 implements two features that effectively enhance the efficiency of the regulator even more. These features are Diode Emulation and Gate Voltage Optimization.

DIODE EMULATION

While in Power Savings Mode, the active phases will behave as if they are in a standard buck configuration. To accomplish this, the lower MOSFET is turned on only while there is current flowing to the load. This behavior emulates the diode in a standard buck. The conduction loss across the $R_{DS}(on)$ of the MOSFET, however, is much less than a diode, resulting in a measurable power savings.

GATE VOLTAGE OPTIMIZATION

While in Power Savings Mode, the gate drive voltage for the lower MOSFETs of the active phases is reduced from the nominal 12V that is utilized in Normal mode to 5.75V. Lowering the gate drive voltage can have an appreciable effect on the efficiency of the converter.

In order to utilize 5V gate drive at all times, 5V should be tied to the PVCC pin and the GVOT pin should be shorted to the PVCC pin. This configuration will allow for 5V gate drive in all modes of operation.

Voltage Regulation

The integrating compensation network shown in Figure 8 insures that the steady-state error in the output voltage is limited only to the error in the reference voltage and offset errors in the OFS current source, remote-sense and error amplifiers. Intersil specifies the guaranteed tolerance of the ISL6328 to include the combined tolerances of each of these elements.

The output of the error amplifier, V_{COMP}, is used by the modulator to generate the PWM signals. The PWM signals control the timing of the Internal MOSFET drivers and regulate the converter output so that the voltage at FB is equal to the voltage at REF. This will regulate the output voltage to be equal to Equation 15. The internal and external circuitry that controls voltage regulation is illustrated in Figure 8.

$$V_{OUT} = V_{REF} - V_{OFS} - V_{DROOP} \quad \text{(EQ. 15)}$$

The ISL6328 incorporates differential remote-sense amplification in the feedback path. The differential sensing removes the voltage error encountered when measuring the output voltage relative to the controller ground reference point resulting in a more accurate means of sensing output voltage.

Load-Line (Droop) Regulation

By adding a well controlled output impedance, the output voltage can effectively be level shifted in a direction which works to achieve a cost-effective solution can help to reduce the output-voltage spike that results from fast load-current demand changes.

The magnitude of the spike is dictated by the ESR and ESL of the output capacitors selected. By positioning the no-load voltage level near the upper specification limit, a larger negative spike can be sustained without crossing the lower limit. By adding a well controlled output impedance, the output voltage under load can effectively be level shifted down so that a larger positive spike can be sustained without crossing the upper specification limit.

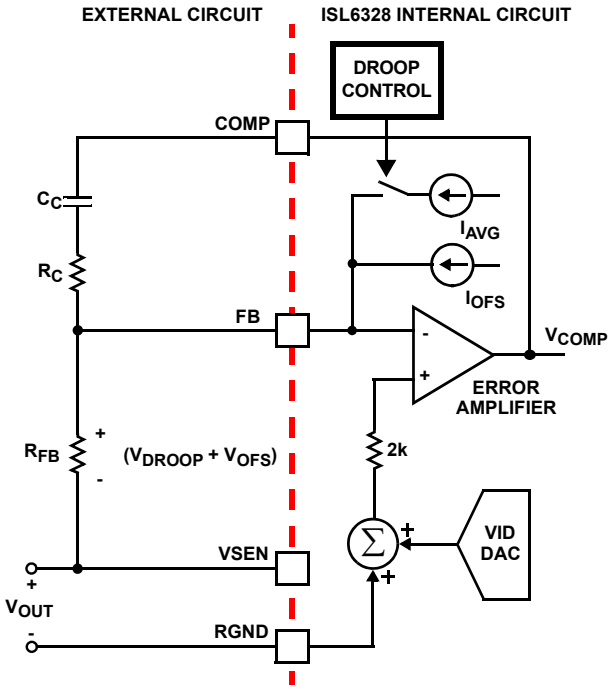


FIGURE 8. OUTPUT VOLTAGE AND LOAD-LINE REGULATION WITH OFFSET ADJUSTMENT

As shown in Figure 8, with droop enabled, the average current of all active channels, I_{AVG}, flows from FB through a load-line regulation resistor R_{FB}. The resulting voltage drop across R_{FB} is proportional to the output current, effectively creating an output voltage droop with a steady-state value defined as:

$$V_{DROOP} = I_{AVG} \cdot R_{FB} \quad \text{(EQ. 16)}$$

The regulated output voltage is reduced by the droop voltage V_{DROOP}. The output voltage as a function of load current is shown in Equation 17.

$$V_{OUT} = V_{REF} - V_{OFS} - \left(\frac{I_{OUT}}{N} \cdot \frac{DCR}{R_{ISEN}} \cdot K \cdot R_{FB}\right) \quad \text{(EQ. 17)}$$

In Equation 17, V_{REF} is the reference voltage, V_{OFS} is the programmed offset voltage, I_{OUT} is the total output current of the converter, K is the DC gain of the RC filter across the inductor (K is defined in Equation 8), N is the number of active channels, and DCR is the distributed inductor impedance value.

Droop Control

The DRPCTRL (Droop Control) pin is used to enable and/or disable load line regulation on both the Core and Northbridge regulators. The pin is also used to set the number of phases in Power Savings Mode (PSI) mode. A single resistor tied from the DRPCTRL pin to either GND or VCC will program the ISL6328 to either enable or disable droop on both Core and Northbridge simultaneously.

TABLE 4. DRPCTRL FUNCTIONALITY

RESISTOR VALUE	CORE DROOP	NB DROOP
100kΩ	Disabled	Disabled
50kΩ	Disabled	Enabled
20kΩ	Enabled	Enabled
0Ω	Enabled	Disabled

If the DRPCTRL resistor is tied to ground, then the number of phases in PSI mode is 1. If the DRPCTRL resistor is tied to VCC, then the minimum number of phases in PSI mode is 2.

Output-Voltage Offset Programming

The ISL6328 allows the designer to accurately adjust the offset voltage by connecting a resistor, R_{OFS}, from the OFS pin to VCC or GND. When R_{OFS} is connected between OFS and VCC, the voltage across it is regulated to 1.6V. This causes a proportional current (I_{OFS}) to flow into the FB pin and out of the OFS pin. If R_{OFS} is connected to ground, the voltage across it is regulated to 0.3V, and I_{OFS} flows into the OFS pin and out of the FB pin. The offset current flowing through the resistor between VDIFF and FB will generate the desired offset voltage which is equal to the product (I_{OFS} x R_{FB}). These functions are shown in Figures 9 and 10.

Once the desired output offset voltage has been determined, use the following formulas to set R_{OFS}:

For Positive Offset (connect R_{OFS} to GND):

$$R_{OFS} = \frac{0.3 \cdot R_{FB}}{V_{OFFSET}} \quad \text{(EQ. 18)}$$

For Negative Offset (connect R_{OFS} to VCC):

$$R_{OFS} = \frac{1.6 \cdot R_{FB}}{V_{OFFSET}} \quad \text{(EQ. 19)}$$

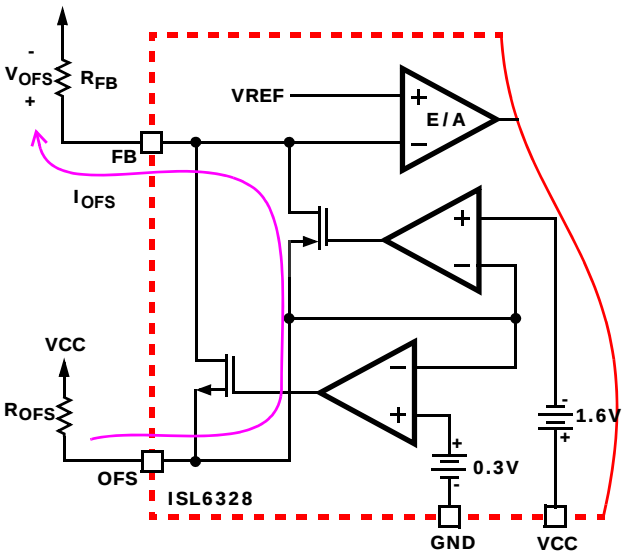


FIGURE 9. NEGATIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

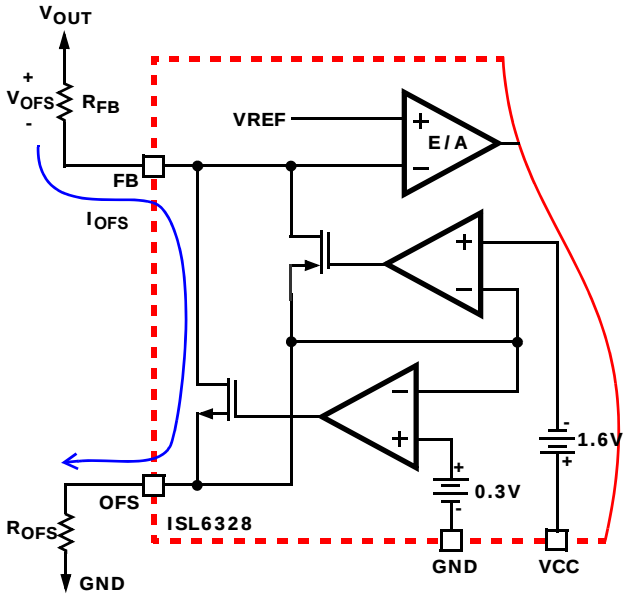


FIGURE 10. POSITIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

Dynamic VID

The AMD processor does not step the output voltage commands up or down to the target voltage, but instead passes only the target voltage to the ISL6328 through the SVI interface. The ISL6328 manages the resulting VID-on-the-Fly transition in a controlled manner, supervising a safe output voltage transition without discontinuity or disruption. The ISL6328 begins slewing the DAC at 3.0mV/µs until the DAC and target voltage are equal. Thus, the total time required for a dynamic VID transition is dependent only on the size of the DAC change.

Advanced Adaptive Zero Shoot-Through Deadtime Control (Patent Pending)

The integrated drivers incorporate a unique adaptive deadtime control technique to minimize deadtime, resulting in high efficiency from the reduced freewheeling time of the lower MOSFET body-diode conduction, and to prevent the upper and lower MOSFETs from conducting simultaneously. This is accomplished by ensuring either rising gate turns on its MOSFET with minimum and sufficient delay after the other has turned off.

During turn-off of the lower MOSFET, the PHASE voltage is monitored until it reaches a -0.3V/+0.8V (forward/reverse inductor current). At this time the UGATE is released to rise. An auto-zero comparator is used to correct the $r_{DS(ON)}$ drop in the phase voltage preventing false detection of the -0.3V phase level during $r_{DS(ON)}$ conduction period. In the case of zero current, the UGATE is released after 35ns delay of the LGATE dropping below 0.5V. When LGATE first begins to transition low, this quick transition can disturb the PHASE node and cause a false trip, so there is 20ns of blanking time once LGATE falls until PHASE is monitored.

Once the PHASE is high, the advanced adaptive shoot-through circuitry monitors the PHASE and UGATE voltages during a PWM falling edge and the subsequent UGATE turn-off. If either the UGATE falls to less than 1.75V above the PHASE or the PHASE falls to less than +0.8V, the LGATE is released to turn-on.

Initialization

Prior to initialization, proper conditions must exist on the EN, VCC, GVOT, PVCC, ISEN2-, ISEN3- and ISEN4- pins. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, the controller asserts VDDPWRGD.

Power-On Reset

The ISL6328 requires VCC, PVCC and GVOT inputs to exceed their rising POR thresholds before the ISL6328 has sufficient bias to guarantee proper operation.

The bias voltage applied to VCC must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, the ISL6328 has enough bias to begin checking the driver POR inputs, EN, and channel detect portions of the initialization cycle. Hysteresis between the rising and falling thresholds assure the ISL6328 will not advertently turn off unless the bias voltage drops substantially (see “Electrical Specifications” on page 9).

The bias voltage applied to the PVCC pin powers the internal MOSFET drivers of each output channel. In order for the ISL6328 to begin operation, the PVCC input must exceed its POR rising threshold to guarantee proper operation of the internal drivers. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6328 will not inadvertently turn off unless the PVCC bias voltage drops substantially (see “Electrical Specifications” on page 9). Depending on the number of active CORE channels determined by the Phase Detect block, the external driver POR checking is supported by the Enable Comparator.

Enable Comparator

The ISL6328 features a dual function enable input (EN) for enabling the controller and power sequencing between the controller and external drivers or another voltage rail. The enable comparator holds the ISL6328 in shutdown until the voltage at EN rises above 0.86V. The enable comparator has about 110mV of hysteresis to prevent bounce. It is important that the driver ICs reach their rising POR level before the ISL6328 becomes enabled. The schematic in Figure 12 demonstrates sequencing the ISL6328 with the ISL66xx family of Intersil MOSFET drivers, which require 12V bias.

When selecting the value of the resistor divider the driver maximum rising POR threshold should be used for calculating the proper resistor values. This will prevent improper sequencing events from creating false trips during soft-start.

If the controller is configured for 1- or 2-phase CORE operation, then the resistor divider can be used for sequencing the controller with another voltage rail. The resistor divider to EN should be selected using a similar approach as the previous driver discussion.

Phase Detection

The ISEN2-, ISEN3- and ISEN4- pins are monitored prior to soft-start to determine the number of active CORE channel phases.

If ISEN4- is tied to VCC, the controller will set the channel firing order and timing for 3-phase operation. If ISEN4- and ISEN3- are tied to VCC, the controller will set the channel firing order and timing for a 2-phase operation. The controller will configure itself as a single phase regulator if ISEN4-, ISEN3- and ISEN2- are tied to VCC (see “PWM Operation” on page 13 for details).

Soft-Start Output Voltage Targets

Once the POR and Phase Detect blocks and enable comparator are satisfied, the controller will begin the soft-start sequence and will ramp the CORE and NB output voltages up to the SVI interface designated target level. Prior to soft-starting both CORE and NB outputs, the ISL6328 must check the state of the SVI interface inputs to determine the correct target voltages for both outputs. When the controller is enabled, the state of the SVD and SVC inputs are checked and the target output voltages set for both CORE and NB outputs are set by the DAC (see “Serial VID Interface (SVI)” on page 15). These targets will only change if the EN signal is pulled low or after a POR reset of VCC.

Soft-Start

The soft-start sequence is composed of three periods, as shown in Figure 11. At the beginning of soft-start, the DAC immediately obtains the output voltage target. A 100µs fixed delay time, TDA, proceeds the output voltage rise. After this delay period the ISL6328 will begin ramping both CORE and NB output voltages to the programmed DAC level at a fixed rate of 3.25mV/µs. The amount of time required to ramp the output voltage to the final DAC voltage is referred to as TDB, and can be calculated as shown in Equation 20.

$$TDB = \frac{V_{DAC}}{3.0 \cdot 10^{-3}} \quad \text{(EQ. 20)}$$

After the DAC voltage reaches the final VID setting, PGOOD will be set to high.

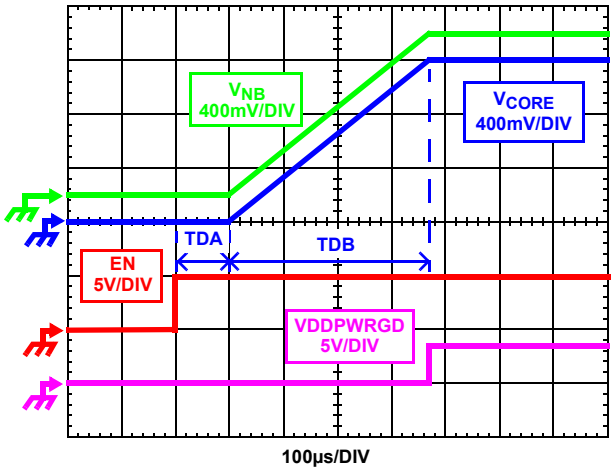


FIGURE 11. SOFT-START WAVEFORMS

Pre-Biased Soft-Start

The ISL6328 also has the ability to start up into a pre-charged output, without causing any unnecessary disturbance. The FB pin is monitored during soft-start, and should it be higher than the equivalent internal ramping reference voltage, the output drives hold both MOSFETs off.

Once the internal ramping reference exceeds the FB pin potential, the output drives are enabled, allowing the output to

ramp from the pre-charged level to the final level dictated by the DAC setting. Should the output be pre-charged to a level exceeding the DAC setting, the output drives are enabled at the end of the soft-start period, leading to an abrupt correction in the output voltage down to the DAC-set level.

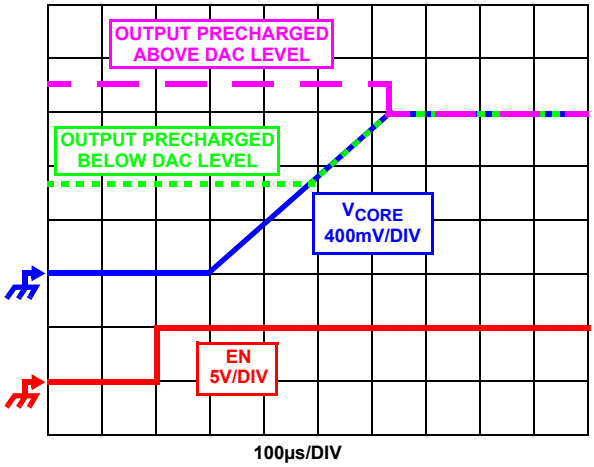


FIGURE 12. SOFT-START WAVEFORMS FOR ISL6328-BASED MULTIPHASE CONVERTER

Both CORE and NB output support start up into a pre-charged output.

Fault Monitoring and Protection

The ISL6328 actively monitors both CORE and NB output voltages and currents to detect fault conditions. Fault monitors trigger protective measures to prevent damage to either load. One common power-good indicator is provided for linking to external system monitors. The schematic in Figure 13 outlines the interaction between the fault monitors and the power-good signal.

Power-Good Signal

The power-good pin (VDDPWRGD) is an open-drain logic output that signals whether or not the ISL6328 is regulating both NB and CORE output voltages within the proper levels, and whether any fault conditions exist. This pin should be tied to a +5V source through a resistor.

During shutdown and soft-start, VDDPWRGD pulls low and releases high after a successful soft-start and both output voltages are operating between the undervoltage and overvoltage limits. PGOOD transitions low when an undervoltage, overvoltage, or overcurrent condition is detected on either output or when the controller is disabled by a POR reset or EN. In the event of an overvoltage or overcurrent condition, the controller latches off and PGOOD will not return high. Pending a POR reset of the ISL6328 and successful soft-start, the PGOOD will return high.

Overvoltage Protection

The ISL6328 constantly monitors the sensed output voltage on the VSEN pin to detect if an overvoltage event occurs. When the output voltage rises above the OVP trip level and exceeds the PGOOD OV limit actions are taken by the ISL6328 to protect the microprocessor load.

At the inception of an overvoltage event, both on-board lower gate pins are commanded low as are the active PWM outputs to the external drivers, the PGOOD signal is driven low, and the ISL6328 latches off normal PWM action. This turns on the all of the lower MOSFETs and pulls the output voltage below a level that might cause damage to the load. The lower MOSFETs remain driven ON until VSEN falls below 400mV. The ISL6328 will continue to protect the load in this fashion as long as the overvoltage condition recurs. Once an overvoltage condition ends the ISL6328 latches off, and must be reset by toggling POR, before a soft-start can be re-initiated.

Pre-POR Overvoltage Protection

Prior to PVCC, VCC and GVOT exceeding their POR levels, the ISL6328 is designed to protect either load from any overvoltage events that may occur. This is accomplished by means of an internal 10kΩ resistor tied from PHASE to LGATE, which turns on the lower MOSFET to control the output voltage until the overvoltage event ceases or the input power supply cuts off. For complete protection, the low side MOSFET should have a gate threshold well below the maximum voltage rating of the load/microprocessor.

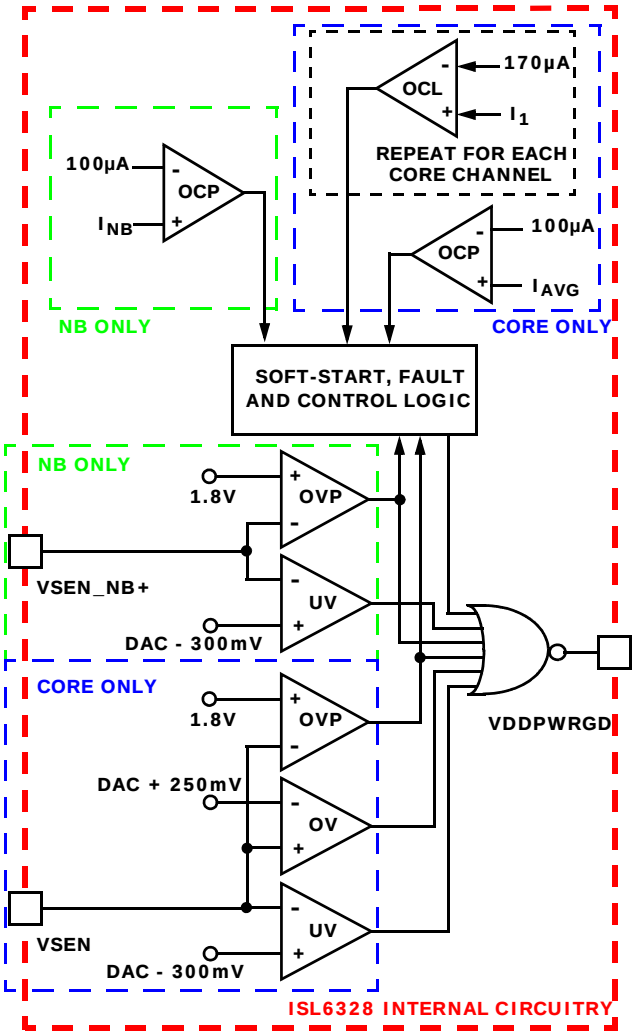


FIGURE 13. POWER GOOD AND PROTECTION CIRCUITRY

In the event that during normal operation if the PVCC, VCC or GVOT voltage falls back below the POR threshold, the pre-POR overvoltage protection circuitry reactivates to protect from any more pre-POR overvoltage events.

Undervoltage Detection

The undervoltage threshold is set at VDAC - 300mV typical. When the output voltage (VSEN-RGND) is below the undervoltage threshold, PGOOD gets pulled low. No other action is taken by the controller. PGOOD will return high if the output voltage rises above VDAC - 250mV typical.

Open Sense Line Protection

In the case that either of the remote sense lines, VSEN or GND, become open, the ISL6328 is designed to detect this and shut down the controller. This event is detected by monitoring small currents that are fed out the VSEN and RGND pins. In the event of an open sense line fault, the controller will continue to remain off until the fault goes away, at which point the controller will re-initiate a soft-start sequence.

Overcurrent Protection

The ISL6328 takes advantage of the proportionality between the load current and the average current, I_{AVG}, to detect an overcurrent condition. See "Continuous Current Sampling" on page 14 and "Channel-Current Balance" on page 15 for more detail on how the average current is measured. Once the average current exceeds 100µA, a comparator triggers the converter to begin overcurrent protection procedures.

The overcurrent trip threshold is dictated by the DCR of the inductors, the number of active channels, the DC gain of the inductor RC filter and the R_{ISEN} resistor. The overcurrent trip threshold is shown in Equation 21.

$$I_{OCP} = 100\,mA \cdot \frac{N}{DCR} \cdot \frac{1}{K} \cdot R_{ISEN} - \frac{V_{IN} - N \cdot V_{OUT}}{2 \cdot L \cdot f_S} \cdot \frac{V_{OUT}}{V_{IN}} \qquad \text{(EQ. 21)}$$

Where:

$K = \frac{R_2}{R_1 + R_2}$ See "Continuous Current Sampling" on page 14.

f_{SW} = Switching Frequency

Equation 21 is valid for both the Core regulator and the Northbridge regulator. This equation includes the DC load current as well as the total ripple current contributed by all the phases. For the Northbridge regulator, N is 1.

During soft-start, the overcurrent trip point is boosted by a factor of 1.35. Instead of comparing the average measured current to 100µA, the average current is compared to 135µA. Immediately after soft-start is over, the comparison level changes to 100µA. This is done to allow for start-up into an active load while still supplying output capacitor in-rush current.

OVERCURRENT PROTECTION SHUTDOWN

At the beginning of overcurrent shutdown, the controller sets all of the UGATE and LGATE signals low, puts PWM3 and PWM4 (if active) in a high-impedance state, and forces VDDPWRGD low. This turns off all of the upper and lower MOSFETs. The system remains in this state for fixed period of 12ms. If the controller is still enabled at the end of this wait period, it will attempt a soft-start, as shown in Figure 14. If the fault remains, the trip-retry cycles will continue until either the fault is cleared or for a total of seven attempts. If the fault is not cleared on the final attempt, the controller disables UGATE and LGATE signals for both Core and Northbridge and latches off requiring a POR of VCC to reset the ISL6328.

It is important to note that during soft-start, the overcurrent trip point is increased by a factor of 1.35. If the fault draws enough current to trip overcurrent during normal run mode, it may not draw enough current during the soft-start ramp period to trip overcurrent while the output is ramping up. If a fault of this type is affecting the output, then the regulator will complete soft-start and the trip-retry counter will be reset to zero. Once the regulator has completed soft-start, the overcurrent trip point will return to it's nominal setting and an overcurrent shutdown will be initiated. This will result in a continuous hiccup mode.

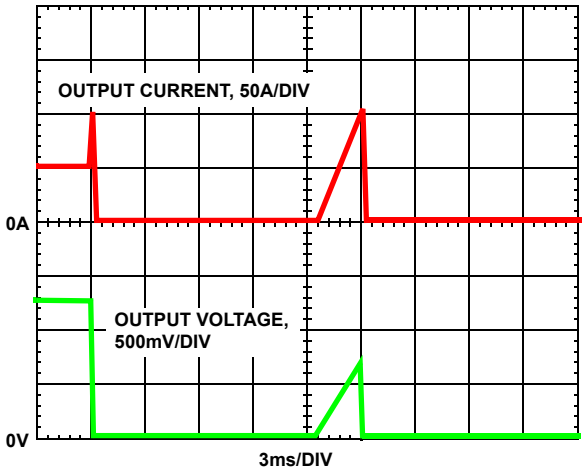


FIGURE 14. OVERCURRENT BEHAVIOR IN HICCUP MODE

Note that the energy delivered during trip-retry cycling is much less than during full-load operation, so there is no thermal hazard.

CORE REGULATOR OVERCURRENT

The ISL6328 features a Dual Overcurrent Protection (OCP) feature on the Core that allows AMD processors to "throttle" the load current beyond the normal OCP threshold for brief periods of time. These current spikes occur when idle processor cores are enabled. Dual OCP is not enabled until soft-start is complete.

When the Core average sensed current, I_{AVG}, exceeds 100µA, the Core regulator does not immediately initiate overcurrent protection shutdown. The ISL6328 will, instead, source an amount of current out of the OCP pin that is equivalent to the amount of sensed current that exceeds 100µA. A capacitor tied between the OCP pin and ground will immediately begin charging. If the voltage across the capacitor, and thus the voltage on the OCP pin, exceeds 2V then the ISL6328 will immediately initiate overcurrent protection shutdown. If I_{AVG} decreases to a level below 100µA prior to the voltage on the OCP pin exceeding 2V, then the OCP pin is internally pulled to ground and the voltage on the OCP capacitor is discharged. If, at any time, the average sensed current exceeds 145µA, the ISL6328 will immediately initiate overcurrent protection shutdown.

It is recommended that the maximum current spike correspond to an average sensed current level of 120µA. It is also recommended that if the maximum current spike load was applied to the Core regulator that overcurrent protection shutdown initiate after 1ms. This would require a 0.01µF capacitor be tied to the OCP pin. To calculate the OCP capacitor, use Equation 22.

$$C_{OCP} = \frac{20\mu A \cdot t_{DELAY}}{2V} \quad \text{(EQ. 22)}$$

NORTHBRIDGE REGULATOR OVERCURRENT

The Northbridge regulator does not incorporate dual OCP. When the sensed current of the Northbridge exceeds 100µA, Overcurrent Protection Shutdown is initiated. The overcurrent shutdown for the Northbridge regulator will only disable the MOSFET drivers for the Northbridge. Once 7 retry attempts have been executed unsuccessfully, the controller will disable UGATE and LGATE signals for both Core and Northbridge and will latch off requiring a POR of VCC to reset the ISL6328.

OVERCURRENT PROTECTION IN POWER SAVINGS MODE

While in Power Savings Mode, the OCP trip point will be lower than when running in Normal Mode and there is no accommodation for current throttling. Equation 21, with N = 1, will yield the OCP trip point for the Core regulator while in Power Savings mode.

If an overcurrent event should occur while the system is in Power Savings Mode, the ISL6328 will restart in the Normal state with the PSI_L bit set to 1.

Individual Channel Overcurrent Limiting

The ISL6328 has the ability to limit the current in each individual channel of the Core regulator without shutting down the entire regulator. This is accomplished by continuously comparing the sensed currents of each channel with a constant 170µA OCL reference current. If a channel's individual sensed current exceeds this OCL limit, the UGATE signal of that channel is immediately forced low, and the LGATE signal is forced high. This turns off the upper MOSFET(s), turns on the lower MOSFET(s), and stops the rise of current in that channel, forcing the current in the channel to decrease. That channel's UGATE signal will not be able to return high until the sensed channel current falls back below the 170µA reference.

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multiphase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts for all common microprocessor applications.

Power Stages

The first step in designing a multiphase converter is to determine the number of phases. This determination depends heavily on the cost analysis which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board, whether through-hole components are permitted, the total board space available for power-supply circuitry, and the maximum amount of load current. Generally speaking, the most economical solutions are those in which each phase handles between 25A and 30A. All surface-mount designs will tend toward the lower end of this current range. If through-hole MOSFETs and inductors can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat-dissipating surfaces.

MOSFETS

The choice of MOSFETs depends on the current each MOSFET will be required to conduct, the switching frequency, the capability of the MOSFETs to dissipate heat, and the availability and nature of heat sinking and air flow.

LOWER MOSFET POWER CALCULATION

The calculation for power loss in the lower MOSFET is simple, since virtually all of the loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 23, I_M is the maximum continuous output current, I_{PP} is the peak-to-peak inductor current (see Equation 2), and d is the duty cycle (V_{OUT}/V_{IN}).

$$P_{LOW,1} = r_{DS(ON)} \cdot \left[\left(\frac{I_M}{N}\right)^2 \cdot (1-d) + \frac{I_{L,PP}^2 \cdot (1-d)}{12}\right] \quad \text{(EQ. 23)}$$

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$, the switching frequency, f_S, and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower-MOSFET conduction interval respectively.

$$P_{LOW,2} = V_{D(ON)} \cdot f_S \cdot \left[\left(\frac{I_M}{N} + \frac{I_{PP}}{2}\right) \cdot t_{d1} + \left(\frac{I_M}{N} - \frac{I_{PP}}{2}\right) \cdot t_{d2}\right] \quad \text{(EQ. 24)}$$

The total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW,1}$ and $P_{LOW,2}$.

UPPER MOSFET POWER CALCULATION

In addition to $r_{DS(ON)}$ losses, a large portion of the upper-MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper-MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper-MOSFET switching times, the lower-MOSFET body-diode reverse-recovery charge, Q_{rr}, and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 25, the required time for this

commutation is t_1 and the approximated associated power loss is $P_{UP,1}$.

$$P_{UP,1} \approx V_{IN} \cdot \left(\frac{I_M}{N} + \frac{I_{PP}}{2}\right) \cdot \left(\frac{t_1}{2}\right) \cdot f_S \quad \text{(EQ. 25)}$$

At turn on, the upper MOSFET begins to conduct and this transition occurs over a time t_2. In Equation 26, the approximate power loss is $P_{UP,2}$.

$$P_{UP,2} \approx V_{IN} \cdot \left(\frac{I_M}{N} - \frac{I_{PP}}{2}\right) \cdot \left(\frac{t_2}{2}\right) \cdot f_S \quad \text{(EQ. 26)}$$

A third component involves the lower MOSFET reverse-recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET body diode can recover all of Q_{rr}, it is conducted through the upper MOSFET across VIN. The power dissipated as a result is $P_{UP,3}$.

$$P_{UP,3} = V_{IN} \cdot Q_{rr} \cdot f_S \quad \text{(EQ. 27)}$$

Finally, the resistive part of the upper MOSFET is given in Equation 28 as $P_{UP,4}$.

$$P_{UP,4} \approx r_{DS(ON)} \cdot \left[\left(\frac{I_M}{N}\right)^2 \cdot d + \frac{I_{PP}^2}{12}\right] \quad \text{(EQ. 28)}$$

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 25, 26, 27 and 28. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

Internal Bootstrap Device

All three integrated drivers feature an internal bootstrap schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the PHASE node. This reduces voltage stress on the boot to phase pins.

The bootstrap capacitor must have a maximum voltage rating above PVCC + 4V and its capacitance value can be chosen from Equation 29:

$$C_{BOOT_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT_CAP}}$$
$$Q_{GATE} = \left(\frac{Q_{G1} \cdot PVCC}{V_{GS1}} \cdot N_{Q1}\right) \quad \text{(EQ. 29)}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive.

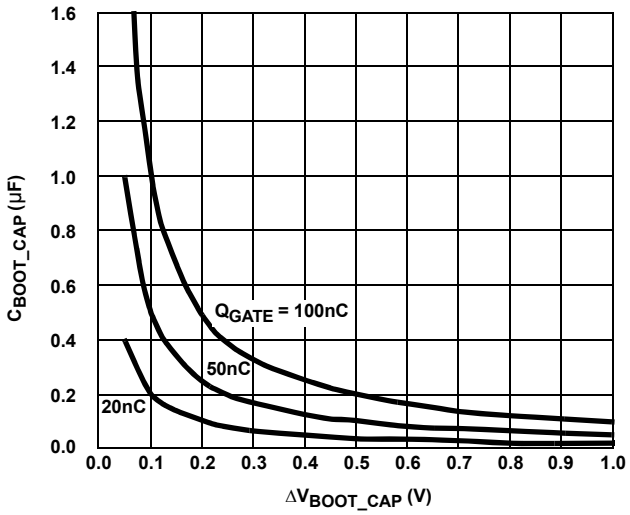


FIGURE 15. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Gate Drive Voltage Versatility

The ISL6328 provides the user flexibility in choosing the gate drive voltage for efficiency optimization. The controller ties the upper and lower drive rails together. Simply applying a voltage from 5V up to 12V on PVCC sets both gate drive rail voltages simultaneously.

Package Power Dissipation

When choosing MOSFETs it is important to consider the amount of power being dissipated in the integrated drivers located in the controller. Since there are a total of three drivers in the controller package, the total power dissipated by all three drivers must be less than the maximum allowable power dissipation for the QFN package.

Calculating the power dissipation in the drivers for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. The maximum allowable IC power dissipation for the 6x6 QFN package is approximately 3.5W at room temperature. See “Layout Considerations” on page 29 for thermal transfer improvement suggestions.

When designing the ISL6328 into an application, it is recommended that the following calculation is used to ensure safe operation at the desired frequency for the selected MOSFETs. The total gate drive power losses, P_{Qg_TOT}, due to the gate charge of MOSFETs and the integrated driver’s internal circuitry and their corresponding average driver current can be estimated with Equations 30 and 31, respectively.

$$P_{Qg_TOT} = P_{Qg_Q1} + P_{Qg_Q2} + I_Q \cdot VCC$$
$$P_{Qg_Q1} = \frac{3}{2} \cdot Q_{G1} \cdot PVCC \cdot F_{SW} \cdot N_{Q1} \cdot N_{PHASE} \quad \text{(EQ. 30)}$$
$$P_{Qg_Q2} = Q_{G2} \cdot PVCC \cdot F_{SW} \cdot N_{Q2} \cdot N_{PHASE}$$

$$I_{DR} = \left(\frac{3}{2} \cdot Q_{G1} \cdot N_{Q1} + Q_{G2} \cdot N_{Q2}\right) \cdot N_{PHASE} \cdot F_{SW} + I_Q \quad \text{(EQ. 31)}$$

In Equations 30 and 31, P_{Qg_Q1} is the total upper gate drive power loss and P_{Qg_Q2} is the total lower gate drive power loss; the gate charge (Q_{G1} and Q_{G2}) is defined at the particular gate to source drive voltage PVCC in the corresponding MOSFET data sheet; I_Q is the driver total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are the number of upper and lower MOSFETs per phase, respectively; N_{PHASE} is the number of active phases. The I_Q*VCC product is the quiescent power of the controller without capacitive load and is typically 75mW at 300kHz.

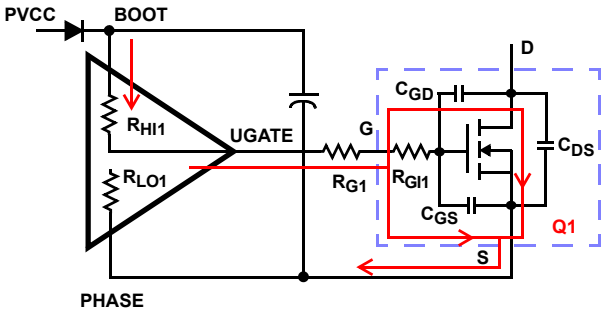


FIGURE 16. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

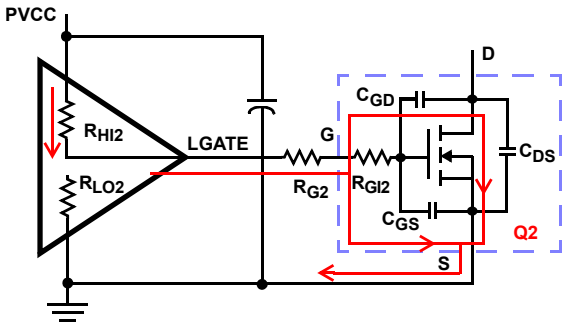


FIGURE 17. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

The total gate drive power losses are dissipated among the resistive components along the transition path and in the bootstrap diode. The portion of the total power dissipated in the controller itself is the power dissipated in the upper drive path resistance (P_{DR_UP}), the lower drive path resistance (P_{DR_UP}), and in the boot strap diode (P_{BOOT}). The rest of the power will be dissipated by the external gate resistors (R_{G1} and R_{G2}) and the internal gate resistors (R_{GI1} and R_{GI2}) of the MOSFETs. Figures 16 and 17 show the typical upper and lower gate drives turn-on transition path. The total power dissipation in the controller itself, P_{DR}, can be roughly estimated as:

$$P_{DR} = P_{DR_UP} + P_{DR_LOW} + P_{BOOT} + (I_Q \cdot VCC)$$

$$P_{BOOT} = \frac{P_{Qg_Q1}}{3}$$

$$P_{DR_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \cdot \frac{P_{Qg_Q1}}{3} \qquad \text{(EQ. 32)}$$

$$P_{DR_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \cdot \frac{P_{Qg_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

Inductor DCR Current Sensing Component Fine Tuning

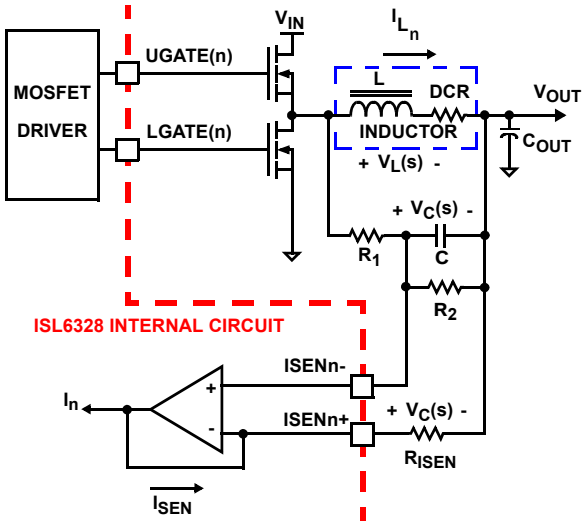


FIGURE 18. DCR SENSING CONFIGURATION

Due to errors in the inductance and/or DCR it may be necessary to adjust the value of R_1 and R_2 to match the time constants correctly. The effects of time constant mismatch can be seen in the form of droop overshoot or undershoot during the initial load transient spike, as shown in Figure 19. Follow the steps below to ensure the R-C and inductor L/DCR time constants are matched accurately.

1. If the regulator is not utilizing droop, modify the circuit by placing the frequency set resistor between FS and Ground for the duration of this procedure.
2. Capture a transient event with the oscilloscope set to about L/DCR/2 (sec/div). For example, with L = 1µH and DCR = 1mΩ, set the oscilloscope to 500µs/div.
3. Record ΔV1 and ΔV2 as shown in Figure 19.

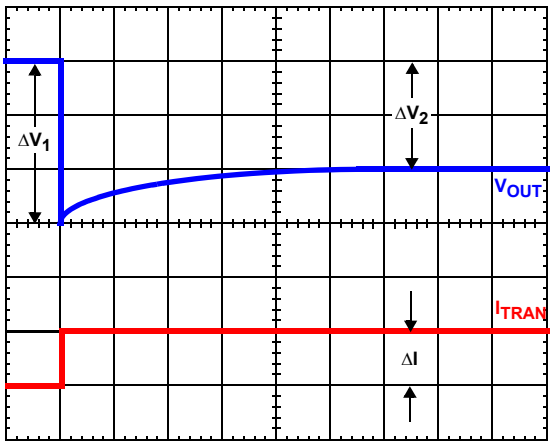


FIGURE 19. TIME CONSTANT MISMATCH BEHAVIOR

4. Select new values, $R_{1,NEW}$ and $R_{2,NEW}$, for the time constant resistors based on the original values, $R_{1,OLD}$ and $R_{2,OLD}$, using Equations 33 and 34.

$$R_{1,NEW} = R_{1,OLD} \cdot \frac{\Delta V_1}{\Delta V_2} \quad \text{(EQ. 33)}$$

$$R_{2,NEW} = R_{2,OLD} \cdot \frac{\Delta V_1}{\Delta V_2} \quad \text{(EQ. 34)}$$

5. Replace R_1 and R_2 with the new values and check to see that the error is corrected. Repeat the procedure if necessary.

Loadline Regulation Resistor

The loadline regulation resistor, labeled R_{FB} in Figure 8, sets the desired loadline required for the application. Equation 35 can be used to calculate R_{FB}.

$$R_{FB} = \frac{V_{DROOP_{MAX}}}{\left(\frac{I_{OUT_{MAX}}}{N} \cdot DCR\right)} \cdot K \quad \text{(EQ. 35)}$$

To choose the value for R_{FB} in this situation, please refer to "Compensation Without Loadline Regulation" on page 26.

Compensation With Loadline Regulation

The load-line regulated converter behaves in a similar manner to a peak current mode controller because the two poles at the output filter L-C resonant frequency split with the introduction of current information into the control loop. The final location of these poles is determined by the system function, the gain of the current signal, and the value of the compensation components, R_C and C_C.

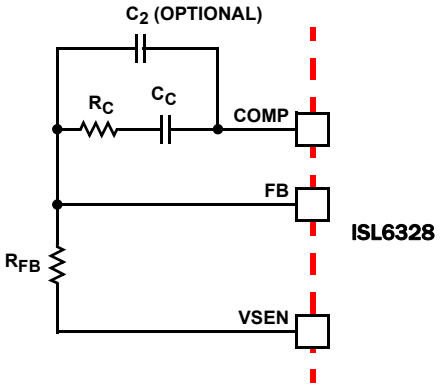


FIGURE 20. COMPENSATION CONFIGURATION FOR LOAD-LINE REGULATED ISL6328 CIRCUIT

Since the system poles and zero are affected by the values of the components that are meant to compensate them, the solution to the system equation becomes fairly complicated. Fortunately, there is a simple approximation that comes very close to an optimal solution. Treating the system as though it were a voltage-mode regulator, by compensating the L-C poles and the ESR zero of the voltage mode approximation, yields a solution that is always stable with very close to ideal transient performance.

Select a target bandwidth for the compensated system, f_0. The target bandwidth must be large enough to assure adequate transient performance, but smaller than 1/3 of the per-channel switching frequency. The values of the compensation components depend on the relationships of f_0 to the L-C pole frequency and the ESR zero frequency. For each of the following three, there is a separate set of equations for the compensation components.

In Equation 36, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent series resistance of the bulk output filter capacitance; and V_{P-P} is the peak-to-peak sawtooth signal amplitude as described in the "Electrical Specifications" on page 9.

Once selected, the compensation values in Equation 36 assure a stable converter with reasonable transient performance. In most cases, transient performance can be improved by making adjustments to R_C. Slowly increase the value of R_C while observing the transient performance on an oscilloscope until no further improvement is noted. Normally, C_C will not need adjustment. Keep the value of C_C from Equation 36 unless some performance issue is noted

The optional capacitor C_2, is sometimes needed to bypass noise away from the PWM comparator (see Figure 20). Keep a position available for C_2, and be prepared to install a high-frequency capacitor of between 22pF and 150pF in case any leading edge jitter problem is noted.

Case 1:

$$\frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} > f_0$$

$$R_C = R_{FB} \cdot \frac{2 \cdot \pi \cdot f_0 \cdot V_{pp} \cdot \sqrt{L \cdot C}}{0.66 \cdot V_{IN}}$$

$$C_C = \frac{0.66 \cdot V_{IN}}{2 \cdot \pi \cdot V_{PP} \cdot R_{FB} \cdot f_0}$$

Case 2:

$$\frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \leq f_0 < \frac{1}{2 \cdot \pi \cdot C \cdot ESR}$$

$$R_C = R_{FB} \cdot \frac{V_{PP} \cdot (2 \cdot \pi)^2 \cdot f_0^2 \cdot L \cdot C}{0.66 \cdot V_{IN}} \quad \text{(EQ. 36)}$$

$$C_C = \frac{0.66 \cdot V_{IN}}{(2 \cdot \pi)^2 \cdot f_0^2 \cdot V_{PP} \cdot R_{FB} \cdot \sqrt{L \cdot C}}$$

Case 3:

$$f_0 > \frac{1}{2 \cdot \pi \cdot C \cdot ESR}$$

$$R_C = R_{FB} \cdot \frac{2 \cdot \pi \cdot f_0 \cdot V_{pp} \cdot L}{0.66 \cdot V_{IN} \cdot ESR}$$

$$C_C = \frac{0.66 \cdot V_{IN} \cdot ESR \cdot \sqrt{C}}{2 \cdot \pi \cdot V_{PP} \cdot R_{FB} \cdot f_0 \cdot \sqrt{L}}$$

Compensation Without Loadline Regulation

The non load-line regulated converter is accurately modeled as a voltage-mode regulator with two poles at the L-C resonant frequency and a zero at the ESR frequency. A type III controller, as shown in Figure 21, provides the necessary compensation.

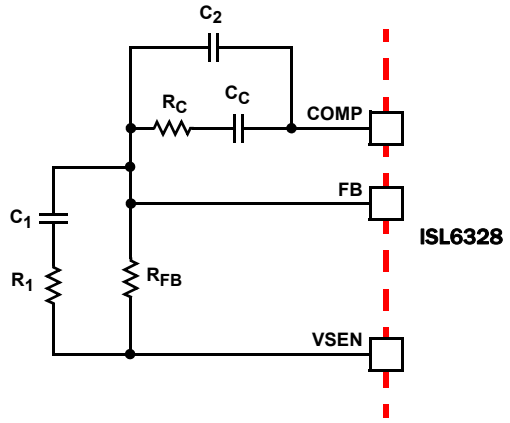


FIGURE 21. COMPENSATION CIRCUIT WITHOUT LOAD-LINE REGULATION

The first step is to choose the desired bandwidth, f_0, of the compensated system. Choose a frequency high enough to assure adequate transient performance but not higher than 1/3 of the switching frequency. The type-III compensator has an extra high-frequency pole, f_{HF}. This pole can be used for added noise rejection or to assure adequate attenuation at the error-amplifier high order pole and zero frequencies. A good general rule is to choose $f_{HF} = 10f_0$, but it can be higher if desired. Choosing f_{HF} to be lower than $10f_0$ can cause problems with too much phase shift below the system bandwidth.

$$R_1 = R_{FB} \cdot \frac{C \cdot ESR}{\sqrt{L \cdot C} - C \cdot ESR}$$

$$C_1 = \frac{\sqrt{L \cdot C} - C \cdot ESR}{R_{FB}}$$

$$C_2 = \frac{0.75 \cdot V_{IN}}{(2 \cdot \pi)^2 \cdot f_0 \cdot f_{HF} \cdot (\sqrt{L \cdot C}) \cdot R_{FB} \cdot V_{P-P}} \qquad \text{(EQ. 37)}$$

$$R_C = \frac{V_{PP} \cdot (2\pi)^2 \cdot f_0 \cdot f_{HF} \cdot L \cdot C \cdot R_{FB}}{0.75 \cdot V_{IN} \cdot (2 \cdot \pi \cdot f_{HF} \cdot \sqrt{L \cdot C} - 1)}$$

$$C_C = \frac{0.75 \cdot V_{IN} \cdot (2 \cdot \pi \cdot f_{HF} \cdot \sqrt{L \cdot C} - 1)}{(2 \cdot \pi)^2 \cdot f_0 \cdot f_{HF} \cdot (\sqrt{L \cdot C}) \cdot R_{FB} \cdot V_{P-P}}$$

In the solutions to the compensation equations, there is a single degree of freedom. For the solutions presented in Equation 38, R_{FB} is selected arbitrarily. The remaining compensation components are then selected according to Equation 38.

In Equation 38, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and V_{PP} is the peak-to-peak sawtooth signal amplitude as described in “Electrical Specifications” on page 9.

Case 1:

$$\frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} > f_0$$

$$R_C = R_{FB} \cdot \frac{2 \cdot \pi \cdot f_0 \cdot V_{pp} \cdot \sqrt{L \cdot C}}{0.66 \cdot V_{IN}}$$

$$C_C = \frac{0.66 \cdot V_{IN}}{2 \cdot \pi \cdot V_{PP} \cdot R_{FB} \cdot f_0}$$

Case 2:

$$\frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \leq f_0 < \frac{1}{2 \cdot \pi \cdot C \cdot ESR}$$

$$R_C = R_{FB} \cdot \frac{V_{PP} \cdot (2 \cdot \pi)^2 \cdot f_0^2 \cdot L \cdot C}{0.66 \cdot V_{IN}} \qquad \text{(EQ. 38)}$$

$$C_C = \frac{0.66 \cdot V_{IN}}{(2 \cdot \pi)^2 \cdot f_0^2 \cdot V_{PP} \cdot R_{FB} \cdot \sqrt{L \cdot C}}$$

Case 3:

$$f_0 > \frac{1}{2 \cdot \pi \cdot C \cdot ESR}$$

$$R_C = R_{FB} \cdot \frac{2 \cdot \pi \cdot f_0 \cdot V_{pp} \cdot L}{0.66 \cdot V_{IN} \cdot ESR}$$

$$C_C = \frac{0.66 \cdot V_{IN} \cdot ESR \cdot \sqrt{C}}{2 \cdot \pi \cdot V_{PP} \cdot R_{FB} \cdot f_0 \cdot \sqrt{L}}$$

Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter limits the system transient response. The output capacitors must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI, the load-current slew rate, di/dt, and the maximum allowable output-voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount:

$$\Delta V \approx ESL \cdot \frac{di}{dt} + ESR \cdot \Delta I \quad \text{(EQ. 39)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current (see "Interleaving" on page 12 and Equation 3), a voltage develops across the bulk capacitor ESR equal to $I_{C,PP}(ESR)$. Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{PP(MAX)}$, determines the lower limit on the inductance.

$$L \geq ESR \cdot \frac{\left(V_{IN} - N \cdot V_{OUT}\right) \cdot V_{OUT}}{f_S \cdot V_{IN} \cdot V_{PP(MAX)}} \quad \text{(EQ. 40)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 41 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 42 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, C is the total output capacitance, and N is the number of active channels.

$$L \leq \frac{2 \cdot N \cdot C \cdot V_O}{(\Delta I)^2} \cdot \left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right] \quad \text{(EQ. 41)}$$

$$L \leq \frac{1.25 \cdot N \cdot C}{(\Delta I)^2} \cdot \left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right] \cdot \left(V_{IN} - V_O\right) \quad \text{(EQ. 42)}$$

Switching Frequency

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper MOSFET loss calculation. These effects are outlined in "MOSFETs" on page 23, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple as outlined in "Output Filter Design" on page 27. Choose the lowest switching frequency that allows the regulator to meet the transient-response requirements.

Switching frequency is determined by the selection of the frequency-setting resistor, R_T. Figure 22 and Equation 43 are provided to assist in selecting the correct value for R_T.

$$R_T = 10^{[10.61 - (1.035 \cdot \log(f_S))]} \quad \text{(EQ. 43)}$$

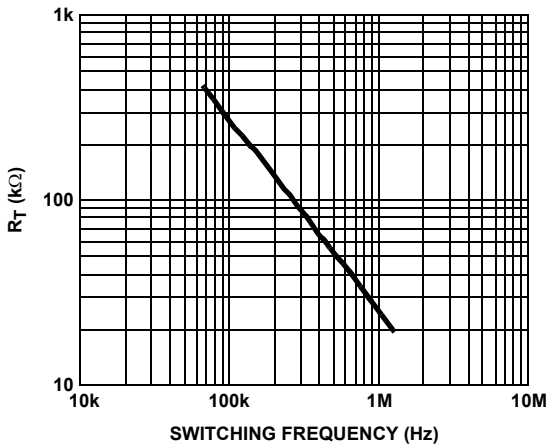


FIGURE 22. R_T vs SWITCHING FREQUENCY

Input Capacitor Selection

The input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases.

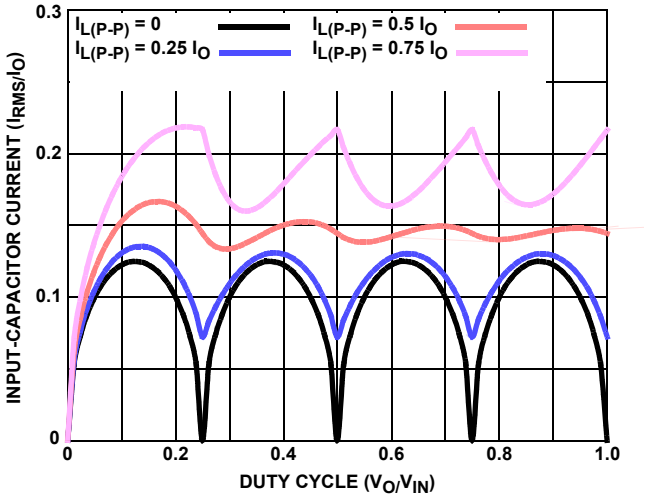


FIGURE 23. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 4-PHASE CONVERTER

For a four-phase design, use Figure 23 to determine the input-capacitor RMS current requirement set by the duty cycle, maximum sustained output current (I_O), and the ratio of the peak-to-peak inductor current ($I_{L(P-P)}$) to I_O. Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated.

The voltage rating of the capacitors should also be at least 1.25x greater than the maximum input voltage. Figures 24 and 25 provide the same input RMS current information for three-phase and 2-phase designs respectively. Use the same approach for selecting the bulk capacitor type and number.

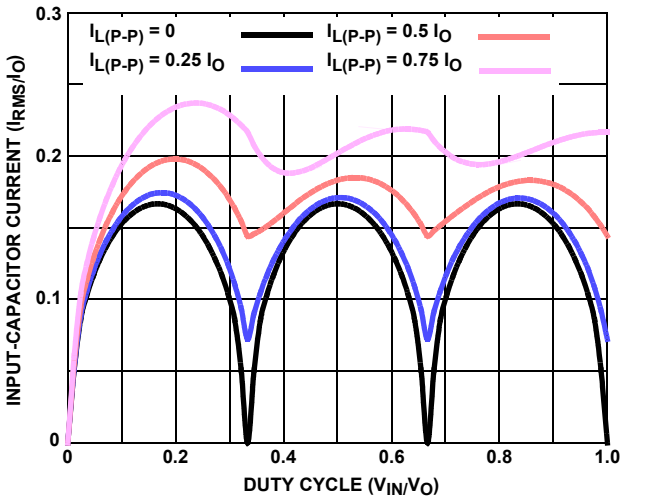


FIGURE 24. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

Low capacitance, high-frequency ceramic capacitors are needed in addition to the input bulk capacitors to suppress leading and falling edge voltage spikes. The spikes result from the high current slew rate produced by the upper MOSFET turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitics and maximize suppression.

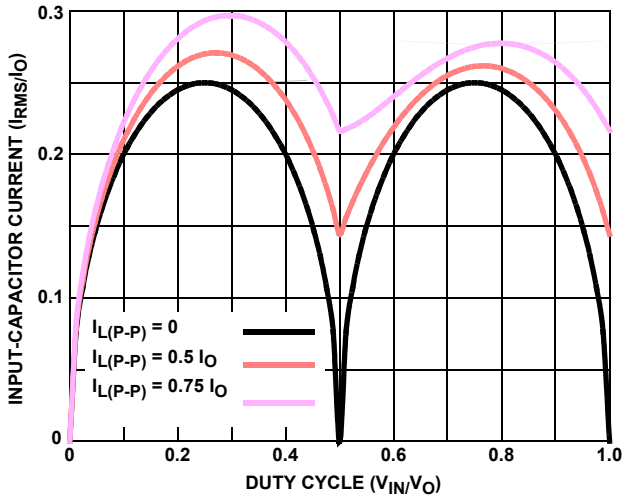


FIGURE 25. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 2-PHASE CONVERTER

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component selection, layout, and placement minimizes these voltage spikes. Consider, as an example, the turnoff transition of the upper PWM MOSFET. Prior to turnoff, the upper MOSFET was carrying channel current. During the turnoff, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC/DC converter using a ISL6328 controller. The power components are the most critical because they switch large amounts of energy. Next are small signal components that connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first, which include the MOSFETs, input and output capacitors, and the inductors. It is important to have a symmetrical layout for each power train, preferably with the controller located equidistant from each. Symmetrical layout allows heat to be dissipated equally across all power trains. Equidistant placement of the controller to the CORE and NB power trains it controls through the integrated drivers helps keep the gate drive traces equally short, resulting in equal trace impedances and similar drive capability of all sets of MOSFETs.

When placing the MOSFETs try to keep the source of the upper FETs and the drain of the lower FETs as close as thermally possible. Input high-frequency capacitors, C_{HF}, should be placed close to the drain of the upper FETs and the source of the lower FETs. Input bulk capacitors, CBULK, case size typically limits following the same rule as the high-frequency input capacitors. Place the input

bulk capacitors as close to the drain of the upper FETs as possible and minimize the distance to the source of the lower FETs.

Locate the output inductors and output capacitors between the MOSFETs and the load. The high-frequency output decoupling capacitors (ceramic) should be placed as close as practicable to the decoupling target, making use of the shortest connection paths to any internal planes, such as vias to GND next or on the capacitor solder pad.

The critical small components include the bypass capacitors (C_{FILTER}) for VCC and PVCC, and many of the components surrounding the controller including the feedback network and current sense components. Locate the VCC/PVCC bypass capacitors as close to the ISL6328 as possible. It is especially important to locate the components associated with the feedback circuit close to their respective controller pins, since they belong to a high-impedance circuit loop, sensitive to EMI pick-up.

A multi-layer printed circuit board is recommended. Figure 26 shows the connections of the critical components for the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually the one underneath the component side of the board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminal to output inductors short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring.

Routing UGATE, LGATE, and PHASE Traces

Great attention should be paid to routing the UGATE, LGATE, and PHASE traces since they drive the power train MOSFETs using short, high current pulses. It is important to size them as large and as short as possible to reduce their overall impedance and inductance. They should be sized to carry at least one ampere of current (0.02” to 0.05”). Going between layers with vias should also be avoided, but if so, use two vias for interconnection when possible.

Extra care should be given to the LGATE traces in particular since keeping their impedance and inductance low helps to significantly reduce the possibility of shoot-through. It is also important to route each channels UGATE and PHASE traces in as close proximity as possible to reduce their inductances.

Current Sense Component Placement and Trace Routing

One of the most critical aspects of the ISL6328 regulator layout is the placement of the inductor DCR current sense components and traces. The R-C current sense components must be placed as close to their respective ISEN+ and ISEN- pins on the ISL6328 as possible.

The sense traces that connect the R-C sense components to each side of the output inductors should be routed on the bottom of the board, away from the noisy switching components located on the top of the board. These traces should be routed side by side, and they should be very thin traces. It’s important to route these traces as far away from any other noisy traces or planes as possible. These traces should pick up as little noise as possible. These traces should also originate from the geometric center of the inductor pin pads and that location should be the single point of contact the trace makes with its respective net.

Thermal Management

For maximum thermal performance in high current, high switching frequency applications, connecting the thermal GND pad of the ISL6328 to the ground plane with multiple vias is recommended. This heat spreading allows the part to achieve its full thermal potential. It is also recommended that the controller be placed in a direct path of airflow if possible to help thermally manage the part.

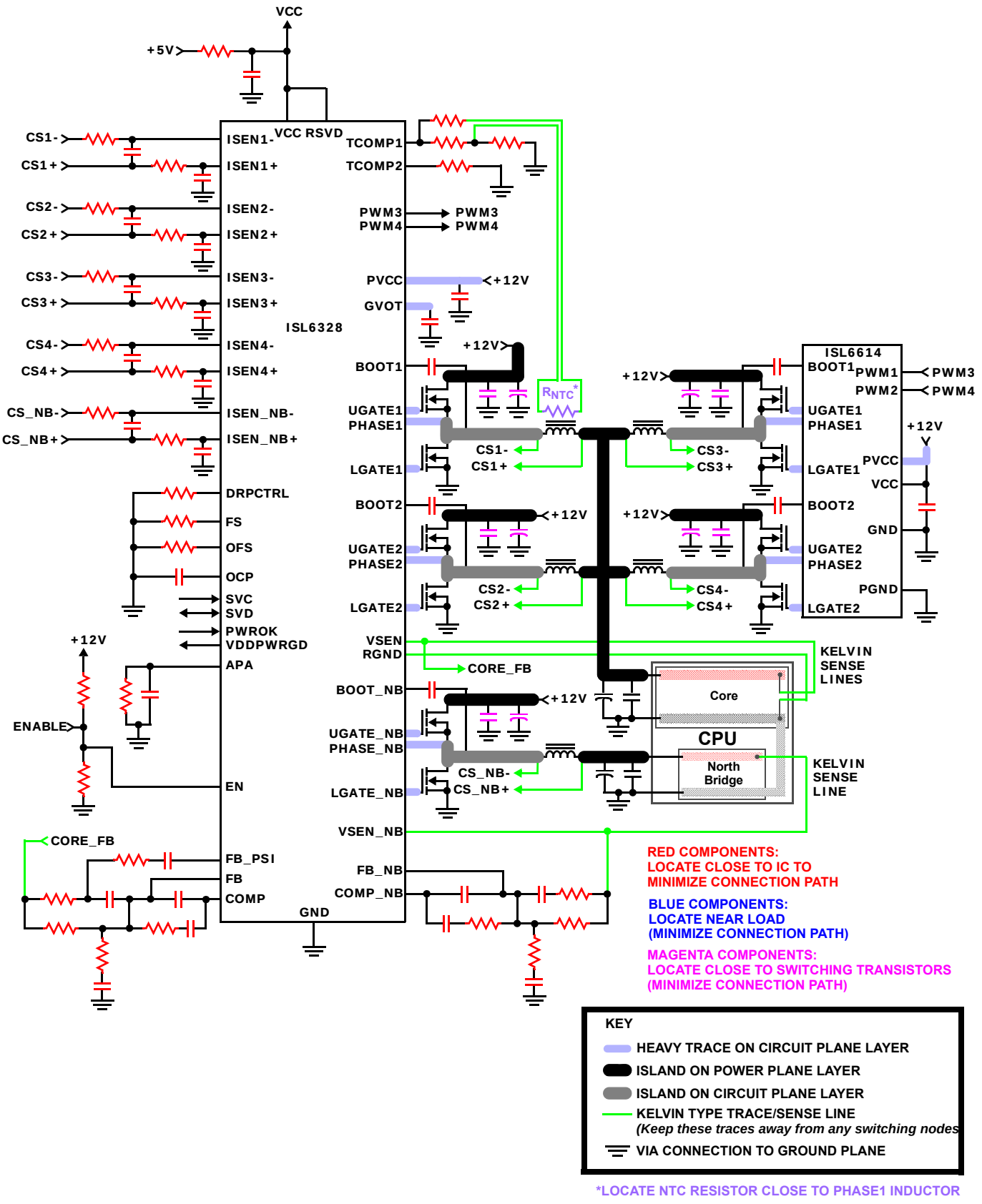


FIGURE 26. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
6/7/11	FN7621.1	Initial Release to web.

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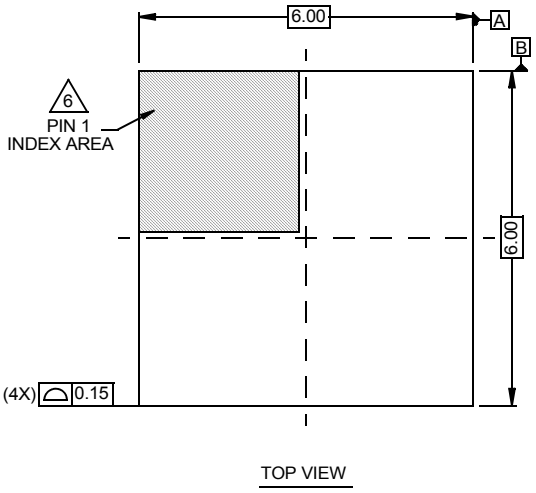
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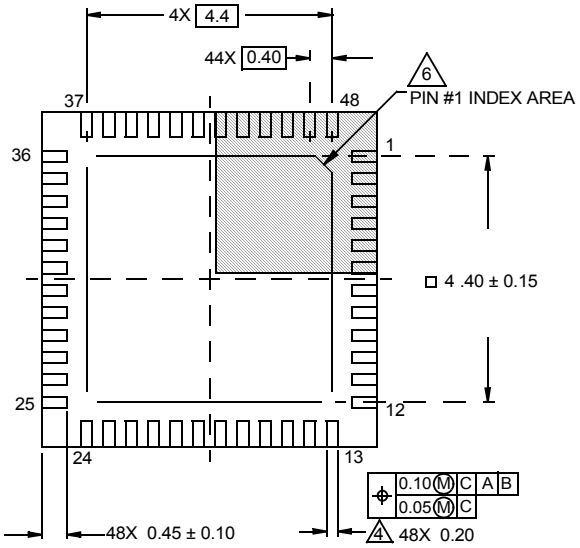
Package Outline Drawing

L48.6x6B

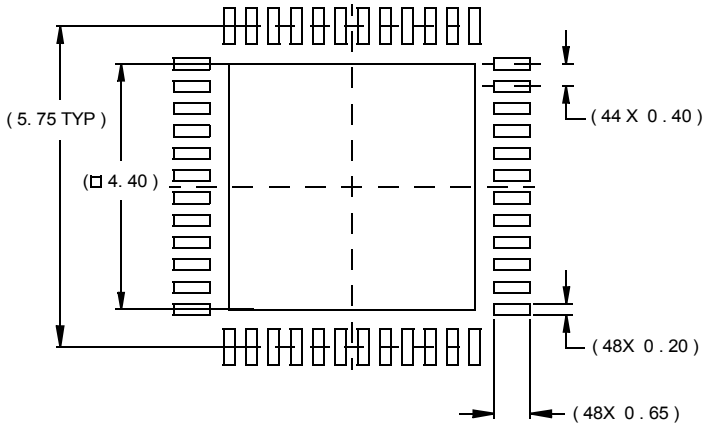
48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 9/09



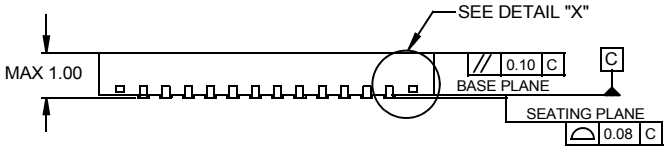
TOP VIEW



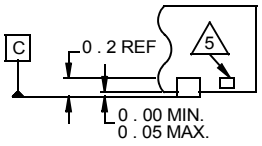
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.