MC3447

OCTAL BIDIRECTIONAL BUS TRANSCEIVER WITH TERMINATION NETWORKS

SILICON MONOLITHIC INTEGRATED CIRCUIT

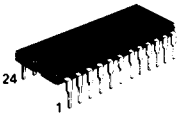
BIDIRECTIONAL INSTRUMENTATION BUS (GPIB) TRANSCEIVER

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

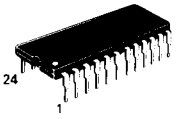
Low power consumption has been achieved by trading a minimum of speed for low current drain on non-critical channels. A fast channel is provided for critical ATN and EOI paths.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by a Send/Receive input with the disabled output of the pair forced to a high impedance state. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

- Low Power —
  Average Power Supply Current = 30 mA Listening
  75 mA Talking
- Eight Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis — 600 mV (Typ)
- Fast Propagation Times — 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output with Terminations
- Power Up/Power Down Protection
  (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power is Removed From Device
- Terminations Provided: Termination Removed When Device is Unpowered

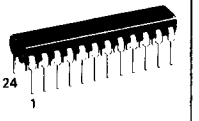


L SUFFIX
CERAMIC PACKAGE
CASE 623

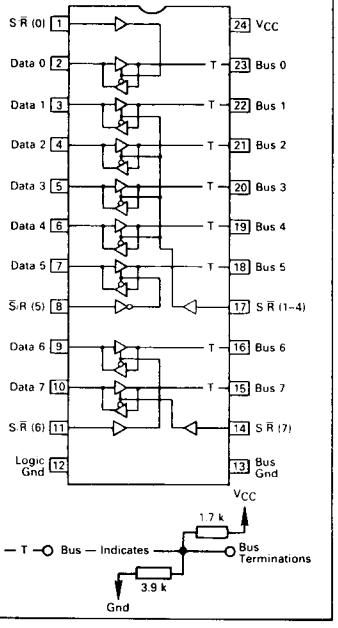


P SUFFIX
PLASTIC PACKAGE
CASE 649

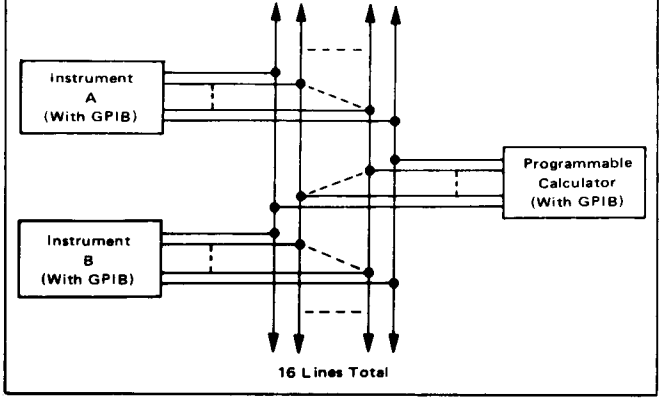
P3 SUFFIX
PLASTIC PACKAGE
CASE 724



PIN CONNECTIONS



TYPICAL MEASUREMENT SYSTEM APPLICATION



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS
(Unless otherwise noted 4.50 V ≤ V_{CC} ≤ 5.50 V and 0 ≤ T_A ≤ 70°C; typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic — Note 1		Symbol	Min	Typ	Max	Unit
Bus Voltage (Bus Pin Open)($V_{I(S/\overline{R})}$ = 0.8 V) ($I_{(Bus)}$ = −12 mA)		$V_{(Bus)}$ $V_{IC(Bus)}$	2.5 –	– –	3.7 −1.5	V
Bus Current (5.0 V ≤ $V_{(Bus)}$ ≤ 5.5 V) ($V_{(Bus)}$ = 0.5 V) (V_{CC} = 0 V, 0 V ≤ $V_{(Bus)}$ ≤ 2.75 V)		$I_{(Bus)}$	0.7 −1.3 –	– – –	2.5 −3.2 +0.04	mA
Receiver Input Hysteresis ($V_{I(S/\overline{R})}$ = 0.8 V)		–	400	600	–	mV
Receiver Input Threshold ($V_{I(S/\overline{R})}$ = 0.8 V)	Low to High High to Low	$V_{ILH(R)}$ $V_{IHL(R)}$	– 0.8	1.6 1.0	2.0 –	V
Receiver Output Voltage — High Logic State ($V_{I(S/\overline{R})}$ = 0.8 V, $I_{OH(R)}$ = −200 μA, $V_{(Bus)}$ = 2.0 V)		$V_{OH(R)}$	2.4	–	–	V
Receiver Output Voltage — Low Logic State ($V_{I(S/\overline{R})}$ = 0.8 V, $I_{OL(R)}$ = 4.0 mA, ($V_{(Bus)}$ = 0.8 V		$V_{OL(R)}$	–	–	0.5	V
Receiver Output Short Circuit Current ($V_{I(S/\overline{R})}$ = 0.8 V, $V_{(Bus)}$ = 2.0 V)		$I_{OS(R)}$	−4.0	–	−20	mA
Driver Input Voltage — High Logic State ($V_{I(S/\overline{R})}$ = 2.0 V)		$V_{IH(D)}$	2.0	–	–	V
Driver Input Voltage — Low Logic State ($V_{I(S/\overline{R})}$ = 2.0 V)		$V_{IL(D)}$	–	–	0.8	V
Driver Input Current — Data Pins ($V_{I(S/\overline{R})}$ = 2.0 V) (0.5 ≤ $V_{I(D)}$ ≤ 2.7 V) ($V_{I(D)}$ = 5.5 V)		$I_{I(D)}$ $I_{IB(D)}$	−100 –	– –	40 200	μA
Input Current — Send/Receive (0.5 ≤ $V_{I(S/R)}$ ≤ 2.7 V) ($V_{I(S/\overline{R})}$ = 5.5 V)		$I_{I(S/\overline{R})}$ $I_{IB(S/\overline{R})}$	−250 –	– –	20 100	μA
Driver Input Clamp Voltage ($V_{I(S/\overline{R})}$ = 2.0 V, $I_{IC(D)}$ = −18 mA)		$V_{IC(D)}$	–	–	−1.5	V
Driver Output Voltage — High Logic State ($V_{IS/\overline{R})}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V)		$V_{OH(D)}$	2.5	–	–	V
Driver Output Voltage — Low Logic State (Note 2) **($V_{I(S/\overline{R})}$ = 2.0 V, $V_{IL(D)}$ = 0.8 V, $I_{OL(D)}$ = 48 mA)**		$V_{OL(D)}$	–	–	0.5	V
Power Supply Current (Listening Mode — All Receivers On) (Talking Mode — All Drivers On)		I_{CCL} I_{CCH}	– –	30 75	45 95	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Propagation Delay of Driver (Output Low to High) (Output High to Low)	$t_{PLH(D)}$ $t_{PHL(D)}$	– –	7.0 16	15 30	ns
Propagation Delay of Receiver (Channels 0 to 5, 7) (Output Low to High) (Output High to Low)	$t_{PLH(R)}$ $t_{PHL(R)}$	– –	28 15	50 30	ns
Propagation Delay of Receiver (Channel 6, Note 3) (Output Low to High) (Output High to Low)	$t_{PLH(R)}$ $t_{PHL(R)}$	– –	17 12	30 22	ns

NOTES: 1. Specified test conditions for $V_{I(S/\overline{R})}$ are 0.8 V (Low) and 2.0 V (High). Where $V_{I(S/\overline{R})}$ is specified as a test condition, $V_{I(\overline{S}/R)}$ uses the opposite logic levels.
2. The IEEE 488-1979 Bus Standard changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.
3. In order to meet the IEEE 488-1978 Standard for total system delay on the ATN and EOI channels, a fast receiver has been provided on Channel 6 (Pins 9 and 16).

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SWITCHING CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Send/Receiver to Data					ns
Logic High to Third State	$t_{PHZ(R)}$	–	15	30	
Third State to Logic High	$t_{PZH(R)}$	–	15	30	
Logic Low to Third State	$t_{PLZ(R)}$	–	15	25	
Third State to Logic Low	$t_{PZL(R)}$	–	10	25	
Propagation Delay Time — Send/Receiver to Bus					ns
Logic Low to Third State	$t_{PLZ(D)}$	–	13	25	
Third State to Logic Low	$t_{PZL(D)}$	–	30	50	

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

FIGURE 1 — BUS INPUT TO DATA OUTPUT (RECEIVER)

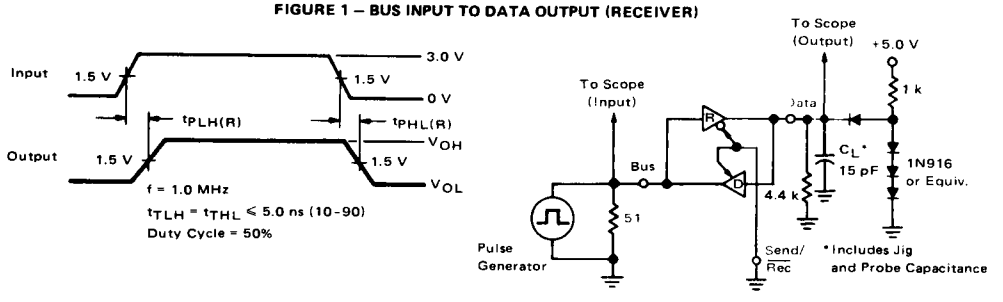


FIGURE 2 — DATA INPUT TO BUS OUTPUT (DRIVER)

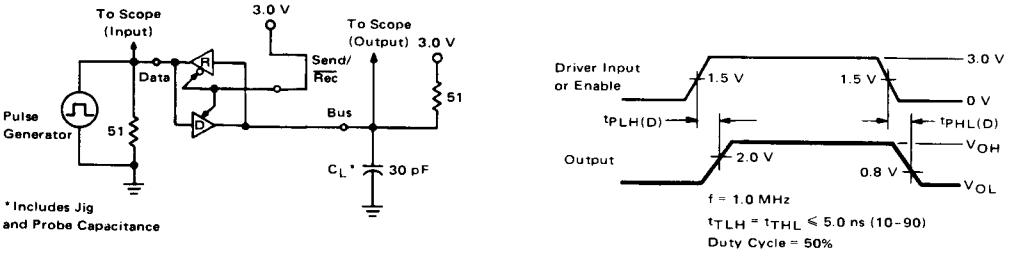


FIGURE 3 — SEND/$\overline{\text{RECEIVE}}$ INPUT TO BUS OUTPUT (DRIVER)

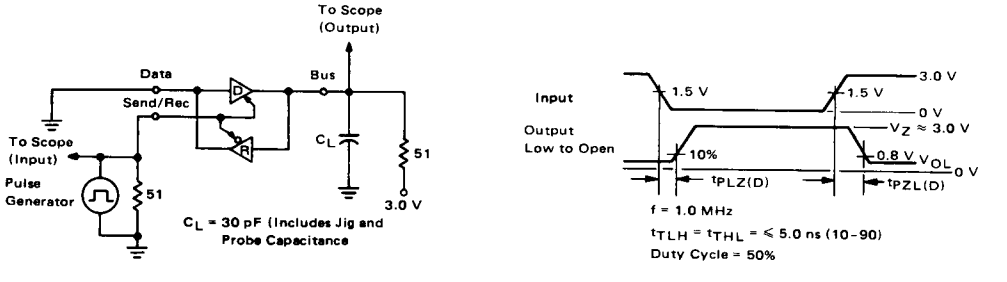


FIGURE 4 – SEND/$\overline{\text{RECEIVE}}$ INPUT TO DATA OUTPUT (RECEIVER)

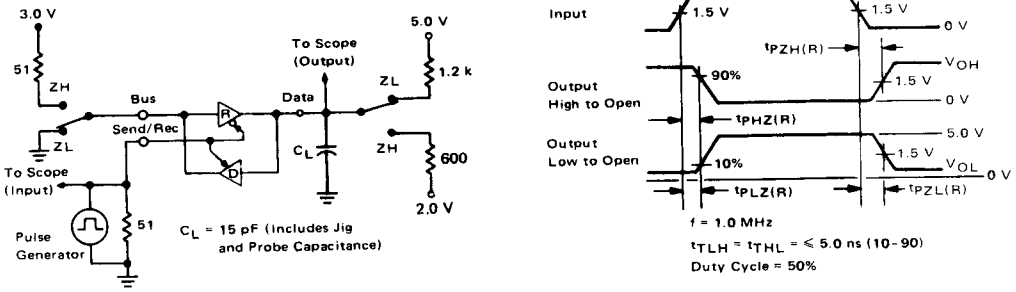


FIGURE 5 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

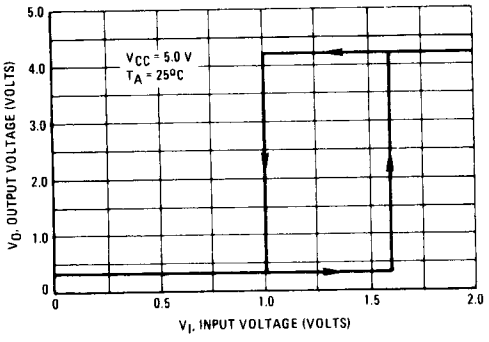


FIGURE 6 – TYPICAL BUS LOAD LINE

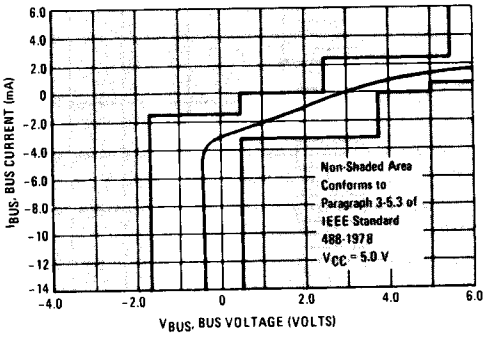


FIGURE 7 – SUGGESTED PRINTED CIRCUIT BOARD LAYOUT USING MC3447s AND MC68488

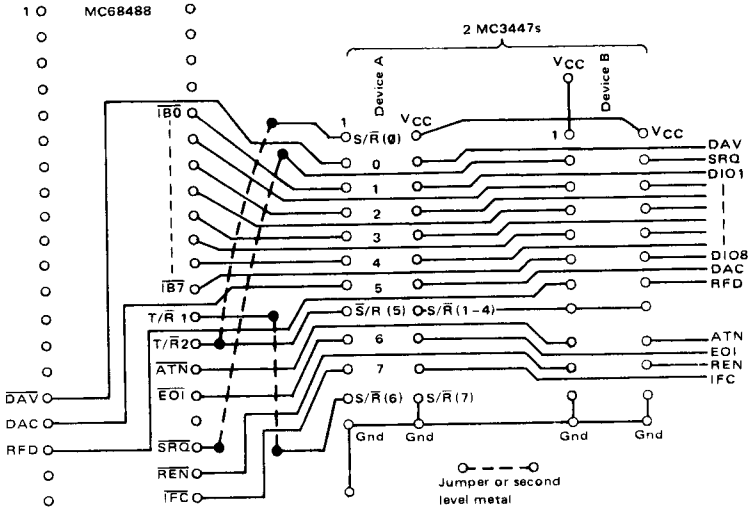
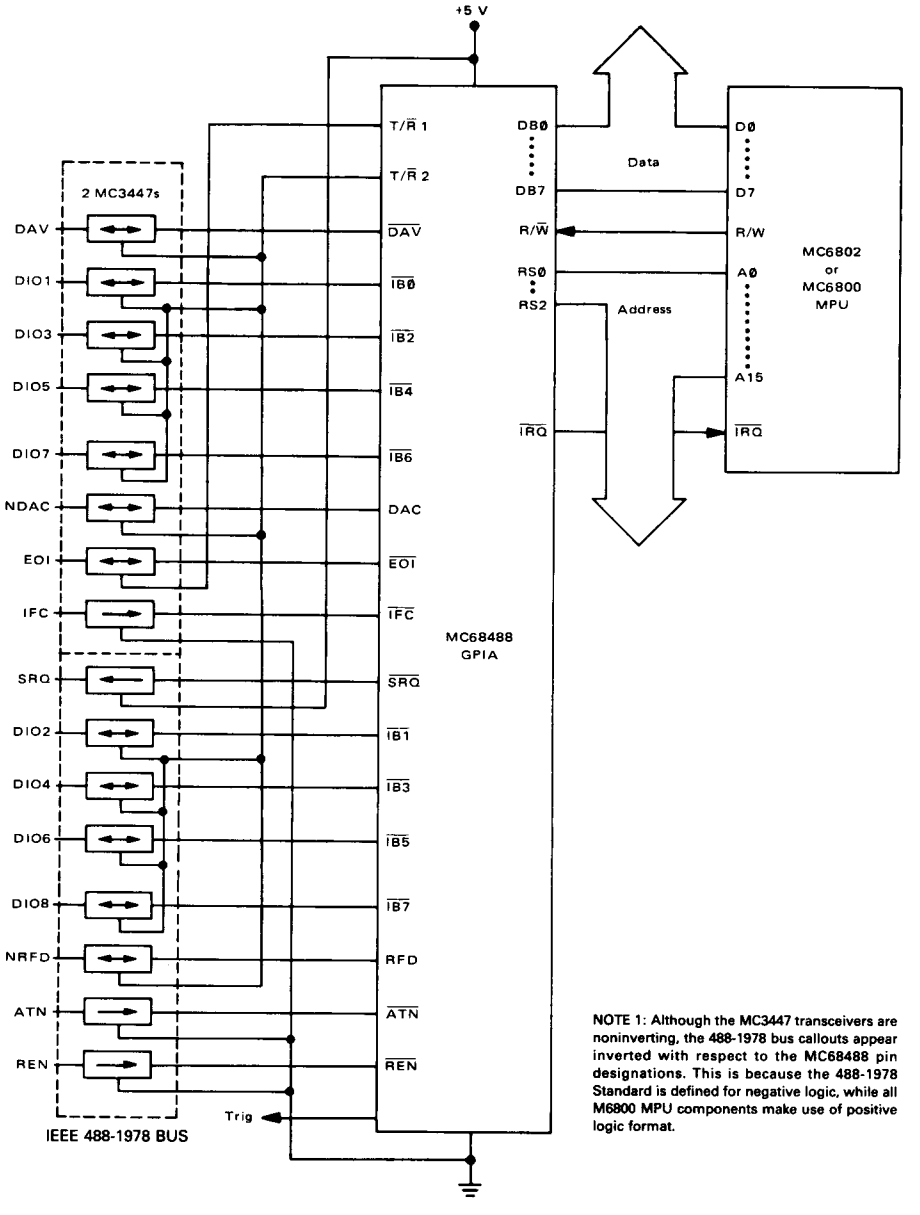


FIGURE 8 – SIMPLE SYSTEM CONFIGURATION



NOTE 1: Although the MC3447 transceivers are noninverting, the 488-1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

FIGURE 9 – SUGGESTED PIN DESIGNATIONS FOR USE WITH MC68488

MC68488 Connections		MC3447 Pin Designations					MC68488 Connections	
A	B						A	B
T/$\overline{R}$ 2	V_{CC}	S/$\overline{R}$ (0)	1		24	V_{CC}	V_{CC}	V_{CC}
$\overline{DAV}$	$\overline{SRQ}$	Data 0 0	2		23	Bus 0	DAV	SRQ
$\overline{IB0}$	$\overline{IB1}$	Data 1	3		22	Bus 1	DIO 1	DIO 2
$\overline{IB2}$	$\overline{IB3}$	Data 2	4		21	Bus 2	DIO 3	DIO 4
$\overline{IB4}$	$\overline{IB5}$	Data 3	5		20	Bus 3	DIO 5	DIO 6
$\overline{IB6}$	$\overline{IB7}$	Data 4	6	Octal GPIB	19	Bus 4	DIO 7	DIO 8
DAC	RFD	Data 5	7	Transceiver	18	Bus 5	NDAC	NRFD
T/$\overline{R}$ 2	T/$\overline{R}$ 2	$\overline{S}$/R (5)	8		17	S/$\overline{R}$ (1–4)	T/$\overline{R}$ 2	T/$\overline{R}$ 2
$\overline{EOI}$	$\overline{ATN}$	Data 6	9		16	Bus 6	EOI	ATN
$\overline{IFC}$	$\overline{REN}$	Data 7	10		15	Bus 7	IFC	REN
T/$\overline{R}$ 1	Gnd	S/$\overline{R}$ (6)	11		14	S/$\overline{R}$ (7)	Gnd	Gnd
Gnd	Gnd	Logic Gnd	12		13	Bus Gnd	Gnd	Gnd

