

## General Description

The DM562AP integrated modem is a two-chipset design that provides a complete solution for state-of-the-art, voice-band Plain Old Telephone Switching (POTS) communication. The modem provides for Data (up to 56,000bps), Fax (up to 33,600bps), fast connection, Voice and Full Duplex Speaker-phone functions to comply with various international standards.

The design of the DM562AP is optimized for desktop personal computer applications, embedded microprocessor applications, Set-Top-Box (STB), Point-Of-Sale (POS), and Multi-Function Peripheral (MFP) FAX application. It provides a low cost, highly reliable, maximum integration, with the minimum amount of supports required. The DM562AP modem can operate over a dial-up network (PSTN) or 2 wire leased lines.

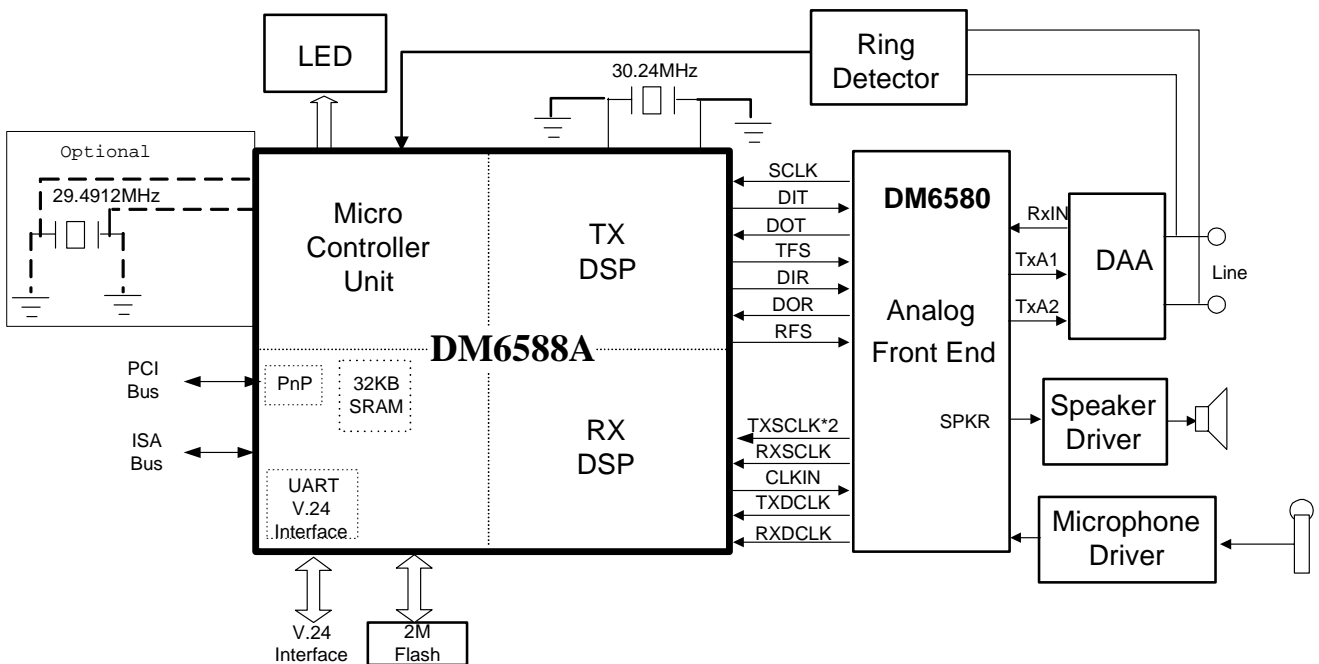
The modem integrates auto dial and answer capabilities, synchronous/asynchronous data transmissions, serial and parallel interfaces, various tone detection schemes and data test modes.

The DM562AP modem reference design is pre-approved for FCC part 68 and provides minimum design cycle time, with minimum cost to insure the maximum amount of success.

The simplified modem system, shown in figure below, illustrates the basic interconnection between the MCU, DSP, AFE and other basic components of a modem. The individual elements of the DM562AP are:

- DM6580 Analog Front End (AFE). 48-pin LQFP package.
- DM6588A ITU-T V.90 integrated Processors with 32K bytes SRAM built in 128-pin QFP package

## Block Diagram





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**Features**

- Data
  - ITU-T V.90 (56000 to 28000 bps)
  - ITU-T V.34 (33600 to 2400 bps)
  - ITU-T V.32bis (14400, 12000, 9600, 7200, 4800bps)
  - ITU-T V.32 (9600, 4800bps)
  - ITU-T V.22bis (2400, 1200bps)
  - ITU-T V.22 (1200bps)
  - ITU-T V.23 (1200/75bps)
  - ITU-T V.21 (300bps)
  - Bell 212A (1200bps)
  - Bell 103 (300bps)
  - V.22 fast connect
- Fax
  - ITU-T V.34 (33600 to 2400bps)
  - ITU-T V.17 (14400, 12000, 9600, 7200bps)
  - ITU-T V.29 (9600, 7200bps)
  - ITU-T V.27ter (4800, 2400bps)
  - ITU-T V.21 Channel 2 (300bps)
  - Group III, Class 1,2
  - Automatic rate adaptation in V.34 half-duplex mode
  - Support ECM mode
  - Support Rx Polling function
- Data Error Correction
  - MNP Class 4
  - ITU-T V.42 LAPM
- Data Compression
  - MNP Class 5
  - ITU-T V.42bis
- Voice compression
  - 4 bit ADPCM (ITU-T)
  - 2, 3 and 4 bit ADPCM (Davicom proprietary)
  - 8 Bit PCM
- Synchronous mode
  - Legacy synchronous DCE mode
- DTE Interface
  - Asynchronous DTE speed up to 115200bps
  - Serial V.24 (EIA-232-D)
- Integrated UART 16550
- Enhanced "AT" command set and S registers
  - TIA/EIA 602 ITU V.25ter AT command set
  - TIA/EIA 578 Fax Class 1,2 command set
  - TIA/EIA IS-101 Voice command set
- Parallel (ISA/PCI) and Serial (UART) interfaces
  - 6, 7 and 8 bit character support
  - Even, odd, mark and none parity detection and generation
  - 1 and 2 stop bit support
  - Auto DTE data speed detection
- Support Caller identification (Caller ID)
- Speakerphone
- Selectable world wide call progress tone detection
- Enhanced 8032 compatible micro-controller
- Power down mode
- Access up to 256K bytes external program memory
- Access up to 64K bytes external data memory
- NVRAM to store two user configurable, selectable profiles with three programmable telephone numbers
- 32K bytes SRAM built in

**Parallel bus for embedded microprocessor**

Compatible to ISA bus

**PCI internal modem only**

- PCI Plug and Play (PnP) support
- Compliant with PCI specification 2.1
- Compliant with PCI bus Power Management Interface Specification revision 1.0

**Applications:**

- MFP/FAX machine, EFAQ Box
- Set-Top-Box (STB), reply channel
- Electronic Point-Of-Sale (EPOS)
- Industrial/Medical monitoring devices
- Voice Broadcasting devices, Utility meters
- Security Systems
- FWT,CDMA/GSM/GPRS Wireless FAX

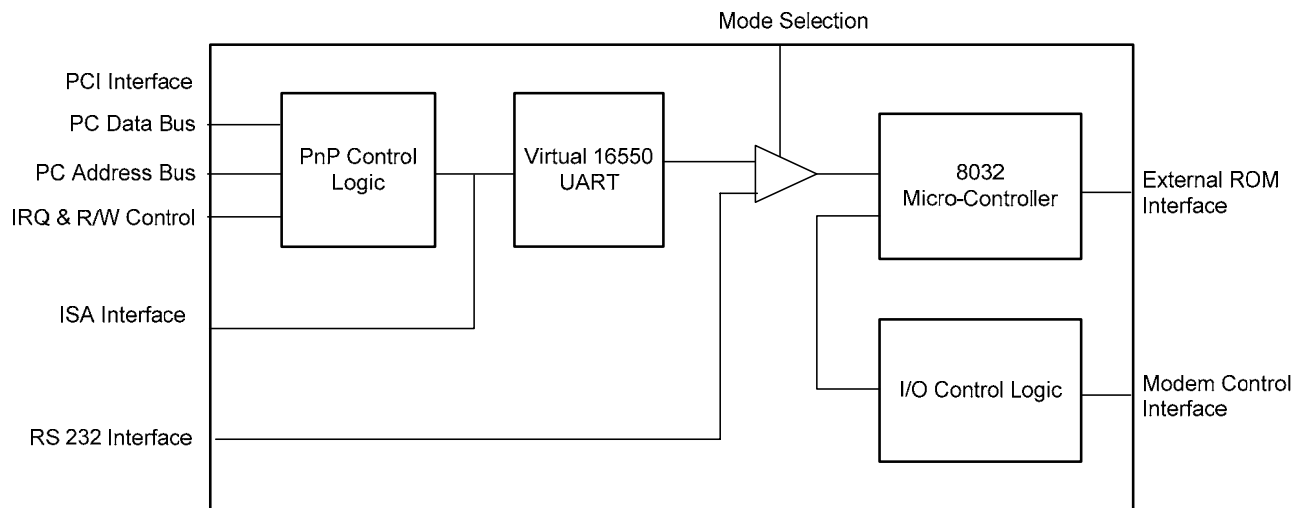
## Chip 1: Integrated Processor Unit with PnP

### DM6588A Description

The DM6588A Modem Control Unit is designed for use in high speed internal and external modem applications. The DM6588A incorporates a 80C32 micro-controller, a virtual 16550A UART with FIFO mode, and Plug & Play control logic.

The DM6588A MCU performs general modem control functions, and is also designed to provide Plug and Play capability for PCI bus systems.

### DM6588A Block Diagram



### DM6588A Features

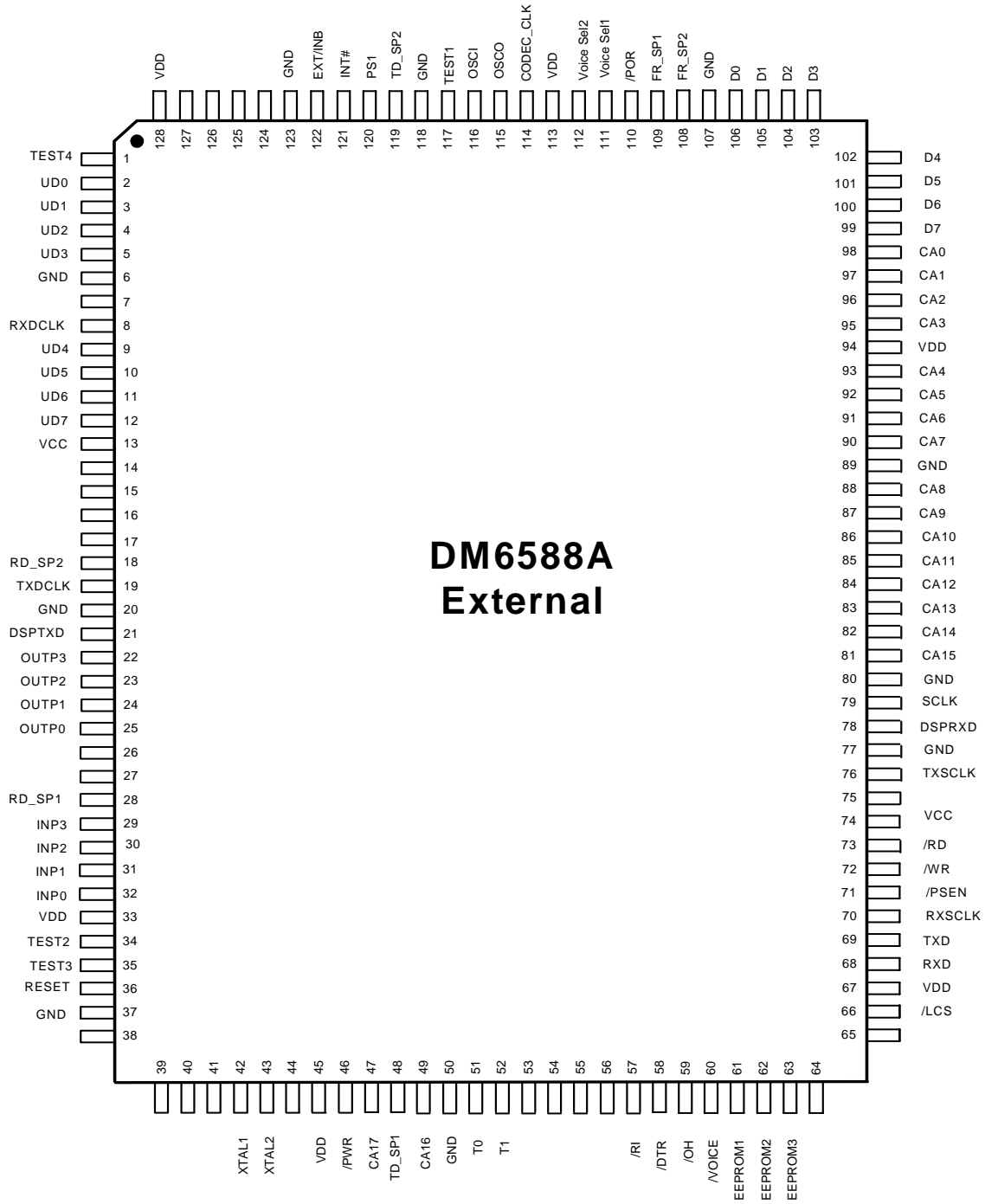
- Control interface support
- Supports parallel and serial interfaces
- Includes a 80C32 micro-controller
- 256K bytes maximum external program memory
- 32K bytes data memory built in
- Provides automatic Plug and Play or software configuration capabilities
- Virtual 16550A UART compatible parallel interface
- Fully programmable serial interface:
  - 6, 7 or 8-bit characters
  - Even, odd, mark and none parity bit generation and detection
  - 1 and 2 stop bit generation
  - Baud rate generation
  - Includes I/O control logic for modem control interface



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Modem Device Single Chip with Memory Built in

## DM6588A External Pin Configuration

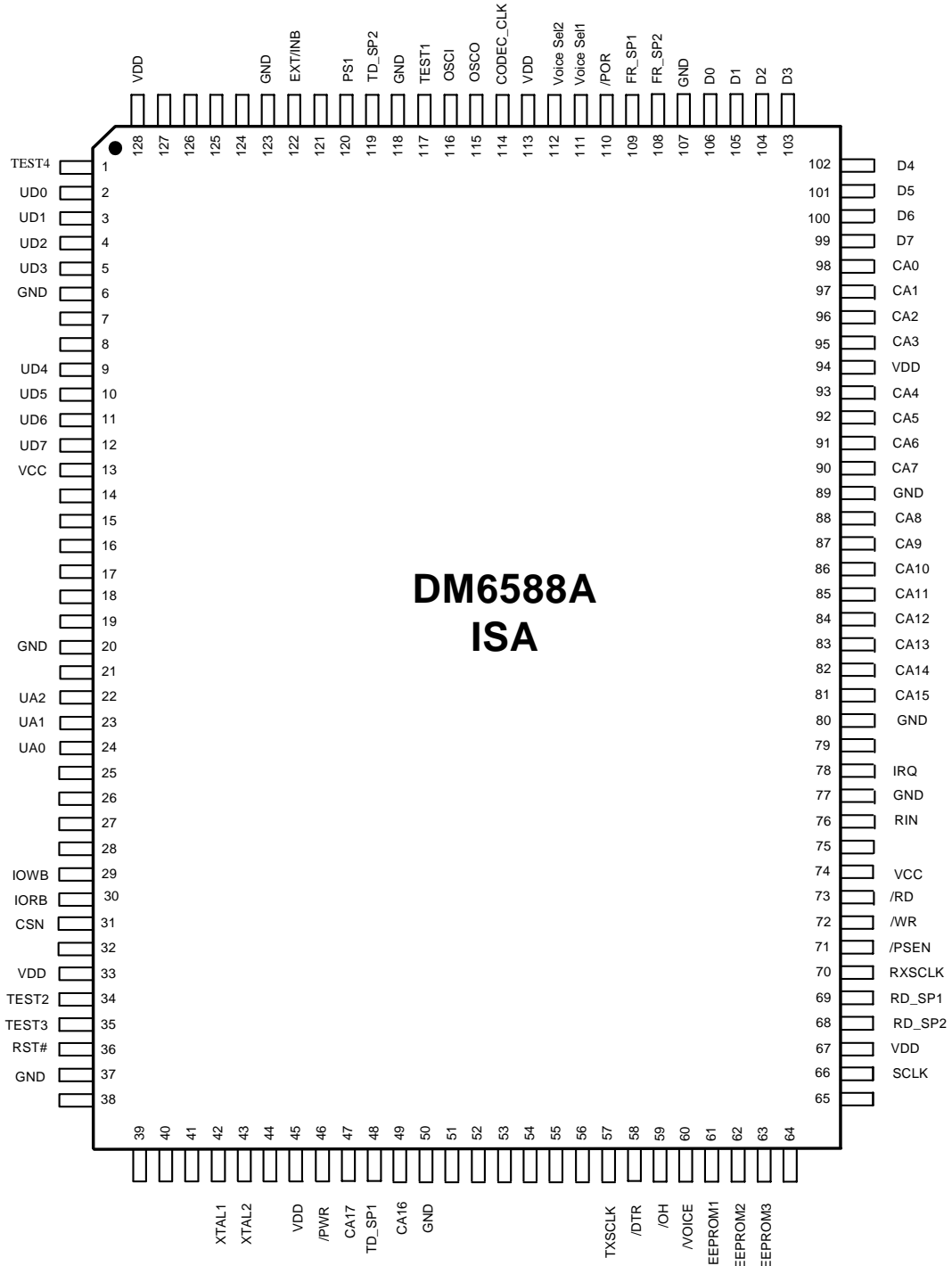




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## DM6588A ISA Pin Configuration

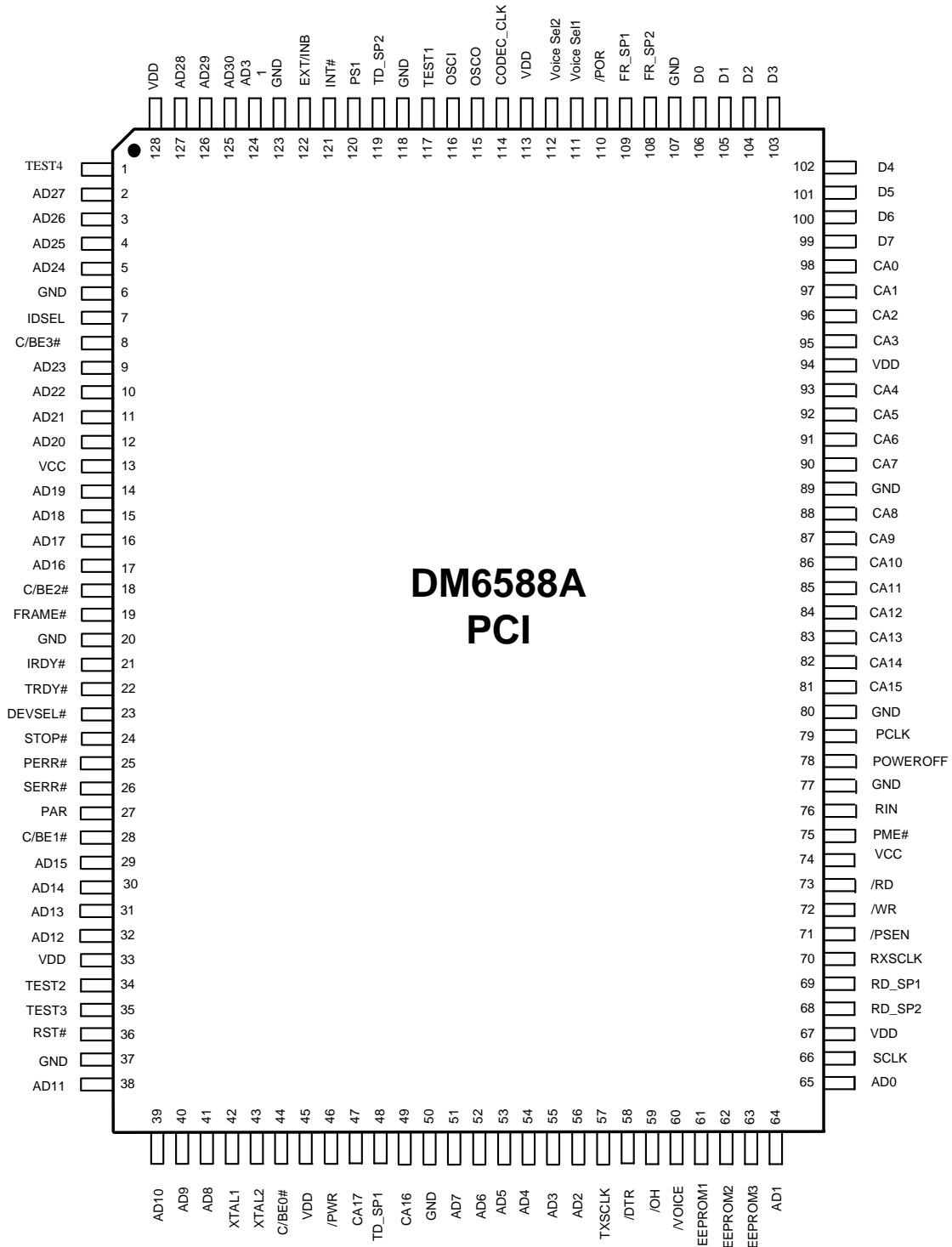




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## DM6588A PCI Pin Configuration





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## DM6588A Pin Description

| Pin No. External                           | Pin No. Internal PCI                   | Pin No. Internal ISA                       | Pin Name                            | I/O | Description  |
|--|--|--|-------------------------------------|-----|--|
| 1  | 1                                      | 1  | TEST4                               | I   | <b>Test pin 4, normal ground.</b><br>External: N/C (low).<br>PCI: N/C (low).<br>ISA: connect to 3.3V.  |
| 2,3,4,5,<br>9,10,11,<br>12                 |  |  | UD0 - UD7                           | O   | <b>Modem Control Output</b> , for external modem:<br>Memory address mapping of the controller is E800H.  |
| 8  |  |  | RxDCLK                              | I   | <b>Receive Data Rate Clock:(External)</b><br>This pin is used as reference clock of DSPRXD pin.  |
| 18   | 68                                     | 68   | RD_SP2                              | I   | <b>Data Input Pin Of The Serial Port 2:</b><br>The serial data is sampled at the falling edge of the SCLK. The MSB is coming immediately after the falling of FR_SP2 signal. |
| 19   |  |  | TXDCLK                              | I   | <b>Transmit Data Rate Clock:(External)</b><br>This pin is used as reference clock of DSPTXD pin.   |
| 21   |  |  | DSPTxD                              | I   | <b>Modem Transmit Data (External)</b><br>Shifted into Tx /Rx DSP from EIA port through this pin at the rising edge of TXDCLK.  |
| 28   | 69                                     | 69   | RD_SP1                              | I   | <b>Data Input Pin Of The Serial Port 1:</b><br>The serial data is sampled at the falling edge of the SCLK. The MSB is coming immediately after the falling of FR_SP1 signal. |
| 6,20,37<br>50,77,80,<br>89,107,<br>118,123 | 6,20,37<br>50,80,89<br>107,118,<br>123 | 6,20,37<br>50,77,80,<br>89,107,<br>118,123 | GND                                 | P   | <b>Ground</b>  |
| 22,<br>23,<br>24,<br>25                    |  |  | OUTP3,<br>OUTP2,<br>OUTP1,<br>OUTP0 | O   | <b>Modem Control Output</b><br>For external modem, these pins are bit7~4 of the modem control output. Memory address mapping of the controller is C800H.                     |
| 29,<br>30,<br>31,<br>32                    |  |  | INP3,<br>INP2,<br>INP1,<br>INP0     | I   | <b>Modem Control Input:(External)</b><br>These pins are bit3~0 of the modem control input. Memory address mapping of the controller is C800H.                                |
| 33,45<br>67,94,<br>113,128                 | 33,45,<br>67,94,<br>113,128            | 33,45,<br>67,94,<br>113,128                | VDD                                 | P   | <b>+3.3V Power Supply</b>  |
| 13,74                                      | 13,74                                  | 13,74                                      | VCC                                 | P   | <b>+2.5V Power Supply</b>  |
| 34   | 34                                     | 34   | TEST2                               | I   | <b>Test pin 2,normal ground</b>  |
| 35   | 35                                     | 35   | TEST3                               | I   | <b>Test pin 3,normal ground</b>  |
| 36   |  |  | RESET                               | I   | <b>Reset:</b><br>An active high signal used to reset the DM6588A.  |
| 42   | 42                                     | 42   | XTAL1                               | I   | <b>Crystal Oscillator Input</b>  |



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| 43                                  | 43                                  | 43                                  | XTAL2   | O   | <b>Crystal Oscillator Output</b>  |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
|-------------------------------------|-------------------------------------|-------------------------------------|---|-----|---|--|------|------|--------|---|---|--------|---|---|--------|---|---|--------|---|---|
| 46                                  | 46                                  | 46                                  | /PWR  | O   | <b>Controller Program Write Enable:</b><br>This pin is used to enable FLASH ROM programming.  |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 48                                  | 48                                  | 48                                  | TD_SP1  | O   | <b>Data Output Pin Of Serial Port 1</b><br>The serial data is clocked out through this pin according to the rising edge of SCLK. The MSB is sent immediately after the falling edge of the FR_SP1 signal.   |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 49                                  | 49                                  | 49                                  | CA16  | O   | <b>Bank Switch Control:</b><br>These signals are used to switch external program memory between banks. <table style="margin-left: 40px;"> <thead> <tr> <th></th> <th>CA16</th> <th>CA17</th> </tr> </thead> <tbody> <tr> <td>Bank 0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Bank 1</td> <td>1</td> <td>0</td> </tr> <tr> <td>Bank 2</td> <td>0</td> <td>1</td> </tr> <tr> <td>Bank 3</td> <td>1</td> <td>1</td> </tr> </tbody> </table> |  | CA16 | CA17 | Bank 0 | 0 | 0 | Bank 1 | 1 | 0 | Bank 2 | 0 | 1 | Bank 3 | 1 | 1 |
|                                     | CA16                                | CA17                                |   |     |   |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| Bank 0                              | 0                                   | 0                                   |   |     |   |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| Bank 1                              | 1                                   | 0                                   |   |     |   |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| Bank 2                              | 0                                   | 1                                   |   |     |   |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| Bank 3                              | 1                                   | 1                                   |   |     |   |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 47                                  | 47                                  | 47                                  | CA17  |     |   |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 51                                  |                                     |                                     | T0  | I   | <b>Controller Counter 0 Input</b>   |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 52                                  |                                     |                                     | T1  | I   | <b>Controller Counter 1 Input</b>   |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 57                                  | 76                                  | 76                                  | /RI   | I   | <b>Ring Signal Input</b>  |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 76                                  | 57                                  | 57                                  | TxSCLK*2  | I   | <b>TxDSP Interrupt 1 Input</b>  |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 58                                  | 58                                  | 58                                  | /DTR  | I   | <b>DTR Input Pin (P1.1)</b>   |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 59                                  | 59                                  | 59                                  | /OH   | O   | <b>Hook Relay Control (P1.2)</b>  |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 60                                  | 60                                  | 60                                  | /VOICE  | O   | <b>Voice Relay Control. Modem Control Output</b><br>(memory map is bit 3 of DAA at memory address D000H)  |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 61-63                               | 61-63                               | 61-63                               | EEPROM 1-3  | I/O | <b>EEPROM Control Pins (P1.4-P1.6)</b>  |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 66                                  |                                     |                                     | /LCS  | I   | <b>Loop Current Detection. Modem Input Control:</b><br>This pin is mapped to bit0 of address D000H.   |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 79                                  | 66                                  | 66                                  | SCLK  | I   | <b>Reference Clock For Serial Port 1 And Serial Port 2</b>  |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 68                                  |                                     |                                     | RXD   | I   | <b>Controller Serial Port Data Input</b>  |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 69                                  |                                     |                                     | TXD   | O   | <b>Controller Serial Port Data Output</b>   |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 70                                  | 70                                  | 70                                  | RxSCLK  | I   | <b>Rx DSP Interrupt 3 Input</b>   |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 71                                  | 71                                  | 71                                  | /PSEN   | O   | <b>Controller Program Store Enable:</b><br>This output goes low during a fetch from external program memory.  |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 72                                  | 72                                  | 72                                  | /WR   | O   | <b>Controller External Data Memory Write Control</b>  |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 73                                  | 73                                  | 73                                  | /RD   | O   | <b>Controller External Data Memory Read Control</b>   |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 78                                  |                                     |                                     | DSPRxD  | O   | <b>Modem Received Data :(External)</b><br>Shifted out to the EIA port through this pin according to the rising edge of RXDCLK.  |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 117                                 | 117                                 | 117                                 | TEST1   |     | <b>Test pin 1, normal ground</b>  |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |
| 81,82,<br>83,84,<br>85,86,<br>87,88 | 81,82,<br>83,84,<br>85,86,<br>87,88 | 81,82,<br>83,84,<br>85,86,<br>87,88 | CA15,CA14,<br>CA13,CA12,<br>CA11,CA10,<br>CA9,CA8 | O   | <b>Controller Address Bus</b>   |  |      |      |        |   |   |        |   |   |        |   |   |        |   |   |



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|   |  |   |                                     |     |   |
|---|--|---|-------------------------------------|-----|---|
| 90,91,<br>92,93,<br>95,96,<br>97,98   | 90,91,<br>92,93,<br>95,96,<br>97,98        | 90,91,<br>92,93,<br>95,96,<br>97,98   | CA7 - CA0                           | O   | <b>Controller Address Bus</b>   |
| 99,100,<br>101,102,<br>103,104,<br>105,106  | 99,100,<br>101,102,<br>103,104,<br>105,106 | 99,100,<br>101,102,<br>103,104,<br>105,106  | D7,D6,<br>D5,D4,<br>D3,D2,<br>D1,D0 | I/O | <b>Controller Data Bus</b>  |
| 108   | 108  | 108   | FR_SP2                              | I/O | <b>Frame Signal Of Serial Port 2</b>  |
| 109   | 109  | 109   | FR_SP1                              | I/O | <b>Frame Signal Of Serial Port 1</b>  |
| 110   | 110  | 110   | /POR                                | O   | <b>DSP Reset Output</b>   |
| 111<br>112  | 111<br>112                                 | 111<br>112  | VOICE Se1 1<br>VOICE Se1 2          | O   | <b>Modem Control Output</b><br>Memory map is bit 1-2 of DAA at memory address D000H   |
| 114   | 114  | 114   | CODEC_CLK                           | O   | <b>20.16MHz Clock Output For DM6580 Chip</b>  |
| 115   | 115  | 115   | OSCO                                | O   | <b>Optional Codec X'tal clock output</b>  |
| 116   | 116  | 116   | OSCI                                | I   | <b>Optional Codec X'tal clock input</b>   |
| 117   | 117  | 117   | TEST1                               | I   | <b>Test pin 1,normal ground</b>   |
| 119   | 119  | 119   | TD_SP2                              | O   | <b>Data Output Pin Of Serial Port 2</b><br>The serial data is clocked out through this pin according to the rising edge of SCLK. The MSB is sent immediately after the falling edge of the FR_SP2 signal. |
| 120   | 120  | 120   | PS1                                 | O   | <b>Modem Control Port Select Output:</b><br>Memory address mapping of the controller is D800H.  |
| 122   | 122  | 122   | EXT/INTB                            | I   | <b>Select Pin:</b> Used to select internal or external operation.<br>0: internal modem, PCI or ISA.<br>1: external modem  |
| 7,14,15,<br>16,17,26,<br>27,38,39,<br>40,41,44,<br>53,54,55,<br>56,64,65,<br>75,121,<br>124,125,<br>126,127 |  | 7,8,<br>14,15,16,<br>17,21,25,<br>26,27,28,<br>32,38,39,<br>40,41,44,<br>51,52,53,<br>55,56,<br>64,65,75,<br>79,121,<br>124,125,<br>126,127 | NC                                  | N   | <b>NC</b>   |



## DM6588A Pin Description-ISA Interface only

| Pin No.      | Pin Name            | I/O | Description  |
|--------------|---------------------|-----|--|
| 2-5,<br>9-12 | UD0-UD3,<br>UD4-UD7 | I/O | <b>Data Bus Signal:</b><br>These signals are connected to the data bus of the PC (or Host) I/O. They are used to transfer data between the PC and the DM6588A. |
| 22-24        | UA0-UA2             | I   | <b>System Address:</b><br>These signals are connected to the bus of PC (or Host) I/O. They are used to select the DM6588A offset UART I/O address.             |
| 29           | /IOWB               | I   | <b>I/O Write:</b><br>An active low input signal used to write data to the DM6588A.   |
| 30           | /IORB               | I   | <b>I/O Read:</b><br>An active low input signal used to read data from the DM6588A.   |
| 31           | /CSN                | I   | <b>Address Enable:</b><br>This is an active low signal to enable the system address for DM6588A.   |
| 36           | /RST                | I   | <b>Reset:</b><br>An active low signal used to reset the DM6588A.   |
| 78           | IRQ                 | O   | <b>Interrupt Request:</b><br>The active pin will go high when an interrupt request is generated from the DM6588A.  |



## DM6588A Pin Description-PCI Interface only

| Pin No.   | Pin Name                             | I/O | Description  |
|---|--------------------------------------|-----|--|
| 78  | POWEROFF                             | O   | <b>Power Off when high</b>   |
| 121   | INT#                                 | O   | <b>PCI Interrupt Request</b><br>This signal will be asserted low when an interrupt condition as defined in CR5 is set and the corresponding mask bit in CR7 is not set.  |
| 79  | PCLK                                 | I   | <b>PCI System Clock</b><br>This signal is the PCI bus clock that provides timing for all bus phases. The frequency is 33MHz.   |
| 75  | PME#                                 | O   | <b>Power Management Event</b><br>The signal indicates that a power management event.   |
| 124-127,2-5<br>9-12,14-17<br>29-32,38-41<br>51-56,64,65 | AD31-AD0                             | I/O | <b>PCI Address &amp; Data Bus</b><br>These are the multiplexed address and data signals. DM6588A will decode each address on the bus and respond if it is the target being addressed.  |
| 7   | IDSEL                                | I   | <b>Initialization Device Select</b><br>For the accesses to the configuration address space, the device select Decoding is done externally and is signaled via this pin. This signal is asserted high during configuration read and write access.   |
| 8<br>18<br>28<br>44                                     | C/BE3#<br>C/BE2#<br>C/BE1#<br>C/BE0# | I   | <b>PCI Bus Command/Byte Enable</b><br>During the address phase, these signals define the bus command or the type of the bus transaction that will take place.<br>During the data phase, these pins indicate which byte lanes contain valid data. C/BE0# applies to bit7~0 and C/BE3# applies to bit 31~24. |
| 19  | FRAME#                               | I   | <b>PCI Cycle Frame</b><br>This signal is driven low by the master to indicate the beginning and duration of a bus transaction. It is de-asserted when the transaction is in its final phase.   |
| 21  | IRDY#                                | I   | <b>PCI Initiator Ready</b><br>This signal is driven low when the master is ready to complete the current data phase of the transaction. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted.  |
| 22  | TRDY#                                | I/O | <b>PCI Target Ready</b><br>This signal is driven low when the target is ready to complete the current data phase of the transaction. During a read, it indicates that the valid data is asserted. During write, it indicates that the target prepares to accept data.                                      |
| 23  | DEVSEL#                              | I/O | <b>PCI Device Select</b><br>DM6588A asserts the signal low when it recognizes its target address after FRAME# is asserted.   |
| 24  | STOP#                                | I/O | <b>PCI Stop</b><br>This signal is asserted low by the target device to request the master device to stop the current transaction.  |
| 25  | PERR#                                | I/O | <b>PCI Parity Error</b><br>DM6588A will assert this signal low to indicate a parity error on any incoming data.  |
| 26  | SERR#                                | O   | <b>PCI System Error</b><br>This signal is asserted low when an address parity is detected with PCICS bit31 enabled. The system error asserts two clock cycles after the address if an address parity error is detected.  |



# DM562AP

V.90 Integrated Data/ Fax/Voice/Speakerphone  
Modem Device Single Chip with Memory Built in

|    |         |     |   |
|----|---------|-----|---|
| 27 | PAR     | I/O | <b>PCI Parity</b><br>This signal indicates even parity across AD0~AD31 and C/BE0#~C/BE3# including the PAR pin. It is stable and valid one clock after the address phase. |
| 36 | RST#    | I   | <b>Reset:</b><br>An active low signal used to reset the DM6588A.  |
| 76 | RIN     | I   | <b>Ring Signal Input for Auxiliary Power</b>  |
| 77 | GND_AUX | P   | <b>Auxiliary Ground</b>   |

## DM6588A Functional Description

### 1. Operating Mode Selection

The DM6588A can be used in internal or external modem applications. When operating as an internal modem, the EXT/INTB input (pin 122) must be attached to ground, and vice versa (VDD) when operating as an external modem.

External mode is operated with host by UART. Internal mode can support parallel (ISA) and PCI interface to host. The TEST4 input (Pin 1) is for ISA or PCI selection.

### 2. Micro-controller Program Memory

The DM6588A supports two bank switch control pins to switch external program memory among four banks. The DM6588A can access a total of 256K of external program memory.

Address mapping:

bank0: 00000H - 0FFFFH  
bank1: 10000H - 1FFFFH  
bank2: 20000H - 2FFFFH  
bank3: 30000H - 3FFFFH

For bank switching, three instructions must be included in software.

Switch to bank1:

```
CLR   P1.3
SETB  P1.7
JMP   BANK 1 ADDRESS
```

Switch to bank2:

```
CLR   P1.7
SETB  P1.3
JMP   BANK 2 ADDRESS
```

Switch to bank3:

```
CLR   P1.7
CLR   P1.3
JMP   BANK 3 ADDRESS
```

Return to bank 0:

```
SETB  P1.7
SETB  P1.3
JMP   BANK 0 ADDRESS
```

\* For detailed information about the micro-controller, refer to the *Programmer's Guide to 8032*.

### 3. Micro-controller Power Down Mode

An instruction that sets the register PD (PCON.1) will cause the 80C32 to enter power down mode. There are three ways to wake up the 80C32

- (1) Positive pulse signal occurring at the reset pin of the 80C32
- (2) Negative pulse occurring at /RI (P1.0) of the 80C32
- (3) Programming the PnP Wake Up Controller Register.

### 4. Enhanced Internal Direct Memory

There are two 128 byte banks of internal direct memory in the 80C32. The system uses the lower 128 bytes under normal conditions. Switching to the upper bank is achieved by loading register 8FH.1 (SFR of the 80C32) with 1. Switching to the lower bank can be achieved by loading the same register with 0.

### 5. Re-flash Program Memory

By setting 8FH.2 the system can switch program and data memory. If the system uses FLASH memory as program memory this function is used to re-flash program code by downloading the program to data memory then switching them.

Example:

```
SETB  8FH.2
LJMP  0000H
```

### 6. Micro-controller I/O Description

**MODEM expansion port: Address C800H (external only)**

| Bit7   | Bit6   | bit5   | bit4   | bit3 | bit2 | bit1 | bit0 |
|--------|--------|--------|--------|------|------|------|------|
| OUT P3 | OUT P2 | OUT P1 | OUT P0 | INP3 | INP2 | INP1 | INP0 |

Bit0 to Bit3: read only

Bit4 to Bit7: write only

**Modem Output Port 1 Register: Address D000H**

Write only

| Bit7 | bit6 | bit5 | bit4 | Bit3   | bit2        | bit1        | bit0 |
|------|------|------|------|--------|-------------|-------------|------|
|      |      |      |      | /Voice | Voice -sel2 | Voice -Sel1 | /POR |



These 4 bits control the DM6588A output ports.

**Modem Output Port 2 Register: Address D800H**

Write only

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2      | bit1       | bit0 |
|------|------|------|------|------|-----------|------------|------|
|      |      |      |      |      | /MUT<br>E | /PUL<br>SE | /CID |

These 3 bits control the DM6588A output ports.

**Memory Mapping of Micro-controller 80C32 :**

| Address | Description                                  | External | Internal |
|---------|--|----------|----------|
| C800H   | GPIO OUTP3-OUTP0(Bit7~4);INP3~INP0(Bit3~0)   | Y        | N        |
| D000H   | DAA Port                                     | Y        | Y        |
| D400H   | UART Clock Register                          | N        | Y        |
| D800H   | PS1 Port (Modem hybrid circuit control port) | Y        | Y        |
| DC0XH   | HDLC registers                               | Y        | Y        |
| E000H   | Modem UART Status Register                   | N        | Y        |
| E400H   | /RUCS Port(RX DSP Dual Port Registers)       | Y        | Y        |
| E800H   | Modem LED Output Port UD7~UD0                | Y        | N        |
| EC00H   | UART Baud Generator Divisor Latch Register   | N        | Y        |
| F000H   | /TUCS Port (TX DSP Dual Port Register)       | Y        | Y        |
| F80XH   | PCI Vender & Device ID Port Register         | N        | Y        |



## 7. HDLC Description

### HDLC RxDataBits Register: Address DC00H

Write only

Once the RxDataBit set to 1, the data in the RxBuffer will be transferred to Rx FIFO. The transfer bit number is the same as the programming value of RxDataBits Register.

### HDLC RxBuffer: Address DC01H

Write only

Receive data will be written to the RxBuffer and will be input to the RxHDLC circuit. The RxBuffer is 16 bytes wide.

### HDLC RxFiFo: Address DC01H

Read only

After the data has been passed from the RxBuffer to the RxHDLC circuit, the RxHDLC circuit will remove the 7eH patterns and transfer the results to the Rx FIFO. There Rx FIFO is 21 bytes wide.

### HDLC TxDataBits Register: Address DC02H

Write only

Data written to TxDataBits will be presented to the Tx FIFO. The data in Tx FIFO will be transferred to TXHDLC circuit. The transfer bit number is the same as the value of TxDataBits register. If the Tx FIFO is empty, a 7e pattern will be loaded to the Tx FIFO. If Tx FIFO is not empty and the data frame has the pattern of five consecutive "1", then the TXHDLC circuit will insert "0" automatically.

### HDLC TxFiFo Register: Address DC03H

Write only

The original HDLC frame data will be loaded to the Tx FIFO, presented to the input of the TxHDLC circuit. The Tx FIFO is 21 bytes wide.

### HDLC TxBuffer: Address DC03H

Read only

According to TxDataBits, the TxHDLC circuit will transfer the same number data bits to the TxBuffer. The TxBuffer is 16 bytes wide.

### HDLC CNTL/STATUS Register: Address DC04H

Bit0:TxReady0

0: indicates the data in the Tx FIFO has decreased to zero and the HDLC circuit has transferred the 1<sup>st</sup> 7eH pattern.

1: indicates that the Tx FIFO data is greater than or equal to the threshold value.

Bit1:Rxdata

0: all the data in the RxBuffer has been read.

1: Programed by software to indicate that all data in the RxDataBits register has been written to the RxBuffer.

Bit2:Tx FIFO Threshold

0: Tx FIFO threshold No. = 11

1: Tx FIFO threshold No. = 16

Bit3:TxFiFo Status

0: data No. in Tx FIFO  $\geq$  threshold

1: data No. in Tx FIFO  $\leq$  threshold

Bit4:Txdata

0: A write action to TxDataBits register will clear this bit.

1: Bit No. in TxBuffer = TxDataBits register.

Bit5: Rx FIFO empty

0: data bytes No. in Rx FIFO  $<$  0

1: data bytes No. in Rx FIFO = 0

Bit6: Reset

0: Normal state

1: reset HDLC circuit

### Zero Deletion In \_ buffer register: Address DC08H

write only

Controller write the original data to this temp buffer.

### Zero Deletion Out \_ buffer register: Address DC08H

read only

Controller read the result data from this buffer

### Zero Deletion Status/Rst register: Address DC09H

Bit0: data ready flag (read only)

1: data has been load to out \_ buffer. (clear automatically by a read from out \_ buffer)

0: data has not been load to out \_ buffer.



Bit1: frame end flag (read only)  
1:Indicate end of HDLC frame (clear by a reset action)

Bit2: fram ready flag (read only)  
1: CRC check ok.  
0: CRC check fail.

Bit3: In \_ buffer empty flag  
1: In \_ buffer empty (clear automatically by a write to In \_buffer)  
0: In \_ buffer not empty

Bit7: reset bit (write only)  
1: software reset

**CRCL register: Address DC0AH (read only)**

**CRCH register: Address DC0BH (read only)**

## 8. Micro-controller Control Register for Internal Mode

### UART Clock (internal mode only)

The internal clock of the virtual UART logic is fixed at 1.8432MHz. The clock is derived from an external 30MHz crystal. The UART 1.8432MHz clock will be obtained by division. When the operating frequency of the DM6588A controller changes, the divider should be changed accordingly. This divider is specified by the Configuration Register which can be written by the DM6588A controller. The address mapping of the register is D400H: (DM6588A controller memory mapping)

Bit 0: Always 0.

Bit 6-1: define the clock divider range from 2 to 64 (even number).

Bit 7: Not used.

### UART Clock Register: ( internal mode only )

Address D400H Reset State: 06H

Write Only

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------|------|------|------|------|------|------|------|
| X    | dat6 | dat5 | dat4 | dat3 | dat2 | dat1 | 0    |

### UART Baud Generator Divisor Latch Register: Address EC00H ( internal mode only )

Read only

| bit7 | bit6 | bit5 | bit4 | bit3 | Bit2 | bit1 | bit0 |
|------|------|------|------|------|------|------|------|
| dat7 | dat6 | dat5 | dat4 | dat3 | Dat2 | dat1 | dat0 |

By reading this register, the micro-controller can monitor the value of the low byte divisor latch of the virtual UART baud generator (see DLL in next section) and determine the baud rate clock itself.

### Modem Status Control Register (MSCR): Address E000H ( internal mode only )

Write only

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------|------|------|------|------|------|------|------|
| 0    | 0    | 0    | 0    | /CTS | /DSR | /DCD | /RI  |

This register contains information about the line status of the modem. The available signals are Ring Detect (/RI), Carrier Detect (/DCD), Data Set Ready (/DSR) and Clear To Send (/CTS).

### 9. Host Control Register for Virtual 16550A UART (internal mode only)

Receiver Buffer (Read), Transmitter Holding Register (Write): Address: 0 (DLAB=0)

Reset State 00h

| bit7 | bit6 | bit5 | bit4 | bit3 | Bit2 | bit1 | Bit0 |
|------|------|------|------|------|------|------|------|
| dat7 | dat6 | dat5 | dat4 | dat3 | Dat2 | dat1 | Dat0 |

When this register address is read, it contains the parallel received data. Data to be transmitted is written to this register.

### Interrupt Enable Register (IER): Address 1

Reset State 00h, Write Only

| bit7 | Bit 6 | bit 5 | bit4 | bit3                     | bit2                    | bit1                            | bit0                |
|------|-------|-------|------|--------------------------|-------------------------|---------------------------------|---------------------|
| 0    | 0     | 0     | 0    | Enable Modem Status Intr | Enable Line Status Intr | Enable TX Holding Register Intr | Enable RX Data Intr |

This 8-bit register enables the four types of interrupts as described below. Each interrupt source can activate the INT output signal if enabled by this register. Resetting bits 0 through 3 will disable all UART interrupts.

Bit 0: This bit enables the Received Data Available and timeout interrupts in the FIFO mode when set to logic 1.



Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bit 4-7: Not used

### Interrupt Identification Register (IIR): Address 2

Reset State 01h, Read only

| Bit7        | Bit6 | bit5 | bit4 | bit3      | bit2      | bit1      | bit0            |
|-------------|------|------|------|-----------|-----------|-----------|-----------------|
| FIFO Enable | 0    | 0    | 0    | D3: INTD2 | D2: INTD1 | D1: INTD0 | D0: int Pending |

In order to provide minimum software overhead during data transfers, the virtual UART prioritizes interrupts into four levels as follows: Receiver Line Status (priority 1), Receiver Data Available (priority 2), Character Timeout Indication (priority 2, FIFO mode only), Transmitter Holding Register Empty (priority 3), and Modem Status (priority 4).

### Interrupt Identification Register (IIR): Address 2 (continued)

| D3 | D2 | D1 | D0 | Priority Level | Interrupt Type                     | Condition  | Reset   |
|----|----|----|----|----------------|------------------------------------|--|---|
| 0  | 0  | 0  | 1  | -              | -                                  | -  | -   |
| 0  | 1  | 1  | 0  | Highest        | Receiver Line Status               | Overrun Error, Parity Error, Framing Error or Break Interrupt  | Reads the Line Status Register  |
| 0  | 1  | 0  | 0  | Second         | Receiver Data Available            | Receiver Data Available or Trigger Level Reached   | Reads the Receiver Buffer Register or the FIFO has Dropped Below the threshold value          |
| 1  | 1  | 0  | 0  | Second         | Character Timeout Indication       | No characters have been read from or written to the Rx FIFO during programming time interval, and the Rx FIFO is not empty | Reads The Receiver Buffer Register  |
| 0  | 0  | 1  | 0  | Third          | Transmitter Holding Register Empty | Ready to accept new data for transmission  | Reads the IIR Register or (if source of interrupt) Writes To The Transmitter Holding Register |
| 0  | 0  | 0  | 0  | Fourth         | Modem Status                       | Clear to Send, Data Set Ready, Ring Indicator or Data Carrier Detected   | Reads the Modem Status Register   |

The IIR register gives prioritized information regarding the status of interrupt conditions. When accessed, the IIR indicates the highest priority interrupt that is pending.

Bit 0: This bit can be used in either a prioritized interrupt or polled environment to indicate whether an interrupt is pending. When this bit is logic 0, an interrupt is pending, and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is logic 1, no interrupt is pending, and polling (if used) continues.

Bit 1-2: These two bits of the IIR are used to identify the highest priority interrupt pending, as indicated in the table below.

Bit 3: In character mode, this bit is 0. In FIFO mode, this bit is set, along with bit 2, when a timeout interrupt is pending.

Bit 4-6: Not used

Bit 7: FIFO always enabled.



## FIFO Control Register (FCR): Address 2

Reset State 00h , write only

| bit7            | bit6            | bit5 | bit4 | bit3     | bit2         | bit1         | bit0        |
|-----------------|-----------------|------|------|----------|--------------|--------------|-------------|
| RCVR Trig (MSB) | RCVR Trig (LSB) | 0    | 0    | DMA Mode | TxFIFO Reset | RxFIFO Reset | FIFO Enable |

This is a write only register at the same location as the IIR, which is a read only register. This register is used to enable the FIFOs, clear the FIFOs, set the RxFIFO trigger level, and select the type of DMA signal.

Bit 0: FIFO Enable, This bit is always high

Bit 1: Writing a 1 to FCR1 clears all bytes in the RxFIFO and resets the counter logic to 0.

Bit 2: Writing a 1 to FCR2 clears all bytes in the TxFIFO and resets the counter logic to 0.

Bit 3: Setting FCR3 to 1 will cause the RXRDY and TXRDY pins to change from mode 0 to mode 1 if FCR0 = 1.

Bit 4-5: Reserved

Bit 6-7: FCR6, FCR7 are used to set the trigger level for the RxFIFO interrupt.

| FCR7 | FCR6 | RxFIFO Trigger Level |
|------|------|----------------------|
| 0    | 0    | 01                   |
| 0    | 1    | 04                   |
| 1    | 0    | 08                   |

## Line Control Register (LCR): Address 3

Reset State 00h, Write Only

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------|------|------|------|------|------|------|------|
| DLAB | SBRK | STP  | EPS  | PEN  | STB  | WLS1 | WLS0 |

This register is available to maintain compatibility with the standard 16550 register set, and provides information to the internal hardware that is used to determine the number of bits per character.

| WLS1 | WLS0 | Word Length |
|------|------|-------------|
| 0    | 0    | 5 bits      |
| 0    | 1    | 6 bits      |
| 1    | 0    | 7 bits      |
| 1    | 1    | 8 bits      |

Bit 0-1: WLS0-1 specifies the number of bits in each transmitted and received serial character.

Bit 2: STB specifies the number of stop bits in each transmitted character. If bit 2 is logic 0, one stop bit is generated in the transmitted data. If bit 2 is logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half stops are generated. If bit 2 is a logic 1 when either a 6-, 7- or 8-bit word length is selected, two stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: Logic 1 indicates that the PC has enabled parity generation and checking.

Bit 4: Logic 1 indicates that the PC is requesting an even number of logic 1s (even parity generation) to be transmitted or checked. Logic 0 indicates that the PC is requesting odd parity generation and checking.

Bit 5: When bits 3, 4 and 5 are logic 1, the parity bit is transmitted and checked by the receiver as logic 0. If bits 3 and 5 are 1 and bit 4 is logic 0, then the parity is transmitted and checked as logic 1.

Bit 6: This is a Break Control bit. When it is set to logic 1, a break condition is indicated.

Bit 7: The Divisor Latch Access bit must be set to logic 1 to access the Divisor Latches of the baud generator during a read or write operation. It must be set to logic 0 to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

## Modem Control Register (MCR): Address 4

Reset State 00h

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------|------|------|------|------|------|------|------|
| 0    | 0    | 0    | 0    | 0    | 0    | RTS  | DTR  |

Bit 0: This bit asserts a Data Terminal Ready condition that is readable via port P1.1 of the micro-controller 80C32. When bit 0 is set to logic 1, the P1.1 is forced to logic 0. When bit 0 is reset to logic 0, the P1.1 is forced to logic 1.

Bit 1: This bit asserts a Request To Send condition that is readable via port P3.4 of the micro-controller 80C32. When bit 1 is set to logic 1, the P3.4 is forced to logic 0. When bit 1 is reset to logic 0, the P3.4 is forced to logic 1.

## Line Status Register (LSR): Address 5

Reset State 60h, Read only

| bit7 | bit6  | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------|-------|------|------|------|------|------|------|
| RCV  | ETEMT | THRE | BI   | FE   | PE   | OE   | DR   |

This register provides status information to the host PC concerning character transfer. Bit 1-4 indicates error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected. The Line Status Register is valid for read operations only.

Bit 0: Set to logic 1 when a received character is available in the Rx FIFO. This bit is reset to logic 0 when the Rx FIFO is empty.

Bit 1: An Overrun error will occur only after the Rx FIFO is full and the next character has overwritten the unread FIFO data. This bit is reset upon reading the Line Status Register.

Bit 2: A logic 1 indicates that a received character does not have the correct even or odd parity as selected by the Parity Select bit. This error is set when the corresponding character is at the top of the Rx FIFO. It will remain set until the CPU reads the LSR.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to logic 1 whenever the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE bit is reset whenever the CPU reads the contents of the Line Status Register. The FE error condition is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 4: This bit is a Break Interrupt (BI) indicator. Bit 4 is set to logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register. The BI error condition is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 5: This bit is a Transmitter Holding Register Empty indicator. Bit 5 indicates that UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt Enable is set high. The THRE bit is reset to logic 0 when the host CPU loads a character into the Transmit Holding register. In the FIFO mode, this bit is set when the Tx FIFO is empty, and is cleared when at least 1 byte is written to the Tx FIFO.

Bit 6: This bit is the Transmitter Empty indicator. Bit 6 is set to logic 1 whenever the Transmitter Holding Register (THR) is empty, and is reset to logic 0 whenever the THR contains a character. In FIFO mode, this bit is set to 1 whenever the transmit FIFO is empty.

Bit 7: In character mode, this bit is 0. In FIFO mode, this bit is set when there is at least one parity error, framing error, or break indication in the FIFO. If there are no subsequent errors in the FIFO, LSR7 is cleared when the CPU reads the LSR.



### Modem Status Register (MSR): Address 6

Reset State bit 0-3 : low , bit 4-7: Input Signal

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------|------|------|------|------|------|------|------|
| DCD  | RI   | DSR  | CTS  | DDCD | TERI | DDSR | DCTS |

This 8-bit register provides the current state of the control lines from the Modem to the CPU. In addition, four bits of the Modem Status Register provide change information. These bits are set to logic 1 whenever a control input from the Modem changes state. They are reset to logic 0 whenever the CPU reads the Modem Status Register.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS (MSR Bit 4) has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the DSR (MSR Bit 5) has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring indicator. Bit 2 indicates that the RI (MSR Bit 6) has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the DCD (MSR Bit 7) has changed state.

Note: Whenever bit 0, 1, 2 or 3 is set to logic 1, a Modem Status Interrupt is generated.

Bit 4: This bit reflects the value of MSR Bit 4 (CTS).

Bit 5: This bit reflects the value of MSR Bit 5 (DSR).

Bit 6: This bit reflects the value of MSR Bit 6 (RI).

Bit 7: This bit reflects the value of MSR Bit 7 (DCD).

### Scratch Register (SCR): Address 7

Reset State 00h

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a Scratch Pad Register to be used by the programmer to hold data temporarily.

### Divisor Latch (DLL): Address 0 (DLAB = 1)

Reset State 00h

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------|------|------|------|------|------|------|------|
| DAT7 | DAT6 | DAT5 | DAT4 | DAT3 | DAT2 | DAT1 | DAT0 |

This register contains baud rate information from the host PC. The PC sets the Divisor Latch Register values.

### Divisor Latch (DLM): Address 1 (DLAB = 1)

Reset State 00h

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------|------|------|------|------|------|------|------|
| DAT7 | DAT6 | DAT5 | DAT4 | DAT3 | DAT2 | DAT1 | DAT0 |

This register contains baud rate information from the host PC.

Note: Two 8-bit latches (DLL-DLM) store the divisor in 16-digit binary format. The desired baud rate can be obtained by dividing the 115200Hz clock by the divisor.

| Desired Baud Rate | Divisor Value |
|-------------------|---------------|
| 50                | 2304          |
| 75                | 1536          |
| 110               | 1047          |
| 150               | 768           |
| 300               | 384           |
| 600               | 192           |
| 1200              | 96            |
| 2400              | 48            |
| 4800              | 24            |
| 9600              | 12            |
| 19200             | 6             |
| 38400             | 3             |
| 57600             | 2             |
| 115200            | 1             |



## 10. Micro-controller Control Register for PCI interface

### PCI Vender ID Low Byte Data Port: Address F800H (pci only)

Write only

This port configures PCI Vender ID low byte. (Offset 00 of PCI configuration register space)

### PCI Vender ID High Byte Data Port: Address F801H (pci only)

Write only

This port configures PCI Vender ID high byte. (Offset 01 of PCI configuration register space)

### PCI Device ID Low Byte Data Port: Address F802H

Write only

This port configures PCI Device ID low byte. (Offset 02 of PCI configuration register space)

### PCI Device ID High Byte Data Port: Address F803H

Write only

This port configures PCI Device ID low byte. (Offset 00 of PCI configuration register space)

### PCI Subsystem Vender ID Low Byte Data Port: Address F804H (pci only)

Write only

This port configures PCI Subsystem Vender ID low byte. (Offset 2C of PCI configuration register space)

### PCI Subsystem Vender ID High Byte Data Port: Address F805H (pci only)

Write only

This port configures PCI Subsystem Vender ID high byte. (Offset 2D of PCI configuration register space)

### PCI Subsystem Device ID Low Byte Data Port: Address F806H

Write only

This port configures PCI Subsystem Device ID low

byte. (Offset 2E of PCI configuration register space)

### PCI Subsystem Device ID High Byte Data Port: Address F807H

Write only

This port configures PCI Subsystem Device ID low

byte. (Offset 2F of PCI configuration register space)

### PCI Power Management New Capability: Address F808H, Bit 4 (pci only)

Write only

This bit configures if support PCI Power Management. (Offset 06 bit 4 of PCI configuration register space)

### PCI Power Management Power State: Address F809H, Bit[1..0] (pci only)

Write / Read

These bits configure PCI Power management Power State. (Offset 54 bit [1..0] of PCI configuration register space)

### PCI Power Management PME\_STATUS: Address F80AH, Bit 1

Write only

This bit configures PCI Power status. (Offset 55 bit 7 of PCI configuration register space)

### PCI Power Management PME\_EN: Address F80AH, Bit 0

Write only

This bit configures PCI if enable PME wake up (Offset 55 bit 0 of PCI configuration register space)

### PCI PME\_D3\_Support: Address F80BH, Bit 0

Write only

This port configures PCI if support PME wake up at D3 state. (Offset 53 bit [8..7] of PCI configuration register space)

**11. PCI Configuration Register Definition**

The definitions of PCI Configuration Registers are based on the PCI specification revision 2.1 and provide the initialization and configuration information to operate the PCI interface in the DM6588A. All registers can be accessed with byte,

word, or double word mode. As defined in PCI specification 2.1, read accesses to reserve or unimplemented registers will return a value of "0." These registers are to be described in the following sections.

**PCI Configuration Registers Mapping:**

| Description                       | Identifier | Address Offset | Value of Reset |
|-----------------------------------|------------|----------------|----------------|
| Identification                    | PCIID      | 00H            | 6588A1282H     |
| Command & Status                  | PCICS      | 04H            | 04100001H      |
| Revision                          | PCIRV      | 08H            | 07000210H      |
| Miscellaneous                     | PCILT      | 0CH            | 00000000H      |
| I/O Base Address                  | PCIIO      | 10H            | XXXXXXXXx001   |
| Reserved                          | -----      | 14H - 28H      |                |
| Subsystem Identification          | PCISID     | 2CH            | undefined      |
| Capability Pointer                | CAP_PTR    | 34H            | 00000050H      |
| Reserved                          | -----      | 38H            |                |
| Interrupt & Latency               | PCIINT     | 3CH            | 281401XXH      |
| Power Management Register         | PMR        | 50H            | 00110001H      |
| Power Management Control & Status | PMCSR      | 54H            | 00000000H      |

**Configuration Register Structure**

|                              |             |                                     |                |     |
|------------------------------|-------------|-------------------------------------|----------------|-----|
| Device ID                    |             | Vendor ID                           |                | 00H |
| Status (with bit 4 set to 1) |             | Command                             |                | 04H |
| Class Code = 070002          |             |                                     | Revisio        | 08H |
| BIST                         | Header Type | Latency Timer                       | Cach Line Size | 0CH |
| Bass Address Register CBIO   |             |                                     |                | 10H |
| Reserved                     |             |                                     |                | 14H |
| Reserved                     |             |                                     |                | 18H |
| Reserved                     |             |                                     |                | 1CH |
| Reserved                     |             |                                     |                | 20H |
| Reserved                     |             |                                     |                | 24H |
| Reserved                     |             |                                     |                | 28H |
| Subsystem ID                 |             | Subsystem Vendor ID                 |                | 2CH |
| Reserved                     |             |                                     |                | 30H |
| Reserved                     |             |                                     | Cap_Ptr        | 34H |
| Reserved                     |             |                                     |                | 38H |
| Max_Lat                      | Min_Gnt     | Interrupt Pin = 1                   | Interrupt Line | 3CH |
| Reserved                     |             |                                     |                | 40H |
| Reserved                     |             |                                     |                | 44H |
| Reserved                     |             |                                     |                | 48H |
| Reserved                     |             |                                     |                | 4CH |
| Power Management Capability  |             | Next Item Pointer                   | Capability ID  | 50H |
| Reserved                     |             | Power Management Control and Status |                | 54H |

**Key to Default**

In the register description that follows, the default column takes the form <Reset Value>

Where :

<Reset Value>:

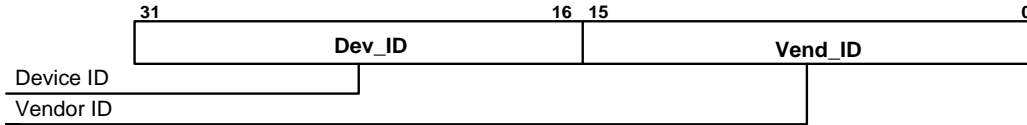
- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value

<Access Type>:

- RO = Read only
- RW = Read/Write
- R/C: means Read / Write & Write "1" for Clear.
- \_WR = Controller Write
- \_RD = Controller Read

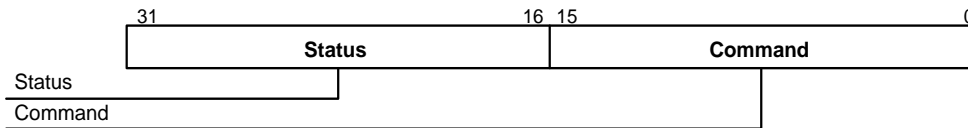


**Identification ID (xxxxxx00 - PCIID)**

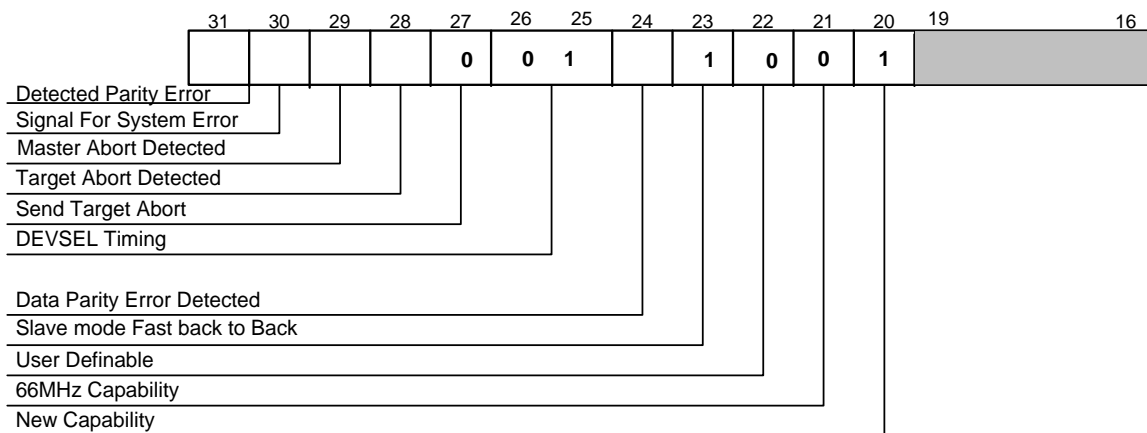


| Bit   | Default | Type      | Description  |
|-------|---------|-----------|--|
| 31:16 | 6588Ah  | RO<br>_WR | The field identifies the particular device. Unique and fixed number for the DM6588A is 6588Ah. It is the product number assigned by DAVICOM. |
| 15:0  | 1282h   | RO<br>_WR | This field identifies the manufacturer of the device. Unique and fixed number for Davicom is 1282h. It is a registered number from SIG.      |

**Command & Status (xxxxxx04 - PCICS)**



**Status Register Definition:**

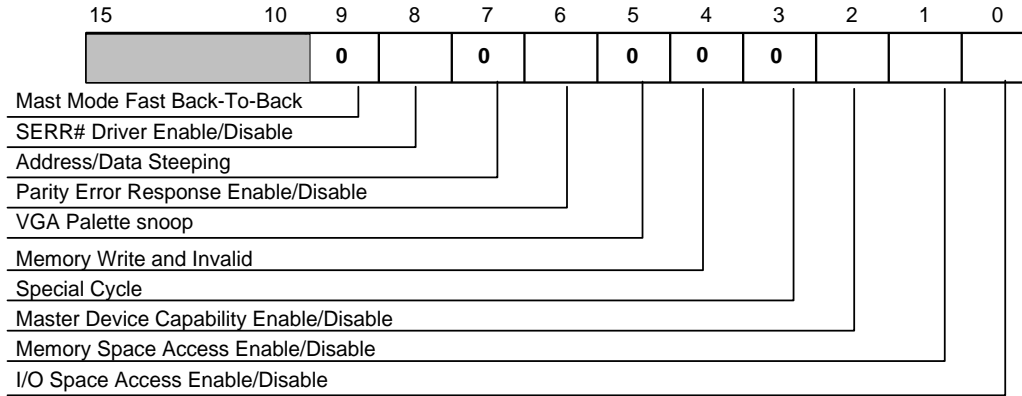




| Bit   | Default | Type      | Description   |
|-------|---------|-----------|---|
| 31    | 0       | R/C       | <b>Detected Parity Error</b><br>The DM6588A samples the AD[0:31], C/BE[0:3]#, and the PAR signal to check parity and to set parity errors.  |
| 30    | 0       | R/C       | <b>Signaled System Error</b><br>This bit is set when the SERR# signal is driven by the DM6588A. This system error occurs when an address parity is detected under the condition that bit 8 and bit 6 in command register below are set.   |
| 29    | 0       | R/C       | <b>Master Abort Detected</b><br>The DM6588A will never support the function   |
| 28    | 0       | R/C       | <b>Target Abort Detected</b><br>The DM6588A will never support the function   |
| 27    | 0       | RO        | <b>Send Target Abort</b> (0 For No Implementation)<br>The DM6588A will never support the function.  |
| 26:25 | 10      | RO        | <b>DEVSEL Timing</b> (10 Select Slow Timing)<br>Slow timing of DEVSEL# means the DM6588A will assert DEVSEL# signal two clocks after FRAME# is sample "asserted."   |
| 24    | 0       | R/C       | <b>Data Parity Error Detected</b><br>The DM6588A will never support the function  |
| 23    | 0       | RO        | <b>Slave mode Fast Back-To-Back Capable</b> (1 For Good Capability)<br>The DM6588A will never support the function  |
| 22    | 0       | RO        | <b>User-Definable-Feature Supported</b><br>(0 For No Support)   |
| 21    | 0       | RO        | <b>66 MHz Capable</b> (0 For No Capability)   |
| 20    | 1       | RO<br>_WR | <b>New Capabilities</b><br>This bit indicates whether this function implements a list of extended capabilities such as PCI power management. When set this bit indicates the presence of New Capabilities. A value of 0 means that this function does not implement New Capabilities. |
| 19:16 | 0000    | RO        | Reserved  |



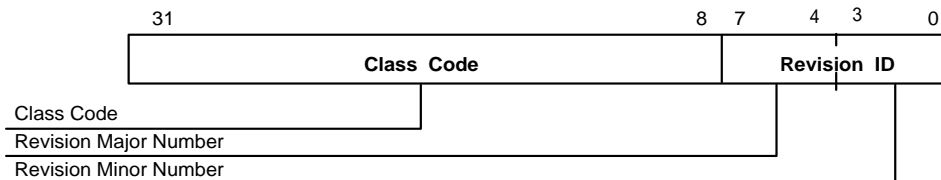
## Command Register Definition:



| Bit   | Default | Type | Description   |
|-------|---------|------|---|
| 15:10 | 000000  | RO   | Reserved  |
| 9     | 0       | RO   | <b>Master Fast Back-to-back Mode</b> (0 For No Support)<br>The DM6588A does not support master mode fast back-to-back capability and will not generate fast back-to-back cycles.                                |
| 8     | 0       | RW   | <b>SERR# Driver Enable/Disable</b><br>This bit controls the assertion of SERR# signal output. The SERR# output will be asserted on detection of an address parity error and if both this bit and bit 6 are set. |
| 7     | 0       | RO   | <b>Address/Data Steeping</b> (0 For No Steeping)  |
| 6     | 0       | RW   | <b>Parity Error Response Enable/Disable</b><br>Setting this bit will enable the DM6588A to assert PERR# on the detection of a data parity error and to assert SERR# for reporting address parity error.         |
| 5     | 0       | RO   | <b>VGA Palette Snooping</b> (0 For No Support)  |
| 4     | 0       | RO   | <b>Memory Write and Invalid</b> (0 For No Support)  |
| 3     | 0       | RO   | <b>Special Cycles</b> (0 For No Implementation)   |
| 2     | 0       | RW   | <b>Master Device Capability Enable/Disable</b><br>The DM6588A will never support the function.  |
| 1     | 0       | RW   | <b>Memory Space Access Enable/Disable</b><br>The DM6588A will never support the function.   |
| 0     | 1       | RW   | <b>I/O Space Access Enable/Disable</b><br>This bit controls the ability of I/O space access.  |

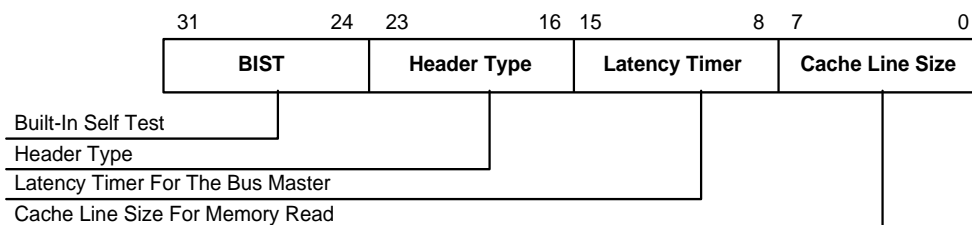


## Revision ID (xxxxxx08 - PCIRV)



| Bit  | Default | Type | Description  |
|------|---------|------|--|
| 31:8 | 070002h | RO   | <b>Class Code (070002h)</b><br>This is the standard code for Simple Communications controller.16550 compatible serial controller.        |
| 7:4  | 0001    | RO   | <b>Revision Major Number</b><br>This is the silicon-major revision number that will increase for the subsequent versions of the DM6588A  |
| 3:0  | 0000    | RO   | <b>Revision Minor Number</b><br>This is the silicon-minor revision number that will increase for the subsequent versions of the DM6588A. |

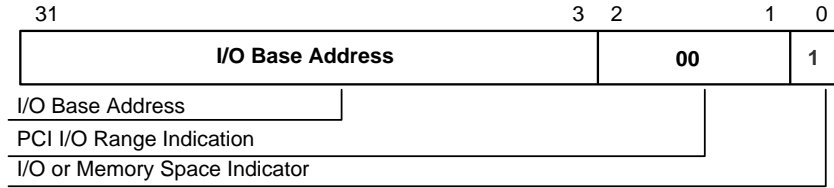
## Miscellaneous Function (Xxxxxx0c - PCILT)



| Bit   | Default | Type | Description   |
|-------|---------|------|---|
| 31:24 | 00h     | RO   | <b>Built-In Self Test</b> (=00h Means No Implementation)                                    |
| 23:16 | 00h     | RO   | <b>Header Type</b> (= 00h Means single function with Predefined Header Type )               |
| 15:8  | 00h     | RO   | <b>Latency Timer For The Bus Master.</b><br>The DM6588A will never support the function.    |
| 7:0   | 00h     | RO   | <b>Cache line Size For Memory Read Mode Selection</b> (00h Means No Implementation For Use) |

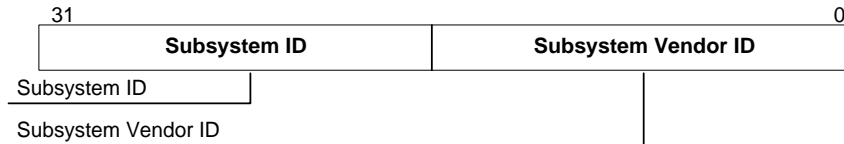


**I/O Base Address (Xxxxxx10 - PCIIO)**



| Bit  | Default   | Type | Description   |
|------|-----------|------|---|
| 31:3 | Undefined | RW   | <b>PCI I/O Base Address</b><br>This is the base address value for I/O access cycles. It will be compared to AD[31:3] in the address phase of bus command cycle for the I/O resource access. |
| 2:1  | 00        | RO   | <b>PCI I/O Range Indication</b><br>It indicates that the minimum I/O resource size is 08h.  |
| 0    | 1         | RO   | <b>I/O Space or Memory Space Base Indicator</b><br>Determines that the register maps into the I/O space.(=1 Indicates I/O Base)   |

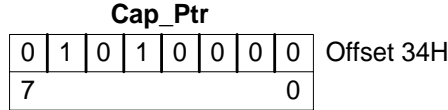
**Subsystem Identification (Xxxxxx2c - PCISID)**



| Bit   | Default | Type      | Description  |
|-------|---------|-----------|--|
| 31:16 | XXXXh   | RO<br>_WR | <b>Subsystem ID</b><br>Node number loaded from Controller and different from each card.  |
| 15:0  | XXXXh   | RO<br>_WR | <b>Subsystem Vendor ID</b><br>Unique number given by PCI SIG and loaded from Controller. |

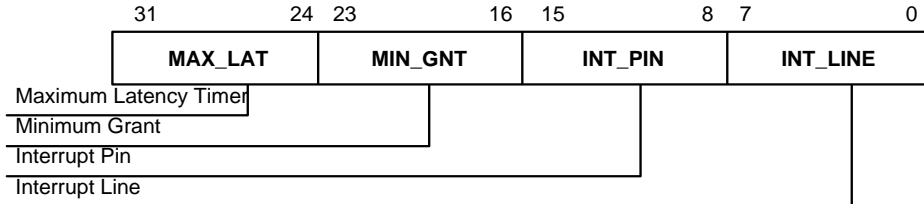


**Capabilities Pointer (Xxxxxx34 - Cap\_Ptr)**

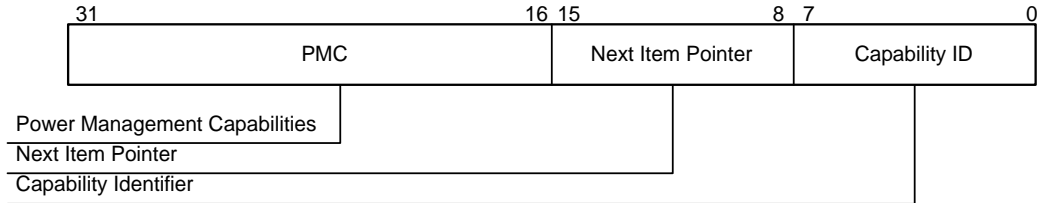


| Bit  | Default  | Type | Description   |
|------|----------|------|---|
| 31:8 | 000000h  | RO   | Reserved  |
| 7:0  | 01010000 | RO   | <b>Capability Pointer</b><br>The Cap_Ptr provides an offset (default is 50h) into the function's PCI Configuration Space for the location of the first term in the Capabilities Linked List. The Cap_Ptr offset is DOUBLE WORD aligned so the two least significant bits significant bits are always "0"s |

**Interrupt & Latency Configuration (Xxxxxx3c - PCIINT)**



| Bit   | Default | Type | Description  |
|-------|---------|------|--|
| 31:24 | 28h     | RO   | <b>Maximum Latency Timer</b> that can be sustained (Read Only and Read As 28h)       |
| 23:16 | 14h     | RO   | <b>Minimum Grant</b><br>Minimum Length of a Burst Period (Read Only and Read As 14h) |
| 15:8  | 01h     | RO   | <b>Interrupt Pin</b> read as 01h to indicate INTA#                                   |
| 7:0   | XXh     | RW   | <b>Interrupt Line</b> that Is Routed to the Interrupt Controller                     |

**Power Management Register (Xxxxxx50h~PMR)**


| Bit   | Default | Type      | Description  |
|-------|---------|-----------|--|
| 31:27 | 00000   | RO<br>_WR | <b>PME_Support</b><br>This five-bit field indicates the power states in which the function may assert PME#. A value of 0 for any bit indicates that the function is not capable of asserting the PME# signal while in that power state.<br>bit27 → PME# support D0<br>bit28 → PME# support D1<br>bit29 → PME# support D2<br>bit30 → PME# support D3(hot)<br>bit31 → PME# support D3(cold)<br>DM6588A's bit31~27=11000 indicates PME# can be asserted from D3(hot) & D(cold). |
| 26:22 | 00000   | RO        | Reserved (DM6588A not supports D1, D2)   |
| 21    | 0       | RO        | A "1" indicates that the function requires a device specific initialization sequence following transition to the D0 un-initialized state.  |
| 20    | 1       | RO        | <b>Auxiliary Power Source</b><br>This bit is only meaningful if bit31 is a "1".<br>This bit is "1" in DM6588A indicates that support for PME# in D3 (cold) requires auxiliary power.   |
| 19    | 0       | RO        | <b>PME# Clock</b><br>"0" indicates that no PCI clock is required for the function to generate PME#.  |
| 18:16 | 001     | RO        | <b>Version</b><br>A value of 001 indicates that this function complies with the Revision 1.0 of the PCI Power Management Interface Specification.  |
| 15:8  | 00h     | RO        | <b>Next Item Pointer</b><br>The offset into the function's PCI Configuration Space pointing to the location of next item in the function's capability list is "00h"  |
| 7:0   | 01h     | RO        | <b>Capability Identifier</b><br>When "01h" indicates the linked list item as being the PCI Power Management Registers.   |



Power Management Control/Status(Xxxxxx54h~PMCSR)

| PMCSR |    |   |   |   |   |   |     |   |   |   |   |     |            |   |
|-------|----|---|---|---|---|---|-----|---|---|---|---|-----|------------|---|
| R/W   | 0  | 0 | 0 | 0 | 0 | 0 | R/W | 0 | 0 | 0 | 0 | R/W | Offset=54H |   |
| 15    | 14 |   |   |   |   |   | 9   | 8 | 7 |   |   | 2   | 1          | 0 |

| Bit   | Default | Type             | Description  |
|-------|---------|------------------|--|
| 31:16 | 0000h   | RO               | Reserved   |
| 15    | 0       | R/C<br>_WR       | <b>PME_Status</b><br>This bit is set when the function would normally assert the PME# signal independent of the state of the PME_En bit. Writing a “1” to this bit will clear it.<br>This bit defaults to “0” if the function does not support PME# generation from D3(cold).<br>If the function supports PME# from D3 (cold) then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded. |
| 14:9  | 000000  | RO               | Reserved.<br>It means that the DM6588A does not support reporting power consumption.   |
| 8     | 0       | RW<br>_WR        | <b>PME_En</b><br>Write “1” to enables the function to assert PME#, write “0” to disable PME# assertion.<br>This bit defaults to “0” if the function does not support PME# generation from D3(cold).<br>If the function supports PME# from D3(cold) then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded.  |
| 7:2   | 000000  | RO               | Reserved   |
| 1:0   | 00      | RW<br>_WR<br>_RD | <b>Power State.</b><br>This two bits field is both used to determine the current power state of a function and to set the function into a new power state. The definitions given below.<br>00 : D0<br>11 : D3(hot)   |

**PCI function power management state**

The DM6588A supports PCI function power states D0, D3 (hot), D3 (cold). Additional PCI signal PME# to pin A19 of the standard PCI connector.

**PME Context**

PME (power Management Event) context is defined as the functional state information and logic required to generate power management events (PMEs), report PME status, and enable PME.

For MODEM, PME context consists of **PME\_En** bit, **PME\_Status** bit , **Ring Detect** ,and **Ring to PME** circuit.

**PCI MODEM Power Management Operation**

During a true power-on situation (no auxiliary and normal power), PME\_En = 0 to avoid to assert PME#. When assert RST#, the pci configuration space is set to default value except PME context which must preserve.

DM6588A can not assert PME# from D0. But can Assert PME# from D3(hot) and D3(cold). Hence the Ring to PME# circuit must check the power state. If ring comes at D0 power state, it can not assert PME#.

Software will enable its use by setting the PME\_En bit in the PMCSR.

It must continue to assert PME# until software either clears the PME\_En bit or clears the PME\_Status bit.

Before enter D3 (cold) state, host must :

1. Write 1 into PME\_Status bit to clear previous PME status
2. Write 1 into PME\_En bit to enable PME function.
3. Write 3 into Power\_state
4. Power off PCI bus.

When Ring comes, Ring to PME# circuit check if PME\_EN=1 and Power\_staus <>0. If yes, assert PME# and set PME\_Status=1.

When host detect PME# asserted, it will power up PCI bus and assert RST# to initialize pci modem. At the same time, it write 1 into PME\_En bit or PME\_Status bit to stop PME#.

Before enter D3(hot) state, host must :

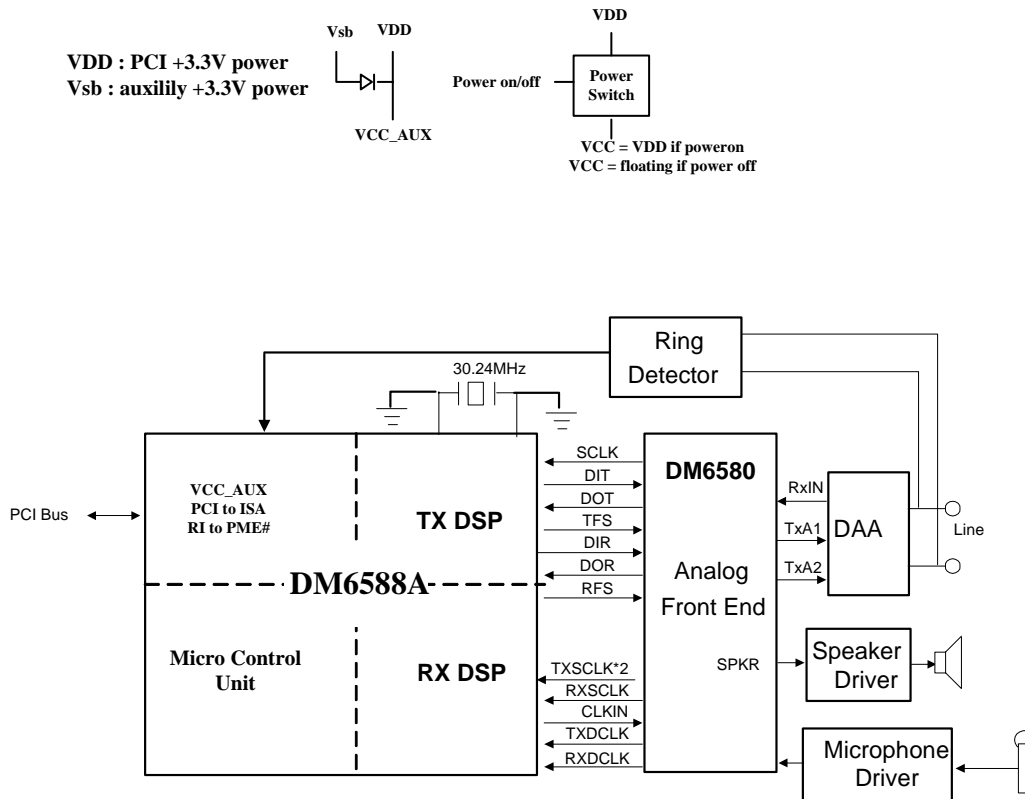
5. Write 1 into PME\_Status bit to clear previous PME status
6. Write 1 into PME\_En bit to enable PME function.
7. Write 3 into Power\_state

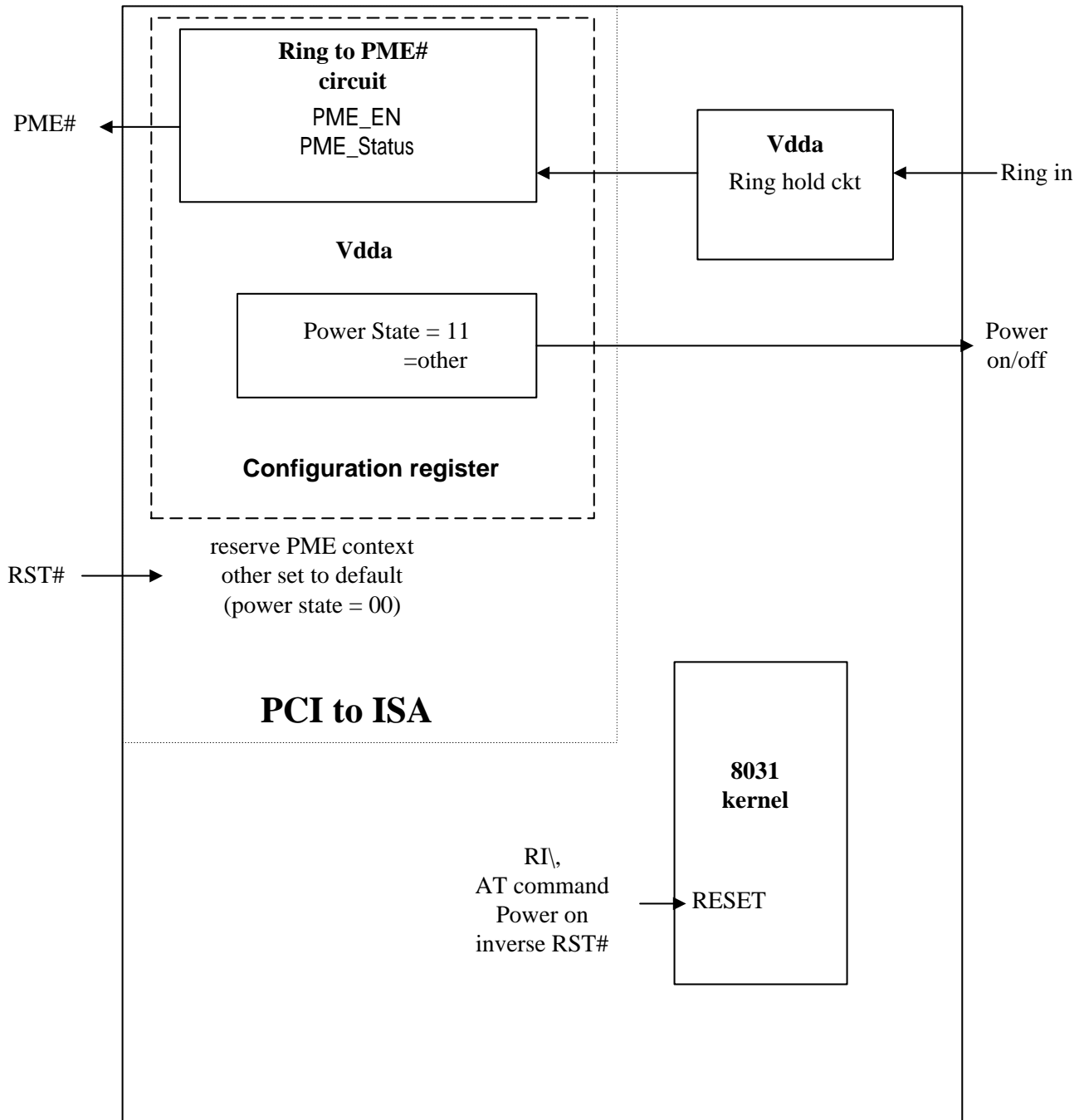
When Ring come, Ring to PME# circuit check if PME\_EN=1 and Power\_staus <>0. If yes, assert PME# and set PME\_Status=1.

When host detect PME# asserted, it will re-initialize pci modem and set Power\_State=0 to return D0 state.

At the same time, it writes 1 into PME\_En bit or PME\_Status bit to stop PME#.

## PCI MODEM Board Power Management





**DM6588A PCI Power Configuration**

**DM6588A External Electrical Characteristics****DM6588A External Absolute Maximum Ratings\* (25°C)**

| Symbol    | Parameter                           | Min. | Max. | Unit | Conditions |
|-----------|-------------------------------------|------|------|------|------------|
| DVCC,AVCC | Supply Voltage                      | -0.3 | 3.6  | V    |            |
| VIN       | DC Input Voltage (VIN)              | -0.5 | 5.5  | V    |            |
| VOUT      | DC Output Voltage(VOUT)             | -0.3 | 3.6  | V    |            |
| TA        | Ambient Temperature                 | 0    | +70  | °C   |            |
| Tstg      | Storage Temperature Rang (Tstg)     | -65  | +150 | °C   |            |
| LT        | Lead Temp. (TL, Soldering, 10 sec.) | -    | 245  | °C   | Pb -Free   |

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings " may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the

operational section of this specification is not implied or intended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

**DM6588A External DC Electrical Characteristics (VDD = 3.3V, GND = 0V)**

| Symbol   | Parameter             | Min. | Typ. | Max. | Unit | Conditions     |
|----------|-----------------------|------|------|------|------|----------------|
| VDD      | Operating Voltage     | 3.15 | 3.3  | 3.45 | V    |                |
| IDD      | Operating Current     |      | 90   |      | mA   |                |
| VIH      | Input High Voltage    | 2.0  |      |      | V    |                |
| VIL      | Input Low Voltage     |      |      | 0.8  | V    |                |
| IIL      | Input Leakage Current | -1.0 |      | 1.0  | μA   | VIN = 0, 3.45V |
| VOH      | Output High Voltage   | 2.4  |      |      | V    | IOH = -0.5mA   |
| VOL      | Output Low Voltage    |      |      | 0.4  | V    | IOL = 1.5mA    |
| CIN      | Input Capacitance     |      | 10.0 |      | pF   |                |
| VILRESET | Reset Schmitt VIL     |      |      | 0.8  | V    |                |
| VIHRESET | Reset Schmitt VIH     | 2.8  |      |      | V    |                |

**DM6588A ISA Electrical Characteristics****DM6588A ISA Absolute Maximum Ratings\* (25°C)**

| Symbol         | Parameter                           | Min. | Max. | Unit | Conditions |
|----------------|-------------------------------------|------|------|------|------------|
| DVCC,AVCC      | Supply Voltage                      | -0.3 | 3.6  | V    |            |
| VIN            | DC Input Voltage (VIN)              | -0.5 | 5.5  | V    |            |
| VOUT           | DC Output Voltage(VOUT)             | -0.3 | 3.6  | V    |            |
| T <sub>A</sub> | Ambient Temperature                 | 0    | +70  | °C   |            |
| Tstg           | Storage Temperature Rang (Tstg)     | -65  | +150 | °C   |            |
| L <sub>T</sub> | Lead Temp. (TL, Soldering, 10 sec.) | -    | 245  | °C   | Pb -Free   |

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings " may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the

operational section of this specification is not implied or intended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

**DM6588A ISA DC Electrical Characteristics (VDD = 3.3V, GND = 0V)**

| Symbol   | Parameter             | Min. | Typ. | Max. | Unit | Conditions     |
|----------|-----------------------|------|------|------|------|----------------|
| VDD      | Operating Voltage     | 3.15 | 3.3  | 3.45 | V    |                |
| IDD      | Operating Current     |      | 90   |      | mA   |                |
| VIH      | Input High Voltage    | 2.0  |      |      | V    |                |
| VIL      | Input Low Voltage     |      |      | 0.8  | V    |                |
| IIL      | Input Leakage Current | -1.0 |      | 1.0  | μA   | VIN = 0, 3.45V |
| VOH      | Output High Voltage   | 2.4  |      |      | V    | IOH = -0.5mA   |
| VOL      | Output Low Voltage    |      |      | 0.4  | V    | IOL = 1.5mA    |
| CIN      | Input Capacitance     |      | 10.0 |      | pF   |                |
| VILRESET | Reset Schmitt VIL     |      |      | 0.8  | V    |                |
| VIHRESET | Reset Schmitt VIH     | 2.8  |      |      | V    |                |

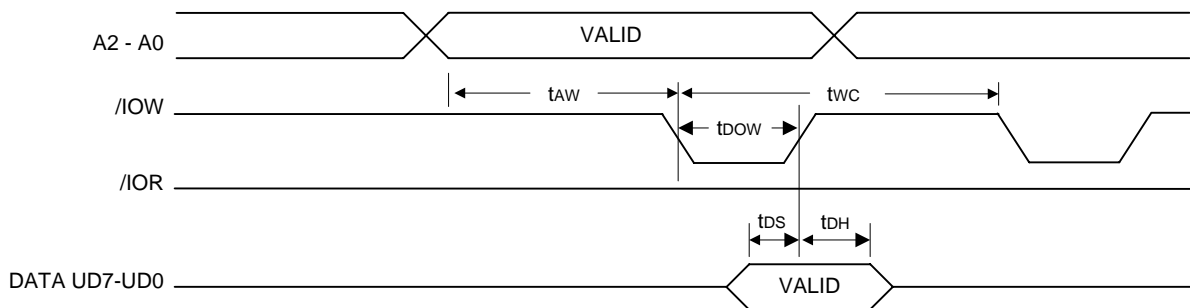
## DM6588A ISA AC Electrical Characteristics & Timing waveforms

### DM6588A ISA AC Electrical Characteristics ( $V_{DD} = 3.3V$ , $G_{ND} = 0V$ )

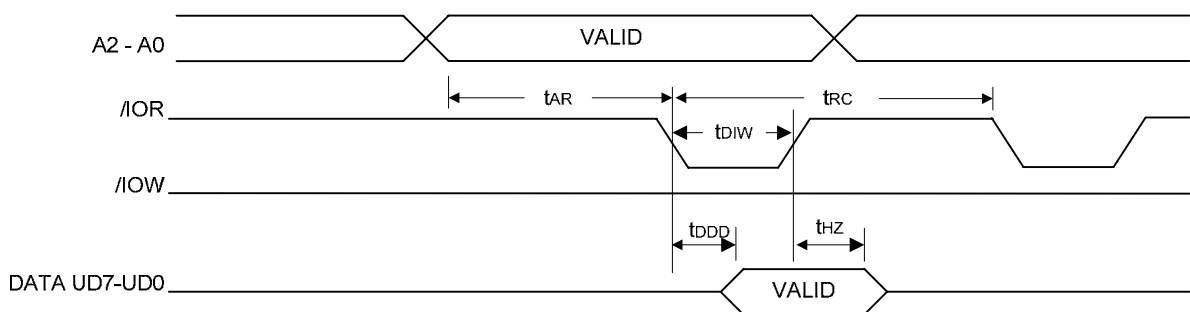
| Symbol | Parameter                    | Min. | Typ. | Max. | Unit | Conditions    |
|--------|------------------------------|------|------|------|------|---------------|
| tAW    | IOW Delay from Address       | 18   |      |      | ns   |               |
| tWC    | Write Cycle                  | 106  |      |      | ns   |               |
| tDOW   | IOW Strobe Width             | 22   |      |      | ns   |               |
| tDS    | Data Setup Time              | 22   |      |      | ns   |               |
| tDH    | Data Hold Time               | 5    |      |      | ns   |               |
| tAR    | IOR Delay from Address       | 5    |      |      | ns   |               |
| tRC    | Read Cycle                   | 102  |      |      | ns   |               |
| tDIW   | IOR Strobe Width             | 22   |      |      | ns   |               |
| tDDD   | Delay from IOR to Data Valid | -    |      | 20   | ns   | 100pF loading |
| tHZ    | IOR to Floating Data Delay   | -    |      | 30   | ns   | 100pF loading |

### DM6588A ISA signals Timing Diagrams

#### Write Cycle



#### Read Cycle



**DM6588A PCI Electrical Characteristics****DM6588A PCI Absolute Maximum Ratings\* (25°C)**

| Symbol           | Parameter                           | Min. | Max. | Unit | Conditions |
|------------------|-------------------------------------|------|------|------|------------|
| DVCC,AVCC        | Supply Voltage                      | -0.3 | 3.6  | V    |            |
| V <sub>IN</sub>  | DC Input Voltage (VIN)              | -0.5 | 5.5  | V    |            |
| V <sub>OUT</sub> | DC Output Voltage(VOUT)             | -0.3 | 3.6  | V    |            |
| T <sub>A</sub>   | Ambient Temperature                 | 0    | +70  | °C   |            |
| T <sub>stg</sub> | Storage Temperature Rang (Tstg)     | -65  | +150 | °C   |            |
| L <sub>T</sub>   | Lead Temp. (TL, Soldering, 10 sec.) | -    | 245  | °C   | Pb -Free   |

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings " may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the

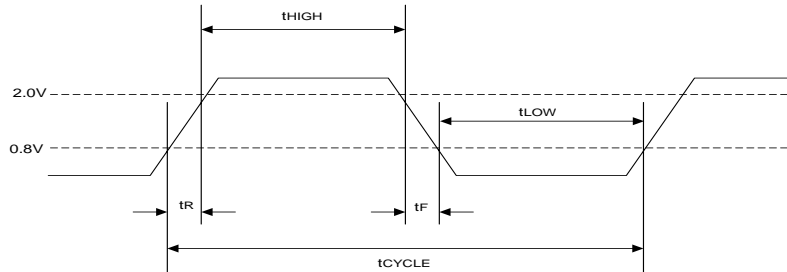
operational section of this specification is not implied or intended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DM6588A PCI DC Electrical Characteristics (VDD = 3.3V, GND = 0V)**

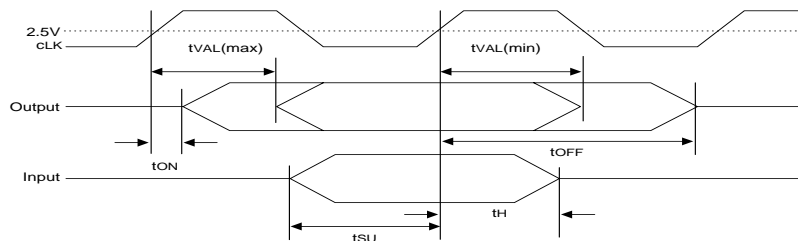
| Symbol                | Parameter             | Min. | Typ. | Max. | Unit | Conditions                 |
|-----------------------|-----------------------|------|------|------|------|----------------------------|
| V <sub>DD</sub>       | Operating Voltage     | 3.15 | 3.3  | 3.45 | V    |                            |
| I <sub>DD</sub>       | Operating Current     |      | 120  |      | mA   |                            |
| V <sub>IH</sub>       | Input High Voltage    | 2.0  |      |      | V    |                            |
| V <sub>IL</sub>       | Input Low Voltage     |      |      | 0.8  | V    |                            |
| I <sub>IL</sub>       | Input Leakage Current | -1.0 |      | 1.0  | μA   | V <sub>IN</sub> = 0, 3.45V |
| V <sub>OH</sub>       | Output High Voltage   | 2.4  |      |      | V    | I <sub>OH</sub> = -0.5mA   |
| V <sub>OL</sub>       | Output Low Voltage    |      |      | 0.4  | V    | I <sub>OL</sub> = 1.5mA    |
| C <sub>IN</sub>       | Input Capacitance     |      | 10.0 |      | pF   |                            |
| V <sub>IL</sub> RESET | Reset Schmitt VIL     |      |      | 0.8  | V    |                            |
| V <sub>IH</sub> RESET | Reset Schmitt VIH     | 2.8  |      |      | V    |                            |

**DM6588A PCI AC Electrical Characteristics & Timing Waveforms**

( $V_{DD} = 3.3V$ ,  $GND = 0V$ ;  $T_A = 25$  )

**PCI Clock Specifications Timing**


| Symbol      | Parameter            | Min. | Typ. | Max. | Unit | Conditions |
|-------------|----------------------|------|------|------|------|------------|
| $t_R$       | PCI_CLK rising time  | 4    | -    | -    | ns   | -          |
| $t_F$       | PCI_CLK falling time | 4    | -    | -    | ns   | -          |
| $t_{CYCLE}$ | Cycle time           | 30   | -    | -    | ns   | -          |
| $t_{HIGH}$  | PCI_CLK High Time    | 12   | -    | -    | ns   | -          |
| $t_{LOW}$   | PCI_CLK Low Time     | 12   | -    | -    | ns   | -          |

**Other PCI Signals Timing Diagram**


| Symbol    | Parameter                                | Min. | Typ. | Max. | Unit | Conditions         |
|-----------|--|------|------|------|------|--------------------|
| $t_{VAL}$ | CLK-To-Signal Valid Delay                | 2    | -    | 15   | ns   | $C_{LOAD} = 50$ pF |
| $t_{ON}$  | Float-To-Active Delay From CLK           | 2    | -    | -    | ns   | -                  |
| $t_{OFF}$ | Active-To-Float Delay From CLK           | -    | -    | 28   | ns   | -                  |
| $t_{SU}$  | Input Signal Valid Setup Time Before CLK | 7    | -    | -    | ns   | -                  |
| $t_H$     | Input Signal Hold Time From CLK          | 5    | -    | -    | ns   | -                  |

## Chip 2: DM6580 Analog Front End

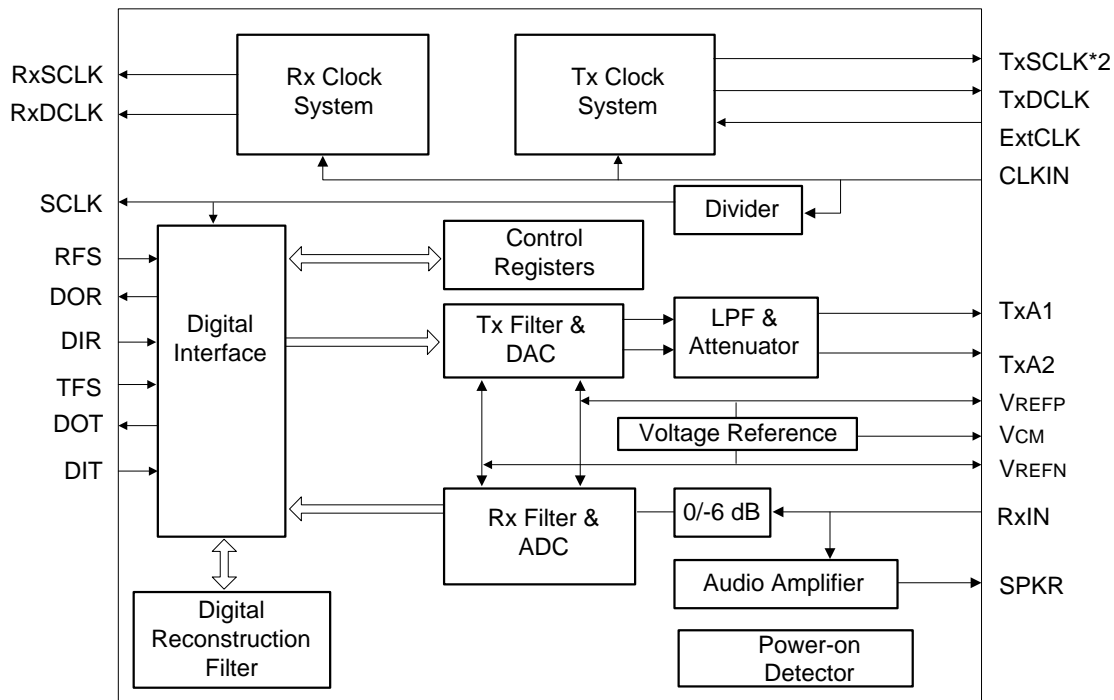
### DM6580 Description

The DM6580 is a single chip Analog Front End (AFE) designed to be implemented in voice grade modems for data rates up to 56000bps. The DM6580 is an essential part the complete modem device set. The AFE converts the analog signal into digital form and transfers the digital data to the DSP through the serial port. All the clock information needed in a modem device is also generated in the DM6580. Differential analog outputs are provided to achieve the maximum output signal level. An audio monitor with programmable volume levels is built in to monitor the on-line signal. Inside the device, a 16-bit ADC and a 16-bit DAC with over-sampling and noise-shaping techniques is implemented to maximize performance.

The DM6580 offers wide-band transmit and receive filters so that the voice band signal is transmitted or received without amplitude distortion and with

minimum group delay. In order to support multi-mode modem standards, such as V.90, V.34+, V.32bis, V.32, V.22bis, V.22, V.23, V.21, Bell 212A, Bell 103, V.17, V.29, V.27ter, programmable baud and data rate clock generators are provided. For asymmetric channel usage, the transmit and receive clock generators are independent. In order to enhance echo-cancellation, the receive clock is synchronized with the transmit clock and the best receive timing sample is reconstructed by a reconstruction filter. The Transmit Digital Phase Lock Loop (DPLL) is self-tuning to provide a master, slave or free-running mode for the data terminal interface. A receive DPLL that is step programmable by the host DSP is implemented to get the best samples for the relevant signal processing.

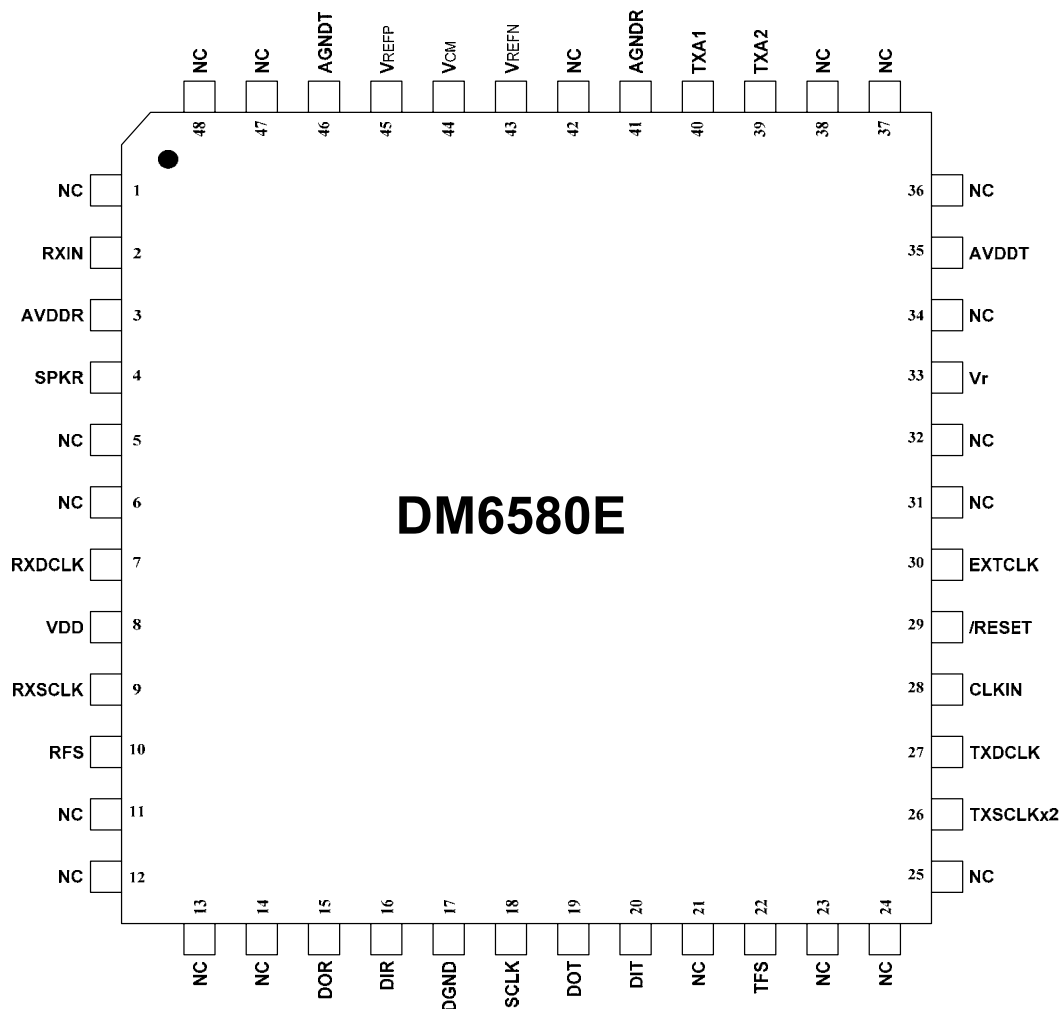
### DM6580 Block Diagram



## DM6580 Features

- 16-bit - A/D and D/A converters
- Dynamic range : 86dB
- Total harmonic distortion : -86dB
- Separate transmit and receive clocks
- Symbol rate : 75, 300, 600, 1200, 1600, 2400, 2743, 2800, 3000, 3200, 3429, 8000Hz
- Data rate V.34 : 75, 300, 600, 1200, 2400, 4800, 7200, 9600, 12000, 14400, 16800, 19200, 21600, 24000, 26400, 28800, 31200, 33600 bps
- Data rate V.90 : up to 56000 bps
- Dual synchronous serial interface to host Digital Signal Processor (DSP)
- Separate transmit digital phase lock loop and receive digital phase lock loop
- Full echo cancellation capability
- Differential analog output
- Single-ended analog input
- Single power supply voltage : +5V
- Low power consumption

## DM6580 Pin Configuration





## DM6580 Pin Description

| Pin No.<br>48pin<br>LQFP   | Pin Name | I/O | Description   |
|--|----------|-----|---|
| 2  | RXIN     | I   | Receive Analog Input                                    |
| 3  | AVDDR    | I   | Analog VDD For The Receiver Analog Circuitry (+5Vdc)    |
| 4  | SPKR     | O   | Speaker Driver  |
| 7  | RXDCLK   | O   | Receive Data Clock                                      |
| 8  | VDD      | P   | Digital Power   |
| 9  | RXSCLK   | O   | Receive Sample Clock                                    |
| 10   | RFS      | I   | Receive Frame Synchronization                           |
| 15   | DOR      | O   | Data Output For Receiver                                |
| 16   | DIR      | I   | Data Input For Receiver                                 |
| 17   | DGND     | P   | Digital Ground  |
| 18   | SCLK     | O   | Serial Clock Synchronized With All Serial Data          |
| 19   | DOT      | O   | Data Output For Transmitter                             |
| 20   | DIT      | I   | Data Input For Transmitter                              |
| 22   | TFS      | I   | Transmit Frame Synchronization                          |
| 26   | TXSCLK*2 | O   | Transmit Sample Clock * 2                               |
| 27   | TXDCLK   | O   | Transmit Data Clock                                     |
| 28   | CLKIN    | I   | Master Clock Input (20.16MHz = 40.32MHz / 2 )           |
| 29   | /RESET   | I   | Codec Reset Input                                       |
| 30   | EXTCLK   | I   | External Transmit Data Clock                            |
| 33   | Vr       | O   | Internal Reference Voltage. Connect 0.1uF to DGND       |
| 35   | AVDDT    | I   | Analog VDD For The Transmitter Analog Circuitry (+5Vdc) |
| 39   | TXA2     | O   | Transmit Negative Analog Output                         |
| 40   | TXA1     | O   | Transmit Positive Analog Output                         |
| 41   | AGNDR    | P   | Analog Receiver Circuitry Signal Return Path            |
| 43   | VREFN    | O   | Negative Reference Voltage, VCM - 1V                    |
| 44   | VCM      | O   | Common Mode Voltage Output, 2.5V                        |
| 45   | VREFP    | O   | Positive Reference Voltage, VCM + 1V                    |
| 46   | AGNDT    | P   | Analog Transmitter Circuitry Signal Return Path         |
| 1,5,6,<br>11,12,13,<br>14,21,23,<br>24,25,31,<br>32,34,36,<br>37,38,42,<br>47,48 | NC       | N   | NC  |

## DM6580 Functional Description

In this chip, we could roughly divide it into two major parts: digital portion and analog portion. The functional blocks are described separately in this section. The analog circuits include a sigma-delta modulator/demodulator, decimation/interpolation filters, a speaker driver, low-pass filter and certain logic circuits. The digital circuits are composed of Tx/Rx clock generator/PLL, serial port, serial/parallel conversions and control registers. All the clock information the analog circuits need should be provided by the digital clock system since the best sampling instant of A/D and D/A depends on the received signal and transmit signals. The data format of A/D and D/A is 2's complement.

The master clock (FQ) is obtained from an external signal connected to CLKIN. The different transmit and receive clocks are obtained by master clock frequency division in several programmable counters. The Tx and Rx clocks can be synchronized on external signals by performing the phase shifts in the frequency division process. Two independent digital phase locked loops are implemented using this principle, one for transmit clock system, the other, receive clock. The tracking of the transmit clock is automatically done by the transmit DPLL circuit. The receive DPLL circuit is controlled by the host processor and it is actually an adjustable phase shifter.

## DM6580 Register Description

| Register      | D11 | D10  | D9   | D8 | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  | Programme Functions    |
|---------------|-----|------|------|----|-----|-----|-----|-----|-----|-----|-----|-----|------------------------|
| <b>TxCR0</b>  | R1  | X3   | X2   | X1 | X0  | N3  | N2  | N1  | N0  | R0  | S   | T   | Tx Data Rate Clock     |
| <b>TxCR1</b>  |     |      | Q1   | D  | M1  | M0  | Q0  | F   | Y   | U2  | U1  | U0  | Tx Baud sample Clock   |
| <b>TxCR2</b>  |     | Vol1 | Vol2 | F1 | F0  | W   | ATT | LTX | LC  | SST | EMX | VF  | Miscellaneous control  |
| <b>TxTest</b> |     |      |      |    |     |     |     |     |     |     |     |     | Reserved               |
| <b>RxCR0</b>  | R1  |      | H2   | H1 | H0  | N3  | N2  | N1  | N0  | R0  | S   | T   | Rx Data Rate Clock     |
| <b>RxCR1</b>  |     | Q1   | RST  | D  | M1  | M0  | Q0  | P   | Y   | U2  | U1  | U0  | Rx Baud SampleClock    |
| <b>RxCR2</b>  |     |      | -6dB | LL | PS4 | PS3 | PS2 | PS1 | PS0 | AP2 | AP1 | AP0 | Rx Phase Shift Control |
| <b>RxTest</b> |     |      |      |    |     |     |     |     |     |     |     |     | Reserved               |



## DM6580 Absolute Maximum Ratings\*

### Absolute Maximum Ratings\* (25°C)

| Symbol           | Parameter                                    | Min. | Max. | Unit | Conditions |
|------------------|--|------|------|------|------------|
| DVCC,AVCC        | Supply Voltage                               | -0.3 | 3.6  | V    |            |
| V <sub>IN</sub>  | DC Input Voltage (V <sub>IN</sub> )          | -0.5 | 5.5  | V    |            |
| V <sub>OUT</sub> | DC Output Voltage(V <sub>OUT</sub> )         | -0.3 | 3.6  | V    |            |
| T <sub>A</sub>   | Ambient Temperature                          | 0    | +70  | °C   |            |
| T <sub>stg</sub> | Storage Temperature Rang (T <sub>stg</sub> ) | -65  | +150 | °C   |            |
| L <sub>T</sub>   | Lead Temp. (TL, Soldering, 10 sec.)          | -    | 260  | °C   | Pb -Free   |

### \*Comments

Stresses above those listed under "Absolute Maximum Ratings " may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the

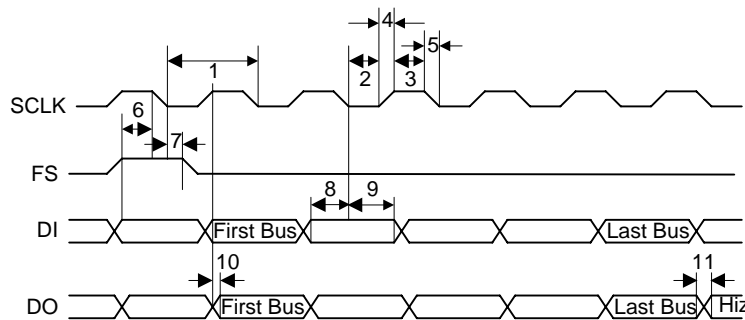
operational section of this specification is not implied or intended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DM6580 DC Electrical Characteristics & Timing Waveforms (VDD = 5V)

| Symbol                         | Parameter                             | Min. | Typ.                | Max. | Unit | Conditions                                    |
|--------------------------------|---------------------------------------|------|---------------------|------|------|---|
| VDD                            | Operating Voltage                     | 4.75 | 5                   | 5.25 | V    |   |
| V <sub>CM</sub>                | Output Common Mode Voltage            |      | 2.5                 |      | V    |   |
| I <sub>DD</sub>                | Supply Current                        |      | 25                  |      | mA   |   |
| V <sub>IL</sub>                | Input Low Voltage                     |      |                     | 0.8  | V    |   |
| V <sub>IH</sub>                | Input High Voltage                    | 2.0  |                     |      | V    |   |
| V <sub>OL</sub>                | Output Low Voltage                    |      |                     | 0.4  | V    |   |
| V <sub>OH</sub>                | Output High Voltage                   | 2.4  |                     |      | V    |   |
| I <sub>IL</sub>                | Input leakage Current                 | -2.0 | ±1.0                | 2.0  | μA   | V <sub>I</sub> =0V,5.25V                      |
| C <sub>IN</sub>                | Input Capacitance                     |      | 5.0                 |      | pF   |   |
| V <sub>REF</sub>               | Differential Reference Voltage Output | 1.9  | 2.0                 | 2.1  | V    |   |
| V <sub>CM<sub>OUT</sub></sub>  | Output Common Mode Offset             | -200 |                     | 200  | mV   | =(TxA1+TxA2)/2-V <sub>CM</sub>                |
| V <sub>DIF<sub>OUT</sub></sub> | Differential Output Voltage           |      | 3 *V <sub>REF</sub> |      | V    | TxA1-TxA2 ≤ 3*V <sub>REF</sub>                |
| V <sub>OFF<sub>OUT</sub></sub> | Differential Output DC Offset Voltage | -100 |                     | 100  | mV   | V <sub>DC</sub> (TxA1)-V <sub>DC</sub> (TxA2) |
| R <sub>IN</sub>                | Input Resistance RxIN                 | 100  |                     |      | kΩ   |   |
| R <sub>OUT</sub>               | Output Resistance TxA1, TxA2, SPKR    |      | 1                   | 2    | kΩ   |   |
| R <sub>L</sub>                 | Load Resistance TxA1, TxA2, SPKR      | 20   |                     |      | kΩ   |   |
| C <sub>L</sub>                 | Load Capacitance TxA1, TxA2, SPKR     |      |                     | 50   | pF   |   |

**DM6580 AC Characteristics & Timing Waveforms (VDD = 5V)**
**Serial Port Timing**

| Symbol | Parameter             | Min. | Typ. | Max. | Unit | Conditions |
|--------|-----------------------|------|------|------|------|------------|
| 1      | SCLK Period           | 49   |      |      | ns   |            |
| 2      | SCLK Low Width        | 24   |      |      | ns   |            |
| 3      | SCLK High Width       | 24   |      |      | ns   |            |
| 4      | SCLK Rise Time        |      |      | 5    | ns   |            |
| 5      | SCLK Fall Time        |      |      | 5    | ns   |            |
| 6      | FS To SCLK Setup      | 17   |      |      | ns   |            |
| 7      | FS To SCLK Hold       | 17   |      |      | ns   |            |
| 8      | DI To SCLK Setup      | 5    |      |      | ns   |            |
| 9      | DI To SCLK Hold       | 5    |      |      | ns   |            |
| 10     | SCLK High To DO Valid |      |      | 8    | ns   |            |
| 11     | SCLK To DO Hiz        |      |      | 8    | ns   |            |

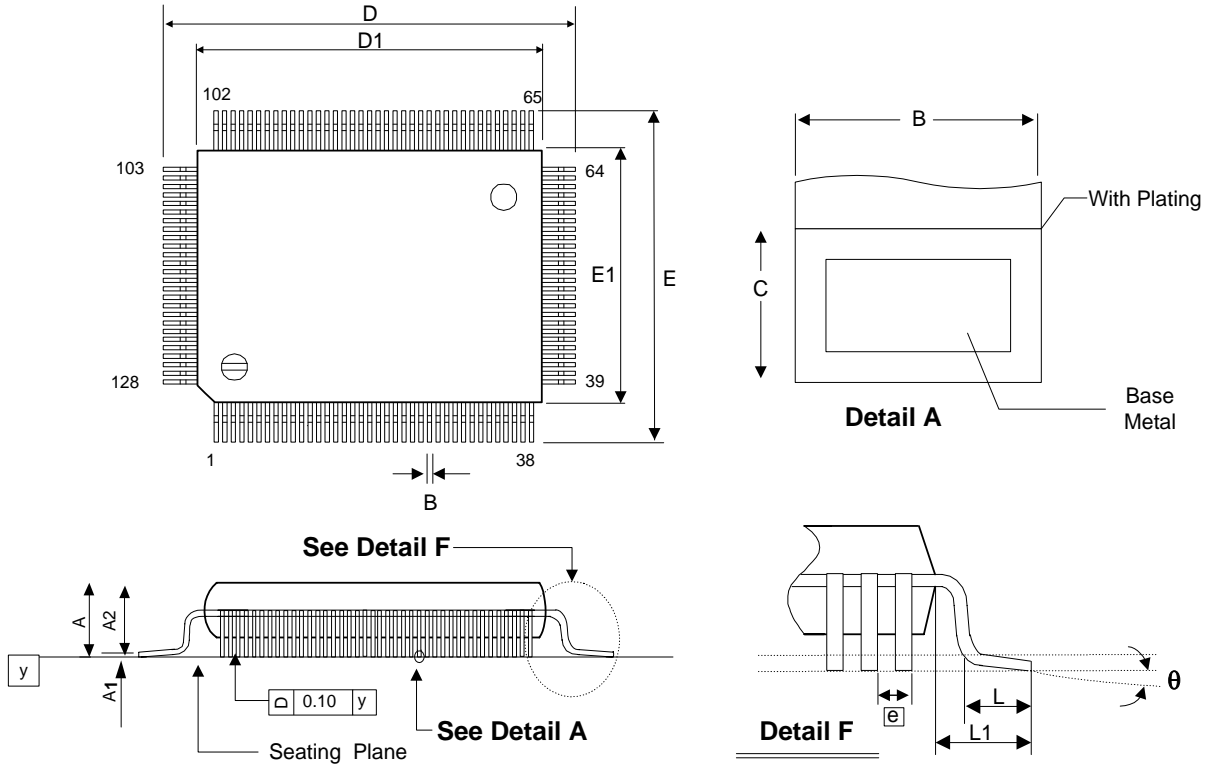

**DM6580 Performance**

(VDD= 5V, FQ= 20.16MHz, Measurement Band = 220Hz to 3.6KHz, RX DPLL Free Running)

| Symbol | Parameter                    | Min. | Typ. | Max. | Unit | Conditions                              |
|--------|------------------------------|------|------|------|------|---|
| Gabs   | Absolute Gain At 1KHz        | -0.5 |      | 0.5  | dB   | Rx signal: VIN= 2.5 VPP, f = 1KHz       |
| THD    | Total Harmonic Distortion    |      | -84  |      | dB   | Tx signal: VOUT (diff)= 5 VPP, f = 1KHz |
| DR     | Dynamic Range                |      | 86   |      | dB   | f = 1KHz                                |
| PSRR   | Power Supply Rejection Ratio |      | 50   |      | dB   | f = 1KHz, VAC = 200m VPP                |
| CTxRx  | Crosstalk                    |      | 95   |      | dB   | Transmit channel to receive channel     |

Package Information  
QFP 128L Outline Dimensions

Unit: Inches/mm



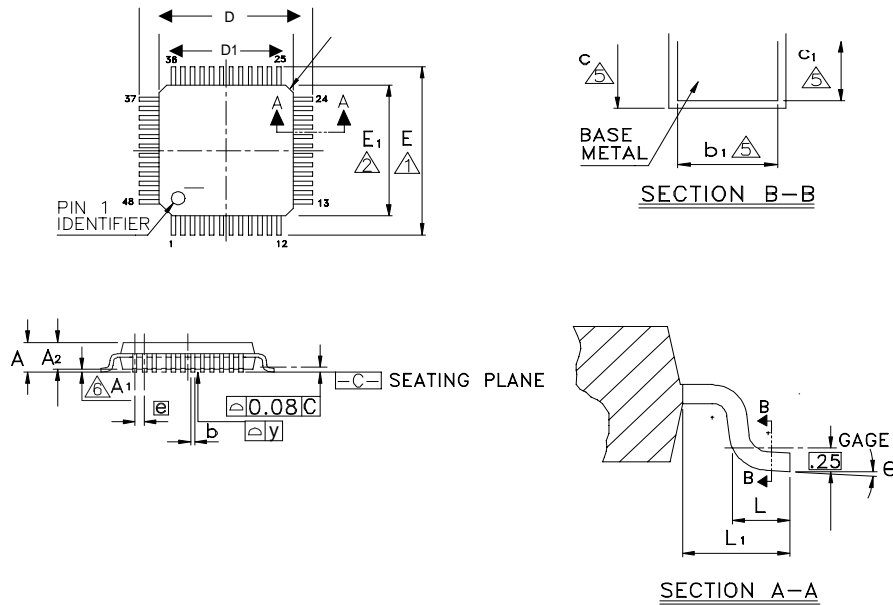
| Symbol       | Dimension In Inch | Dimension In mm   |
|--------------|-------------------|-------------------|
| A            | 0.134 Max.        | 3.40 Max.         |
| A1           | 0.010 Min.        | 0.25 Min.         |
| A2           | $0.112 \pm 0.005$ | $2.85 \pm 0.12$   |
| B            | $0.009 \pm 0.002$ | $0.22 \pm 0.05$   |
| C            | $0.006 \pm 0.002$ | $0.145 \pm 0.055$ |
| D            | $0.913 \pm 0.007$ | $23.20 \pm 0.20$  |
| D1           | $0.787 \pm 0.004$ | $20.00 \pm 0.10$  |
| E            | $0.677 \pm 0.008$ | $17.20 \pm 0.20$  |
| E1           | $0.551 \pm 0.004$ | $14.00 \pm 0.10$  |
| $\text{[e]}$ | 0.020 BSC         | 0.5 BSC           |
| L            | $0.035 \pm 0.006$ | $0.88 \pm 0.15$   |
| L1           | 0.063 BSC         | 1.60 BSC          |
| y            | 0.004 Max.        | 0.10 Max.         |
| θ            | 0°~12°            | 0°~12°            |

**Note:**

1. Dimension D1 and E1 do not include resin fins.
2. All dimensions are based on metric system.
3. General appearance spec. should base itself on final visual inspection spec.

## LQFP 48L (F.P. 2mm) Outline Dimensions

unit: inches/mm



| Symbol    | Dimensions in inches |       |       | Dimensions in mm |      |      |
|-----------|----------------------|-------|-------|------------------|------|------|
|           | Min.                 | Nom.  | Max.  | Min.             | Nom. | Max. |
| A         | -                    | -     | 0.063 | -                | -    | 1.60 |
| A1        | 0.002                | -     | 0.006 | 0.05             | -    | 0.15 |
| A2        | 0.053                | 0.055 | 0.057 | 1.35             | 1.40 | 1.45 |
| b         | 0.007                | 0.009 | 0.011 | 0.17             | 0.22 | 0.27 |
| b1        | 0.007                | 0.008 | 0.009 | 0.17             | 0.20 | 0.23 |
| C         | 0.004                | -     | 0.008 | 0.09             | -    | 0.20 |
| C1        | 0.004                | -     | 0.006 | 0.09             | -    | 0.16 |
| D         | 0.354BSC             |       |       | 9.00BSC          |      |      |
| D1        | 0.276BSC             |       |       | 7.00BSC          |      |      |
| E         | 0.354BSC             |       |       | 9.00BSC          |      |      |
| E1        | 0.276BSC             |       |       | 7.00BSC          |      |      |
| $\bar{e}$ | 0.020BSC             |       |       | 0.50BSC          |      |      |
| L         | 0.018                | 0.024 | 0.030 | 0.45             | 0.60 | 0.75 |
| L1        | 0.039REF             |       |       | 1.00REF          |      |      |
| y         | 0.003MAX             |       |       | 0.08MAX          |      |      |
|           | 0-12°                |       |       | 0-12°            |      |      |

1. To be determined at seating plane.
2. Dimensions D1 and E1 do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimensions b does not include dam bar protrusion. Total in excess of the b dimension at maximum material condition. Dam bar cannot be located on the lower radius of the foot.
4. Exact shape of each corner is optional.
5. These dimensions apply to the flat section of the lead between 0.10mm and 0.25mm from the lead tip.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.
7. Controlling dimension: millimeter.
8. Reference documents: JEDEC MS-026, BBC.

### Notes:



# DM562AP

V.90 Integrated Data/ Fax/Voice/Speakerphone  
Modem Device Single Chip with Memory Built in

## Ordering Information

| Part Number | Pin Count | Package        |
|-------------|-----------|----------------|
| DM6580E     | 48        | LQFP           |
| DM6580EP    | 48        | LQFP(Pb -free) |
| DM6588AF    | 128       | QFP            |
| DM6588AFP   | 128       | QFP(Pb -free)  |

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## Company Overview

DAVICOM Semiconductor, Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that are the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

## Products

We offer only products that satisfy high performance requirements and which are compatible with major hardware and software standards. Our currently available and soon to be released products are based on our proprietary designs and deliver high quality, high performance chipsets that comply with modem communication standards and Ethernet networking standards.

### WARNING

Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.