AKD4524

Evaluation board Rev.A for AK4524

General description

AKD4524 is an evaluation board for 24bit high performance codec, AK4524. A/D converter and D/A converter can be evaluated separately in addition to loopback mode(A/D → D/A). The A/D section can be evaluated by interfacing with AKM's DAC evaluation boards(AKD4319, AKD4320, AKD4321 and AKD4324) directly. The AKD4524 has the interface with AKM's wave generator using ROM data and AKM's ADC evaluation boards(AKD5391/2 and AKD5351/2). Therefore, it is easy to evaluate the D/A section. The AKD4524 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector. In case of access to internal register via serial I/F, software using printer port of PC is supplied.

■ Ordering guide

AKD4524 --- Evaluation board of AK4524
(Cable for connecting with printer port of IBM-AT, compatible PC and control software are packed with this.)

Function

- ☐ On-Board analog input buffer circuit
- ☐ On- Board analog output LPF circuit
- ☐ On-board clock generator
- ☐ Compatible with the following 2 types of interface
  - 1)Direct interface with AKM's A/D and D/A converter, direct interface with a signal generator(AKD43XX) by 10pin Header
  - 2)DIR/DIT with optical input/output
- ☐ A BNC connector for an external clock input
- ☐ 10pin Header for serial control mode

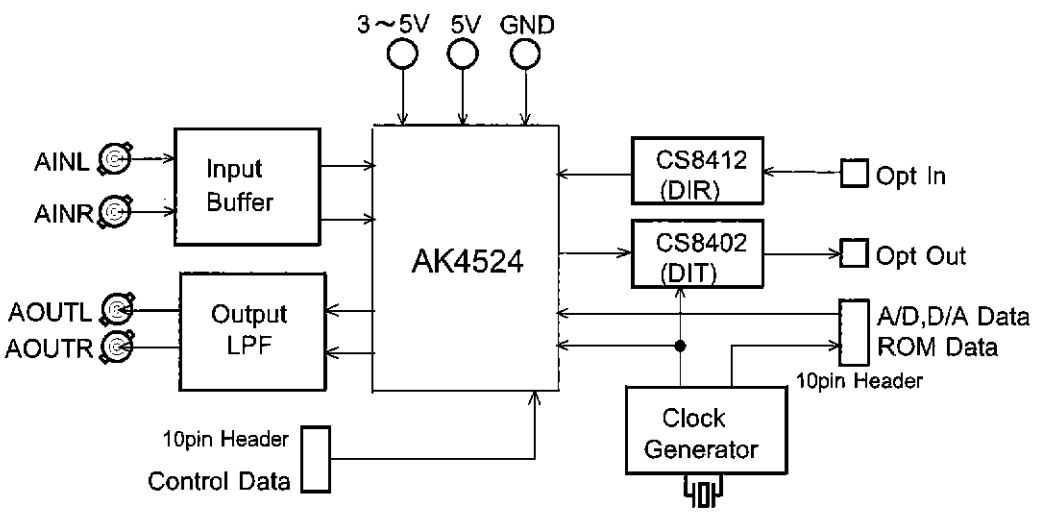
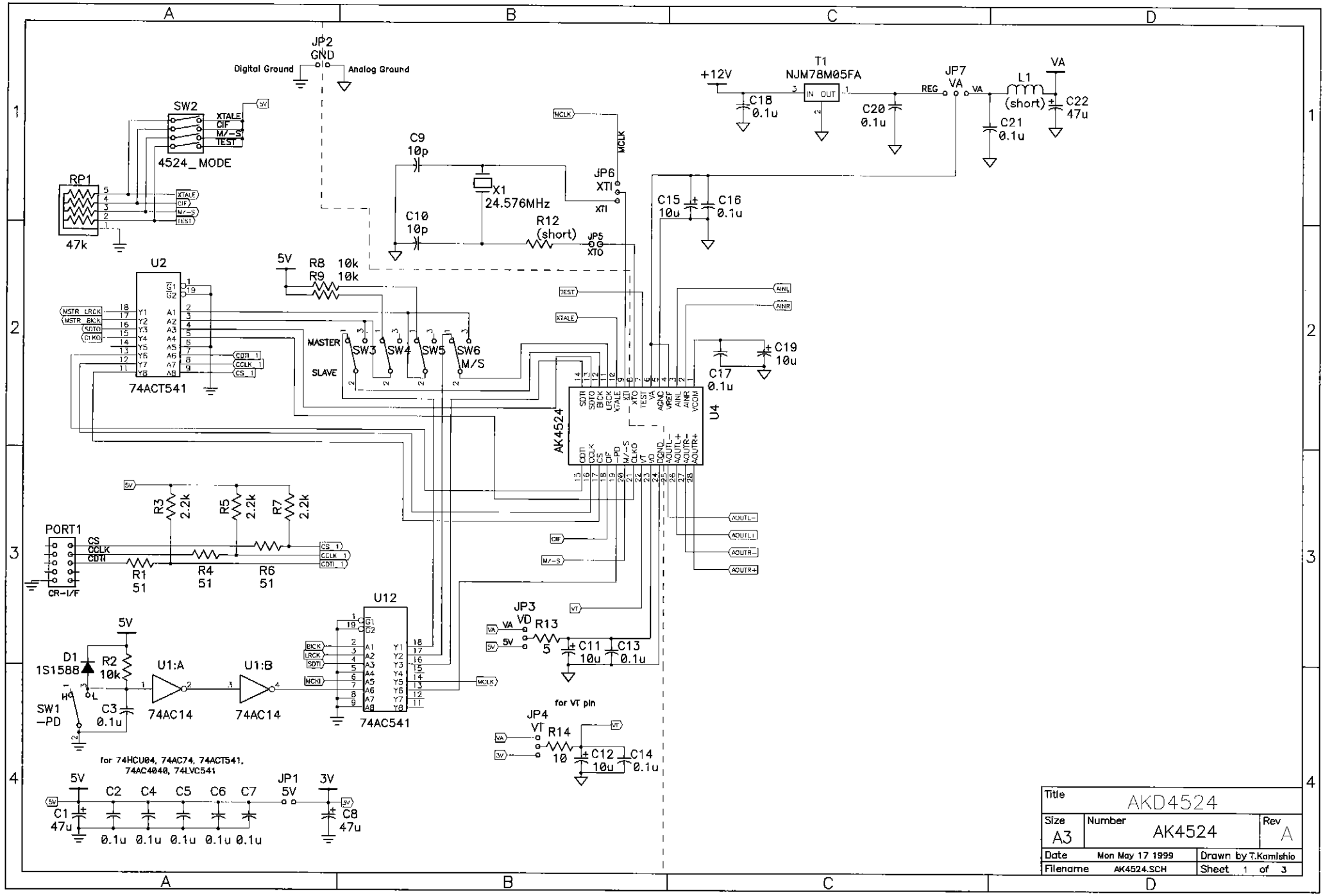
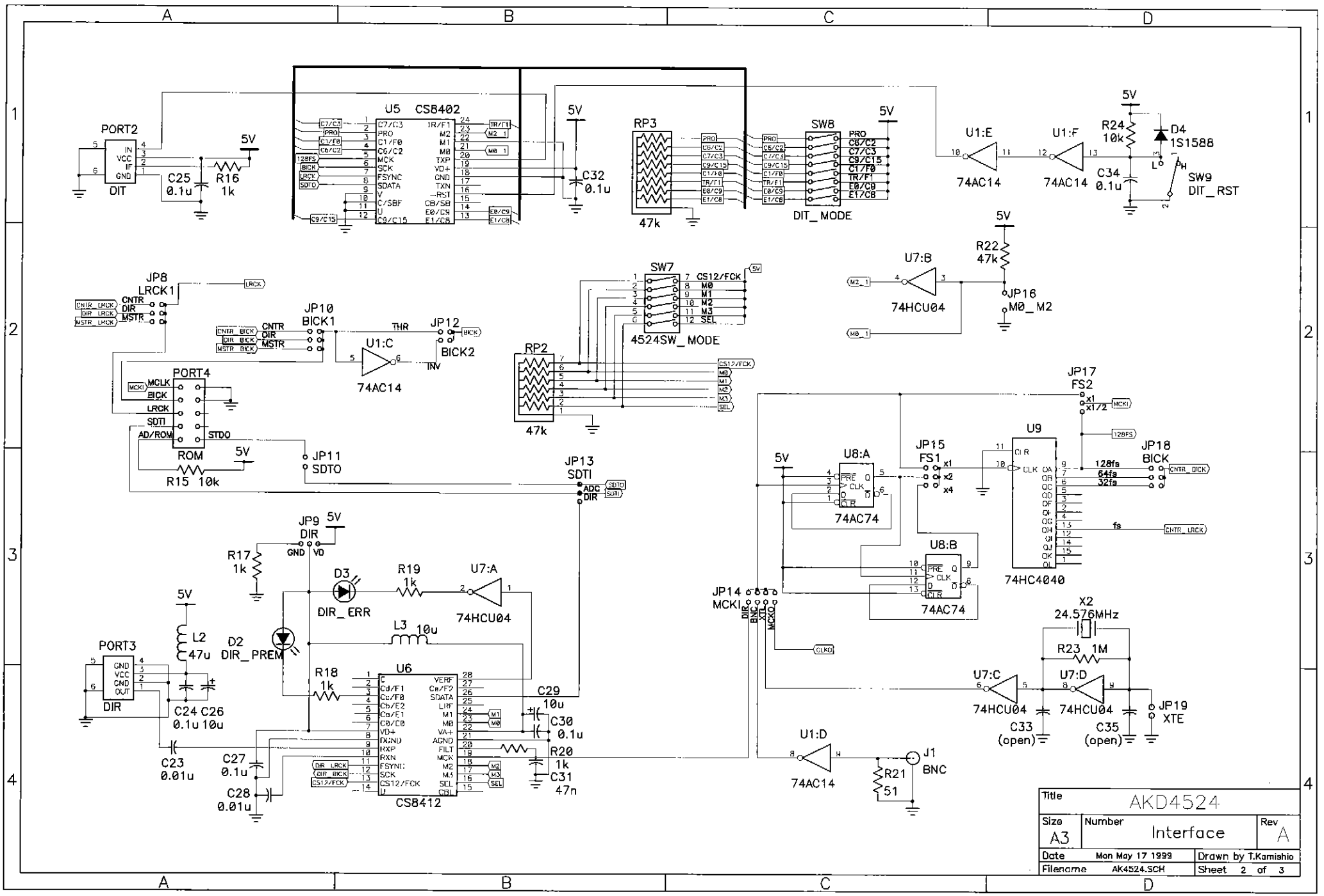
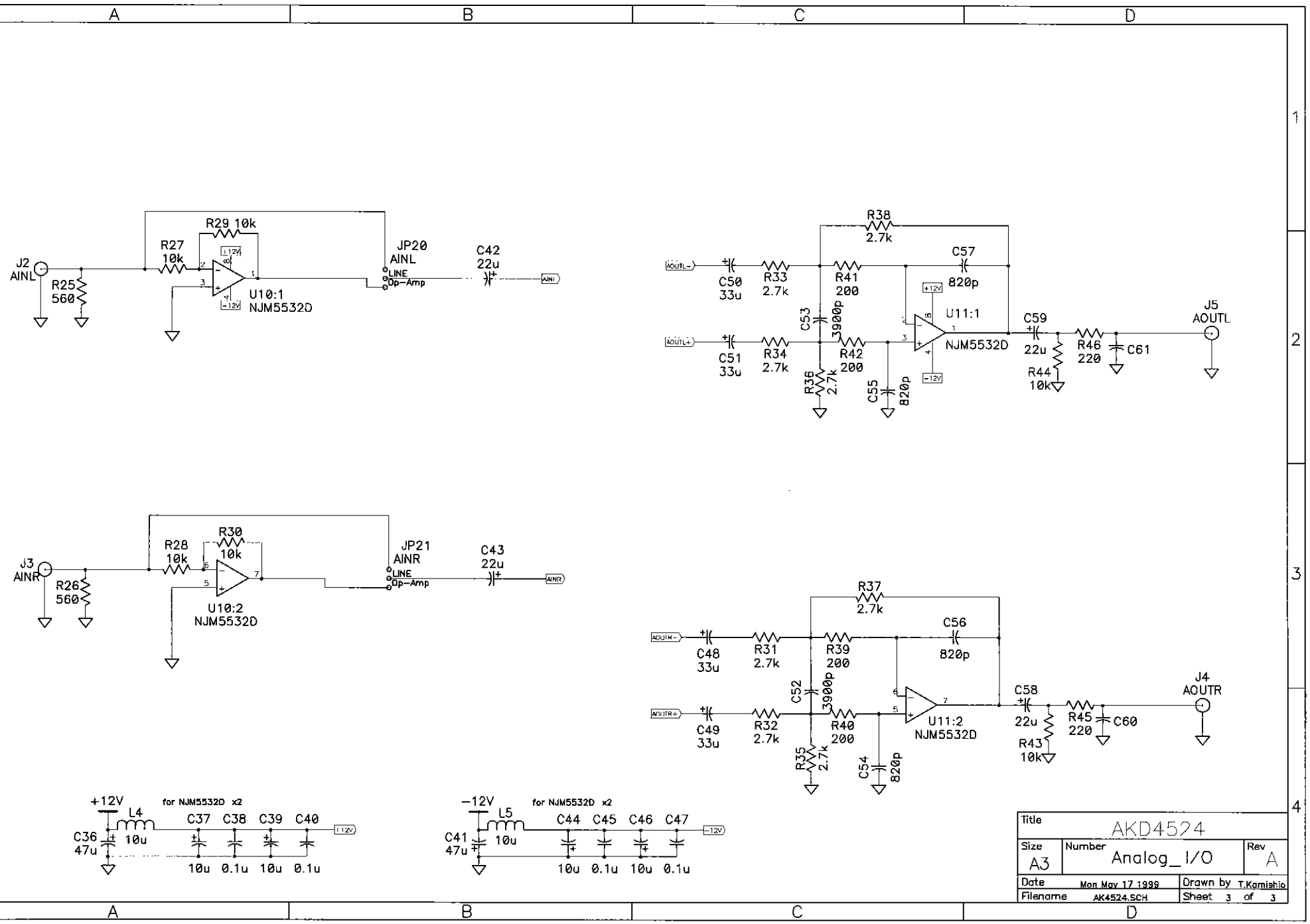


Figure 1. AKD4524 Block Diagram


JP2
GND
Digital Ground
Analog Ground
SW2
XTALE
CIF
M/-S
TEST
4524_MODE
RP1
47k
C9
10p
C10
10p
X1
24.576MHz
R12
(short)
JP6
XTI
JP5
XTO
MCLK
NCLK
+12V
T1
NJM78M05FA
IN
OUT
C18
0.1u
C20
0.1u
JP7
VA
REG
L1
(short)
C21
0.1u
C22
47u
C15
10u
C16
0.1u
5V
R8 10k
R9 10k
U2
74ACT541
MSTR_LRCK
MSTR_BICK
SDTO
CLKO
CDTI_1
CCLK_1
CS_1
MASTER
SLAVE
SW3
SW4
SW5
SW6
M/S
TEST
XTALE
AINL
AINR
C17
0.1u
C19
10u
U4
AK4524
SDTI
SDTO
BICK
LRCK
XTALE
XTI
XTO
TEST
VA
AGND
VREF
AINL
AINR
VCOM
CDTI
CCLK
CS
CIF
-PD
M/-S
CLKO
VT
VD
DGND
AOUTL-
AOUTL+
AOUTR-
AOUTR+
R3
2.2k
R5
2.2k
R7
2.2k
PORT1
CS
CCLK
CDTI
CR-I/F
R1
51
R4
51
R6
51
U12
74AC541
BICK
LRCK
SDTI
MCKI
JP3
VD
R13
5
C11
10u
C13
0.1u
D1
1S1588
R2
10k
SW1
-PD
C3
0.1u
U1:A
74AC14
U1:B
74AC14
for VT pin
JP4
VT
R14
10
C12
10u
C14
0.1u
for 74HCU04, 74AC74, 74ACT541,
74AC4040, 74LVC541
C1
47u
C2
C4
C5
C6
C7
0.1u
JP1
3V
C8
47u
Title
AKD4524
Size
A3
Number
AK4524
Rev
A
Date
Mon May 17 1999
Drawn by T.Kamishio
Filename
AK4524.SCH
Sheet
1
of
3


PORT2
DIT
C25 0.1u
R16 1k
5V
U5 CS8402
C32 0.1u
RP3
47k
SW8
DIT_MODE
U1:E
74AC14
U1:F
74AC14
R24 10k
D4 1S1588
C34 0.1u
SW9 DIT_RST
JP8 LRCK1
JP10 BICK1
JP12 BICK2
U1:C
74AC14
PORT4
ROM
R15 10k
JP11 SDTO
JP13 SDTI
SW7
4524SW_MODE
RP2
47k
U7:B
74HCU04
R22 47k
JP16 M0_M2
JP17 FS2
U9
74HC4040
JP18 BICK
JP15 FS1
U8:A
74AC74
U8:B
74AC74
JP14 MCKI
X2 24.576MHz
R23 1M
U7:C
74HCU04
U7:D
74HCU04
JP19 XTE
C33 (open)
C35 (open)
JP9 DIR
R17 1k
D3 DIR_ERR
R19 1k
U7:A
74HCU04
L3 10u
L2 47u
D2 DIR_PREM
PORT3
DIR
C24 C26 0.1u 10u
C23 0.01u
R18 1k
U6
CS8412
C27 0.1u
C28 0.01u
C29 10u
C30 0.1u
R20 1k
C31 47n
U1:D
74AC14
R21 51
J1 BNC
Title AKD4524
Size A3
Number Interface
Rev A
Date Mon May 17 1999
Drawn by T.Kamishio
Filename AK4524.SCH
Sheet 2 of 3


J2
AINL
R25
560
R27
10k
R29 10k
U10:1
NJM5532D
JP20
AINL
LINE
Op-Amp
C42
22u
AINL
J3
AINR
R26
560
R28
10k
R30
10k
U10:2
NJM5532D
JP21
AINR
LINE
Op-Amp
C43
22u
AINR
R38
2.7k
C57
820p
C50
33u
R33
2.7k
R41
200
C53
3900p
U11:1
NJM5532D
C59
22u
R46
220
C61
J5
AOUTL
C51
33u
R34
2.7k
R42
200
R36
2.7k
C55
820p
R44
10k
R37
2.7k
C56
820p
C48
33u
R31
2.7k
R39
200
C52
3900p
U11:2
NJM5532D
C58
22u
R45
220
C60
J4
AOUTR
C49
33u
R32
2.7k
R40
200
R35
2.7k
C54
820p
R43
10k
+12V
L4
10u
C36
47u
C37
C38
C39
C40
10u
0.1u
10u
0.1u
for NJM5532D x2
-12V
L5
10u
C41
47u
C44
C45
C46
C47
10u
0.1u
10u
0.1u
for NJM5532D x2
Title
AKD4524
Size
A3
Number
Analog_I/O
Rev
A
Date
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Drawn by
T.Kamishio
Filename
AK4524.SCH
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of
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■ Input Buffer Circuit

External analog signal fed through the BNC connector is terminated by a resistor of 560 ohms. The resistor value should be properly selected in order to meet the output impedance of the signal source.
The input buffer circuit of AINL and AINR include inverted-amp of gain 1, and the input buffer circuit can be selected by jumper pins(JP20 and JP21).

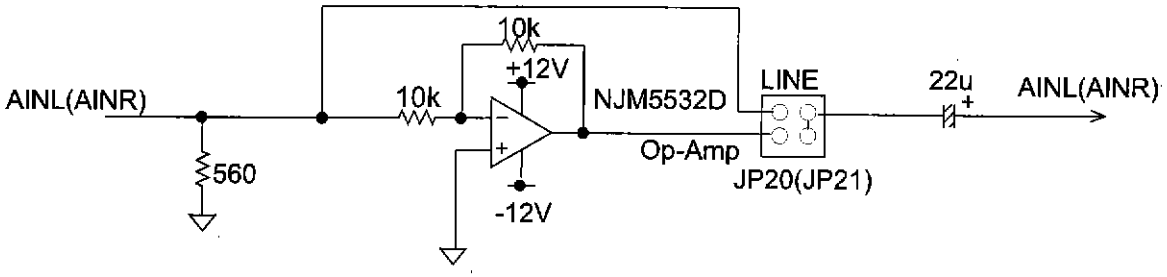


Figure 2. Input buffer circuit on board

※ AKM assumes no responsibility for the trouble when using the circuit examples.

■ Analog Output Circuit

The 2nd-order LPF(fc=85.6kHz, Q=0.731) which adds differential outputs of AK4524 is implemented on the board. When the further attenuation of the out-band noise is needed, some additional LPF is required. Analog signal is output through BNC connectors on the board, and the output level of AK4524 is about 5.6Vpp.

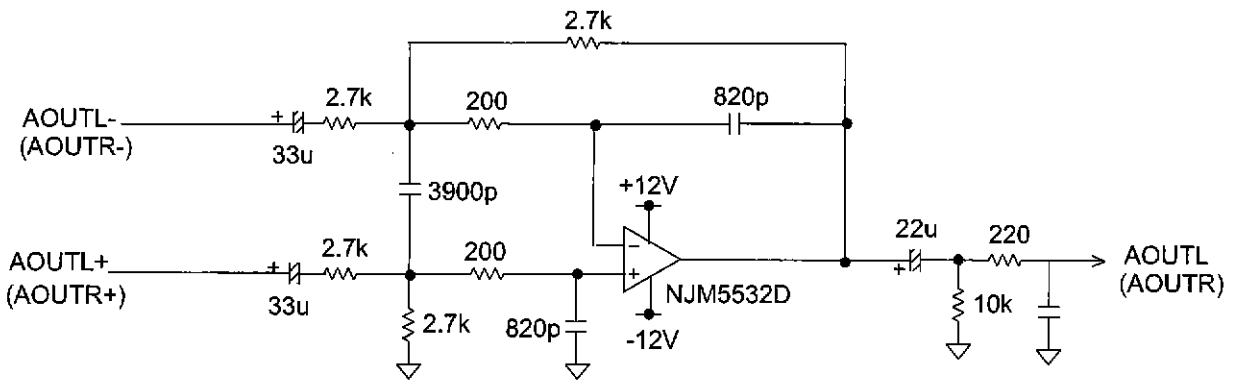


Figure 3. Anlog filter on board

※ AKM assumes no responsibility for the trouble when using the circuit examples.

■ Grounding and Power Supply Decoupling of AK4524

To minimize coupling by digital noise, decoupling capacitors should be connected to VA pin and VD pin, respectively. VA pin is supplied from analog supply in system, and VD pin is supplied from VA pin via 5 ohm resistor. Decoupling capacitors should be as near to the AK4524 as possible, with the small value ceramic capacitor being the nearest.

■ Voltage Reference Inputs of AK4524

The differential Voltage betw een VREF pin and AGND pin sets the analog input/output range. VREF pin is normally connected to VA pin with a 0.1uF ceramic capacitor. VCOM pin is a signal ground of this chip. An electrolytic capacitor 10uF parallel with a 0.1uF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4524.

■ Operation sequence

① **Set up the power supply lines.**

[VA]	(red)	= 4.75 ~ 5.25V
[3V]	(orange)	= 2.70 ~ 5.25V
[5V]	(red)	= 4.75 ~ 5.25V
[+12V]	(orange)	= 12 ~ 15V
[-12V]	(blue)	= -12 ~-15V
[AGND]	(black)	= 0V
[DGND]	(black)	= 0V

Each supply line should be distributed from the power supply unit.
VA should be powered at the same time or earlier than 5V.

② **Set up the evaluation modes and jumper pins.** (See p.7 ~)
There are many jumper pins to cover many evaluation mode. Please take care of setting.

③ **Set up the DIP-SW.** (See p.11 ~)
Set up the AK4524 and DIT. (Upper side is "ON" and lower side is "OFF".)
Please take care of setting.

④ **Power on.**
The AK4524 should be reset once bringing $\overline{PD}$ (SW1)"L" upon power-up.
Next, write "1" to control registers (RSTAD,RSTDA) from AKD4524 control software.

■ Evaluation modes and jumper pins

1. Evaluation Mode

Applicable Evaluation Mode

① Loopback mode (Default)
② Evaluation of D/A using ideal sine wave generated by ROM data.
③ Evaluation of D/A using A/D converted data
④ Evaluation of D/A using DIR(Optical Link)
⑤ Evaluation of A/D usingUsing D/A converted data
⑥ Evaluation of A/D DIT(Optical Link)
⑦ All interface signals including master clock are fed externally.

※① and ⑥ can be evaluated at the same time by the same set up.

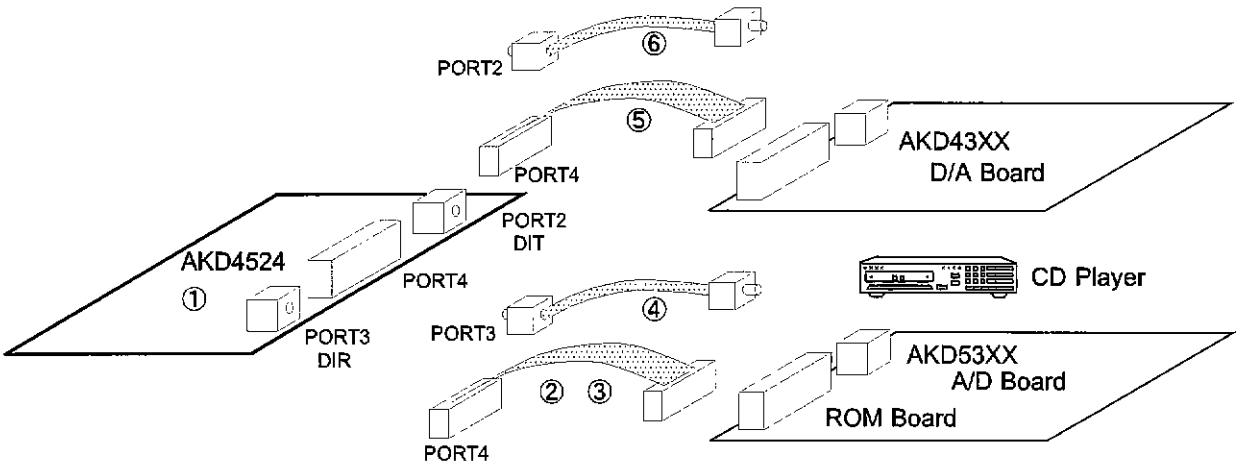


Figure 4. Wiring cables corresponded some evaluation modes

① **Loopback mode** (Default)

Nothing should be connected to PORT3/PORT4. Set-up of each jumper pins is as follows in slave mode and master mode. Though same set-up of each jumper pins for Normal speed and Double speed, please take care of setting master clock(see Table 2.). This mode doesn't correspond to 4times speed.

a. BICK=32fs corresponds to only Mode 0 of Audio Format.

b. BICK=64fs corresponds to only Mode2/Mode3 of Audio Format.

(1) Case of supplying master clock from X1

1) Set-up jumper pins (slave mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKI	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	short	XTI	CNTR	GND	CNTR	ADC	MCKO	short

2) Set-up jumper pins (master mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKI	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	short	XTI	MSTR	GND	MSTR	ADC	MCKO	short

(2) Case of supplying master clock from X2

3) Set-up jumper pins (slave mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKI	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	open	MCLK	CNTR	GND	CNTR	ADC	XTL	open

4) Set-up jumper pins (master mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKI	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	open	MCLK	MSTR	GND	MSTR	ADC	XTL	open

② **Evaluation of D/A using A/D converted data from ideal sine wave generated by ROM data**

Digital signals generated by AKD43XX are used. PORT4 is used for the interface with AKD43XX. Master clock is sent from AKD4524 to AKD43XX and BICK, LRCK, SDTI are sent from AKD43XX to AKD4524. Nothing should be connected to PORT3. Please set-up slave mode(see Table 1.). Though same set-up of each jumper pins for Normal speed and Double speed and 4 times speed, please take care of setting master clock(see Table 2.).

(1) Case of supplying master clock from X1

5) Set-up jumper pins (slave mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKI	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	short	XTI	open	GND	open	open	MCKO	short

(2) Case of supplying master clock from X2

6) Set-up jumper pins (slave mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKI	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	open	MCLK	open	GND	open	open	XTL	open

③ **Evaluation of D/A using A/D converted data**

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's A/D evaluation boards (AKD5391/2, AKD5352/1) with PORT4. Nothing should be connected to PORT3. Set slave mode (see Table 1.).

7) Set-up jumper pins (slave mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKI	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	open	MCLK	open	GND	open	open	XTL	short

④ **Evaluation of D/A using DIR (Optical Link)**

PORT3 is used. DIR generates MCLK, BICK, LRCK and SDATA from the received data through optical connector(TORX174). Used for the evaluation using CD test disk. Nothing should be connected to PORT2/PORT4. CS8412(DIR) needs the operating voltage of VD+≧ 3.4V. Set slave mode (see Table 1.). This mode corresponds to only Normal speed.

8) Set-up jumper pins (slave mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKI	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	open	MCLK	DIR	VD	DIR	DIR	DIR	short

See SW7 and JP12(BICK2) for set-up of DIR.

⑤ **Evaluation of A/D using D/A converted data**

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's D/A evaluation boards (AKD4319, AKD4320 AKD4321 and AKD4324) with PORT4. Nothing should be connected to PORT3. Set-up of each jumper pins is as follows in slave mode and master mode. Though same set-up of each jumper pins for Normal speed and Double speed, please take care of setting master clock(see Table 2.). This mode doesn't correspond to 4times speed.

(1) Case of supplying master clock from X1

9) Set-up jumper pins (slave mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKI	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	short	XTI	CNTR	GND	CNTR	ADC	MCKO	short

10) Set-up jumper pins (master mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKO	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	short	XTI	MSTR	GND	MSTR	ADC	MCKO	short

(2) Case of supplying master clock from X2

11) Set-up jumper pins (slave mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKO	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	open	MCLK	CNTR	GND	CNTR	ADC	XTL	open

12) Set-up jumper pins (master mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKO	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	open	MCLK	MSTR	GND	MSTR	ADC	XTL	open

⑥ **Evaluation of A/D using DIT (Optical Link)**

PORT2 is used. DIT generates SDATA from received data and which is output through optical connector (TOTX174). It is possible to connect AKM's evaluation boards (AKD4319, AKD4320, AKD4321 and AKD4324), digital-amplifier and etc. Nothing should be connected to PORT3/PORT4. This set-up is same as that of ①. CS8402(DIT) needs the operating voltage of VD+≧ 3.4V. SW9 should be kept "H" during normal operation. Set-up of each jumper pins is as follows. Slave mode corresponds to I2S. In this case, JP12(BICK2) is THR, and JP16(M0_M2) is short. Master mode corresponds to MSB justified and I2S. In MSB justified, JP12(BICK2) is INV, and JP16(M0_M2) is open. In I2S, JP12(BICK2) is THR, and JP16(M0_M2) is short. This mode corresponds to only Normal speed.

(1) Case of supplying master clock from X1

13) Set-up jumper pins (slave mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKI	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	short	XTI	CNTR	GND	CNTR	ADC	MCKO	short

14) Set-up jumper pins (master mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKO	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
set-up	short	XTI	MSTR	GND	MSTR	ADC	MCKO	short

(2) Case of supplying master clock from X2

15) Set-up jumper pins (slave mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKO	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	open	MCLK	CNTR	GND	CNTR	ADC	XTL	open

16) Set-up jumper pins (master mode)

Name	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKI	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	open	MCLK	MSTR	GND	MSTR	ADC	XTL	open

⑦ **All interfacing signals including master clock are fed externally.**

Under the following set-up, all external signals needed for the AK4524 to operate could be fed through PORT4. Set slave mode (see Table 1.).

17) Set-up jumper pins (slave mode)

Namme	XTO	XTI	LRCK1	DIR	BICK1	SDTI	MCKO	XTE
Jumper	JP5	JP6	JP8	JP9	JP10	JP13	JP14	JP19
Set-up	open	MCLK	open	GND	open	open	open	short

2. BICK set-up

BICK can be selected 32fs or 64fs or 128fs by JP18(BICK). In master mode, set 64fs. BICK is 64fs at default.

3. Other jumpers set-up

[JP1] Short 5V and 3V.
In case of separating 5V and 3V supplies, JP1 should be open.
[JP2] Short DGND and AGND.
In case of separating DGND and AGND, JP2 should be open.
[JP3, JP4] Select VA(5V) or 5V.
[JP7] Select of analog supply of VA pin for AK4524.
VA : Supply from VA terminal.
REG : Supply from 3-terminal regulator.
[JP11] Always open.

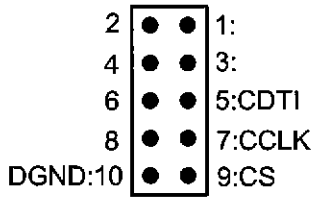
4. Interface circuit for control registers

The control registers in the AK4524 can be controlled by external uP, printer port of PC via PORT1(10pin-Header).

① In case of using printer port for PC

The control registers can be controlled by connecting between PORT1 on the AKD4524 and printer-port of personal computer by using a special cable(10pin-Header - 25pin D-Sub).

The following figure is pin-assignment of 10pin-Header. Please take care of connecting a cable as thre is a sign indicating 1-pin connecter.



■ Master / Slave mode set-up

Table 1. Master/Slave set-up

	Master mode	Slave mode
SW2-3(M/-S)	ON	OFF
SW3,4,5,6	Master	Slave

■ Master clock set-up

Table 2. Master clock set-up

MCLK	Normal speed	JP15	JP17
256fsn	256fsn	x1	x1
512fsn	512fsn	x2	x1
1024fsn	1024fsn	x4	x1

MCLK	Double speed	JP15	JP17
512fsn	256fsn	x1	x1
1024fsn	512fsn	x2	x1

MCLK	4 times speed	JP15	JP17
512fsn	128fsn	x1	x1/2
1024fsn	256fsn	x1	x1

■ The function of the toggle SW.

[SW1] Reset the AK4524. Keep "H" during normal operation.
[SW9] Reset the CS8402. "L" resets the internal counter of CS8402, then Bi-phase signal is not output. Keep "H" during normal operation.(Upper-side is "H" and lower-side is "L".)

■ The indication content for LED.

[D2] Indicate whether the input data of CS8412 is pre-emphasized or not. LED turns on when the data is pre-emphasized.
[D3] Monitor VERF pin of the CS8412. LED turns on when some error has occurred to CS8412.

■ DIP switch and Jumpers set-up

1. SW2 : This switch sets up the operation mode of the AK4524.

Table 3. DIP switch set-up for AK4524

No.	PIN	ON	OFF
4	XTALE	Enable	Disable
3	CIF	CS falling trigger	CS rising trigger
2	M/-S	Master mode	Slave mode
1	TEST	Don't use	Normally ON

2. SW7 : This switch sets up the operation mode of the CS8412(DIR).

No.	PIN	ON	OFF	
1	CS12	Rch	Lch	*1
2	M0	See Table 4.		
3	M1			
4	M2			
5	M3			
6	SEL	Normally ON *2		

*1 : D2 turns on when CS12 is "ON".
*2 : Selectiotn of channel indicating channel status.

Table 4. Set-up CS8412

Mode	AK4524's DIF2	AK4524's DIF1	AK4524's DIF0	AK4524's SDTI	SW7-5 M3	SW7-4 M2	SW7-3 M1	SW7-2 M0	JP12 BICK2
0	0	0	0	16bit LSB	0	1	0	1	THR
1	0	0	1	20bit LSB	—	—	—	—	—
2	0	1	0	24bit MSB	0	0	0	0	INV
3	0	1	1	24bit I2S	0	0	1	0	THR
4	1	0	0	24bit LSB	—	—	—	—	—

DIF2, DIF1, DIF0 are changed internal registers of AK4524.
CS8412 doesn't corresponds to Mode1/Mode4.

3. SW4 : This switch sets the C-bit of CS8402. (Default is the consumer mode)
This set-up does not affect the evaluation of the AK4524. In case of using DIT, need to set it up correctly. For more detailed configurations, please refer to the CS8402 data-sheet.

Table 5. DIP switch set-up of CS8402 (Professional mode)

Switch	OFF=0,ON=1	Contents
1	$\overline{\text{PRO}}$=0	Professional mode, C0=1
2,3	$\overline{\text{C6}}$,$\overline{\text{C7}}$	C6,C7 - Sampling frequency
	1 1	00 - Not indicated. Receiver default to 48kHz.
	1 0	01 - 48kHz
	0 1	10 - 44.1kHz
	0 0	11 - 32kHz
4	$\overline{\text{C9}}$	C8,C9,C10,C11 - 1bit of channel mode
	1	0000 - Mode not indicated. Receiver default to
	0	2-channel mode.
		0100 - Stereophonic.
5	$\overline{\text{C1}}$	C1 - Audio mode
	1	0 - Normal audio
	0	1 - Non-audio
6	TRNPT	Transparent mode * CS8402 is CRE
	0	Normal mode
	1	Transparent mode
8,7	EM1,EM0	C2,C3,C4 - Encoded audio signal emphasis
	1 1	000 - Emphasis not indicated. Receiver defaults to no
	1 0	emphasis with manual override enabled.
	0 1	100 - None
	0 0	110 - 50/15usec
		111 - CCITT J.17

Table 6. DIP switch set-up of CS8402 (Consumer mode)

Switch	OFF=0,ON=1	Contents
1	$\overline{PRO}$=1	Consumer mode, C0=0 (Default)
2	$\overline{C2}$	C2 - Copy
Default	1 0	0 - Copy inhibited 1 - Copy permitted
3	$\overline{C3}$	C3,C4,C5 - Pre-emphasis
Default	1 0	000 - None 100 - 50/15usec
4	$\overline{C15}$	C15 - Generation Status
Default	1 0	0 - See the standard 1 - See the standard
6,5	FC1,FC0	C24,C25,C26,C27- Sampling frequency
Default	0 0 0 1 1 0 1 1	0000 - 44.1kHz 0100 - 48kHz 1100 - 32kHz 0000 - 44.1kHz, CD mode
8,7	$\overline{C8}$,$\overline{C9}$	C8-C14 - Category code
Default	1 1 1 0 0 1 0 0	0000000 - General 0100000 - PCM encoder/decoder 1000000 - CD 1100000 - DAT

AK4524 Measurement Results

■ No.1 (ROHDE & SCHWARZ UPD04)

[Measurement condition]

- Measurement unit : ROHDE & SCHWARZ UPD04 (RMS mode)
- MCLK : 256fsn (Normal speed) , 512fsn (Double speed)
- BICK : 64fs
- Bit : 24bit
- Measurement band width: 20 ~ 20kHz (Normal speed) , 40 ~ 40kHz (Double speed)
- fs : 44.1kHz (Normal speed) , 96kHz (Double speed)
- Power Supply : VA=VD=5.0V, VT=3.0V
- Mode : EXT clock mode, slave mode
- Interface : DIT/DIR/Serial
- temp : Room temp

1. fs=44.1kHz

a. ADC

	Input signal	Additional Filter	A/D Output
S/ (N+D)	1kHz, -0.5dB		89.4 dB
D-Range	1kHz, -60dB	A-weight	101.5 dB
S/N	1kHz, 0dB/"0"data IN	A-weight	101.8 dB

b. DAC

	Input signal	Measurement Filter	D/A Output
S/ (N+D)	1kHz, 0dB	20kHzLPF	94.9 dB
D-Range	1kHz, -60dB	20kHzLPF + A-weight	111.3 dB
S/N	1kHz, 0dB/"0"data IN	20kHzLPF + A-weight	111.5 dB

2. fs=96kHz

a. ADC

	Input signal	Additional Filter	A/D Output
S/ (N+D)	1kHz, -0.5dB	—	86.3 dB
D-Range	1kHz, -60dB	—	95.4 dB
S/N	1kHz, 0dB/"0" data IN	—	96.5 dB

b. DAC

	Input signal	Measurement Filter	D/A Output
S/ (N+D)	1kHz, 0dB	40kHzLPF	91.2 dB
D-Range	1kHz, -60dB	40kHzLPF	105.1 dB
S/N	1kHz, 0dB/"0"data IN	40kHzLPF	105.3 dB

■ No.2 (Audio Precision, System Two)

[Measurement condition]

- Measurement unit : Audio Precision, System Two (RMS mode)
- MCLK : 256fs
- BICK : 64fs
- Bit : 24bit
- Measurement band width: 20 ~ 20kHz
- fs : 44.1kHz
- Power Supply : VA=VD=5.0V, VT=3.0V
- Mode : EXT clock mode, slave mode
- Interface : DIT/DIR
- temp : Room temp

1. fs=44.1kHz

a. ADC

	Input signal	Additional Filter	A/D Output
S/ (N+D)	1kHz, -0.5dB		91.3 dB
D-Range	1kHz, -60dB	A-weight	101.0 dB
S/N	1kHz, 0dB/"0"data IN	A-weight	101.3 dB

b. DAC

	Input signal	Measurement Filter	D/A Output
S/ (N+D)	1kHz, 0dB	20kHzLPF	96.3 dB
D-Range	1kHz, -60dB	22kHzLPF + A-weight	110.8 dB
S/N	1kHz, 0dB/"0"data IN	22kHzLPF + A-weight	111.0 dB

1. ADC Graph

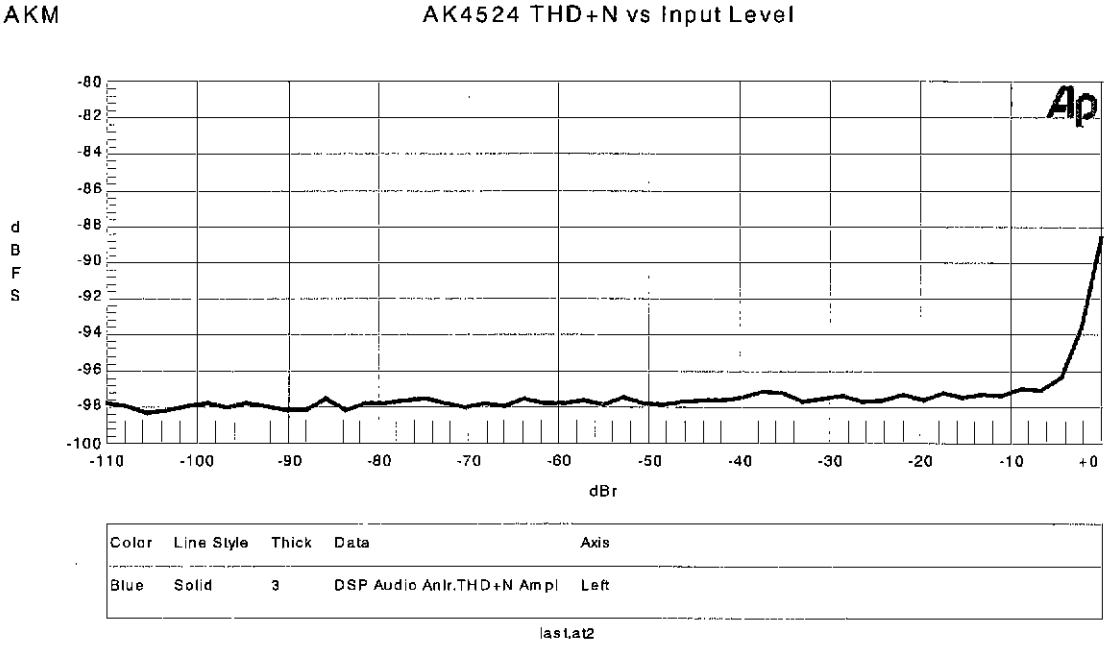


Fig1 : THD + N vs Input level

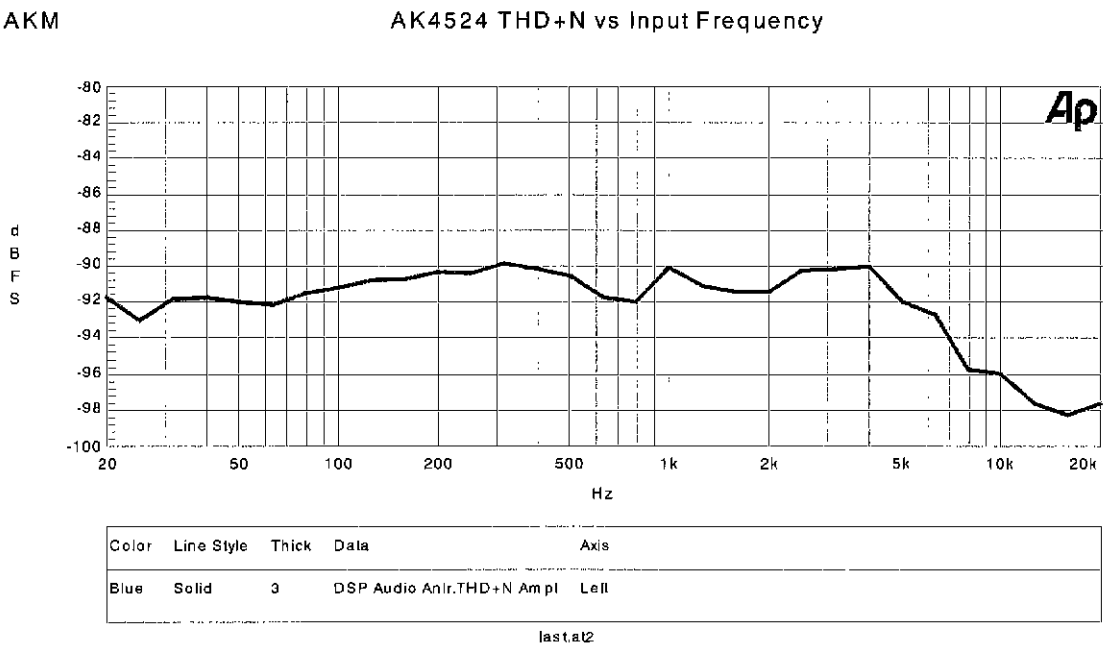


Fig2 : THD + N vs Frequency

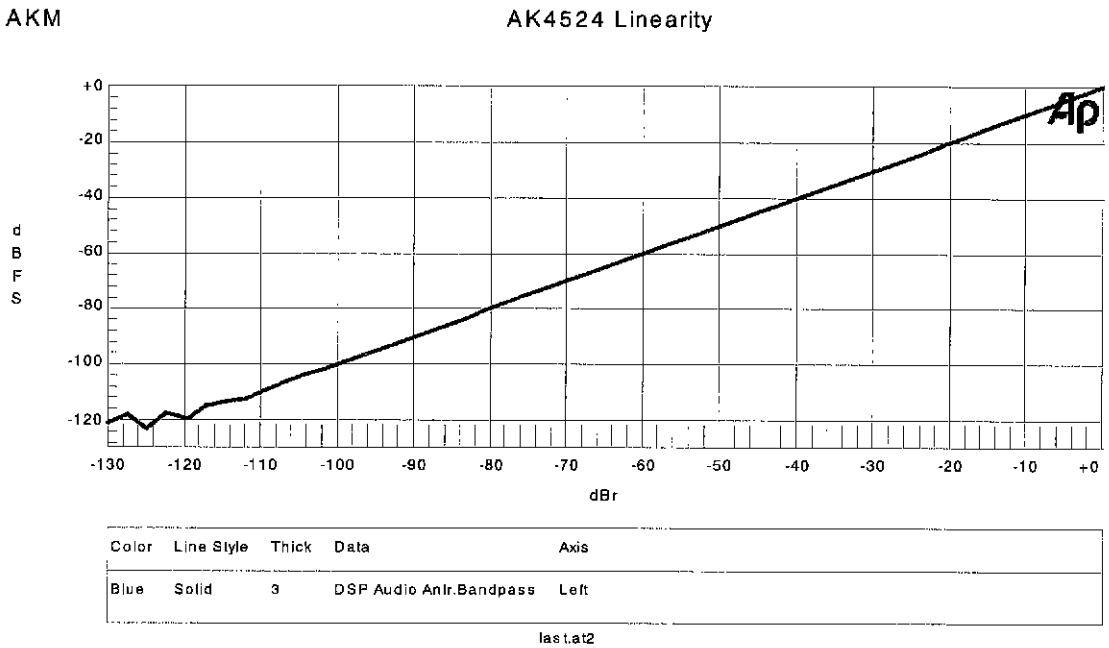


Fig3 : Linearity

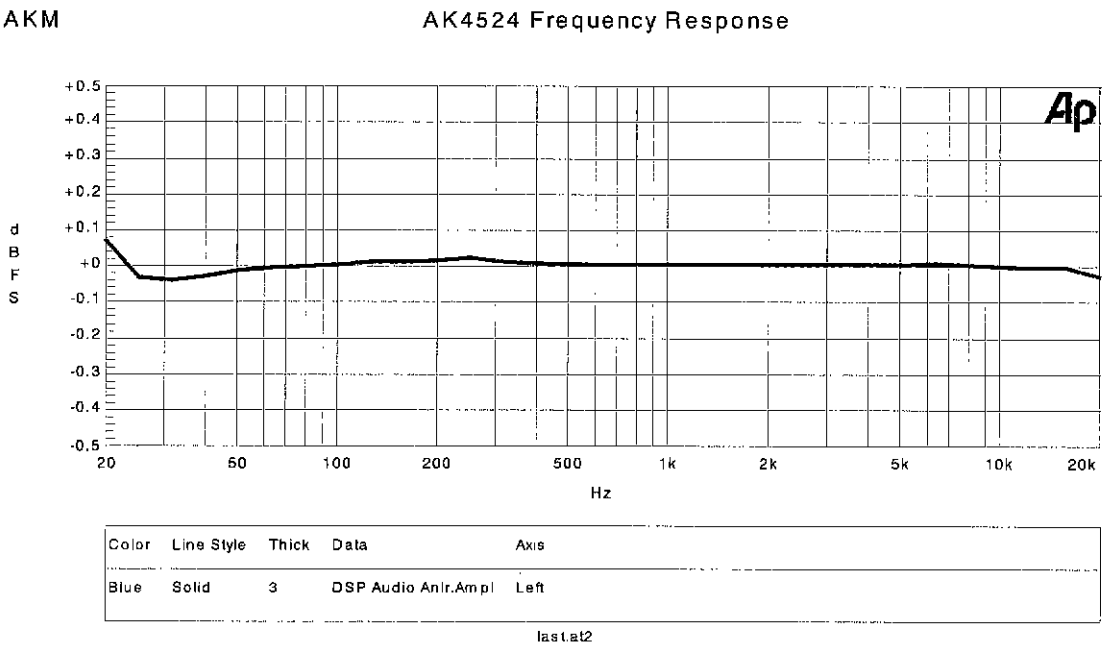
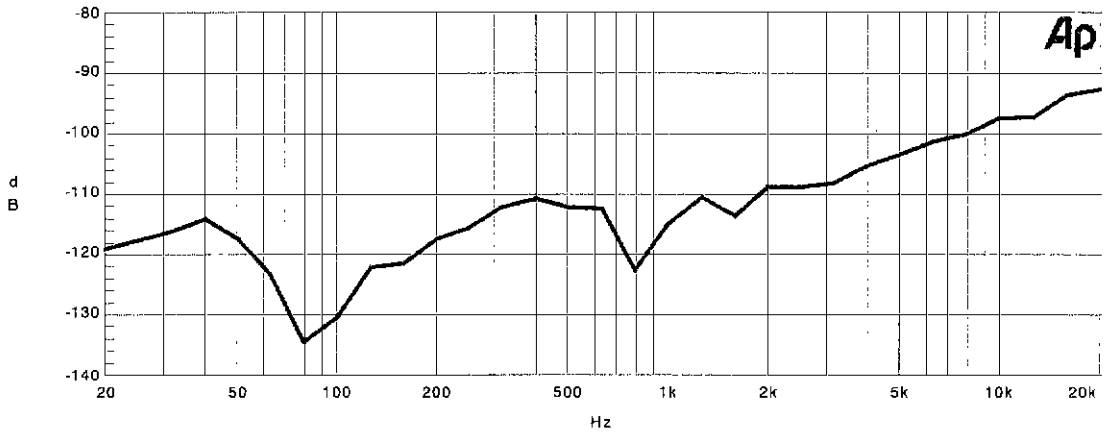


Fig4 : Frequency Response

AKM

AK4524 Crosstalk



Color	Line Style	Thick	Data	Axis
Blue	Solid	3	DSP Audio Anlr.Crosstalk	Left

last.at2

Fig5 : Crosstalk

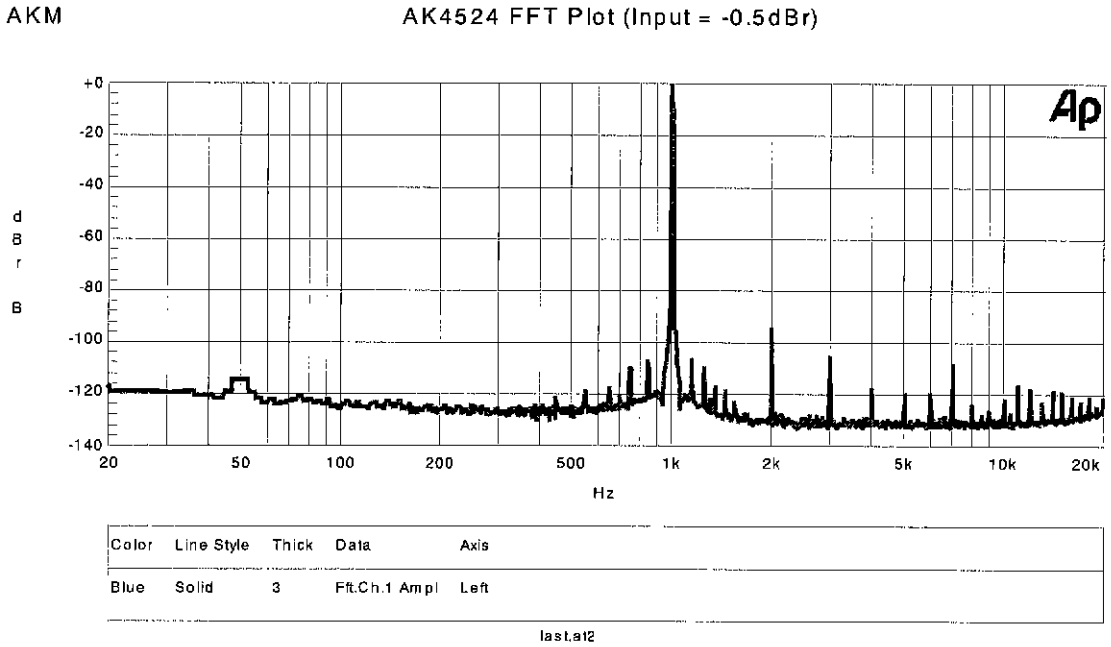


Fig6 : FFT Plot (Input = -0.5dBr)

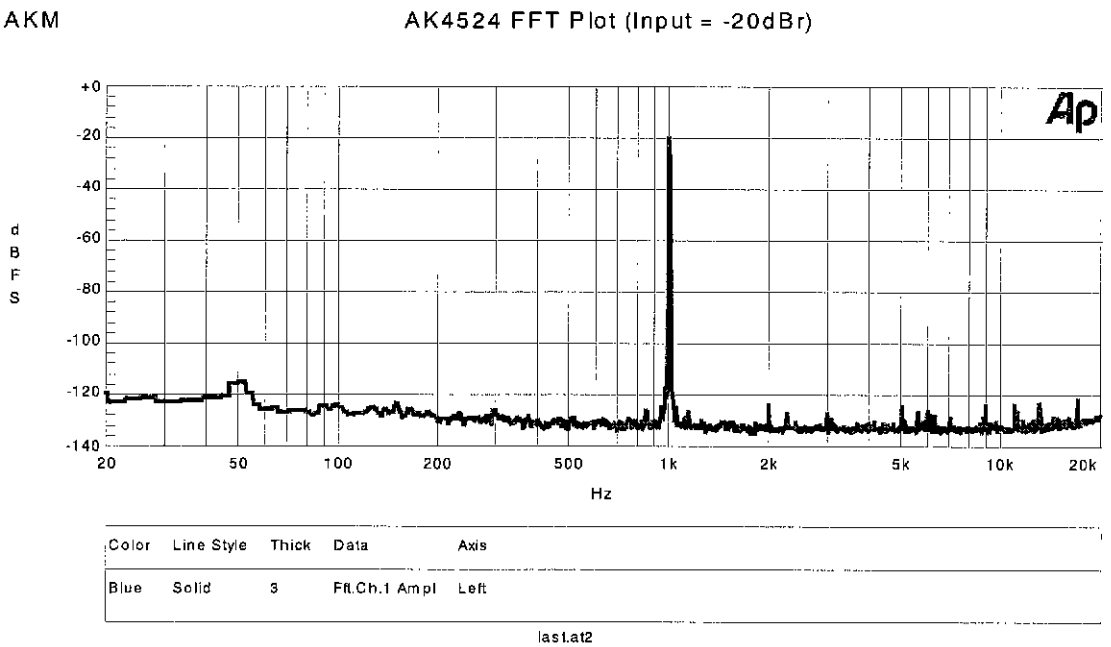


Fig7 : FFT Plot (Input = -20dBr)

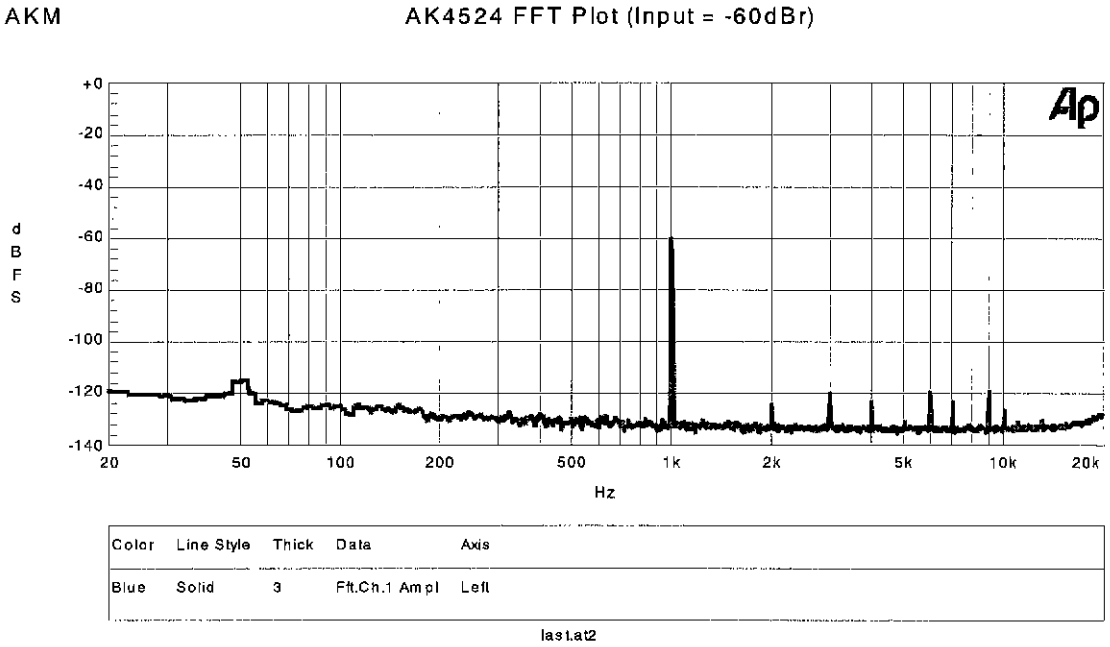


Fig8 : FFT Plot (Input = -60dBr)

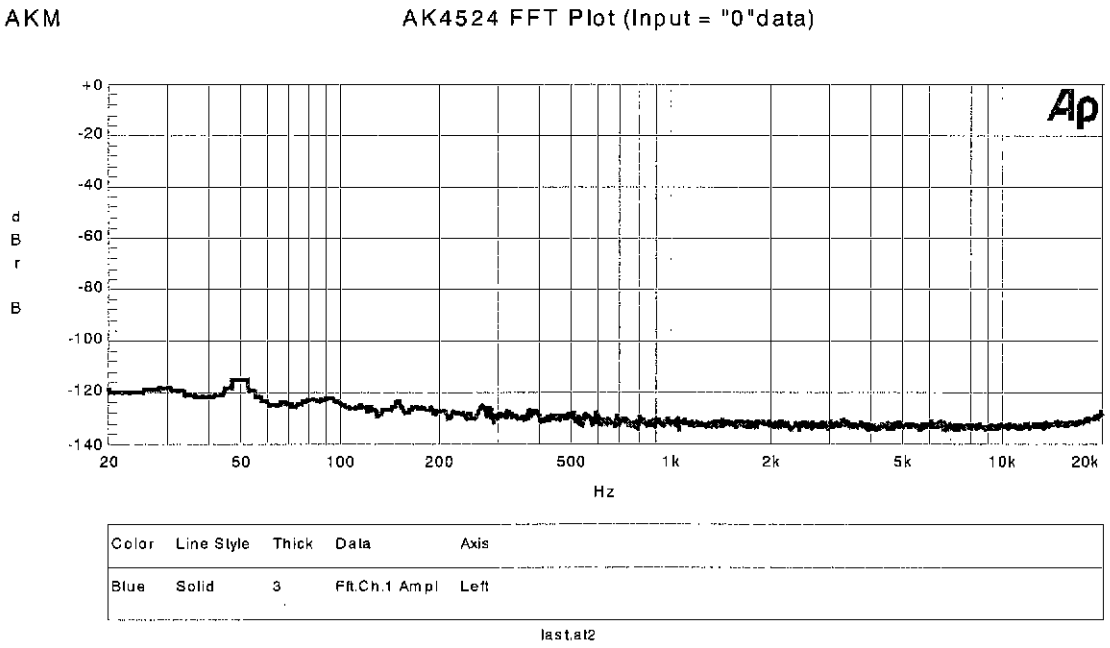


Fig9 : FFT Plot (Input = "0" data)

2. DAC Graph

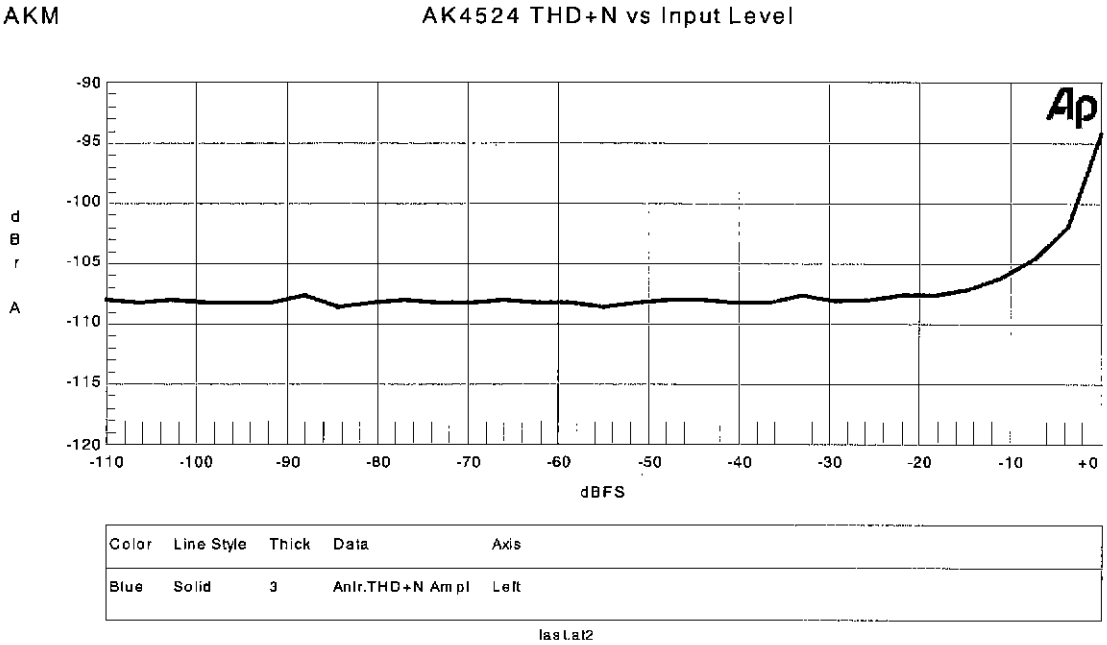


Fig10 : THD + N vs Input level

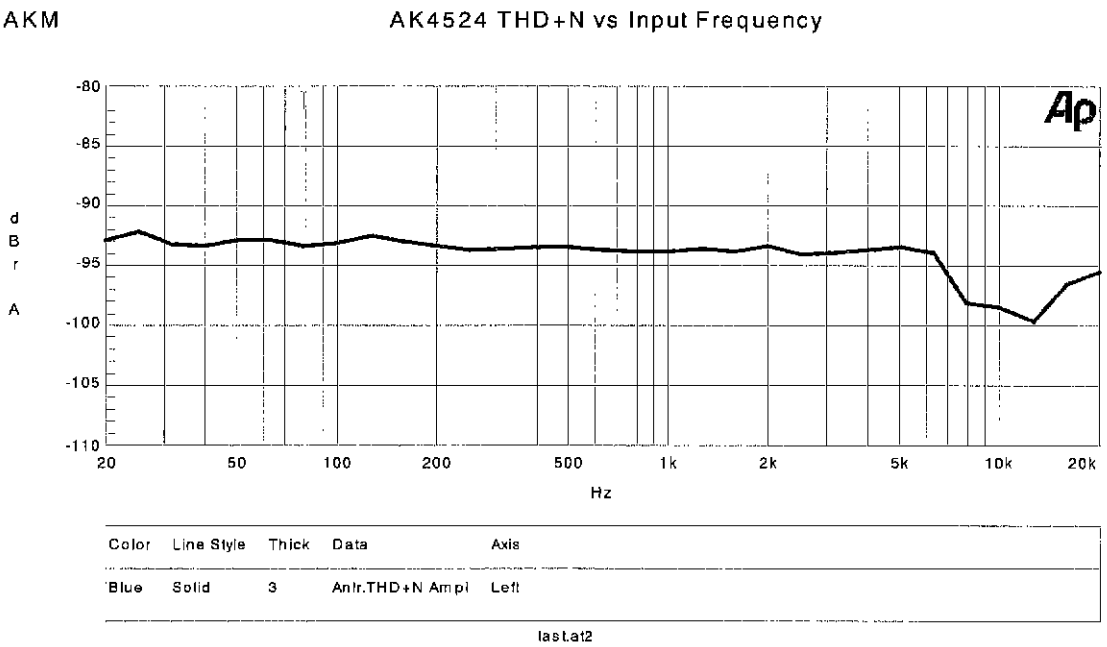


Fig11 : THD + N vs Frequency

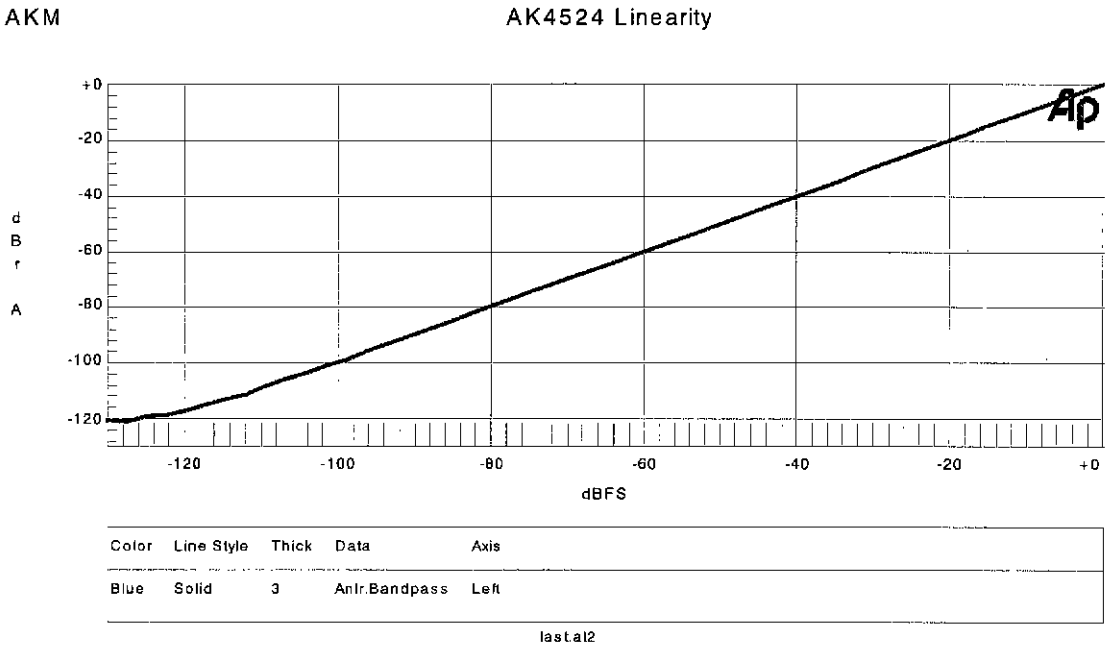


Fig12 : Linearity

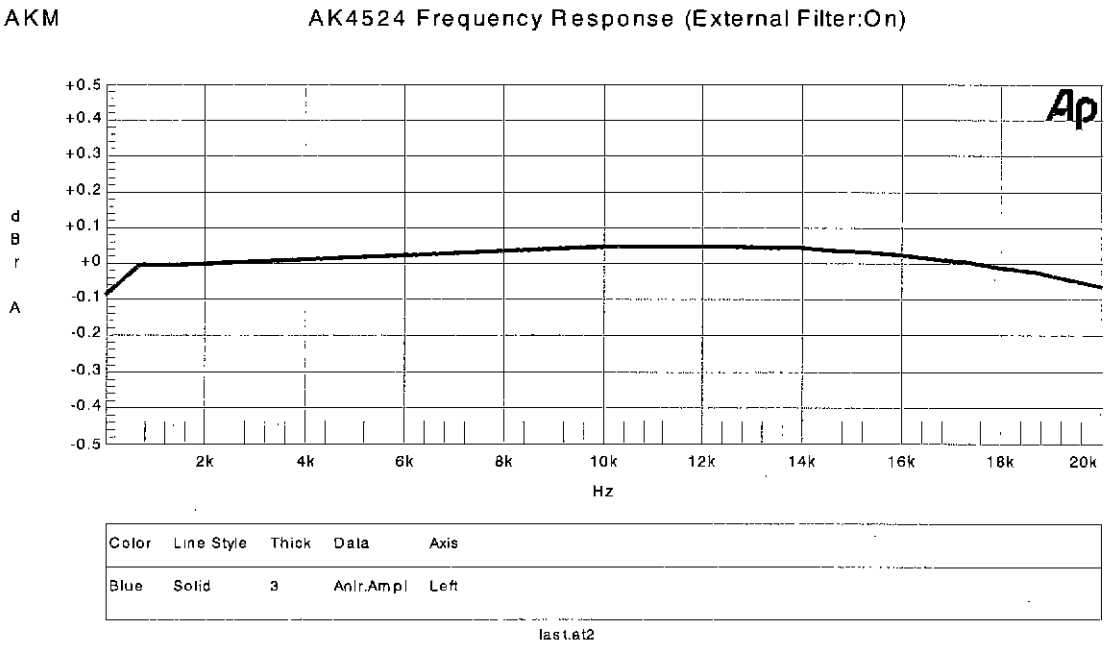


Fig13 : Frequency Response (External Filter: ON)

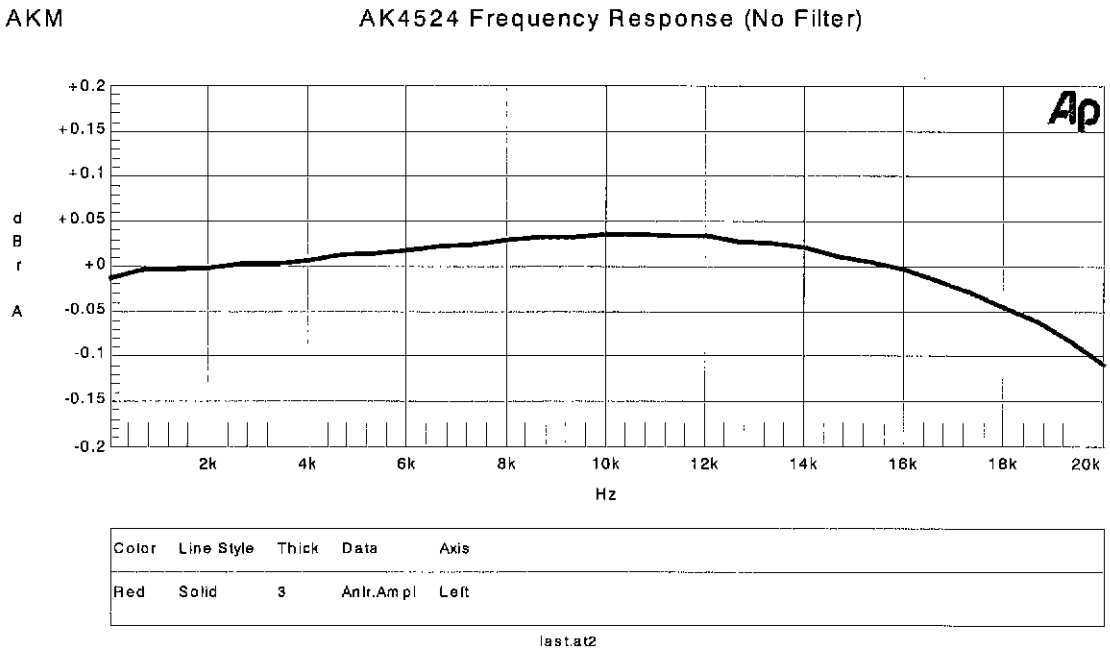


Fig14 : Frequency Response (External Filter: OFF)

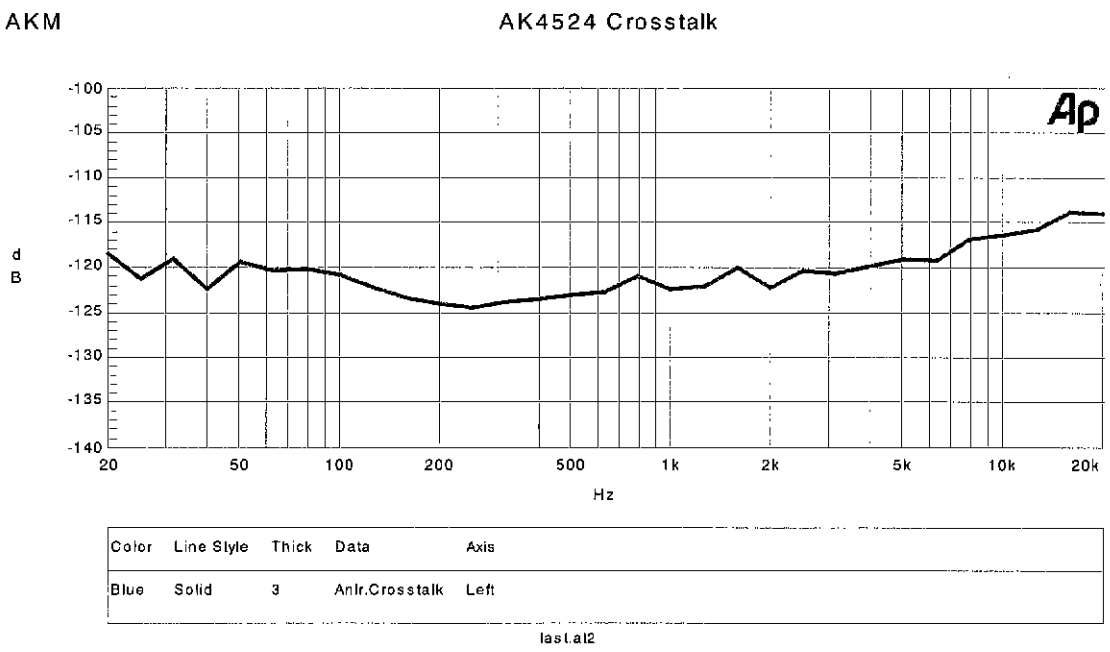


Fig15 : Crosstalk

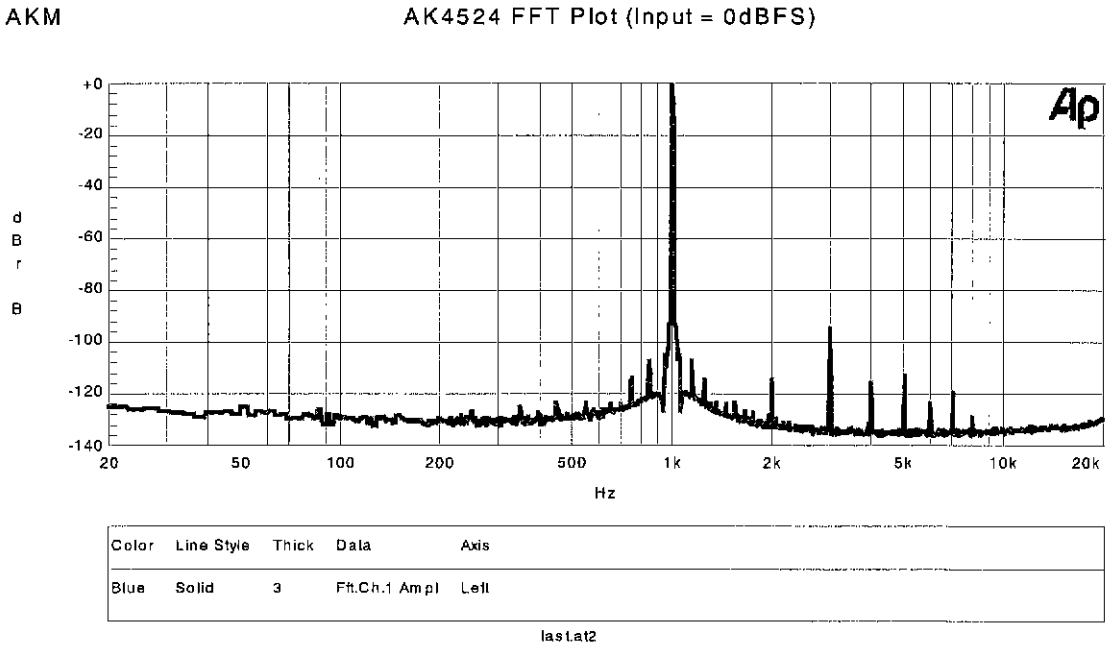


Fig16 : FFT Plot (Input = 0dBFS)

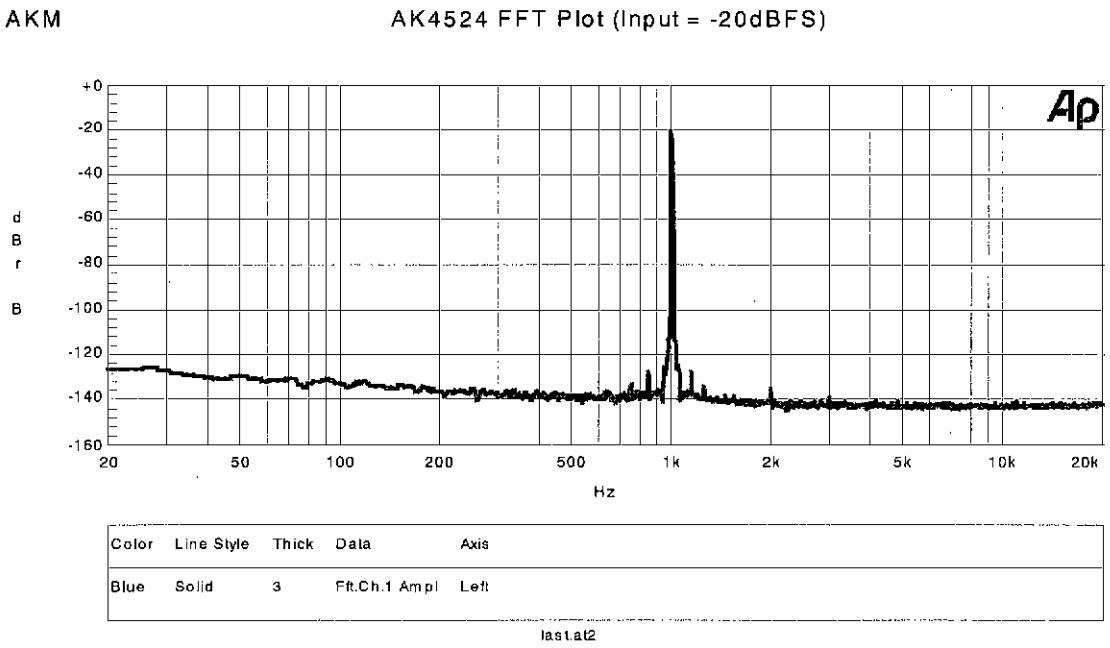


Fig17 : FFT Plot (Input = -20dBFS)

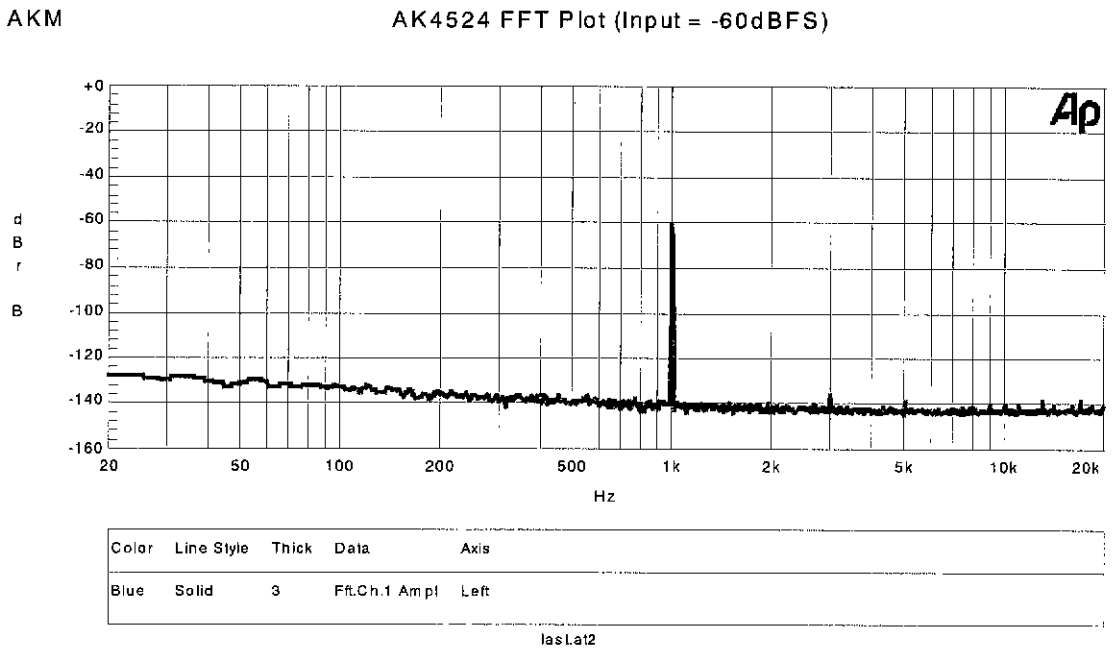


Fig18 : FFT Plot (Input = -60dBFS)

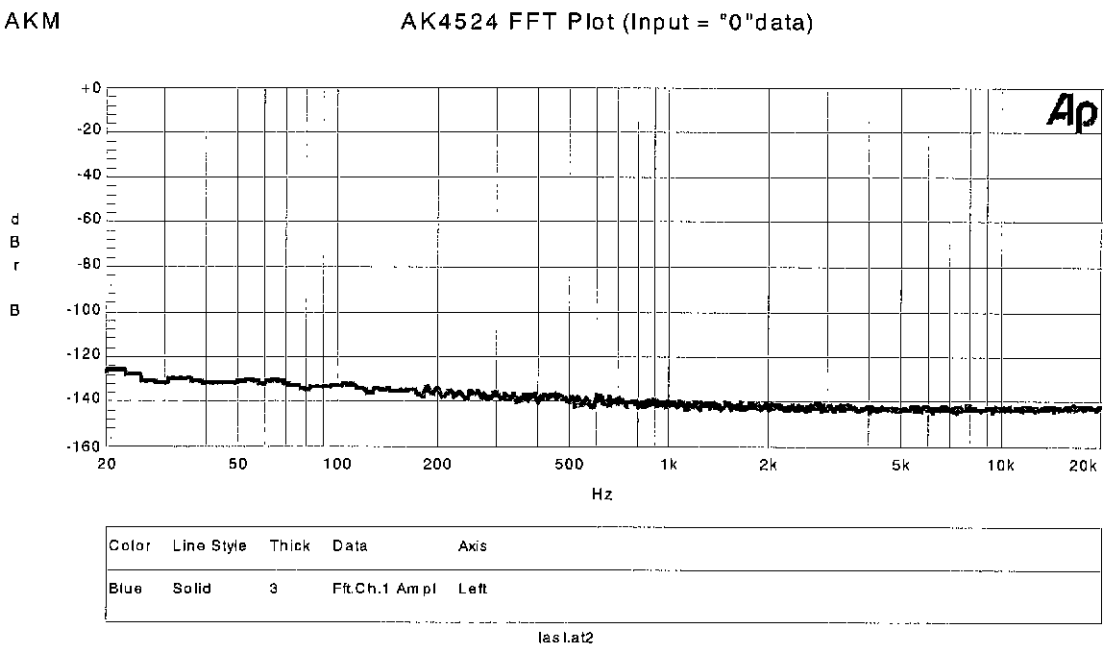
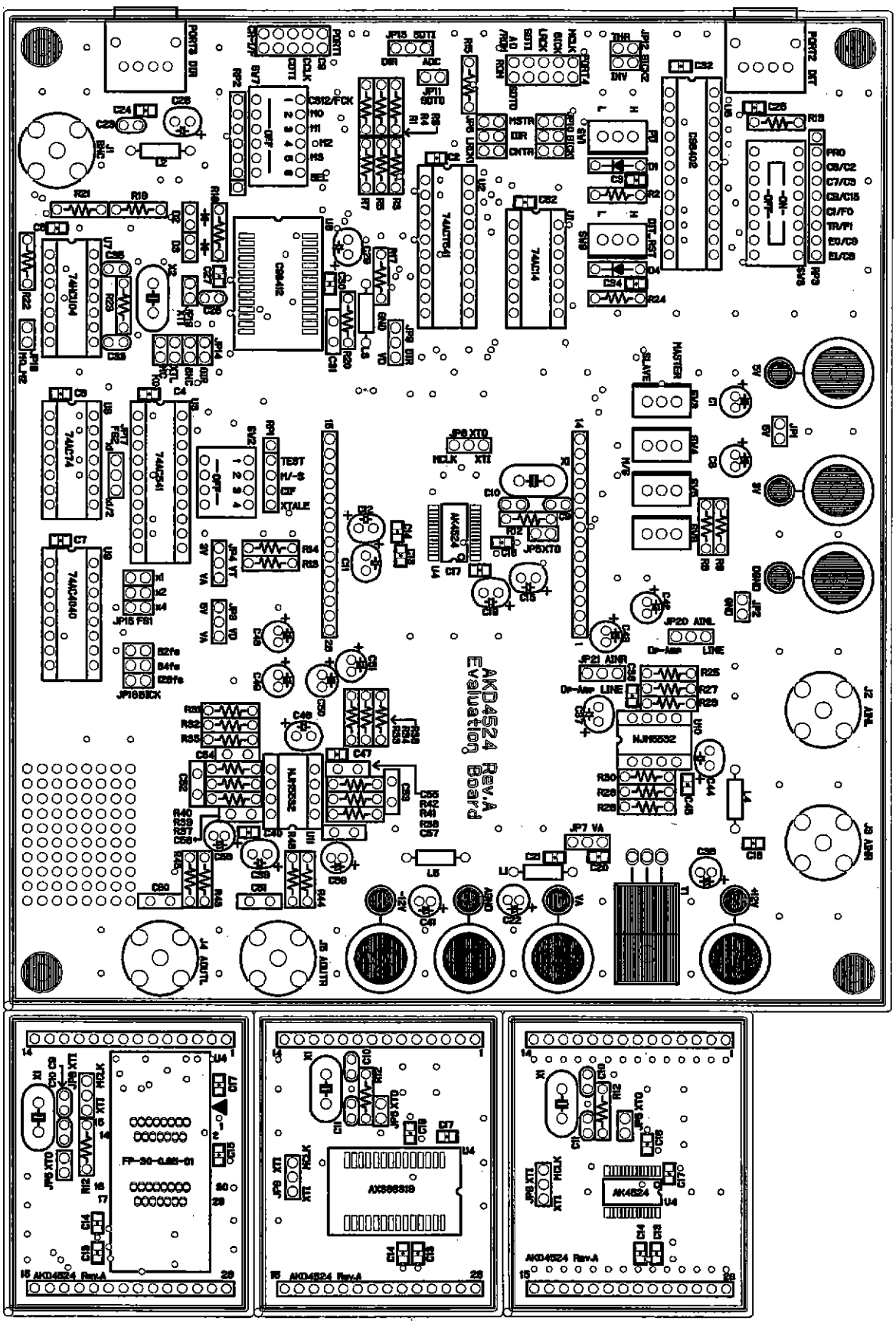


Fig19 : FFT Plot (Input = "0" data)



L1 SBK AKD4524A

L1 部品面 AKD4524A

AK524DYA 基板 SJ