SRAM & FLASH Mixed Module

Austin Semiconductor, Inc. **AS8SF384K32**

128K x 16 SRAM & 512K x 16 FLASH

SRAM / FLASH MEMORY ARRAY

FEATURES

- Operation with single 5V supply
- High speed: 35ns SRAM, 90ns FLASH
- Built in decoupling caps and multiple ground pins for low noise
- Organized as 128K x 16 SRAM and 512K x 16 FLASH
- Low power CMOS
- TTL Compatible Inputs and Outputs
- Both blocks of memory are user configurable as 256K x 8

FLASH MEMORY FEATURES

- Operation with single 5V (±10%)
- Eight equal sectors of 64K bytes
- Any combination of sectors can be concurrently erased
- Supports full chip erase
- Embedded erase and program algorithms
- 20,000 program/erase cycles
- Hardware write protection

OPTIONS MARKINGS

- Operating Temperature Ranges
  - Military (-55°C to +125°C) XT
  - Industrial (-40°C to +85°C) IT
- Timing

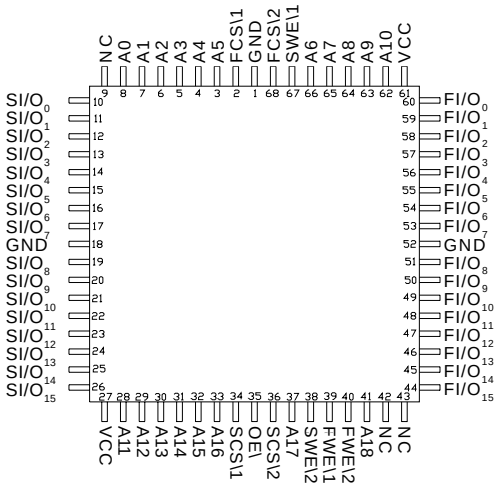
SRAM	FLASH	
35ns	90ns	-35

- Package
  - Ceramic Quad Flatpack QT

PIN ASSIGNMENT

(Top View)

68 Lead CQFP (QT)



PIN DESCRIPTION

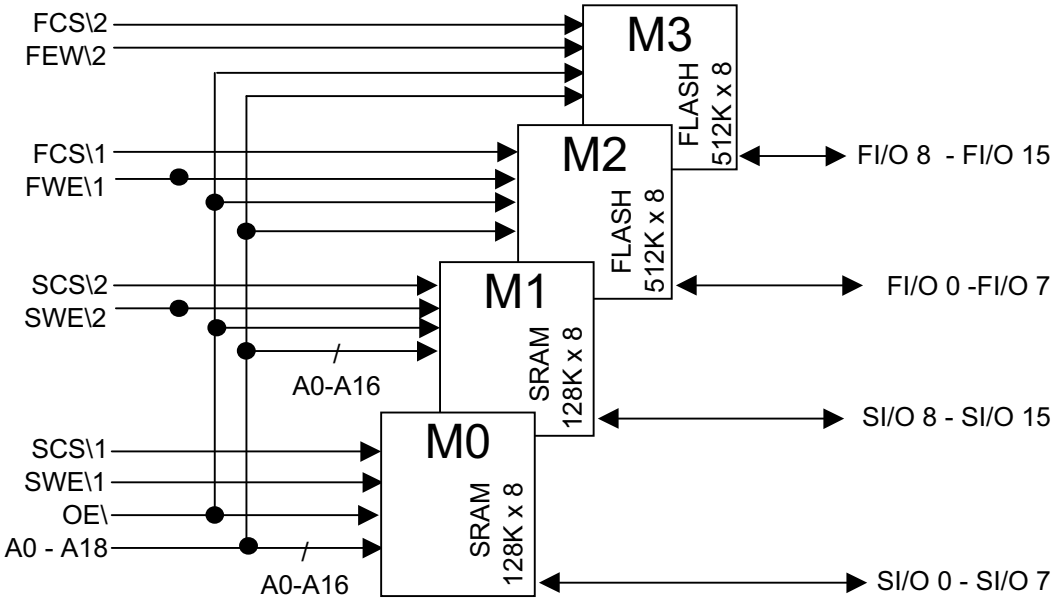
PIN	FUNCTION
A_{0-18}	Address Inputs
SI/O_{0-15}	SRAM Data Input / Outputs
FI/O_{0-15}	FLASH Data Input / Outputs
OE\	Output Enable
$SWE\backslash_{1-2}$	SRAM Write Enables
$FWE\backslash_{1-2}$	FLASH Write Enables
$SCS\backslash_{1-2}$	SRAM Chip Selects
$FCS\backslash_{1-2}$	FLASH Chip Selects
V_{CC}	Power Supply
GND	Ground
NC	No Connect

GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS8SF384K32 is a 2 MEG CMOS SRAM and 8 MEG CMOS FLASH Module organized as 128K x 16 (SRAM) and 512K x 16 (FLASH). These devices achieve high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

For more detailed information regarding the FLASH internal operations, programming, command definitions and functional descriptions, please see the AS8F512K32 data sheet located on our website at www.austinsemiconductor.com

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BLOCK DIAGRAM

SRAM TRUTH TABLE

MODE	OE\	SCS\	SWE\	I\0	POWER
Read	L	L	H	D_{OUT}	Active
Write	X	L	L	D_{IN}	Active
Standby	X	H	X	High Z	Standby

FLASH TRUTH TABLE

USER BUS OPERATIONS								
OPERATION	**FCS\1-4**	**OE**	**FWE\1-4**	**A0**	**A1**	**A6**	**A9**	**I/O**
Read	L	L	H	X	X	X	X	Data Out
Output Disable	L	H	H	X	X	X	X	High Z
Standby and Write Inhibit	H	X	X	X	X	X	X	High Z
Write	L	H	L	A0	A1	A6	A9	Data In
Sector Protect	L	VID	L	X	X	X	VID	X
Verify Sector Protect	L	L	H	H	H	L	VID	Data Out
Sector Unprotect	see note 2	see note 2	L	H	H	H	see note 2	Data Out
Verify Sector Unprotect	L	L	H	H	H	H	VID	Data Out
Erase Operations	L	H	see note 1	see note 1	see note 1	see note 1	see note 1	see note 1

LEGEND:
L = V_{IL}, H = V_{IH}, X = Don't Care, V_{ID} = 12V, See DC Charateristics for voltage levels

NOTE:
1. See Chip/Sector Erase Operation Timings and Alternate CE\ Controlled Write Operation Timings of AS8F512K32 data sheet.
2. See Chart 1 (pg. 6) of AS8F512K32 data sheet.

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ABSOLUTE MAXIMUM RATINGS*

Voltage of Vcc Supply Relative to Vss.....-.5V to +7V
Storage Temperature.....-65°C to +150°C
Short Circuit Output Current(per I/O).....20mA
Voltage on Any Pin Relative to Vss.....-.5V to Vcc+1V
Maximum Junction Temperature**.....+150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation on the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this datasheet for more information.

PARAMETER	
Flash Data Retention	10 years
Flash Endurance (write / erase cycles)	20,000

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55^oC \leq T_A \leq 125^oC$ and -40^oC to $+85^oC$; Vcc = 5V $\pm$10%)

SRAM

PARAMETER	CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +0.3	V	1
Input Low (Logic 1) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$OV \leq V_{IN} \leq Vcc$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) disabled, $OV \leq V_{OUT} \leq Vcc$	IL_O	-10	10	µA	
Output High Voltage	I_{OH} = -4.0 mA, Vcc = 4.5	V_{OH}	2.4	--	V	1
Output Low Voltage	I_{OL} = 8.0 mA, Vcc = 4.5	V_{OL}	--	0.4	V	1
Supply Voltage		Vcc	4.5	5.5	V	1
Power Supply Current: Operating	SCS\<VIL; VCC = MAX f = MAX = 1/ tRC (MIN) Outputs Open, X16	Icc		325	mA	3
Power Supply Current: Standby	SCS\>VIH; VCC = MAX f = MAX = 1/ tRC (MIN) Outputs Open, X16	I_{SBT1}		20	mA	3

1. All voltages referenced to V_{SS} (GND).
2. -2V for pulse width <20ns.
3. ICC is dependent on output loading and cycle rates. The specified value applies with the outputs

FLASH

PARAMETER	CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc Active Current	CE\ = V_{IL}, OE\ = V_{IH}, Vcc = Vcc Max, f = 5MHz	I_{CC1}	--	120	mA	
Vcc Active Current[1, 2]	CE\ = V_{IL}, OE\ = V_{IH}, Vcc = Vcc Max, f = 5MHz	I_{CC2}	--	140	mA	
Output Low Voltage	I_{OL} = 8mA, Vcc = Vcc Min	V_{OL}	--	0.45	V	
Output High Voltage	I_{OH} = -2.5mA, Vcc = Vcc Min	V_{OH1}	0.85 x Vcc	--	V	
Output High Voltage	I_{OH} = -100mA, V_{CC} = Vcc Min	V_{OH1}	V_{CC}-0.4	--	V	
Low V_{CC} Lock Out Voltage		V_{LKO}	3.2		V	

NOTES:

1. Icc active while Embedded Program or Embedded Erase Algorithm is in progress.
2. Not 100% tested.

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CAPACITANCE (V_{IN} = 0V, f = 1MHz, T_A = 25°C)[1]

SYMBOL	PARAMETER	MAX	UNITS
C_{ADD}	A0 - A18 Capacitance	50	pF
C_{OE}	OE\ Capacitance	50	pF
C_{WE}, C_{CS}	WE\ and CS\ Capacitance	20	pF
C_{IO}	I/O 0- I/O 31 Capacitance	20	pF

NOTE:
1. This parameter is sampled.

AC TEST CONDITIONS

Test Specifications

Input pulse levels.....Vss to 3V
Input rise and fall times.....5ns
Input timing reference levels.....1.5V
Output reference levels.....1.5V
Output load.....See Figure 1

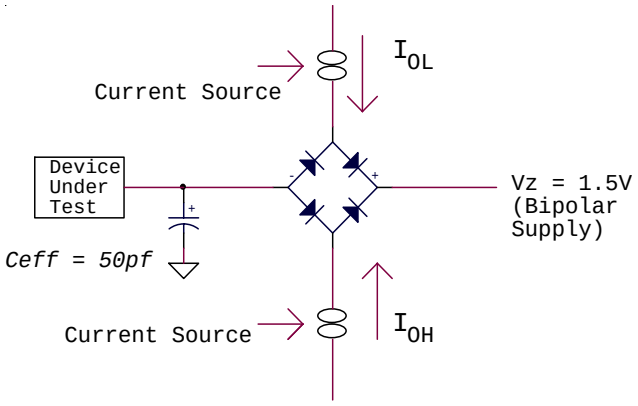


Figure 1

NOTES:
Vz is programmable from -2V to + 7V.
I_{OL} and I_{OH} programmable from 0 to 16 mA.
Vz is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(NOTE 5) ($-55^{o}C \leq T_A \leq 125^{o}C$ and $-40^{o}C$ to $+85^{o}C$; $V_{CC} = 5V \pm 10\%$)

SRAM AC

DESCRIPTION	SYMBOL	-35		UNITS
		MIN	MAX	
READ CYCLE				
READ cycle time	^{t}RC	35		ns
Address access time	^{t}AA		35	ns
Chip select access time	^{t}ACS		35	ns
Output hold from address change	^{t}OH	2		ns
Output enable to output valid	^{t}AOE		20	ns
Chip select to output in low Z[1]	$^{t}LZCS$	3		ns
Output enable to output in low Z[1]	$^{t}LZOE$	0		ns
Chip disable to output in high Z[1]	$^{t}HZCS$		20	ns
Output disable to output in high Z[1]	$^{t}HZOE$		20	ns

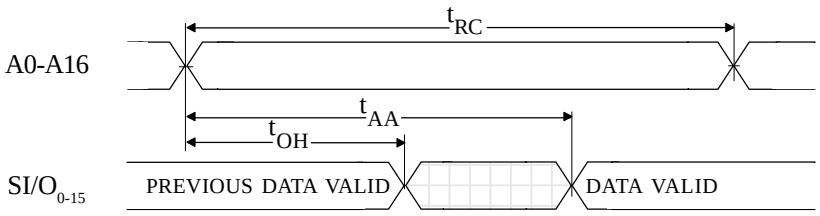
SRAM AC (SWE\ & SCS\ controlled)

DESCRIPTION	SYMBOL	-35		UNITS
		MIN	MAX	
WRITE CYCLE				
WRITE cycle time	^{t}WC	35		ns
Chip select to end of write	^{t}CW	25		ns
Address valid to end of write	^{t}AW	25		ns
Address setup time	^{t}AS	0		ns
Address hold from end of write	^{t}AH	0		ns
Data valid to end of write	^{t}DS	20		ns
Data hold time	^{t}DH	0		ns
WRITE pulse width	$^{t}WP1$	25		ns
Output active from end of write[1]	$^{t}LZWE$	2		ns
Write enable to output in High-Z[1]	$^{t}HZWE$		20	ns

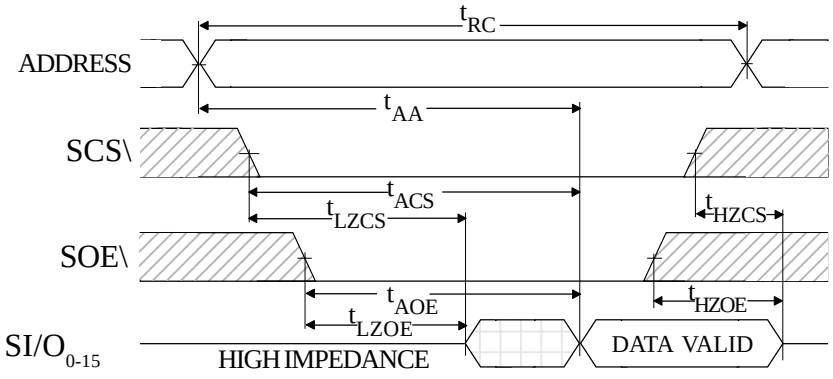
1. This parameter is guaranteed but not tested.

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SRAM READ CYCLE NO. 1



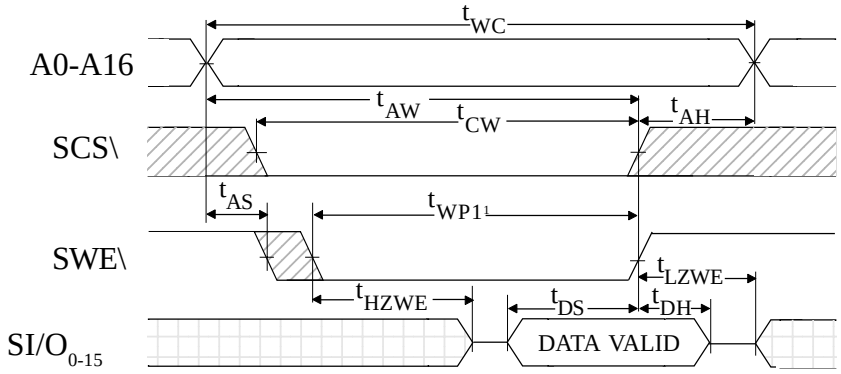
SRAM READ CYCLE NO. 2



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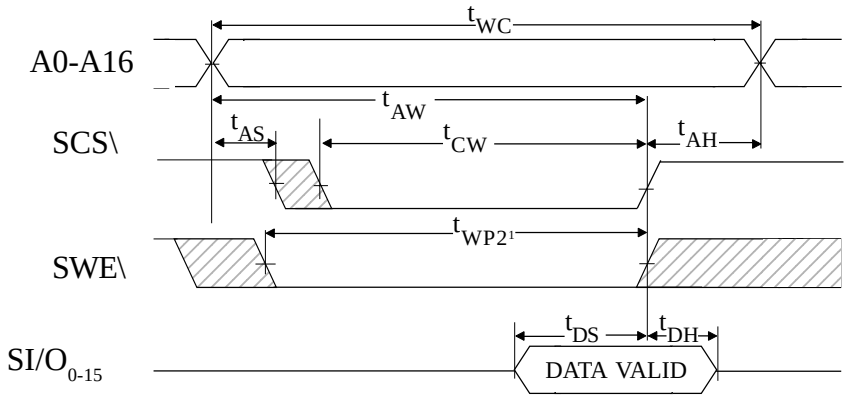
SRAM WRITE CYCLE NO. 1

(Chip Select Controlled)



WRITE CYCLE NO. 2

(Write Enable Controlled)



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FLASH ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (READ ONLY)

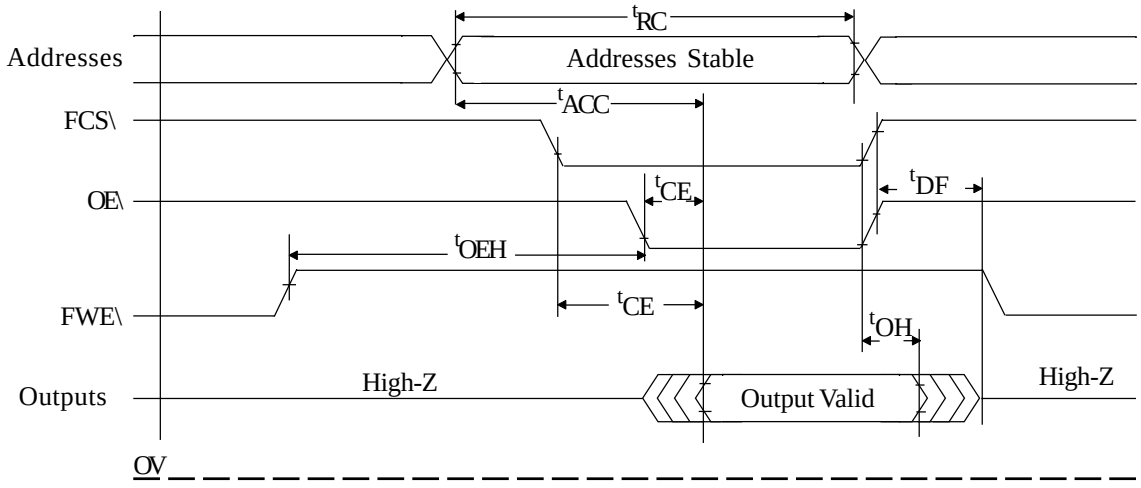
(-55°C < TA < 125°C; V_{CC} = 5V -5%/+10%)

Parameter Symbol		Parameter Description		Test Setup		Speed Options	Units
JEDEC	Std.					-35	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 3)		CE\=V_{IL}, OE\=V_{IL}	Min	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE\=V_{IL}, OE\=V_{IL}	Max	90	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid			Max	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	35	ns
	t_{OEH}	Output Enable Hold Time (Note 3)	Read		Min	0	ns
			Toggle and Data\Polling		Min	10	ns
t_{EHQZ}	t_{HZ}	Chip Enable High to Output High Z (Note 2, 3)			Max	20	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 2,3)				20	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE\ or OE\, Whichever Occurs First			Min	0	ns

NOTES:

1. See Test Specification for test conditions.
2. Output driver disable time.
3. Guaranteed but not Tested.

Read Operation Timings



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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

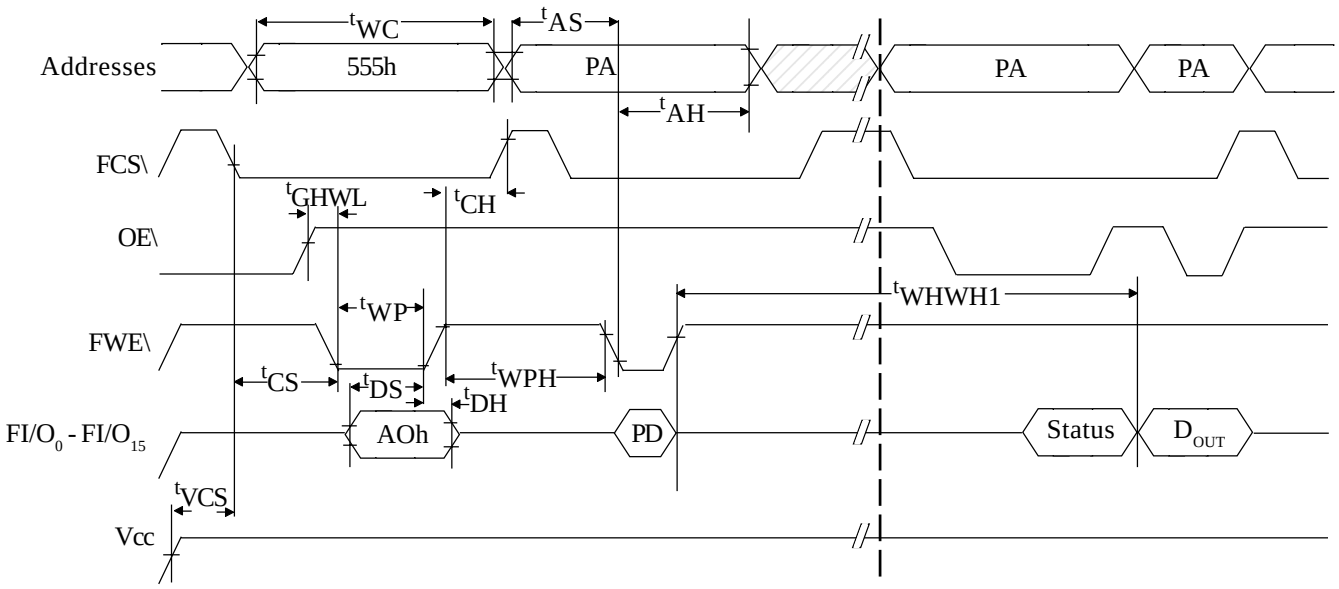
(-55°C < TA < 125°C; V_{CC} = 5V +/- 10%) WRITE / ERASE / PROGRAM

Erase and Program FWE\ Controlled

Parameter Symbol		Parameter Description		Speed Options	Units
JEDEC	Std.			-90	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	90	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	45	ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	ns
t_{GHWL}	t_{GHWL}	Read Recover time Before Write (OE\ high to FWE\ low)	Min	0	ns
t_{ELWL}	t_{CS}	FSC\ Setup Time	Min	0	ns
t_{WHEH}	t_{CH}	FSC\ Hold Time	Min	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	45	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Min	300	us
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Max	15	sec
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation	Max	120	sec
t_{VCHEL}		V_{CC} Setup Time	Min	50	us
		Chip Program Time	Max	11	sec

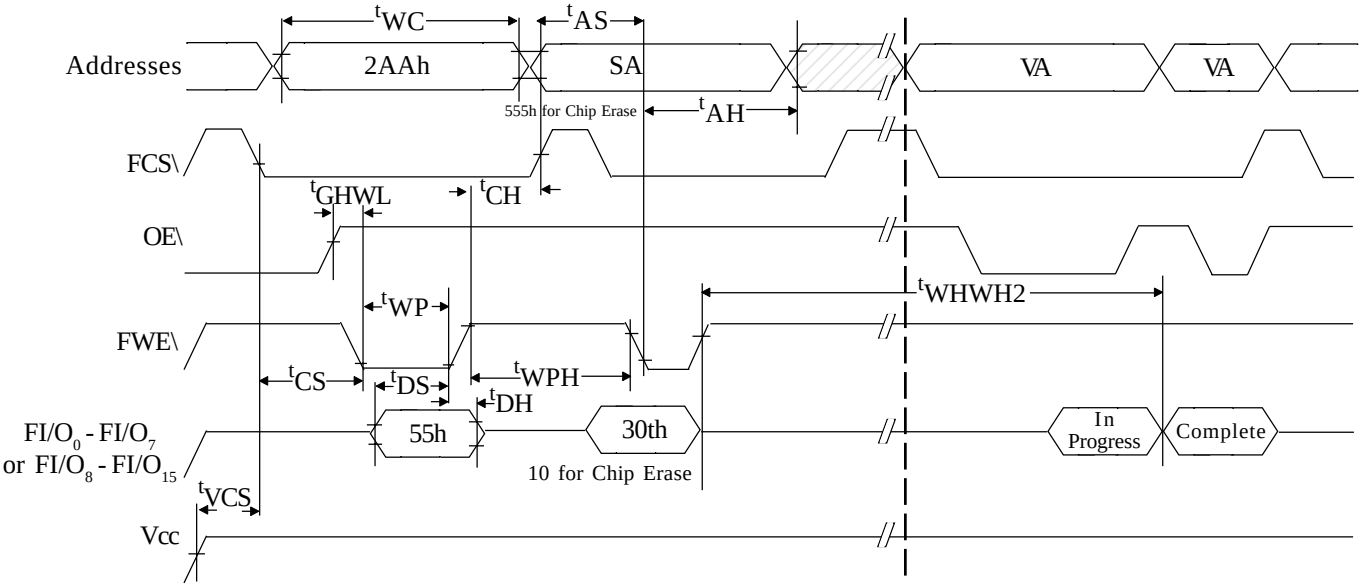
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Program Operation Timings



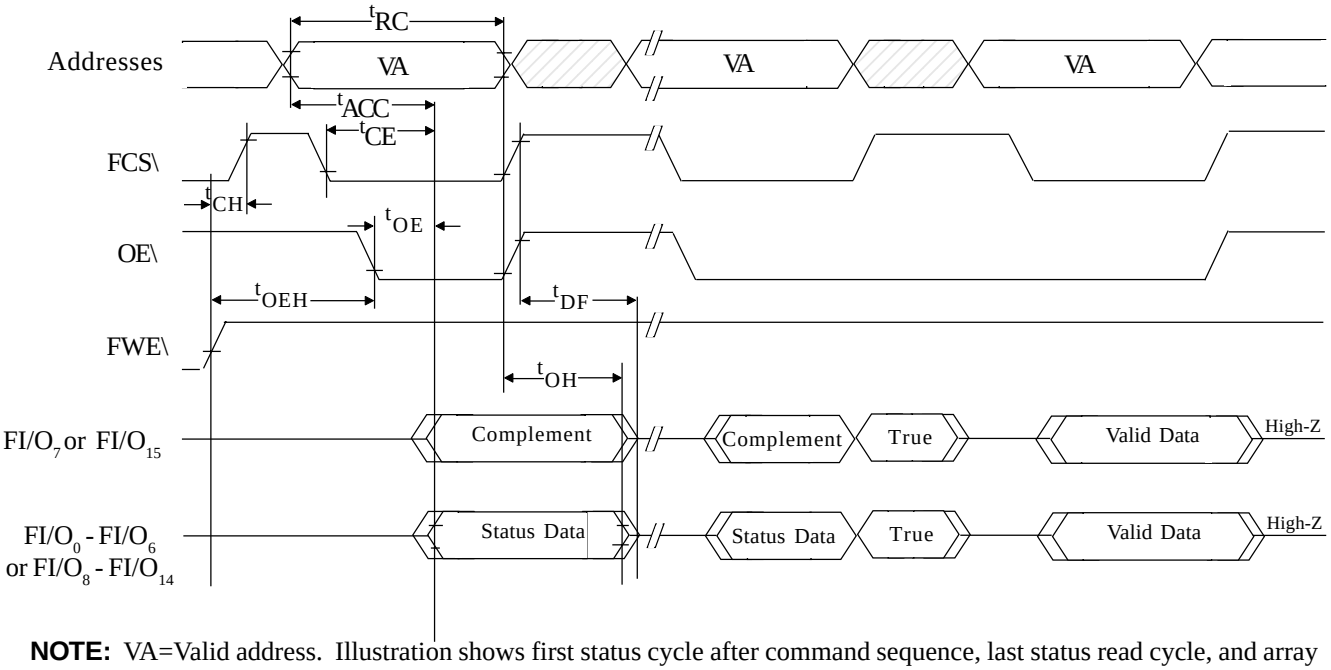
NOTE: PA= Program Address, PD= Program data, D_{OUT} is the true data at the program address.

Chip/Sector Erase Operation Timings



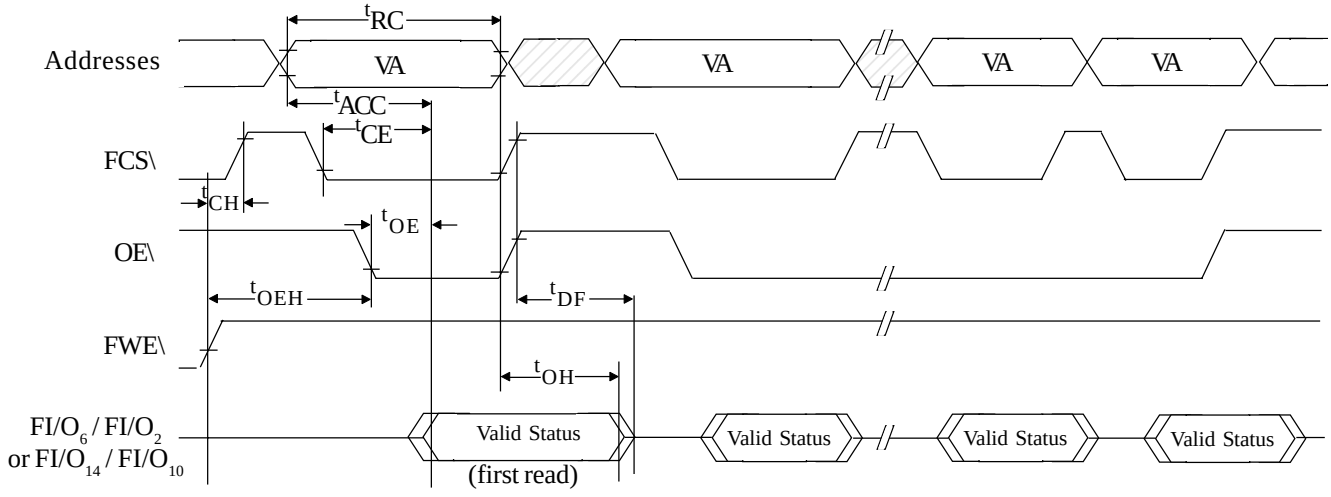
NOTE: SA= Sector Address. VA = Valid Address for reading status data.

Data Polling Timings (During Embedded Algorithms)



NOTE: VA=Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

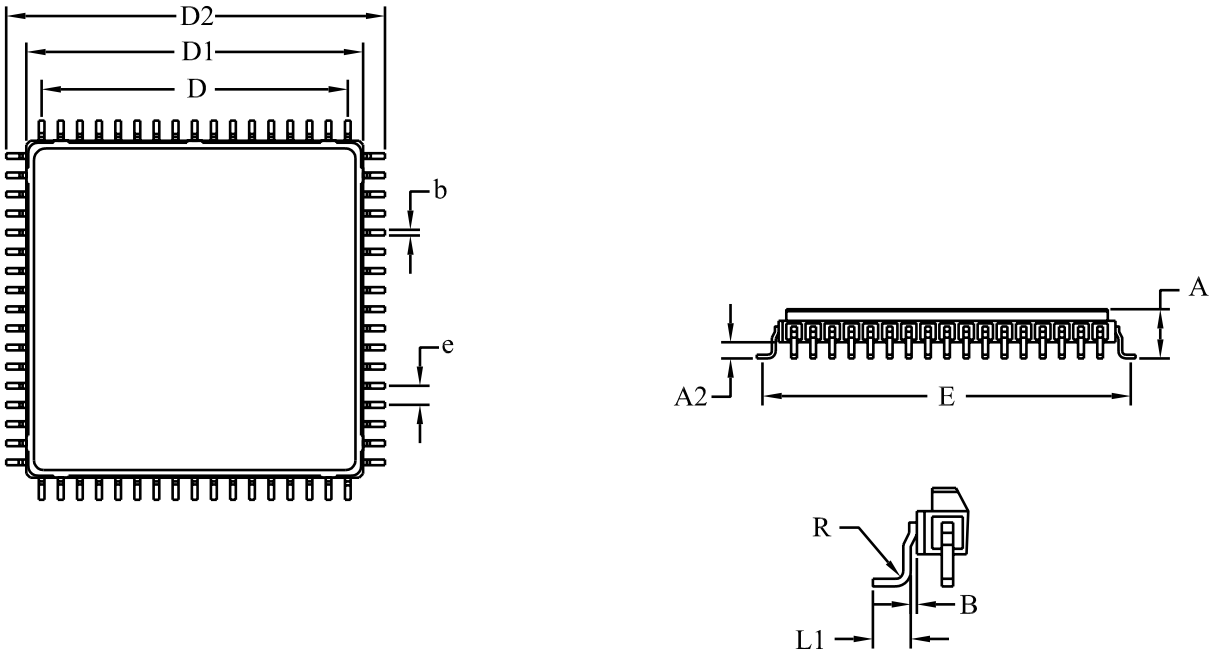
Toggle Bit Timings (During Embedded Algorithms)



NOTE: VA=Valid address; not required for FI/O_6 or FI/O_{14}. Illustration shows first two status cycles after command sequence, last status read cycle, and array data read cycle.

MECHANICAL DEFINATIONS*

Package Designator QT



ASI PACKAGE SPECIFICATION		
Symbol	Min	Max
A	.120	.140
A2	.035	.049
B	.010 REF	
b	.013	.017
D	.800 BSC	
D1	.870	.890
D2	.980	1.000
E	.936	.956
e	.050 BSC	
R	.010 TYP	
L1	.035	.045
Dimensions in inches		

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ORDERING INFORMATION

EXAMPLE's: AS8SF384K32QT-35/XT or AS8SF384K32QT-35/MIL

Device Number	Package Type	Speed ns	Process
AS8SF384K32	QT	-35	/*

***AVAILABLE PROCESSES**

/IT = Industrial Temperature Range	-40°C to +85°C
/XT = Extended Temperature Range	-55°C to +125°C
/MIL = MIL-STD-883 para.1.2.2. NC	-55°C to +125°C

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