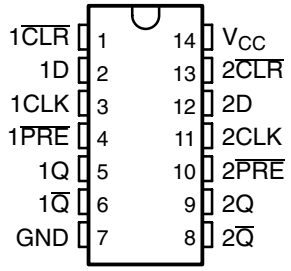
# CD74ACT74-Q1
# DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCHS349A – DECEMBER 2003 – REVISED JANUARY 2008

- **Qualified for Automotive Applications**
- **Inputs Are TTL-Voltage Compatible**
- **Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **±24-mA Output Drive Current**
  - **Fanout to 15 F Devices**
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**

**M PACKAGE**
**(TOP VIEW)**




## description/ordering information

The CD74ACT74 dual positive-edge-triggered device is a D-type flip-flop.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

**ORDERING INFORMATION†**

| $T_A$ | PACKAGE‡ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 125°C | SOIC – M | Tape and reel | CD74ACT74QM96Q1 | ACT74Q |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

**FUNCTION TABLE**
**(each flip-flop)**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H§ | H§ |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |

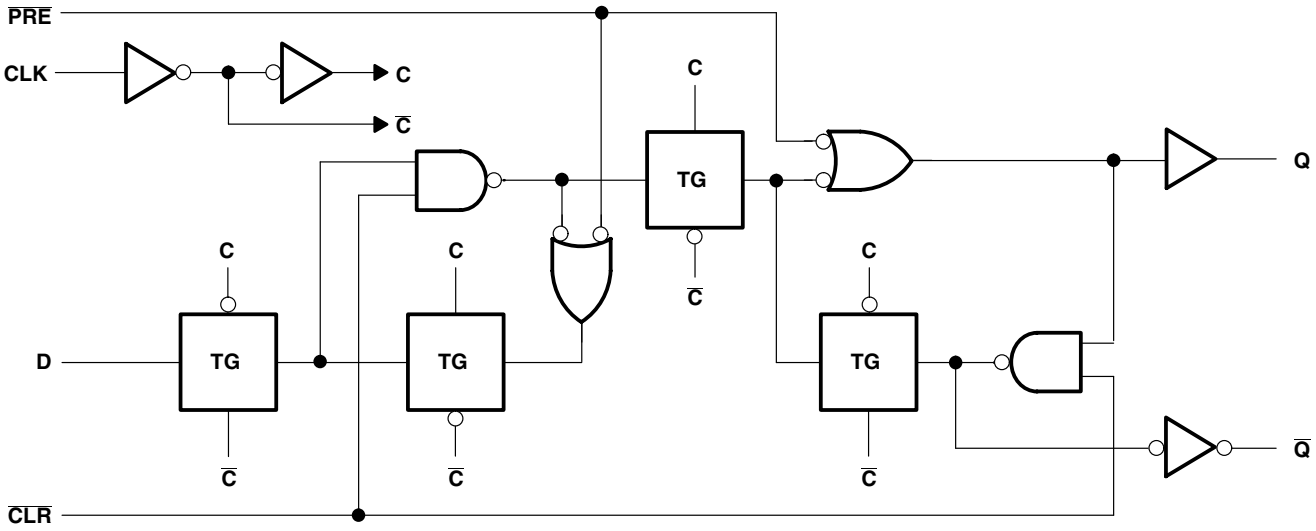
§ This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

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## logic diagram, each flip-flop (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 6 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) . . . . . 86°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | $T_A$ = 25°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –24 | mA |
| $I_{OL}$ | Low-level output current | | 24 | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | ns/V |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | | 4.4 | | V |
| | | $I_{OH}$ = –24 mA | 4.5 V | 3.94 | | 3.7 | | |
| | | $I_{OH}$ = –50 mA† | 5.5 V | | | 3.85 | | |
| $V_{OL}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 4.5 V | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 24 mA | 4.5 V | | 0.36 | | 0.5 | |
| | | $I_{OL}$ = 50 mA† | 5.5 V | | | | 1.65 | |
| $I_I$ | $V_I = V_{CC}$ or GND | | 5.5 V | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, | $I_O$ = 0 | 5.5 V | | 4 | | 80 | μA |
| $\Delta I_{CC}$‡ | $V_I = V_{CC}$ – 2.1 V | | 4.5 V to 5.5 V | | 2.4 | | 3 | mA |
| $C_i$ | | | | | 10 | | 10 | pF |

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75-Ω transmission-line drive capability at 125°C.
‡ Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

**ACT INPUT LOAD TABLE**

| INPUT | UNIT LOAD |
|---|---|
| Data | 0.53 |
| $\overline{PRE}$ or $\overline{CLR}$ | 0.58 |
| CLK | 1 |

Unit load is $\Delta I_{CC}$ limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | 85 | MHz |
| $t_w$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ low | 5 | | ns |
| | | CLK | 5.7 | | |
| $t_{su}$ | Setup time | Data | 4 | | ns |
| $t_h$ | Hold time | Data after CLK↑ | 0 | | ns |
| $t_{rec}$ | Recovery time, before CLK↑ | $\overline{CLR}$↑ or $\overline{PRE}$↑ | 2.7 | | ns |

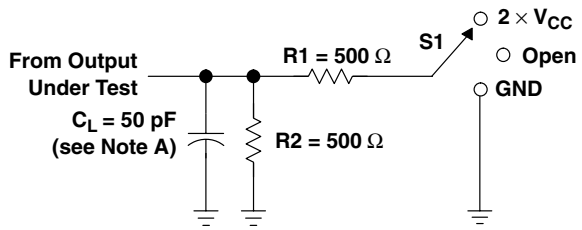
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $f_{max}$ | | | 85 | | MHz |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | 2.4 | 9.5 | ns |
| $t_{PHL}$ | | | 2.4 | 9.5 | |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | 2.9 | 11.5 | ns |
| $t_{PHL}$ | | | 3.1 | 12.5 | |

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

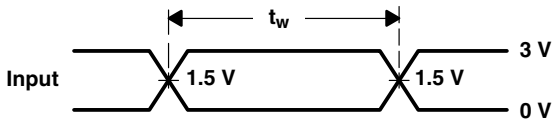
| PARAMETER | | TYP | UNIT |
|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | 55 | pF |

## PARAMETER MEASUREMENT INFORMATION

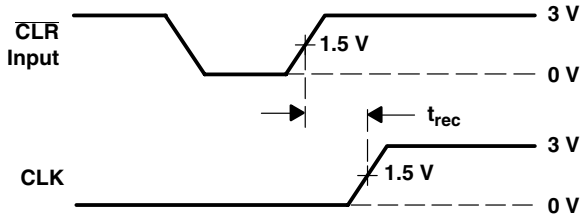



LOAD CIRCUIT

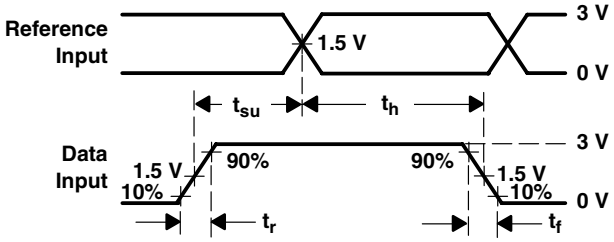
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



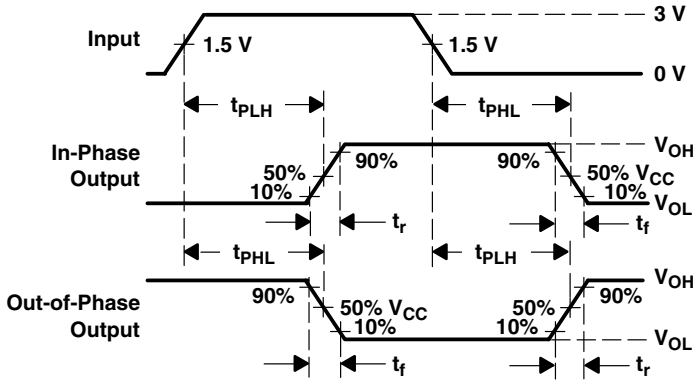

VOLTAGE WAVEFORMS
PULSE DURATION



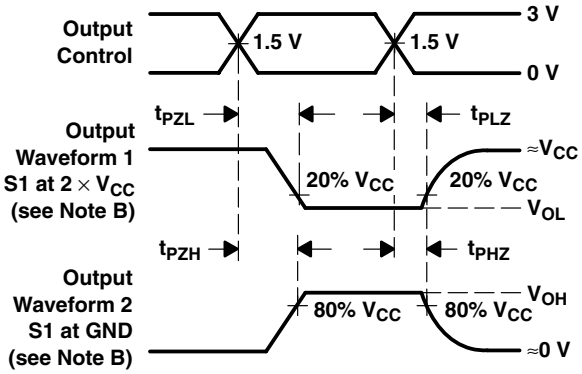

VOLTAGE WAVEFORMS
RECOVERY TIME




VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES




VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns. Phase relationships between waveforms are arbitrary.
D. For clock inputs, $f_{max}$ is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
G. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
H. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74ACT74QM96G4Q1 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ACT74Q | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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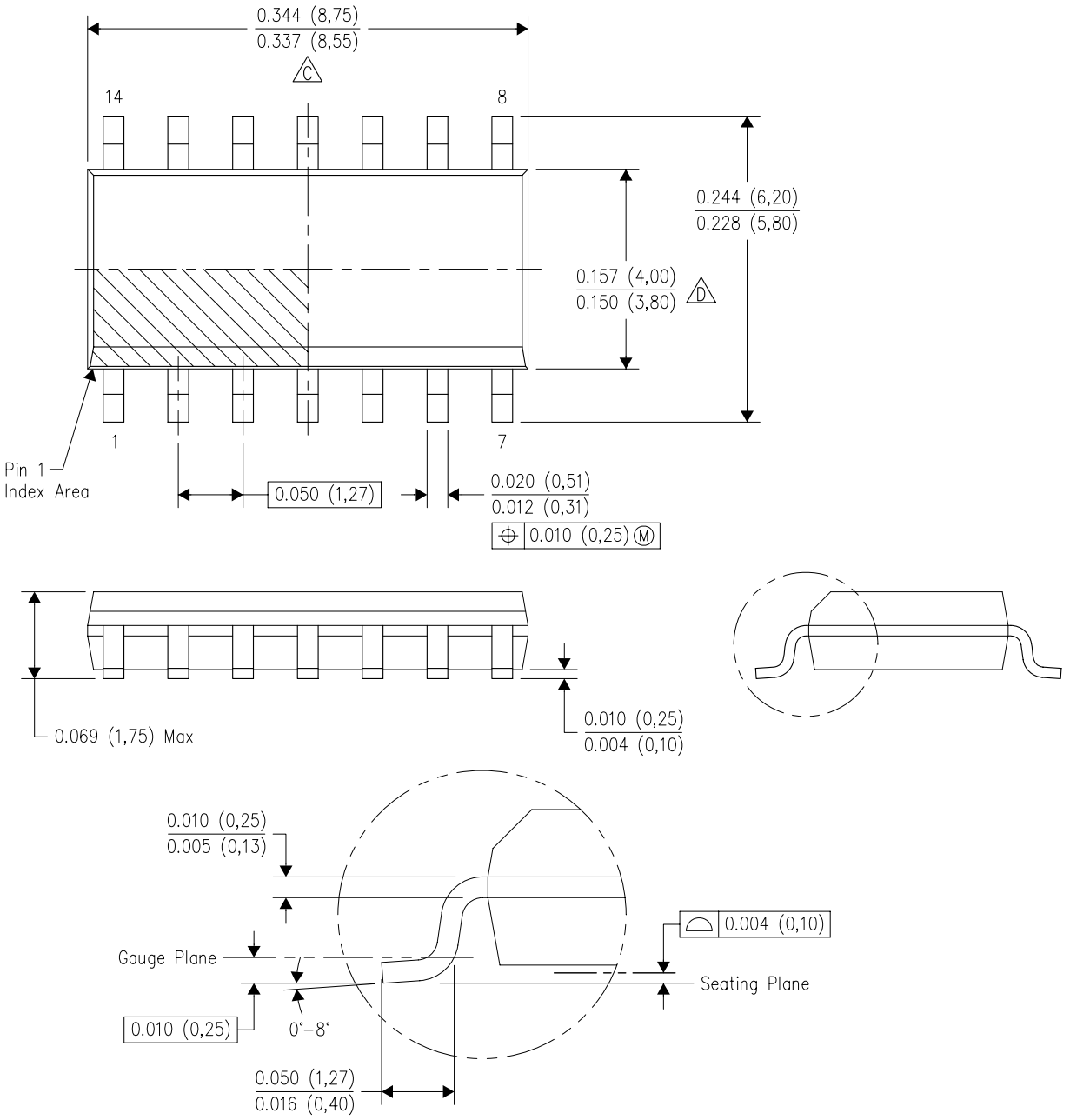
**OTHER QUALIFIED VERSIONS OF CD74ACT74-Q1 :**

- Catalog: CD74ACT74
- Military: CD54ACT74

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

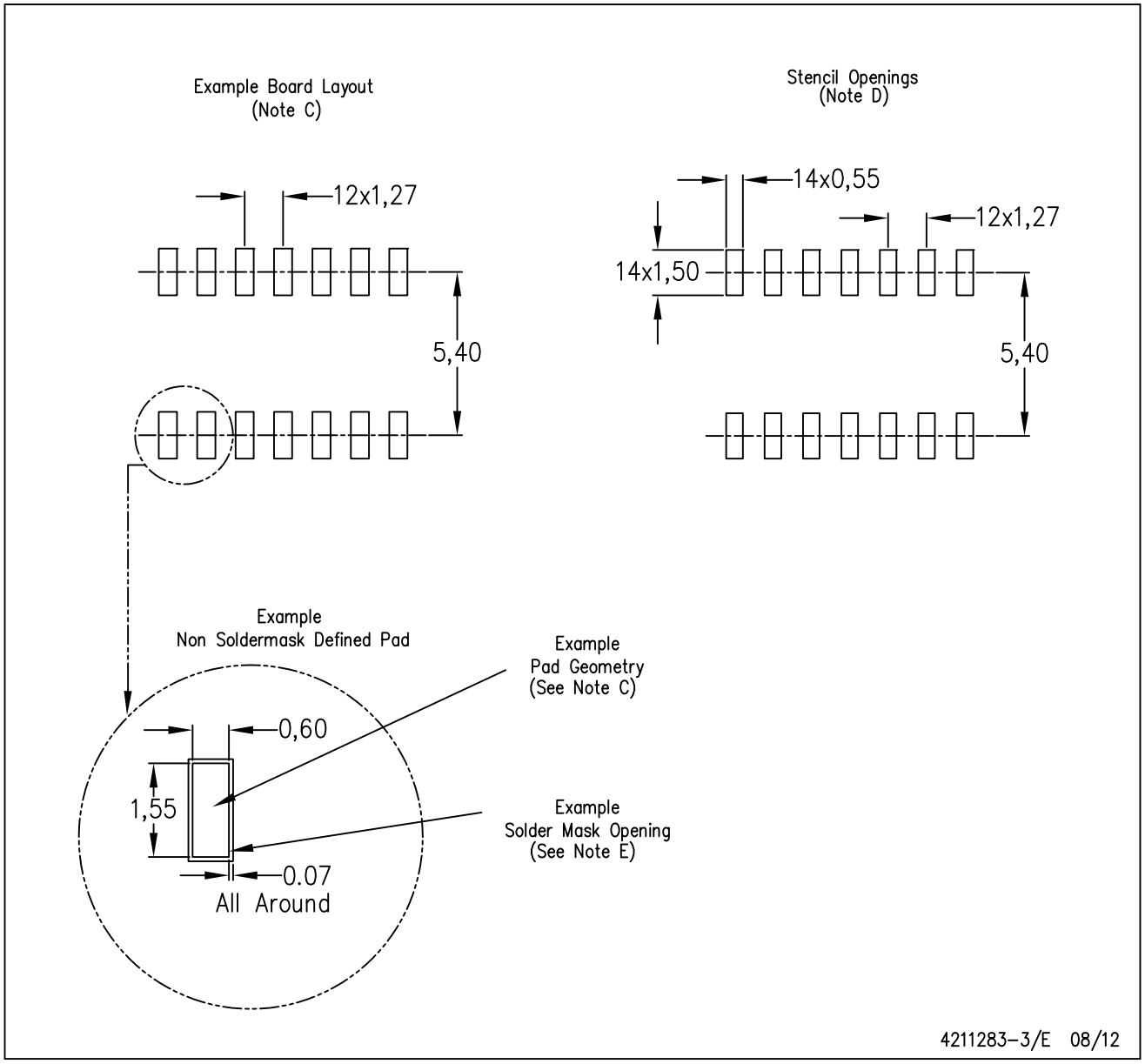
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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