

## Ultra-Low Supply-Current/Supply-Voltage Supervisory Circuits

### FEATURES

- **Controlled Baseline**
  - One Assembly Site
  - One Test Site
  - One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree <sup>(1)</sup>**
- **Precision Supply Voltage Supervision Range: 0.9 V, 1.2 V, 1.5 V, 1.6 V, 2 V, and 3.3 V**
- **High Trip-Point Accuracy: 0.75%**
- **Supply Current of 1.2  $\mu$ A (Typ)**
- **$\overline{\text{RESET}}$  Defined With Input Voltages as Low as 0.4 V**
- **Power-On Reset Generator With a Delay Time of 130 ms**
- **Push/Pull or Open-Drain  $\overline{\text{RESET}}$  Outputs**
- **SOT23-6 Package**

- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

### APPLICATIONS

- **Applications Using Low-Power DSPs, Microcontrollers, or Microprocessors**
- **Portable- and Battery-Powered Equipment**
- **Intelligent Instruments**
- **Wireless Communication Systems**
- **Industrial Equipment**
- **Notebook/Desktop Computers**

### DESCRIPTION

The TPS310x and TPS311x families of supervisory circuits provide circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power-on,  $\overline{\text{RESET}}$  is asserted when the supply voltage ( $V_{DD}$ ) becomes higher than 0.4 V. Thereafter, the supervisory circuit monitors  $V_{DD}$  and keeps the  $\overline{\text{RESET}}$  output active as long as  $V_{DD}$  remains below the threshold voltage ( $V_{IT}$ ). An internal timer delays the return of the output to the inactive state to ensure proper system reset. The delay time starts after  $V_{DD}$  has risen above  $V_{IT}$ . When  $V_{DD}$  drops below  $V_{IT}$ , the output becomes active again.

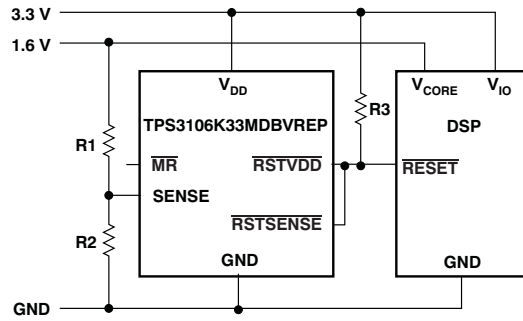
All the devices of this family have a fixed-sense threshold voltage ( $V_{IT}$ ) set by an internal voltage divider.

The TPS3103 and TPS3106 have an active-low, open-drain  $\overline{\text{RESET}}$  output. The TPS3110 has an active-low push/pull  $\overline{\text{RESET}}$ .

The product spectrum is designed for supply voltages of 0.9 V up to 3.3 V. The circuits are available in SOT23-6 packages. The TPS31xx family is characterized for operation over a temperature range of –55°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



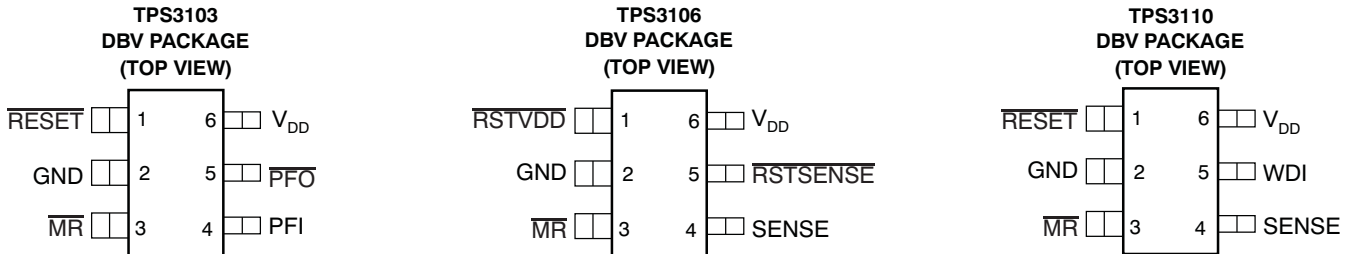
Typical Application Circuit



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN DESCRIPTIONS



## TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
NAME	DEVICE	NO.	
GND	All	2	Ground
MR	All	3	Manual reset input. Pull low to force a reset. RESET remains low as long as MR is low and for the timeout period after MR goes high. Leave unconnected or connect to V <sub>DD</sub> when unused.
PFI	TPS3103	4	Power-fail input. Compares to 0.551 V with no additional delay. Connect to V <sub>DD</sub> if not used.
PFO	TPS3103	5	Power-fail output. Goes high when voltage at PFI rises above 0.551 V.
RESET	TPS3103, TPS3110	1	Active-low reset output. Either push-pull or open-drain output stage.
RSTSENSE	TPS3106	5	Active-low reset output. Logic level at RSTSENSE only depends on the voltage at SENSE and the status of MR.
RSTVDD	TPS3106	1	Active-low reset output. Logic level at RSTVDD only depends on the voltage at V <sub>DD</sub> and the status of MR.
SENSE	TPS3106, TPS3110	4	Sense. A reset is asserted if the voltage at SENSE is lower than 0.551 V. Connect to V <sub>DD</sub> if unused.
V <sub>DD</sub>	All	6	Supply voltage. Powers the device and monitors its own voltage.
WDI	TPS3110	5	Watchdog timer input. If WDI remains high or low longer than the time-out period, reset is triggered. The timer clears when reset is asserted or when WDI sees a rising edge or a falling edge.

## ORDERING INFORMATION<sup>(1)</sup>

ORDERABLE PART NUMBER	NOMINAL SUPPLY VOLTAGE	THRESHOLD VOLTAGE, V <sub>IT</sub> <sup>(2)</sup>	SYMBOL
TPS3103E12MDBVREP <sup>(3)</sup>	1.2 V	1.142 V	TBD
TPS3103E15MDBVREP <sup>(3)</sup>	1.5 V	1.434 V	TBD
TPS3103H20MDBVREP <sup>(3)</sup>	2 V	1.84 V	TBD
TPS3103K33MDBVREP <sup>(3)</sup>	3.3 V	2.941 V	TBD
TPS3106E09MDBVREP <sup>(3)</sup>	0.9 V	0.86 V	TBD
TPS3106E16MDBVREP <sup>(3)</sup>	1.6 V	1.521 V	TBD
TPS3106K33MDBVREP	3.3 V	2.941 V	AAVM
TPS3110E09MDBVREP <sup>(3)</sup>	0.9 V	0.86 V	TBD
TPS3110E12MDBVREP <sup>(3)</sup>	1.2 V	1.142 V	TBD
TPS3110E15MDBVREP <sup>(3)</sup>	1.5 V	1.434 V	TBD
TPS3110K33MDBVREP <sup>(3)</sup>	3.3 V	2.941 V	TBD

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Custom threshold voltages are available. Minimum order quantities apply. Contact TI for details and availability.

(3) Product Preview

### AVAILABLE OPTIONS

DEVICE	RESET OUTPUT	RSTSENSE, RSTVDD OUTPUT	SENSE INPUT	WDI INPUT	PFO OUTPUT
TPS3103	Open drain				Open drain
TPS3106		Open drain	ū		
TPS3110	Push-pull		ū	ū	

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

	VALUE	UNIT
Supply voltage range, $V_{DD}$ <sup>(2)</sup>	-0.3 to 3.6	V
All other pins <sup>(2)</sup>	-0.3 to 3.6	V
Maximum low output current, $I_{OL}$	5	mA
Maximum high output current, $I_{OH}$	-5	mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{DD}$ )	±10	mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DD}$ )	±10	mA
Operating temperature range, $T_A$	-55 to 125	°C
Storage temperature range, $T_{stg}$	-65 to 150	°C
Soldering temperature	260	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND. For reliable operation, the device must not be operated at 3.6 V for more than  $t = 1000h$  continuously

### RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage, $V_{DD}$ <sup>(1)</sup>	0.4	3.3	V
Input voltage, $V_I$	0	$V_{DD} + 0.3$	V
High-level input voltage, $V_{IH}$ at $\overline{MR}$ , WDI	$0.7 \times V_{DD}$		V
Low-level input voltage, $V_{IL}$ at $\overline{MR}$ , WDI		$0.3 \times V_{DD}$	V
Input transition rise and fall rate at $\Delta t/\Delta V$ at $\overline{MR}$ , WDI		100	ns/V
Operating temperature, $T_A$	-55	125	°C

- (1) For proper operation of SENSE, PFI, and WDI functions:  $V_{DD} \geq 0.8$  V.

### ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$V_{DD} = 3.3$ V, $I_{OH} = -3$ mA	$0.8 \times V_{DD}$			V
		$V_{DD} = 1.8$ V, $I_{OH} = -2$ mA				
		$V_{DD} = 1.5$ V, $I_{OH} = -1$ mA				
		$V_{DD} = 0.9$ V, $I_{OH} = -0.4$ mA				
		$V_{DD} = 0.5$ V, $I_{OH} = -5$ $\mu$ A				
$V_{OL}$	Low-level output voltage	$V_{DD} = 3.3$ V, $I_{OL} = 3$ mA			0.3	V
		$V_{DD} = 1.5$ V, $I_{OL} = 2$ mA				
		$V_{DD} = 1.2$ V, $I_{OL} = 1$ mA				
		$V_{DD} = 0.9$ V, $I_{OL} = 500$ $\mu$ A				
$V_{OL}$	Low-level output voltage	RESET only	$V_{DD} = 0.4$ V, $I_{OL} = 5$ $\mu$ A		0.1	V

## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V <sub>IT-</sub>	Negative-going input threshold voltage <sup>(1)</sup>	TPS31xxE09	0.854	0.86	0.866	V	
		TPS31xxE12	1.133	1.142	1.151		
		TPS31xxE15	1.423	1.434	1.445		
		TPS31xxE16	1.512	1.523	1.534		
		TPS31xxH20	1.829	1.843	1.857		
		TPS31xxK33	2.905	2.941	2.970		
V <sub>IT-(S)</sub>	Negative-going input threshold voltage <sup>(2)</sup>	SENSE, PFI	V <sub>DD</sub> ≥ 0.8 V, T <sub>A</sub> = 25°C	0.540	0.551	0.569	V
			V <sub>DD</sub> ≥ 0.8 V, T <sub>A</sub> = Full Range	0.530	0.551	0.575	
V <sub>HYS</sub>	Hysteresis at V <sub>DD</sub> input		0.8 V ≤ V <sub>IT</sub> < 1.5 V	20		mV	
			1.6 V ≤ V <sub>IT</sub> < 2.4 V	30			
			2.5 V ≤ V <sub>IT</sub> < 3.3 V	60			
T <sub>(K)</sub>	Temperature coefficient of V <sub>IT-</sub> , PFI, SENSE	T <sub>A</sub> = -55°C to 125°C		-0.012	-0.019	%/K	
V <sub>HYS</sub>	Hysteresis at SENSE, PFI input	V <sub>DD</sub> ≥ 0.8 V		15		mV	
I <sub>IH</sub>	High-level input current	$\overline{MR}$	$\overline{MR} = V_{DD}$ , V <sub>DD</sub> = 3.3 V	-30		25	nA
		SENSE, PFI, WDI	SENSE, PFI, WDI = V <sub>DD</sub> , V <sub>DD</sub> = 3.3 V	-25		25	
I <sub>IL</sub>	Low-level input current	$\overline{MR}$	$\overline{MR} = 0$ V, V <sub>DD</sub> = 3.3 V	-47	-33	-25	μA
		SENSE, PFI, WDI	SENSE, PFI, WDI = 0 V, V <sub>DD</sub> = 3.3 V	-25		25	nA
I <sub>OH</sub>	High-level output current at RESET <sup>(3)</sup>	Open drain	V <sub>DD</sub> = V <sub>IT</sub> + 0.2 V, V <sub>OH</sub> = 3.3 V			200	nA
I <sub>DD</sub>	Supply current		V <sub>DD</sub> > V <sub>IT</sub> (average current), V <sub>DD</sub> < 1.8 V		1.2	3	μA
			V <sub>DD</sub> > V <sub>IT</sub> (average current), V <sub>DD</sub> > 1.8 V		2	4.5	
			V <sub>DD</sub> < V <sub>IT</sub> , V <sub>DD</sub> < 1.8 V			29	
			V <sub>DD</sub> < V <sub>IT</sub> , V <sub>DD</sub> > 1.8 V			32	
Internal pullup resistor at $\overline{MR}$				70	100	130	kΩ
C <sub>I</sub>	Input capacitance at $\overline{MR}$ , SENSE, PFI, WDI	V <sub>I</sub> = 0 V to V <sub>DD</sub>		1			pF

(1) To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed close to the supply terminals.

(2) To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed close to the supply terminals.

(3) Also refers to  $\overline{RSTVDD}$  and  $\overline{RSTSENSE}$ .

## SWITCHING CHARACTERISTICS

R<sub>L</sub> = 1 MΩ, C<sub>L</sub> = 50 pF, and T<sub>A</sub> = -55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>d</sub>	Delay time	V <sub>DD</sub> ≥ 1.1 × V <sub>IT</sub> , $\overline{MR} = 0.7 \times V_{DD}$ , See <a href="#">Timing Diagrams</a>	65	130	195	ms
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output	V <sub>DD</sub> to $\overline{RESET}$ or $\overline{RSTVDD}$ delay			40	μs
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output	$\overline{SENSE}$ to $\overline{RESET}$ or $\overline{RSTSENSE}$ delay	V <sub>DD</sub> ≥ 0.8 V, V <sub>IH</sub> = 1.1 × V <sub>IT</sub> , V <sub>IL</sub> = 0.9 × V <sub>IT</sub>		40	μs
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output	PFI to $\overline{PFO}$ delay	V <sub>DD</sub> ≥ 0.8 V, V <sub>IH</sub> = 1.1 × V <sub>IT</sub> , V <sub>IL</sub> = 0.9 × V <sub>IT</sub>		40	μs
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	PFI to $\overline{PFO}$ delay	V <sub>DD</sub> ≥ 0.8 V, V <sub>IH</sub> = 1.1 × V <sub>IT</sub> , V <sub>IL</sub> = 0.9 × V <sub>IT</sub>		300	μs

### SWITCHING CHARACTERISTICS (continued)

$R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ , and  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

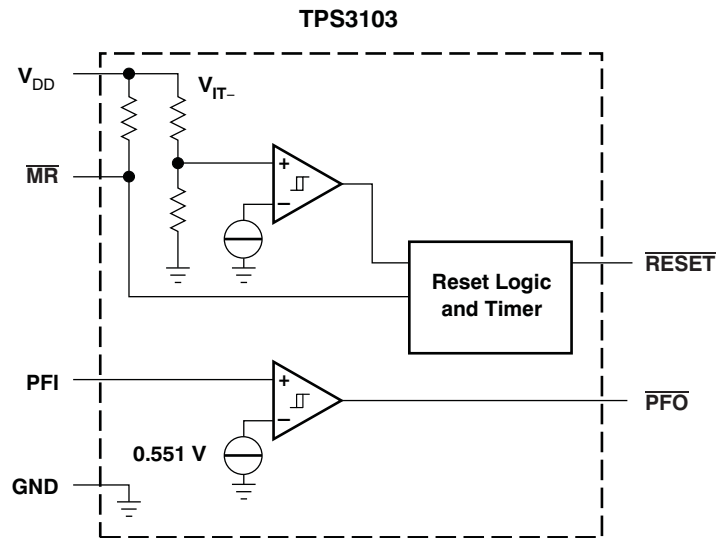
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PHL}$	Propagation delay time, high_to_low-level output	$\overline{MR}$ to RESET, RSTVDD, RSTSENSE delay $V_{DD} \geq 1.1 \times V_{IT}$ , $V_{IL} = 0.3 \times V_{DD}$ , $V_{IH} = 0.7 \times V_{DD}$		1	5	$\mu\text{s}$

### TIMING REQUIREMENTS

$R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ , and  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

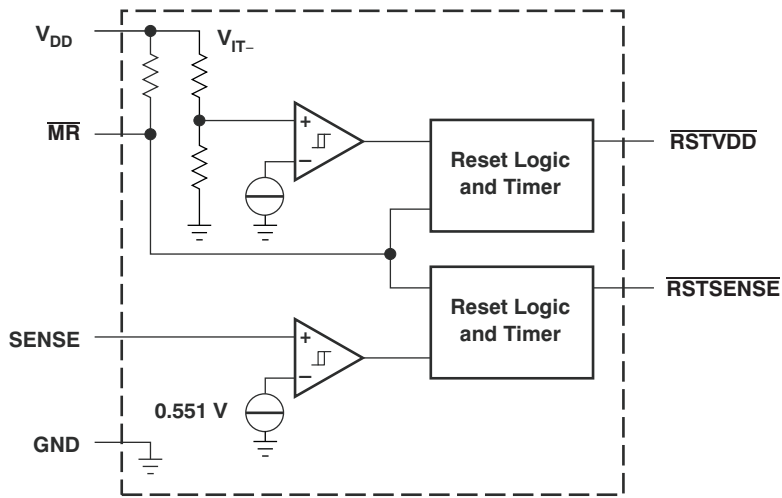
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{T(OUT)}$	Time-out period	at WDI $V_{DD} \geq 0.85\text{ V}$	0.55	1.1	1.65	s
$t_W$	Pulse width	at $V_{DD}$ $V_{IH} = 1.1 \times V_{IT}$ , $V_{IL} = 0.9 \times V_{IT-}$ , $V_{IT-} = 0.86\text{ V}$	20			$\mu\text{s}$
		at $\overline{MR}$ $V_{DD} \geq V_{IT} + 0.2\text{ V}$ , $V_{IL} = 0.3 \times V_{DD}$ , $V_{IH} = 0.7 \times V_{DD}$	0.1			
		at SENSE $V_{DD} \geq V_{IT}$ , $V_{IH} = 1.1 \times V_{IT-(S)}$ , $V_{IL} = 0.9 \times V_{IT-(S)}$	20			
		at PFI $V_{DD} \geq 0.85\text{ V}$ , $V_{IH} = 1.1 \times V_{IT-(S)}$ , $V_{IL} = 0.9 \times V_{IT-(S)}$	20			
		at WDI $V_{DD} \geq V_{IT}$ , $V_{IL} = 0.3 \times V_{DD}$ , $V_{IH} = 0.7 \times V_{DD}$	0.3			

### FUNCTIONAL BLOCK DIAGRAMS

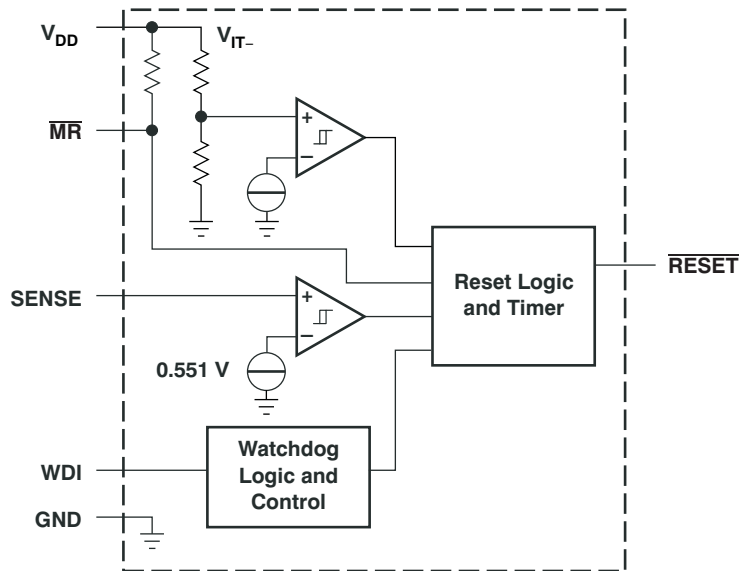


**FUNCTIONAL BLOCK DIAGRAMS (continued)**

**TPS3106**



**TPS3110**



**Table 1. TPS3103 FUNCTION TABLE**

MR	$V_{(PFI)} > 0.551\text{ V}$	$V_{DD} > V_{IT}$	RESET	PFO
L	0	X <sup>(1)</sup>	L	L
L	1	X	L	H
H	0	0	L	L
H	0	1	H	L
H	1	0	L	H
H	1	1	H	H

(1) X = Don't care

**Table 2. TPS3106 FUNCTION TABLE**

MR	$V_{(SENSE)} > 0.551\text{ V}$	$V_{DD} > V_{IT}$	RSTVDD	RSTSENSE
L	X <sup>(1)</sup>	X	L	L
H	0	0	L	L
H	0	1	H	L
H	1	0	L	H
H	1	1	H	H

(1) X = Don't care

**Table 3. TPS3110 FUNCTION TABLE<sup>(1)</sup>**

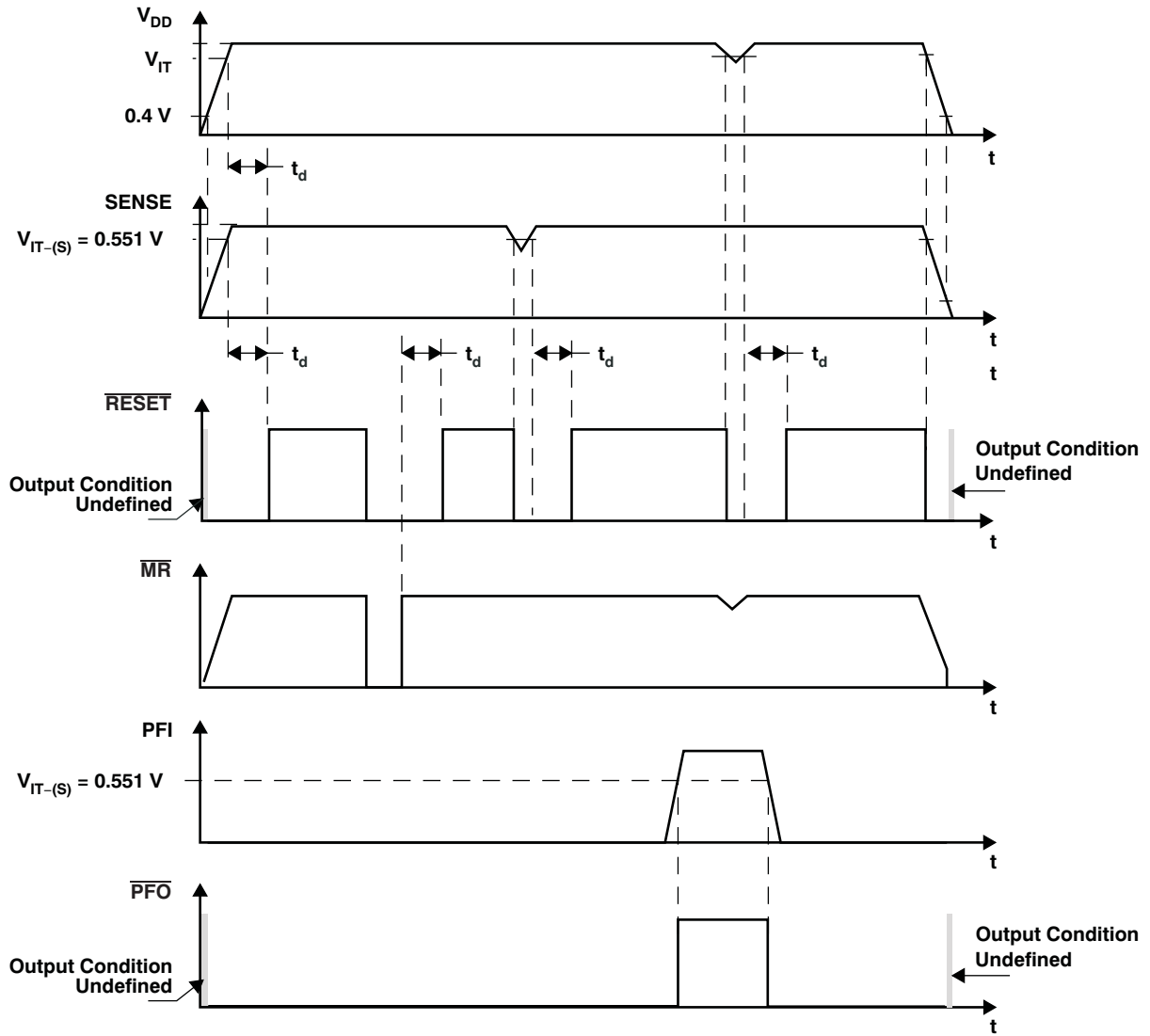
MR	$V_{(SENSE)} > 0.551\text{ V}$	$V_{DD} > V_{IT}$	RESET
L	X <sup>(2)</sup>	X	L
H	0	0	L
H	0	1	L
H	1	0	L
H	1	1	H

(1) Function of watchdog timer not shown

(2) X = Don't care

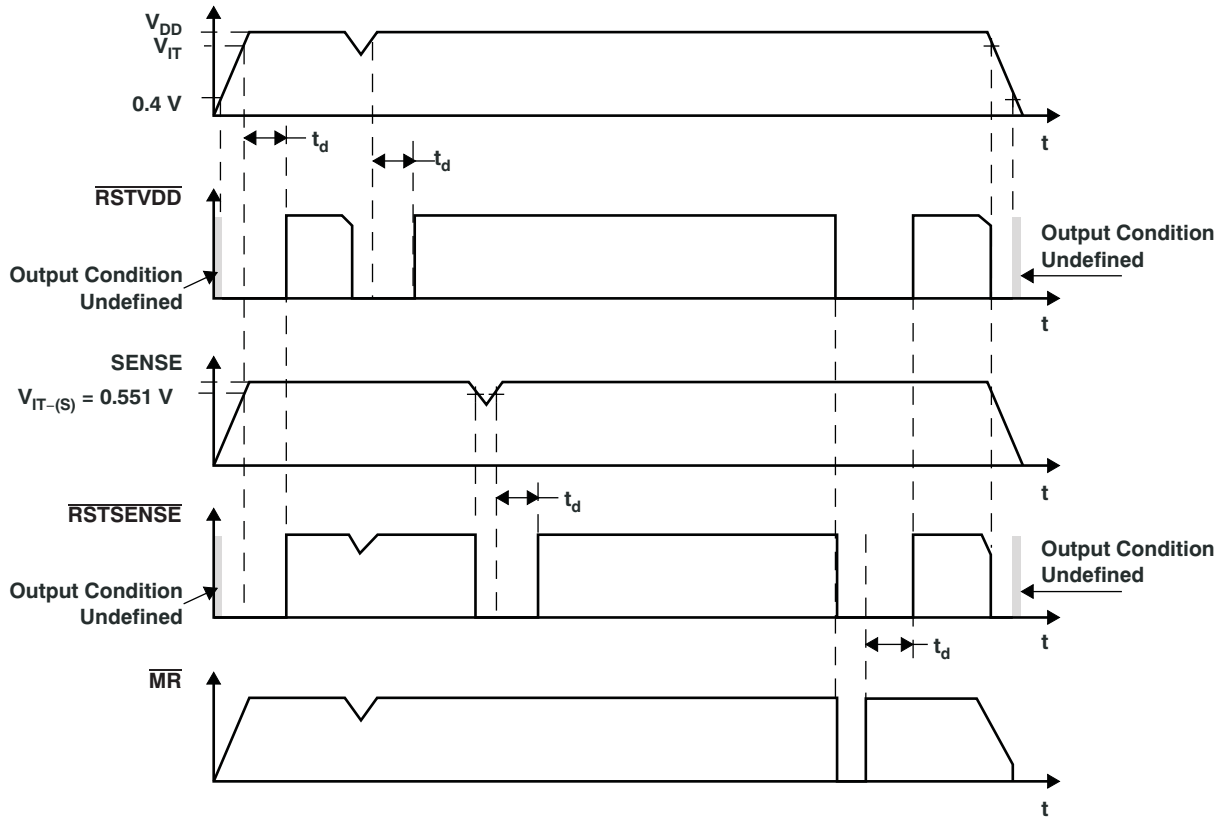


**TIMING DIAGRAMS**



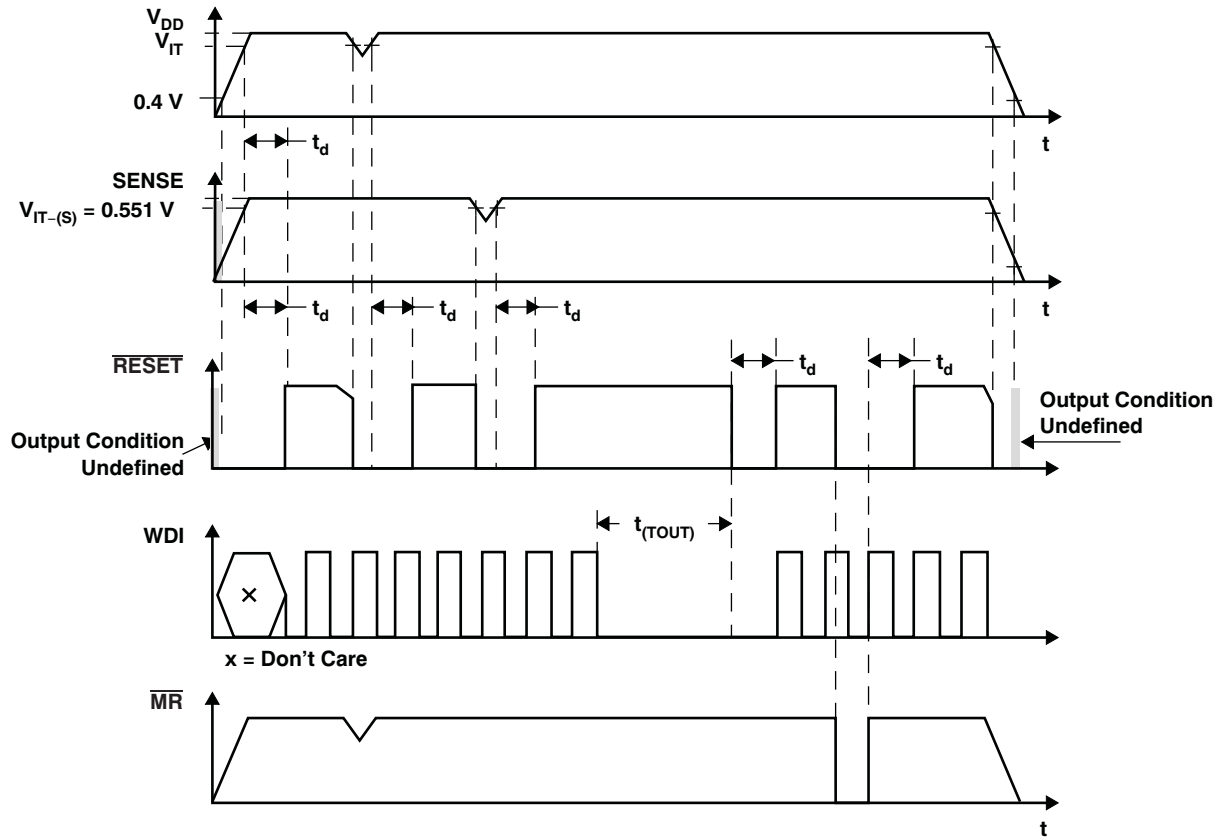
**Figure 1. TPS3103 Timing**

**TIMING DIAGRAMS (continued)**



**Figure 2. TPS3106 Timing**

**TIMING DIAGRAMS (continued)**



**Figure 3. TPS3110 Timing**

TYPICAL CHARACTERISTICS

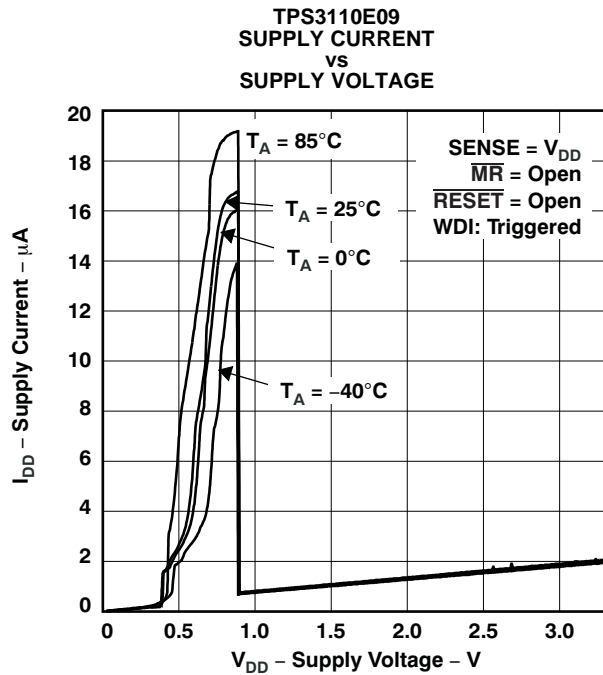


Figure 4.

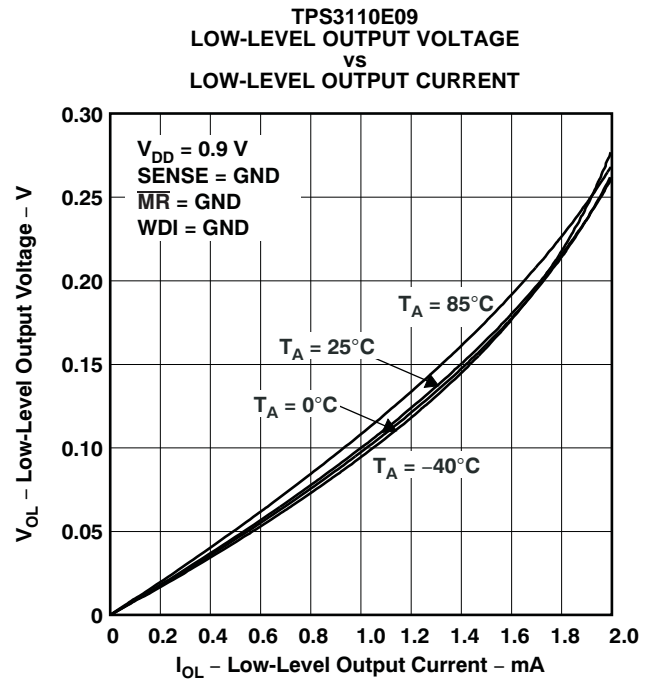


Figure 5.

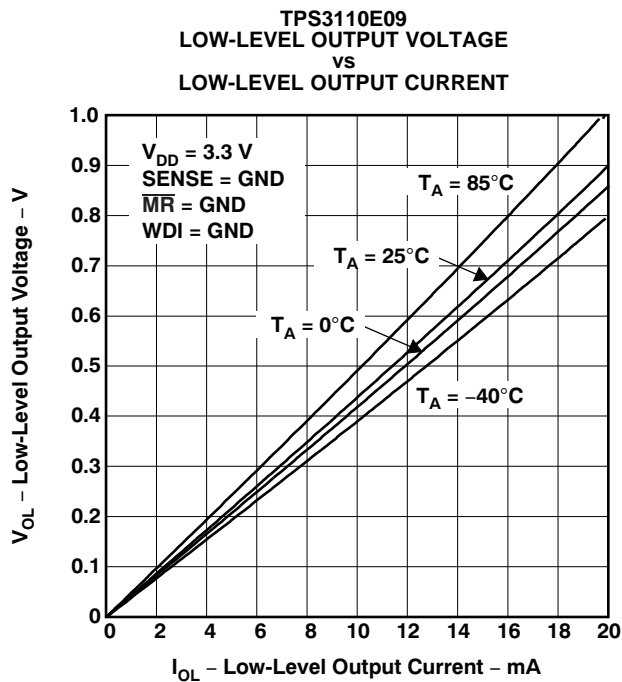


Figure 6.

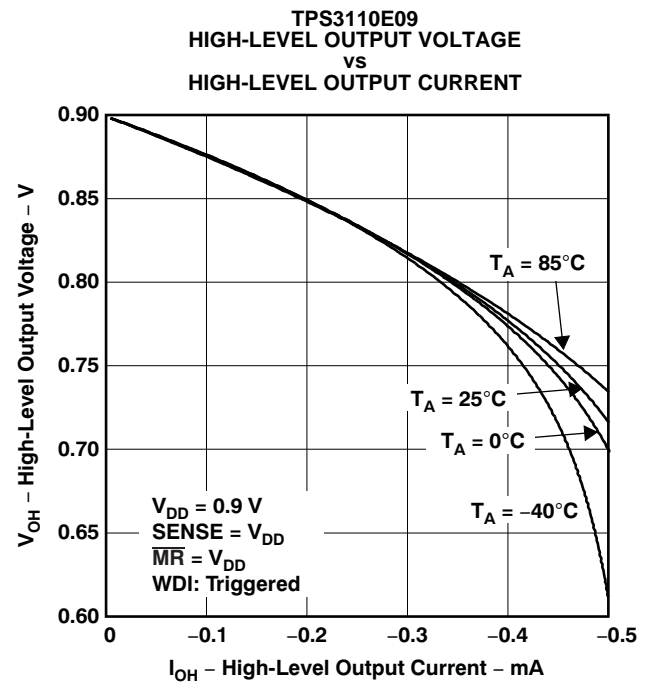


Figure 7.

**TYPICAL CHARACTERISTICS (continued)**

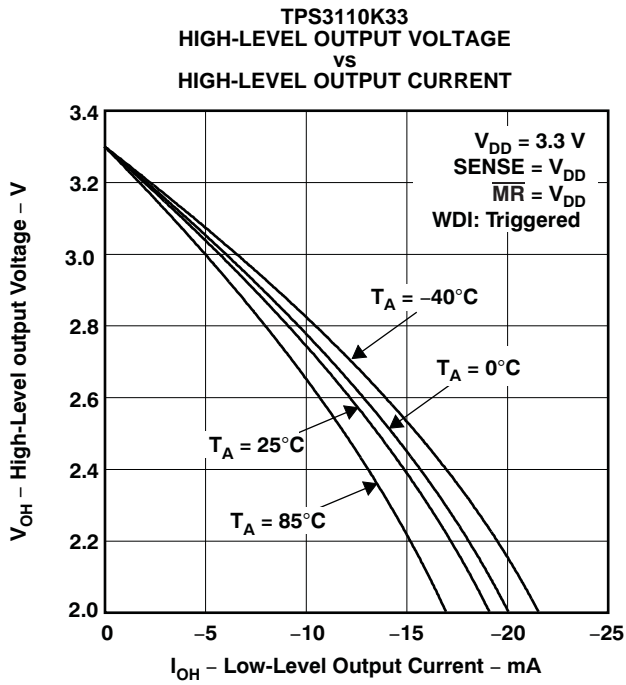


Figure 8.

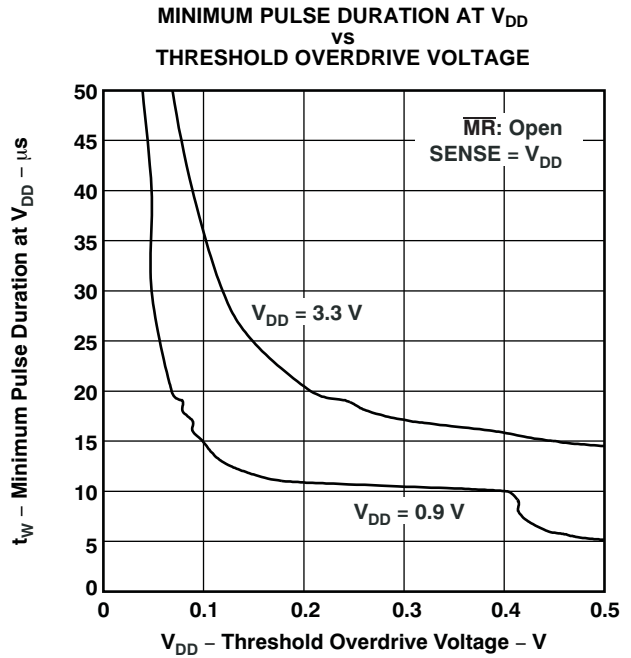


Figure 9.

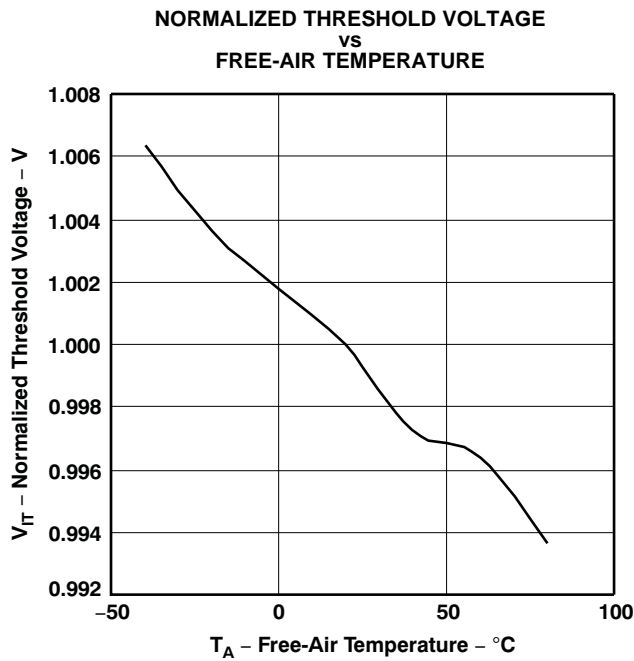


Figure 10.

## APPLICATION INFORMATION

The TPS31xx family has a quiescent current in the 1- $\mu$ A to 2- $\mu$ A range. When  $\overline{\text{RESET}}$  is active, triggered by the voltage monitored at  $V_{\text{DD}}$ , the quiescent current increases to about 20  $\mu$ A (see the [Electrical Characteristics](#)).

In some applications, it is necessary to minimize the quiescent current even during the reset period. This is especially true when the voltage of a battery is supervised and the  $\overline{\text{RESET}}$  is used to shut down the system or for an early warning. In this case, the reset condition lasts for a longer period of time. The current drawn from the battery should almost be zero, especially when the battery is discharged.

For this kind of application, either the TPS3103 or TPS3106 is a good fit. To minimize current consumption, select a version where the threshold voltage is lower than the voltage monitored at  $V_{\text{DD}}$ . The TPS3106 has two reset outputs. One output ( $\overline{\text{RSTVDD}}$ ) is triggered from the voltage monitored at  $V_{\text{DD}}$ . The other output ( $\overline{\text{RSTSENSE}}$ ) is triggered from the voltage monitored at SENSE. In the application shown in [Figure 11](#), the TPS3106E09 is used to monitor the input voltage of two NiCd or NiMH cells. The threshold voltage ( $V_{\text{(TH)}} = 0.86$  V) was chosen as low as possible to ensure that the supply voltage is always higher than the threshold voltage at  $V_{\text{DD}}$ . The voltage of the battery is monitored using the SENSE input. The voltage divider was calculated to assert a reset using the  $\overline{\text{RSTSENSE}}$  output at  $2 \times 0.8$  V = 1.6 V.

$$R1 = R2 \times \left( \frac{V_{\text{TRIP}}}{V_{\text{IT(S)}}} - 1 \right) \quad (1)$$

where:

$V_{\text{TRIP}}$  is the voltage of the battery at which a reset is asserted and

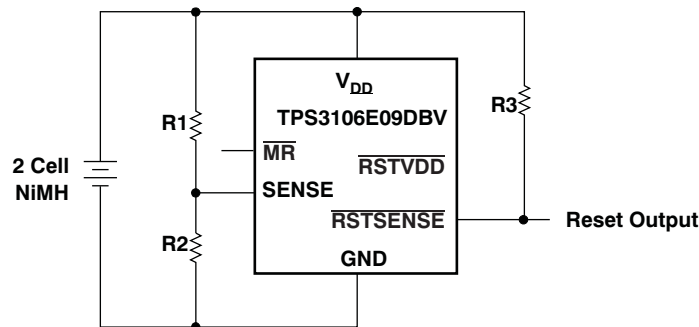
$V_{\text{IT(S)}}$  is the threshold voltage at SENSE = 0.551 V.

R1 was chosen for a resistor current in the 1- $\mu$ A range.

With  $V_{\text{TRIP}} = 1.6$  V:

$$R1 \approx 1.9 \times R2$$

$$R1 = 820 \text{ k}\Omega, R2 = 430 \text{ k}\Omega$$



**Figure 11. Battery Monitoring with 3- $\mu$ A Supply Current for Device and Resistor Divider**

## APPLICATION INFORMATION (continued)

### Watchdog

The TPS3110 device integrates a watchdog timer that must be periodically triggered by a positive or negative transition of WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval,  $\overline{\text{RESET}}$  becomes active for the time period ( $t_D$ ). This event also reinitializes the watchdog timer.

### Manual Reset ( $\overline{\text{MR}}$ )

Many  $\mu\text{C}$ -based products require manual-reset capability, allowing an operator or logic circuitry to initiate a reset. Logic low at  $\overline{\text{MR}}$  asserts reset. Reset remains asserted while  $\overline{\text{MR}}$  is low and for a time period ( $t_D$ ) after  $\overline{\text{MR}}$  returns high. The input has an internal 100-k $\Omega$  pullup resistor, so it can be left open if it is unused.

Connect a normally open momentary switch from  $\overline{\text{MR}}$  to GND to create a manual reset function. External debounce is not required. If  $\overline{\text{MR}}$  is driven from long cables or if the device is used in noisy environments, connecting a 0.1- $\mu\text{F}$  capacitor from  $\overline{\text{MR}}$  to GND provides additional noise immunity.

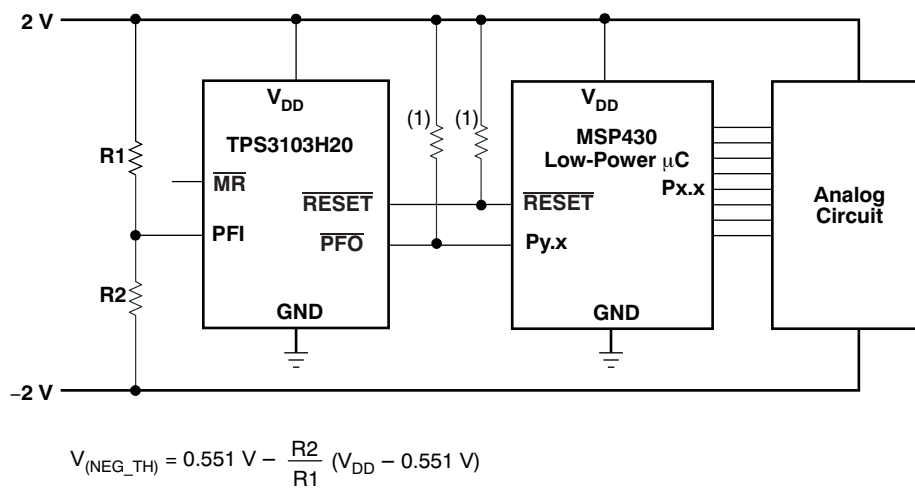
### PFI, $\overline{\text{PFO}}$

The TPS3103 has an integrated power-fail input (PFI) comparator with a separate open-drain power-fail output ( $\overline{\text{PFO}}$ ). The PFI and  $\overline{\text{PFO}}$  can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The PFI is compared with an internal voltage reference of 0.551 V. If the input voltage falls below the power-fail threshold ( $V_{\text{IT-(S)}}$ ), the  $\overline{\text{PFO}}$  goes low. If it goes above 0.551 V plus approximately 15-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltage above 0.551 V. The sum of both resistors should be approximately 1 M $\Omega$ , to minimize power consumption and to ensure that the current into the PFI pin can be neglected, compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, connect PFI to GND and leave  $\overline{\text{PFO}}$  unconnected. For proper operation of the PFI comparator, the supply voltage ( $V_{\text{DD}}$ ) must be higher than 0.8 V.

### SENSE

The voltage at the SENSE input is compared with a reference voltage of 0.551 V. If the voltage at SENSE falls below the sense-threshold ( $V_{\text{IT-(S)}}$ ), reset is asserted. On the TPS3106, a dedicated  $\overline{\text{RSTSENSE}}$  output is available. On the TPS3110, the logic signal from SENSE is OR-wired with the logic signal from  $V_{\text{DD}}$  or  $\overline{\text{MR}}$ . An internal timer delays the return of the output to the inactive state, once the voltage at SENSE goes above 0.551 V plus about 15 mV of hysteresis. For proper operation of the SENSE comparator, the supply voltage must be higher than 0.8 V.



(1) Resistor may be integrated in  $\mu\text{C}$ .

Figure 12. TPS3103 Monitoring a Negative Voltage

APPLICATION INFORMATION (continued)

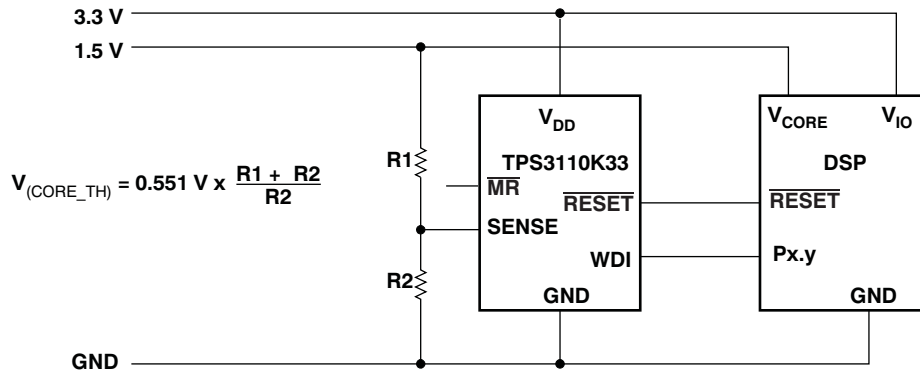


Figure 13. TPS3110 in a DSP System Monitoring Both Supply Voltages



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3106K33MDBVREP	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AAVM	<a href="#">Samples</a>
V62/06643-07XE	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AAVM	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3106K33MDBVREP	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**



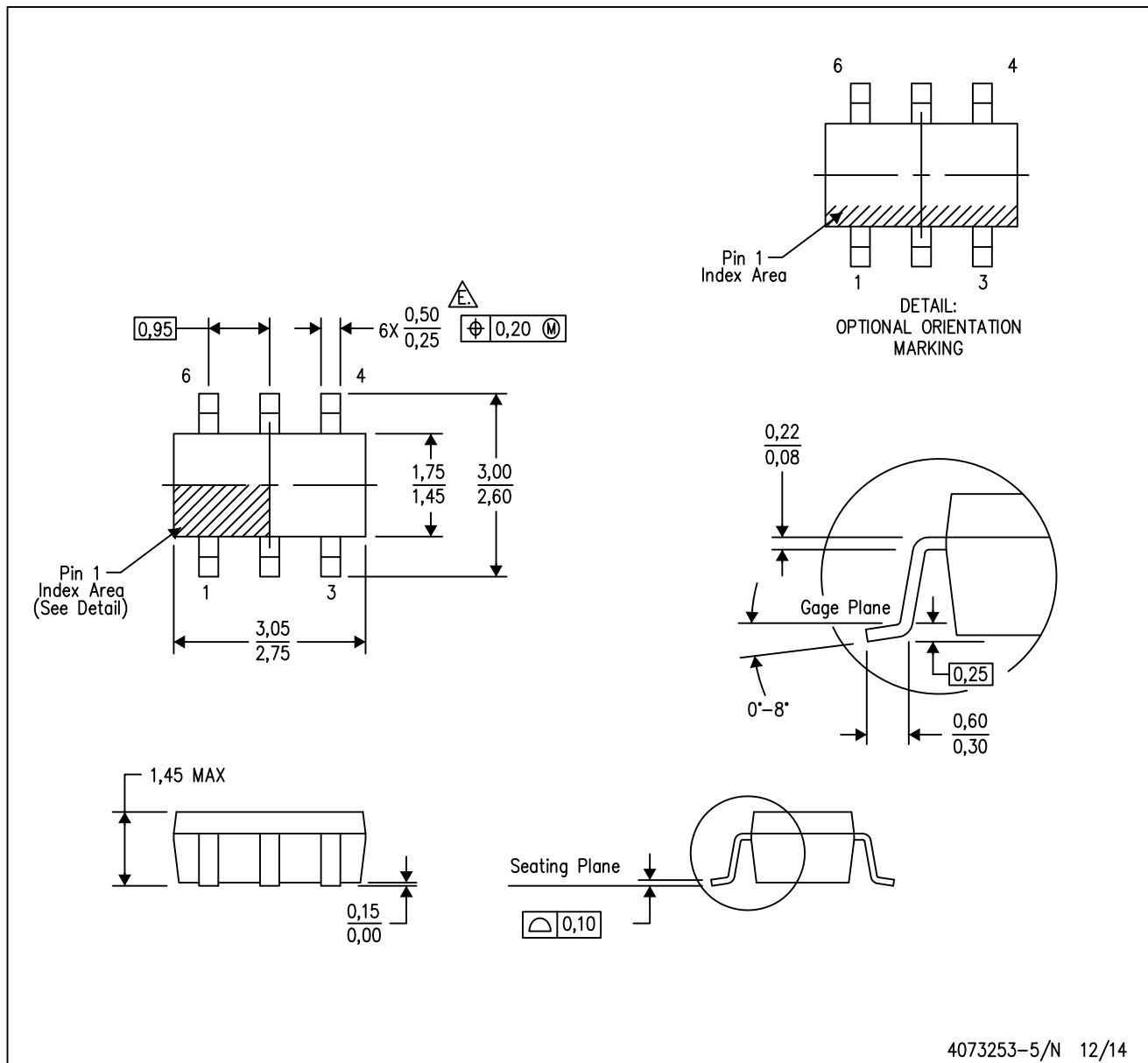
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3106K33MDBVREP	SOT-23	DBV	6	3000	182.0	182.0	20.0

# MECHANICAL DATA

DBV (R-PDSO-G6)

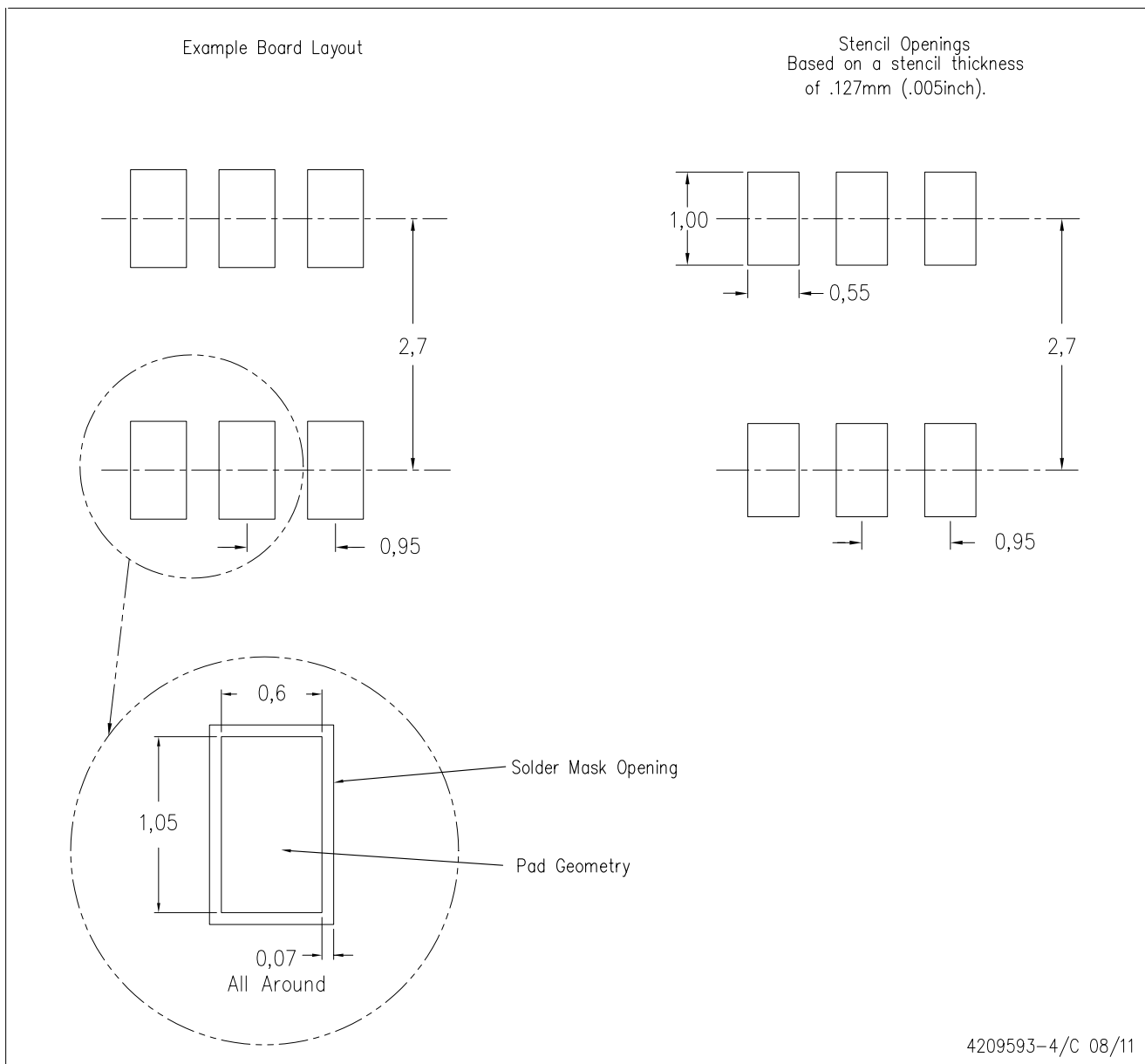
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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