Multi-Purpose Flash (MPF) + SRAM ComboMemory

SST32HF201 / SST32HF202 / SST32HF401 / SST32HF402

Preliminary Specifications

FEATURES:

- **MPF + SRAM ComboMemory**
  - SST32HF201: 128K x16 Flash + 64K x16 SRAM
  - SST32HF202: 128K x16 Flash + 128K x16 SRAM
  - SST32HF401: 256K x16 Flash + 64K x16 SRAM
  - SST32HF402: 256K x16 Flash + 128K x16 SRAM
- **Single 2.7-3.3V Read and Write Operations**
- **Concurrent Operation**
  - Read from or write to SRAM while Erase/Program Flash
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 15 mA (typical) for Flash or SRAM Read
  - Standby Current: 20 µA (typical)
- **Flexible Erase Capability**
  - Uniform 2 KWord sectors
  - Uniform 32 KWord size blocks
- **Fast Read Access Times:**
  - Flash: 70 and 90 ns
  - SRAM: 70 and 90 ns
- **Latched Address and Data for Flash**
- **Flash Fast Erase and Word-Program:**
  - Sector-Erase Time: 18 ms (typical)
  - Block-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 70 ms (typical)
  - Word-Program Time: 14 µs (typical)
  - Chip Rewrite Time:
    SST32HF201/202: 2 seconds (typical)
    SST32HF401/402: 4 seconds (typical)
- **Flash Automatic Erase and Program Timing**
  - Internal V_{PP} Generation
- **Flash End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **CMOS I/O Compatibility**
- **JEDEC Standard Command Set**
- **Conforms to Flash pinout**
- **Package Available**
  - 48-ball LFBGA (6mm x 8mm)

PRODUCT DESCRIPTION

The SST32HF20x/40x ComboMemory devices integrate a 128K x16 or 256K x16 CMOS flash memory bank with a 64K x16 or 128K x16 CMOS SRAM memory bank in a Multi-Chip Package (MCP), manufactured with SST's proprietary, high performance SuperFlash technology.

Featuring high performance Word-Program, the flash memory bank provides a maximum Word-Program time of 14 µsec. The entire flash memory bank can be erased and programmed word-by-word in typically 2 seconds for the SST32HF201/202 and 4 seconds for the SST32HF401/402, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent flash write, the SST32HF20x/40x devices contain on-chip hardware and software data protection schemes.The SST32HF20x/40x devices offer a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST32HF20x/40x devices consist of two independent memory banks with respective bank enable signals. The Flash and SRAM memory banks are superimposed in the same memory address space. Both memory banks share common address lines, data lines, WE# and OE#. The memory bank selection is done by memory bank enable signals. The SRAM bank enable signal, BES# selects the SRAM bank. The flash memory bank enable signal, BEF# selects the flash memory bank. The WE# signal has to be used with Software Data Protection (SDP) command sequence when controlling the Erase and Program operations in the flash memory bank. The SDP command sequence protects the data stored in the flash memory bank from accidental alteration.

The SST32HF20x/40x provide the added functionality of being able to simultaneously read from or write to the SRAM bank while erasing or programming in the flash memory bank. The SRAM memory bank can be read or written while the flash memory bank performs Sector-Erase, Bank-Erase, or Word-Program concurrently. All flash memory Erase and Program operations will automatically latch the input address and data signals and complete the operation in background without further input stimulus requirement. Once the internally controlled Erase or Program cycle in the flash bank has commenced, the SRAM bank can be accessed for Read or Write.

The SST32HF20x/40x devices are suited for applications that use both flash memory and SRAM memory to store code or data. For systems requiring low power and small form factor, the SST32HF20x/40x devices significantly improve performance and reliability, while lowering power

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consumption, when compared with multiple chip solutions. The SST32HF20x/40x inherently use less energy during erase and program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

Device Operation

The ComboMemory uses BES# and BEF# to control operation of either the SRAM or the flash memory bank. When BES# is low, the SRAM Bank is activated for Read and Write operation. When BEF# is low the flash bank is activated for Read, Program or Erase operation. BES# and BEF# cannot be at low level at the same time. If BES# and BEF# are both asserted to low level bus contention will result and the device may suffer permanent damage. All address, data, and control lines are shared by SRAM Bank and flash bank which minimizes power consumption and loading. The device goes into standby when both bank enables are high.

SRAM Operation

With BES# low and BEF# high, the SST32HF201/401 operate as 64K x16 CMOS SRAM, and the SST32HF202/402 operates as 128K x16 CMOS SRAM, with fully static operation requiring no external clocks or timing strobes. The SST32HF201/401 SRAM is mapped into the first 64 KWord address space of the device, and the SST32HF202/402 SRAM is mapped into the first 128 KWord address space. When BES# and BEF# are high, both memory banks are deselected and the device enters standby mode. Read and Write cycle times are equal. The control signals UBS# and LBS# provide access to the upper data byte and lower data byte. See Table 3 for SRAM read and write data byte control modes of operation.

SRAM Read

The SRAM Read operation of the SST32HF20x/40x is controlled by OE# and BES#, both have to be low with WE# high for the system to obtain data from the outputs. BES# is used for SRAM bank selection. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. See Figure 2 for the Read cycle timing diagram.

SRAM Write

The SRAM Write operation of the SST32HF20x/40x is controlled by WE# and BES#, both have to be low for the system to write to the SRAM. During the Word-Write operation, the addresses and data are referenced to the rising edge of either BES# or WE#, whichever occurs first. The write time is measured from the last falling edge to the first rising edge of BES# or WE#. See Figures 3 and 4 for the Write cycle timing diagrams.

Flash Operation

With BEF# active, the SST32HF201/202 operate as 128K x16 flash memory and the SST32HF401/402 operates as 256K x16 flash memory. The flash memory bank is read using the common address lines, data lines, WE# and OE#. Erase and Program operations are initiated with the JEDEC standard SDP command sequences. Address and data are latched during the SDP commands and during the internally timed Erase and Program operations.

Flash Read

The Read operation of the SST32HF20x/40x devices is controlled by BEF# and OE#. Both have to be low, with WE# high, for the system to obtain data from the outputs. BEF# is used for flash memory bank selection. When BEF# and BES# are high, both banks are deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to Figure 5 for further details.

Flash Erase/Program Operation

SDP commands are used to initiate the flash memory bank Program and Erase operations of the SST32HF20x/40x. SDP commands are loaded to the flash memory bank using standard microprocessor write sequences. A command is loaded by asserting WE# low while keeping BEF# low and OE# high. The address is latched on the falling edge of WE# or BEF#, whichever occurs last. The data is latched on the rising edge of WE# or BEF#, whichever occurs first.

Flash Word-Program Operation

The flash memory bank of the SST32HF20x/40x devices is programmed on a word-by-word basis. Before Program operations, the memory must be erased first. The Program

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operation consists of three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load word address and word data. During the Word-Program operation, the addresses are latched on the falling edge of either BEF# or WE#, whichever occurs last. The data is latched on the rising edge of either BEF# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or BEF#, whichever occurs first. The Program operation, once initiated, will be completed, within 20 µs. See Figures 6 and 7 for WE# and BEF# controlled Program operation timing diagrams and Figure 17 for flowcharts. During the Program operation, the only valid flash Read operations are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any SDP commands loaded during the internal Program operation will be ignored.

Flash Sector/Block-Erase Operation

The Flash Sector/Block-Erase operation allows the system to erase the device on a sector-by-sector (or block-by-block) basis. The SST32HF20x/40x offer both Sector-Erase and Block-Erase mode. The sector architecture is based on uniform sector size of 2 KWord. The Block-Erase mode is based on uniform block size of 32 KWord. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The address lines A_{16}-A_{11}, for SST32HF201/202, and A_{17}-A_{11}, for SST32HF401/402, are used to determine the sector address. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (50H) and block address (BA) in the last bus cycle. The address lines A_{16}-A_{15}, for SST32HF201/202, and A_{17}-A_{15}, for SST32HF401/402, are used to determine the block address. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit methods. See Figures 11 and 12 for timing waveforms. Any commands issued during the Sector- or Block-Erase operation are ignored.

Flash Chip-Erase Operation

The SST32HF20x/40x provide a Chip-Erase operation, which allows the user to erase the entire memory array to the “1” state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 9 for timing diagram, and Figure 20 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.

Write Operation Status Detection

The SST32HF20x/40x provide two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Flash Data# Polling (DQ_7)

When the SST32HF20x/40x flash memory banks are in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. Note that even though DQ_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles, after an interval of 1 µs. During internal Erase operation, any attempt to read DQ_7 will produce a ‘0’. Once the internal Erase operation is completed, DQ_7 will produce a ‘1’. The Data# Polling is valid after the rising edge of the fourth WE# (or BEF#) pulse for Program operation. For Sector- or Block-Erase, the Data# Polling is valid after the rising edge of the sixth WE# (or BEF#) pulse. See Figure 8 for Data# Polling timing diagram and Figure 18 for a flowchart.

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Flash Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating '1's and '0's, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the toggling will stop. The flash memory bank is then ready for the next operation. The Toggle Bit is valid after the rising edge of the fourth WE# (or BEF#) pulse for Program operation. For Sector- or Bank-Erase, the Toggle Bit is valid after the rising edge of the sixth WE# (or BEF#) pulse. See Figure 9 for Toggle Bit timing diagram and Figure 18 for a flowchart.

Flash Memory Data Protection

The SST32HF20x/40x flash memory bank provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Flash Hardware Data Protection

Noise/Glitch Protection: A WE# or BEF# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, BEF# high, or WE# high will inhibit the Flash Write operation. This prevents inadvertent writes during power-up or power-down.

Flash Software Data Protection (SDP)

The SST32HF20x/40x provide the JEDEC approved software data protection scheme for all flash memory bank data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte load sequence. The SST32HF20x/40x devices are shipped with the software data protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid SDP commands will abort the device to the read mode, within Read Cycle Time (T_{RC}).

Concurrent Read and Write Operations

The SST32HF20x/40x provide the unique benefit of being able to read from or write to SRAM, while simultaneously erasing or programming the Flash. This allows data alteration code to be executed from SRAM, while altering the data in Flash. The following table lists all valid states.

CONCURRENT READ/WRITE STATE TABLE

Flash	SRAM
Program/Erase	Read
Program/Erase	Write

The device will ignore all SDP commands when an Erase or Program operation is in progress. Note that Product Identification commands use SDP; therefore, these commands will also be ignored while an Erase or Program operation is in progress.

Product Identification

The Product Identification mode identifies the devices as the SST32HF20x/40x and manufacturer as SST. **This mode may be accessed by software operations only. The hardware device ID Read operation, which is typically used by programmers, cannot be used on this device because of the shared lines between flash and SRAM in the multi-chip package. Therefore, application of high voltage to pin A_9 may damage this device.** Users may use the software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Tables 3 and 4 for software operation, Figure 13 for the software ID entry and Read timing diagram, and Figure 19 for the ID entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	0000H	00BFH
Device ID		
SST32HF201/202	0001H	2789H
SST32HF401/402	0001H	2780H

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Product Identification Mode Exit/Reset

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Exit ID command sequence, which returns the device to the Read operation. Please note that the software-reset command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 14 for timing waveform and Figure 19 for a flowchart.

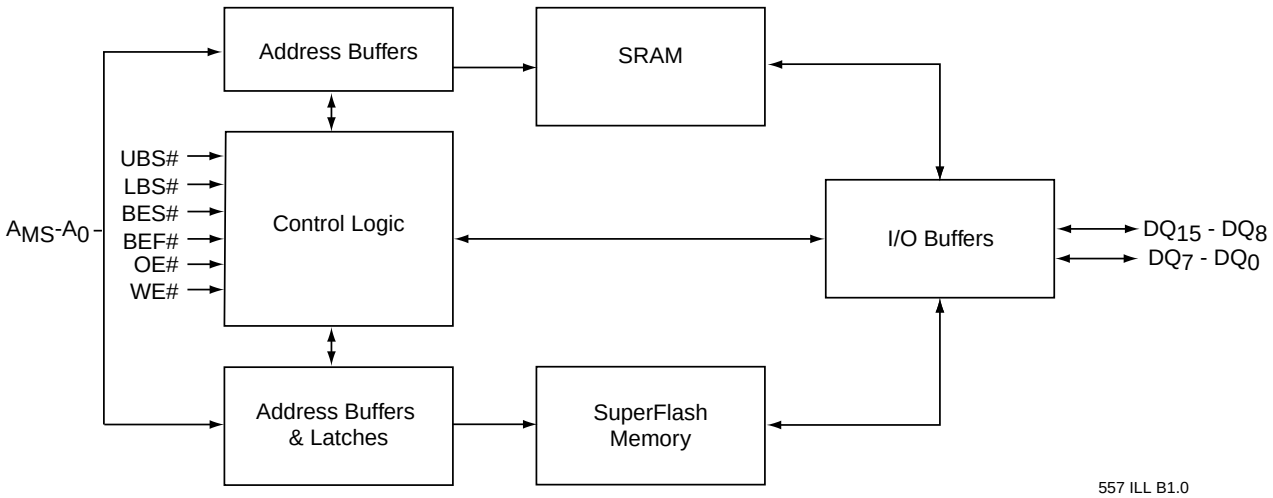
Design Considerations

SST recommends a high frequency 0.1 µF ceramic capacitor to be placed as close as possible between V_{DD} and V_{SS}, e.g., less than 1 cm away from the V_{DD} pin of the

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device. Additionally, a low frequency 4.7 µF electrolytic capacitor from V_{DD} to V_{SS} should be placed within 1 cm of the V_{DD} pin.

FUNCTIONAL BLOCK DIAGRAM



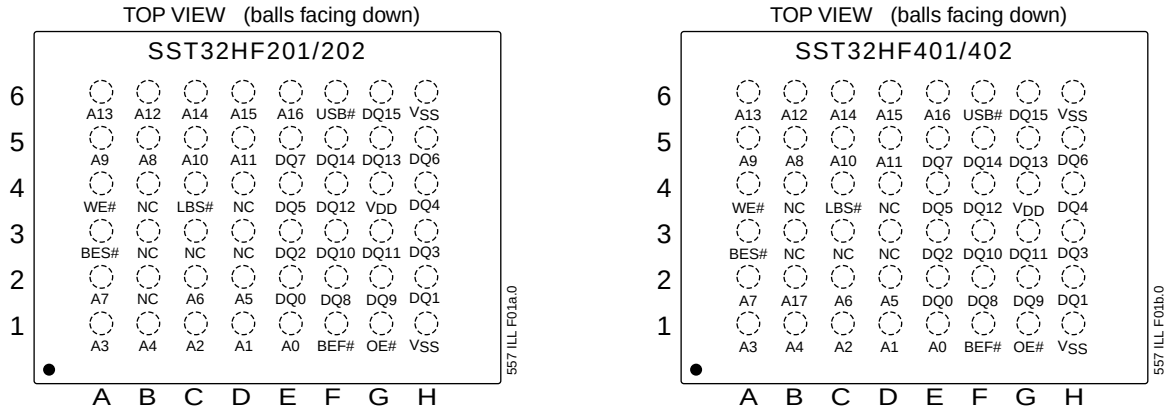


FIGURE 1: PIN ASSIGNMENTS FOR 48-BALL LFBGA

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{MS}[1]-A_0	Address Inputs	To provide flash addresses, A_{16}-A_0 for 2M and A_{17}-A_0 for 4M. To provide SRAM addresses, A_{15}-A_0 for 1M and A_{16}-A_0 for 2M.
DQ_{15}-DQ_0	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a flash Erase/Program cycle. The outputs are in tri-state when OE# or BES# and BEF# are high.
BES#	SRAM Memory Bank Enable	To activate the SRAM memory bank when BES# is low.
BEF#	Flash Memory Bank Enable	To activate the Flash memory bank when BEF# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the Write operations.
V_{DD}	Power Supply	2.7-3.3V power supply
V_{SS}	Ground	
UBS#	Upper Byte Control (SRAM)	To enable DQ_{15}-DQ_8
LBS#	Lower Byte Control (SRAM)	To enable DQ_7-DQ_0
NC	No Connection	Unconnected Pins

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1. A_{MS} = Most significant address

TABLE 3: OPERATION MODES SELECTION

Mode	BES#[1]	BEF#[1]	OE#	WE#	UBS#	LBS#	DQ_{15} to DQ_8	DQ_7 to DQ_0	Address
Not Allowed	V_{IL}	V_{IL}	X[2]	X	X	X	X	X	X
Flash									
Read	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	D_{OUT}	A_{IN}
Program	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	D_{IN}	A_{IN}
Erase	X	V_{IL}	V_{IH}	V_{IL}	X	X	X	X	Sector or Block address, XXH for Chip-Erase
SRAM									
Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	D_{OUT}	D_{OUT}	A_{IN}
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	High Z	A_{IN}
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	High Z	D_{OUT}	A_{IN}
Write	V_{IL}	V_{IH}	X	V_{IL}	V_{IL}	V_{IL}	D_{IN}	D_{IN}	A_{IN}
	V_{IL}	V_{IH}	X	V_{IL}	V_{IL}	V_{IH}	D_{IN}	High Z	A_{IN}
	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	High Z	D_{IN}	A_{IN}
Standby	V_{IHC}	V_{IHC}	X	X	X	X	High Z	High Z	X
Flash Write Inhibit	X	X	V_{IL}	X	X	X	High Z / D_{OUT}	High Z / D_{OUT}	X
	X	X	X	V_{IH}	X	X	High Z / D_{OUT}	High Z / D_{OUT}	X
	X	V_{IH}	X	X	X	X	High Z / D_{OUT}	High Z / D_{OUT}	X
Output Disable	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	High Z	X
	V_{IL}	V_{IH}	X	X	V_{IH}	V_{IH}	High Z	High Z	X
	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	High Z	High Z	X
Product Identification									
Software Mode	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	Manufacturer's ID (00BFH) Device ID[3]		A_{MSF}[4]-A_1=V_{IL}, A_0=V_{IH} (See Table 4)

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1. Do not apply BES#=V_{IL} and BEF#=V_{IL} at the same time
2. X can be V_{IL} or V_{IH}, but no other value.
3. Device ID for: SST32HF201/202 = 2789H and SST32HF401/402 = 2780H
4. A_{MS} = Most significant flash address

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TABLE 4: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Word-Program	5555H	AAH	2AAAH	55H	5555H	A0H	WA[2]	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA_X[3]	30H
Block-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	BA_X[3]	50H
Chip-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry[4,5]	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	XXH	F0H										
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

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1. Address format A_{14}-A_0 (Hex),Address A_{15} can be V_{IL} or V_{IH}, but no other value, for the Command sequence.
2. WA = Program Word address
3. SA_X for Sector-Erase; uses A_{MS}-A_{11} address lines
   BA_X for Block-Erase; uses A_{MS}-A_{15} address lines
   A_{MS} = Most significant address
   A_{MS} = A_{16} for SST32HF201/202 and A_{17} for SST32HF401/402
4. The device does not remain in Software Product ID mode if powered down.
5. With A_{MS}-A_1 = 0; SST Manufacturer's ID = 00BFH, is read with A_0 = 0,
   SST32HF201/202 Device ID = 2789H, is read with A_0 = 1,
   SST32HF401/402 Device ID = 2780H, is read with A_0 = 1.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Operating Temperature . . . . . -20°C to +85°C
Storage Temperature . . . . . -65°C to +125°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.3V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . . 240°C
Output Short Circuit Current[1] . . . . . 50 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	2.7-3.3V
Extended	-20°C to +85°C	2.7-3.3V

AC CONDITIONS OF TEST

Input Rise/Fall Time	5 ns
Output Load	C_L = 30 pF
See Figures 15 and 16	

TABLE 5: DC OPERATING CHARACTERISTICS (V_{DD} = V_{DDF} AND V_{DDS} = 2.7-3.3V)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current				Address input=V_{IL}/V_{IH}, at f=1/T_{RC} Min, V_{DD}=V_{DD} Max, all DQs open
	Read				OE#=V_{IL}, WE#=V_{IH}
	Flash		20	mA	BEF#=V_{IL}, BES#=V_{IH}
	SRAM		20	mA	BEF#=V_{IH}, BES#=V_{IL}
	Concurrent Operation		45	mA	BEF#=V_{IH}, BES#=V_{IL}
	Write				WE#=V_{IL}
	Flash		25	mA	BEF#=V_{IL}, BES#=V_{IH}, OE#=V_{IH}
	SRAM		20	mA	BEF#=V_{IH}, BES#=V_{IL}
I_{SB}	Standby V_{DD} Current		30	µA	V_{DD}=V_{DD} Max, BEF#=BES#=V_{IHC}
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage		0.8	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	0.7 V_{DD}		V	V_{DD}=V_{DD} Max
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	V_{DD}=V_{DD} Max
V_{OLF}	Flash Output Low Voltage		0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OHF}	Flash Output High Voltage	V_{DD}-0.2		V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min
V_{OLS}	Output Low Voltage		0.4	V	I_{OL}=1 mA, V_{DD}=V_{DD} Min
V_{OHS}	Output High Voltage	2.2		V	I_{OH}=-500 µA, V_{DD}=V_{DD} Min

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TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Program/Erase Operation	100	µs

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	24 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	12 pF

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: FLASH RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T8.0 557

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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AC CHARACTERISTICS

TABLE 9: SRAM READ CYCLE TIMING PARAMETERS

Symbol	Parameter	SST32HF201/202/401/402-70		SST32HF201/202/401/402-90		Units
		Min	Max	Min	Max	
T_{RCS}	Read Cycle Time	70		90		ns
T_{AAS}	Address Access Time		70		90	ns
T_{BES}	Bank Enable Access Time		70		90	ns
T_{OES}	Output Enable Access Time		35		45	ns
T_{BYES}	UBS#, LBS# Access Time		70		90	ns
T_{BLZS}[1]	BES# to Active Output	0		0		ns
T_{OLZS}[1]	Output Enable to Active Output	0		0		ns
T_{BYLZS}[1]	UBS#, LBS# to Active Output	0		0		ns
T_{BHZS}[1]	BES# to High-Z Output		25		35	ns
T_{OHZS}[1]	Output Disable to High-Z Output	0	25	0	35	ns
T_{BYHZS}[1]	UBS#, LBS# to High-Z Output		35		45	ns
T_{OHS}	Output Hold from Address Change	10		10		ns

T9.0 557

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: SRAM WRITE CYCLE TIMING PARAMETERS

Symbol	Parameter	SST32HF201/202/401/402-70		SST32HF201/202/401/402-90		Units
		Min	Max	Min	Max	
T_{WCS}	Write Cycle Time	70		90		ns
T_{BWS}	Bank Enable to End-of-Write	60		80		ns
T_{AWS}	Address Valid to End-of-Write	60		80		ns
T_{ASTS}	Address Set-up Time	0		0		ns
T_{WPS}	Write Pulse Width	60		80		ns
T_{WRS}	Write Recovery Time	0		0		ns
T_{BYWS}	UBS#, LBS# to End-of-Write	60		80		ns
T_{ODWS}	Output Disable from WE# Low		30		40	ns
T_{OEWS}	Output Enable from WE# High	0		0		ns
T_{DSS}	Data Set-up Time	30		40		ns
T_{DHS}	Data Hold from Write Time	0		0		ns

T10.0 557

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TABLE 11: FLASH READ CYCLE TIMING PARAMETERS

Symbol	Parameter	SST32HF201/202/401/402-70		SST32HF201/202/401/402-90		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	70		90		ns
T_{BE}	Bank Enable Access Time		70		90	ns
T_{AA}	Address Access Time		70		90	ns
T_{OE}	Output Enable Access Time		35		45	ns
T_{BLZ}[1]	BEF# Low to Active Output	0		0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
T_{BHZ}[1]	BEF# High to High-Z Output		20		30	ns
T_{OHZ}[1]	OE# High to High-Z Output		20		30	ns
T_{OH}[1]	Output Hold from Address Change	0		0		ns

T11.0 557

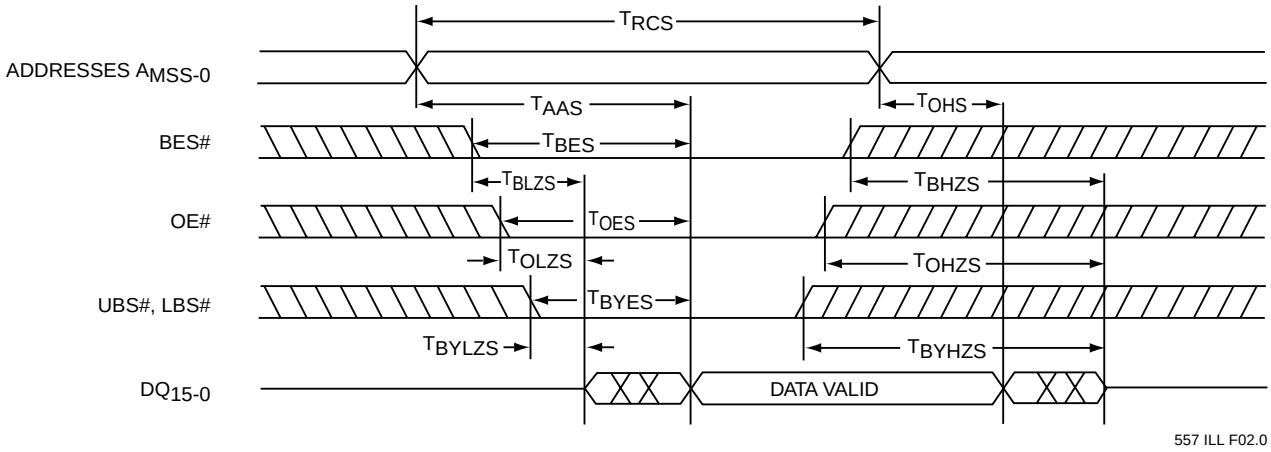
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 12: FLASH PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{BP}	Word-Program Time		20	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	30		ns
T_{BS}	WE# and BEF# Setup Time	0		ns
T_{BH}	WE# and BEF# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{BPW}	BEF# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH}	WE# Pulse Width High	30		ns
T_{BPH}	BEF# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
T_{DH}	Data Hold Time	0		ns
T_{IDA}	Software ID Access and Exit Time		150	ns
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase		100	ms

T12.0 557

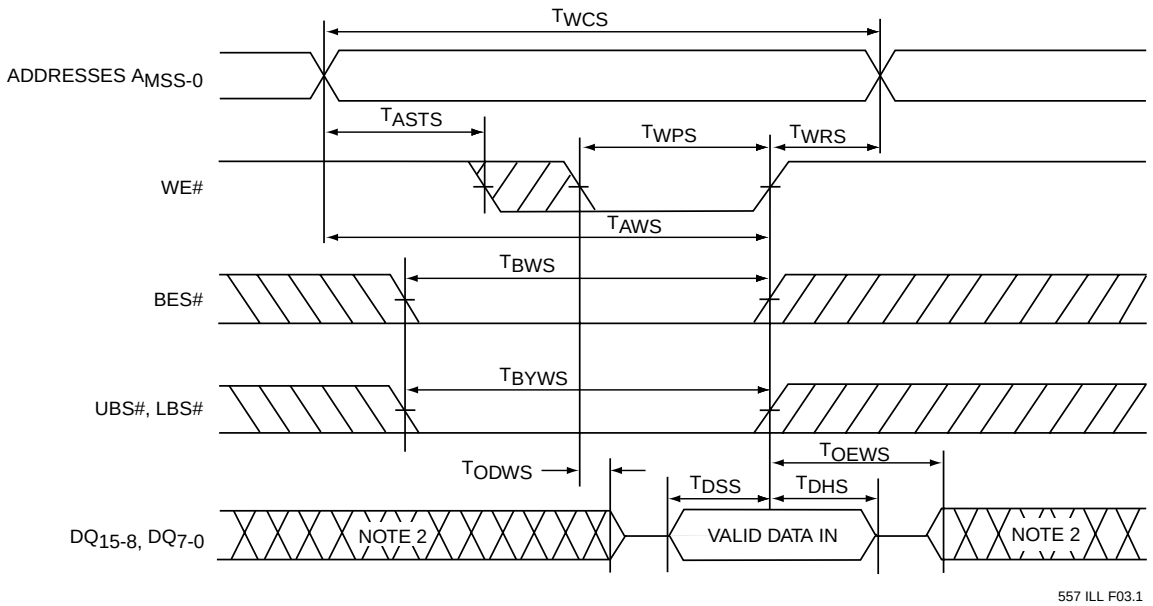
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Note: WE# remains High (V_{IH}) for the Read cycle

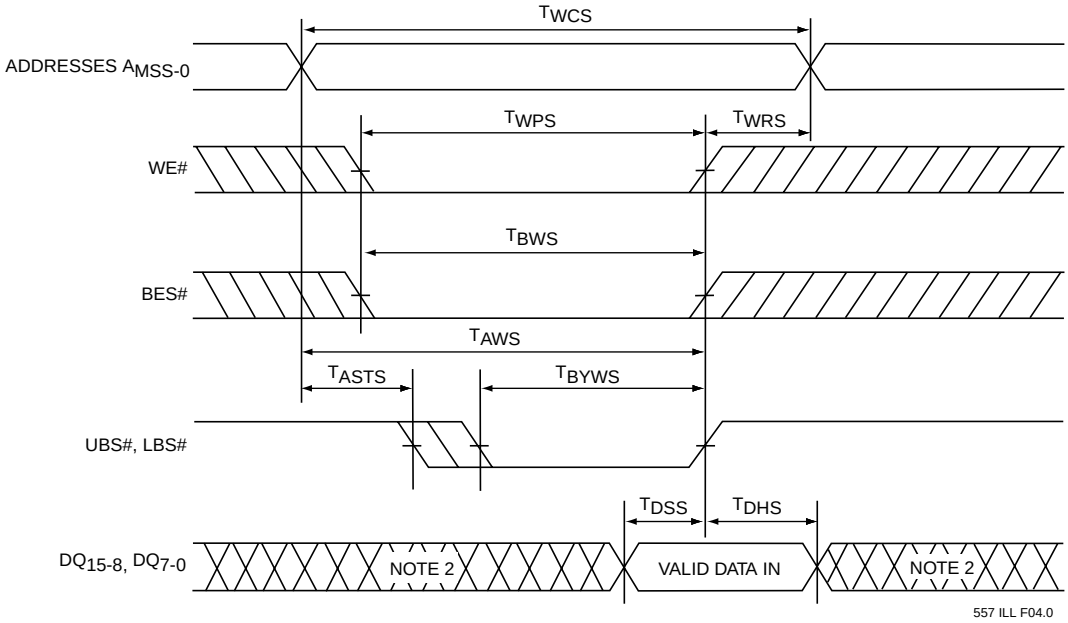
A_{MSS} = Most Significant SRAM Address

FIGURE 2: SRAM READ CYCLE TIMING DIAGRAM



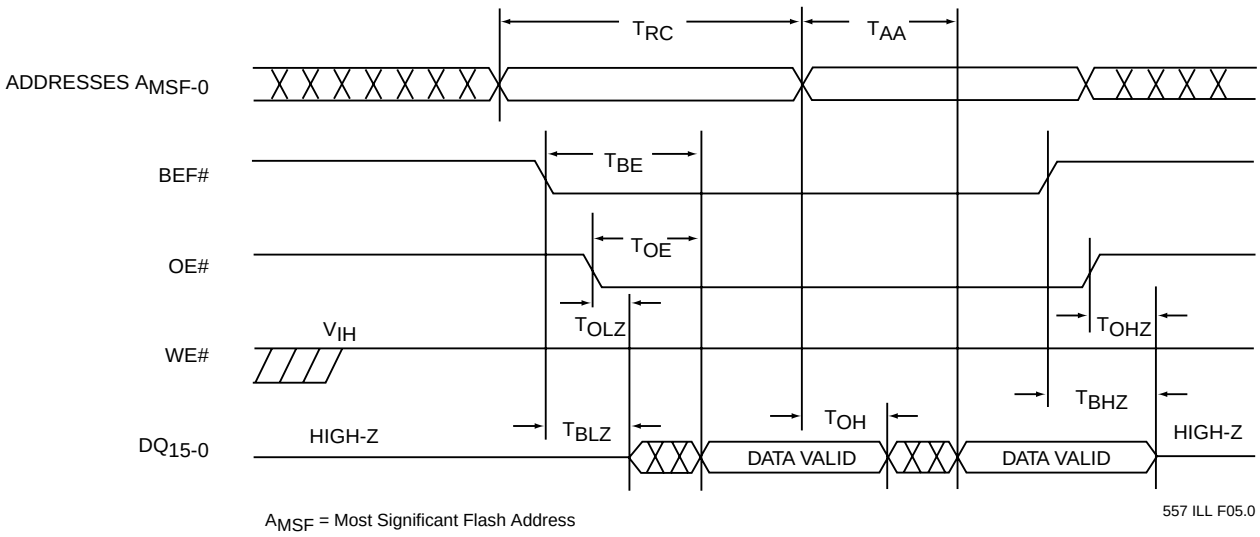
Notes: 1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
2. If BES# goes Low coincident with or after WE# goes Low, the output will remain at high impedance.
If BES# goes High coincident with or before WE# goes High, the output will remain at high impedance.
Because D_{IN} signals may be in the output state at this time, input signals of reverse polarity must not be applied.

FIGURE 3: SRAM WRITE CYCLE TIMING DIAGRAM (WE# CONTROLLED)[1]



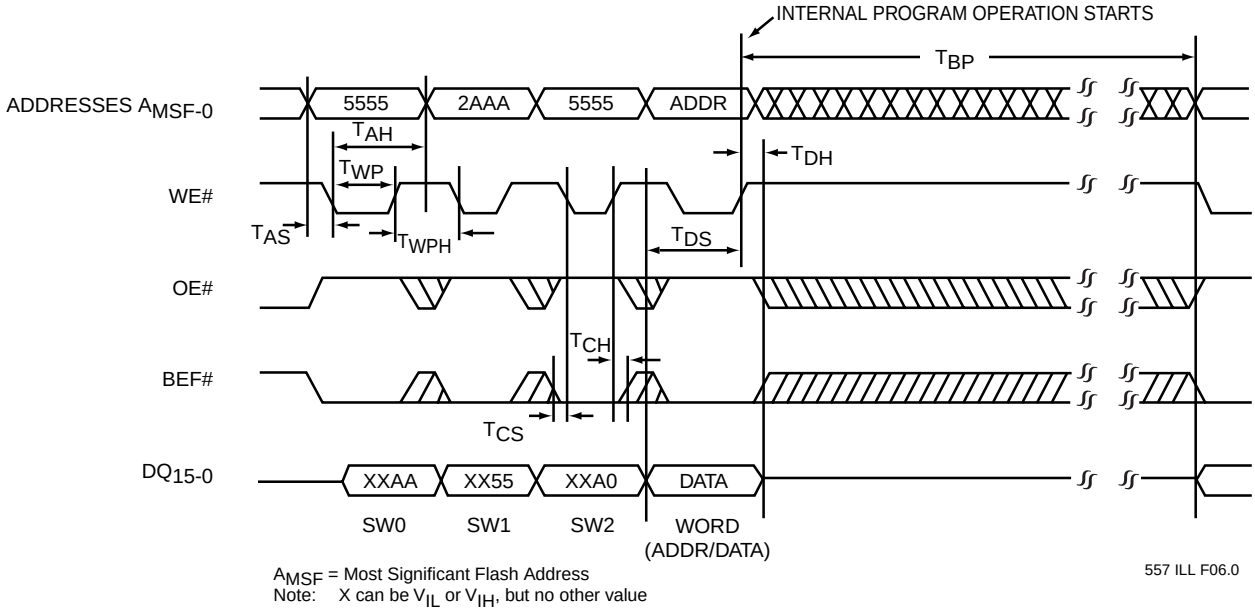
Notes: 1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
2. Because D_{IN} signals may be in the output state at this time, input signals of reverse polarity must not be applied.

FIGURE 4: SRAM WRITE CYCLE TIMING DIAGRAM (UBS#, LBS# CONTROLLED)[1]



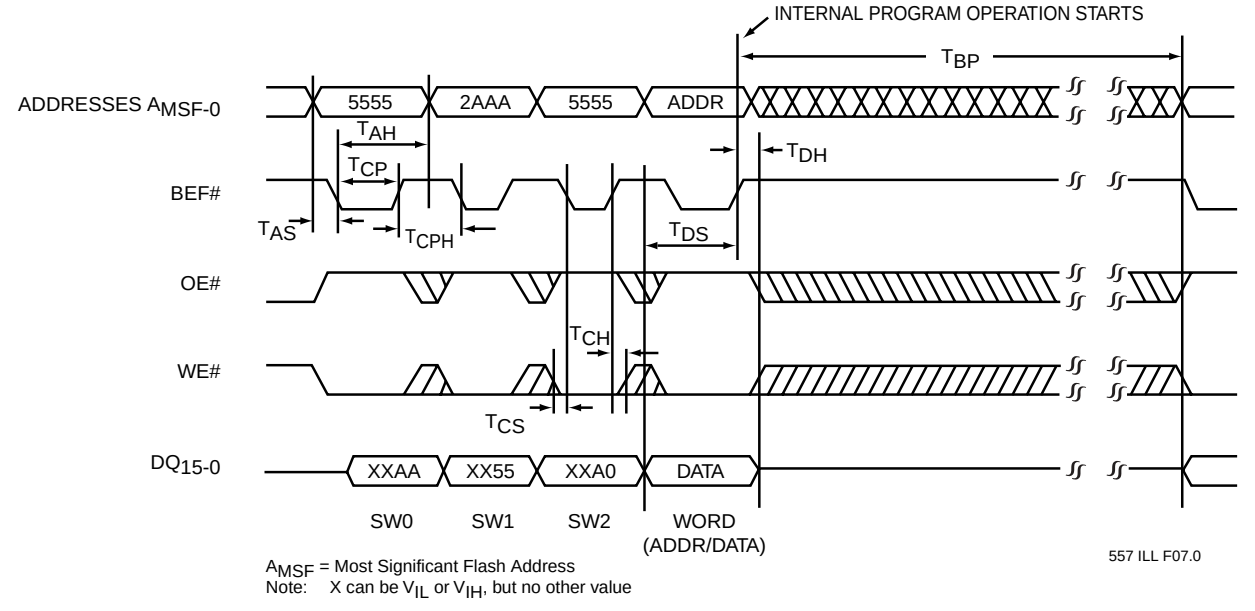
A_{MSF} = Most Significant Flash Address

FIGURE 5: FLASH READ CYCLE TIMING DIAGRAM



A_{MSF} = Most Significant Flash Address
Note: X can be V_{IL} or V_{IH}, but no other value

FIGURE 6: FLASH WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



A_{MSF} = Most Significant Flash Address
Note: X can be V_{IL} or V_{IH}, but no other value

FIGURE 7: BEF# CONTROLLED FLASH PROGRAM CYCLE TIMING DIAGRAM

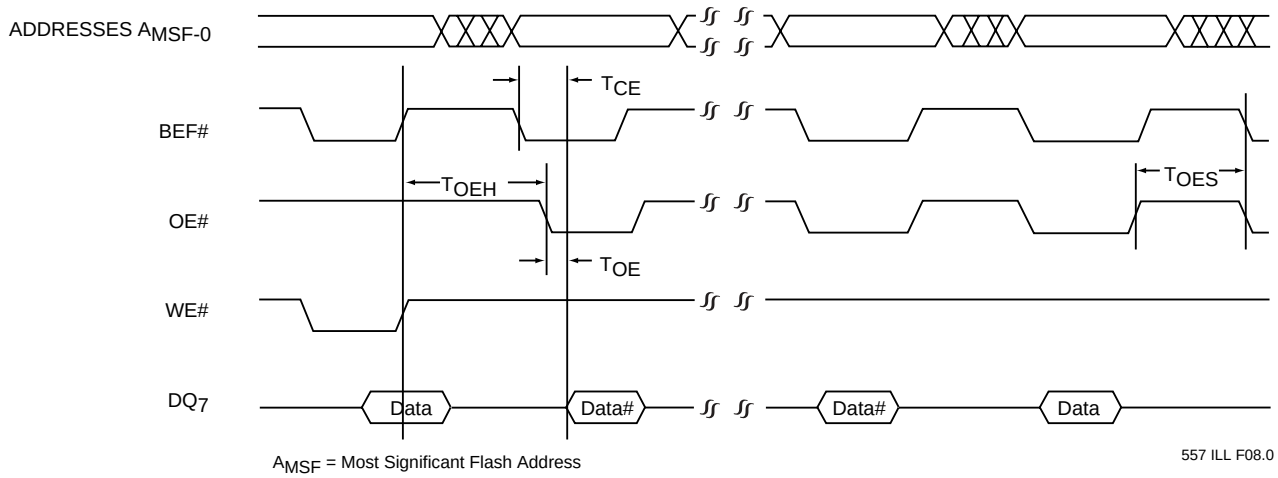


FIGURE 8: FLASH DATA# POLLING TIMING DIAGRAM

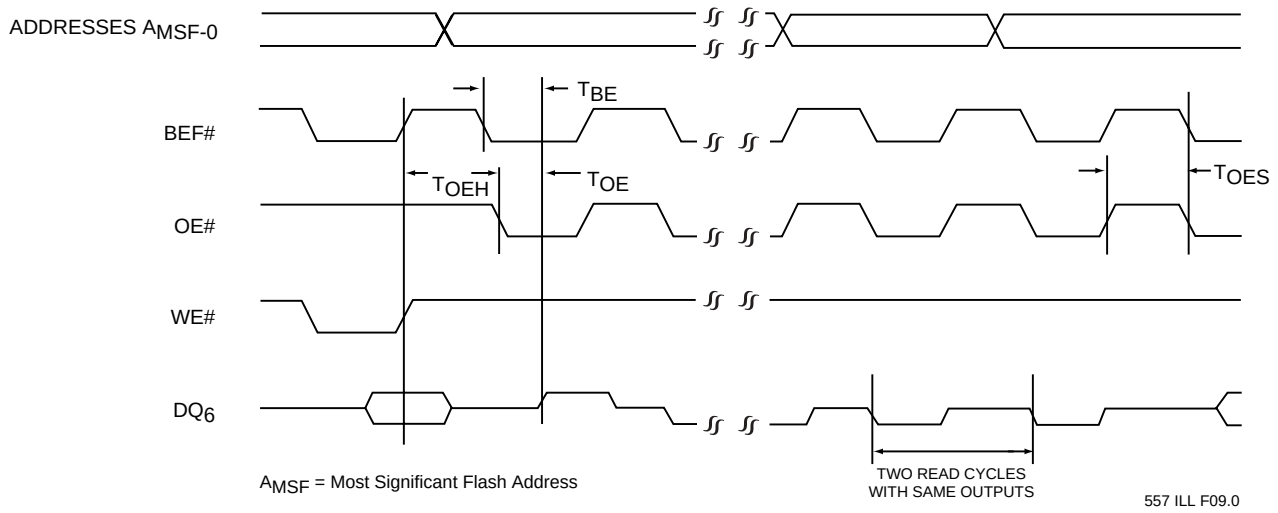
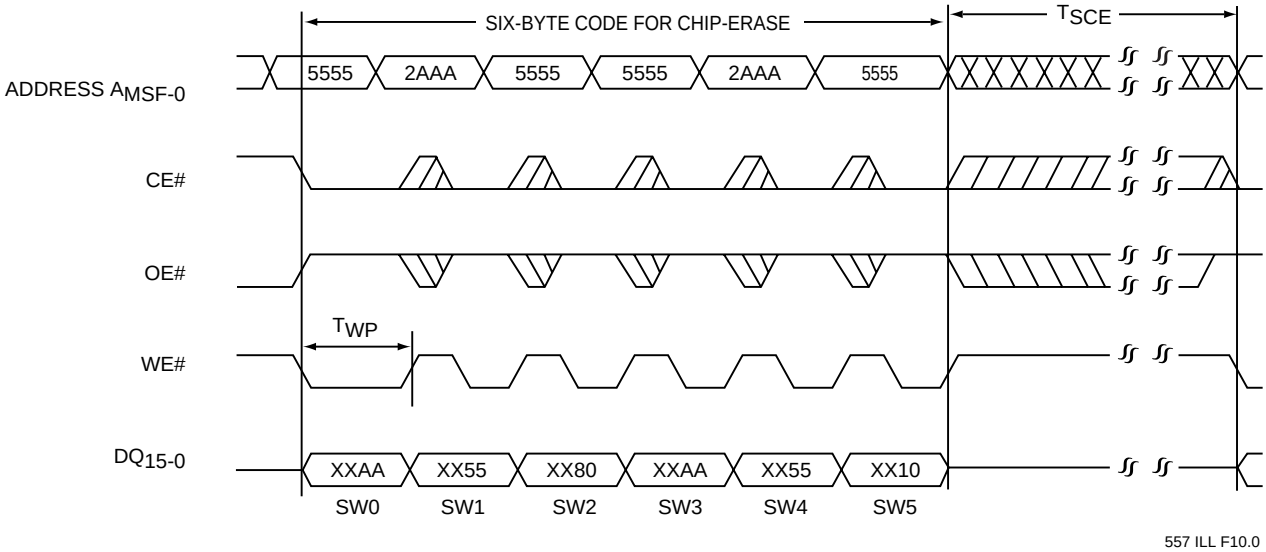
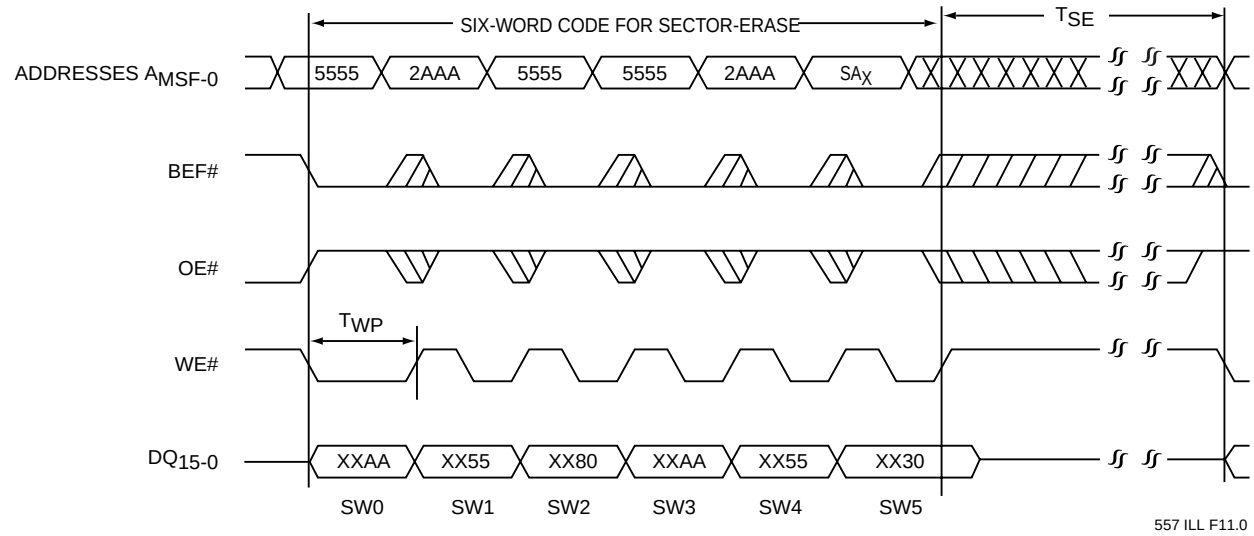


FIGURE 9: FLASH TOGGLE BIT TIMING DIAGRAM



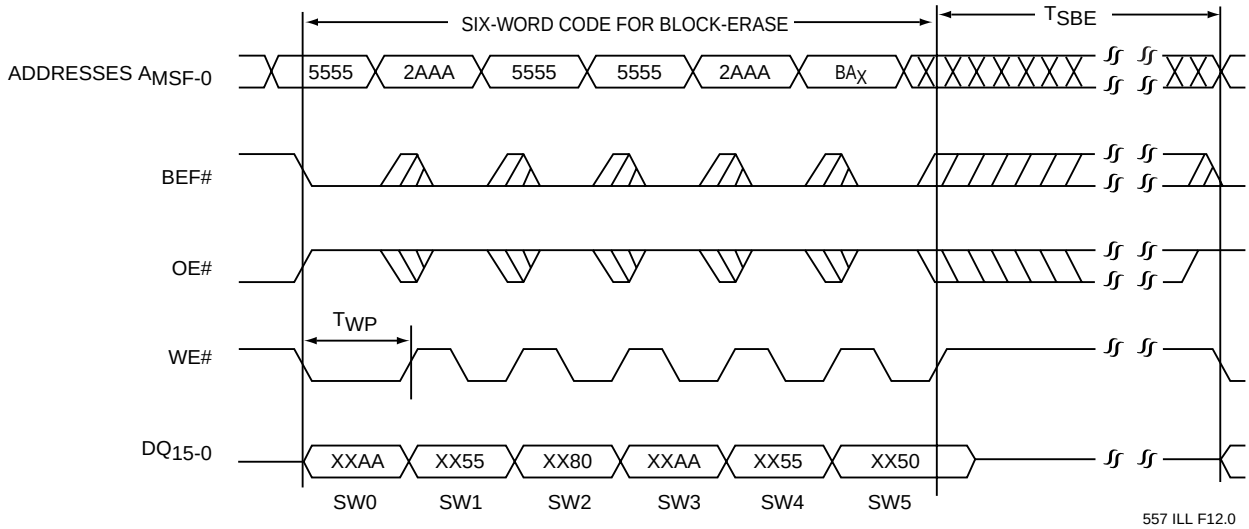
Note: This device also supports CE# controlled Chip-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 12)
X can be V_{IL} or V_{IH}, but no other value
A_{MSF} = Most Significant Flash Address

FIGURE 10: WE# CONTROLLED FLASH CHIP-ERASE TIMING DIAGRAM



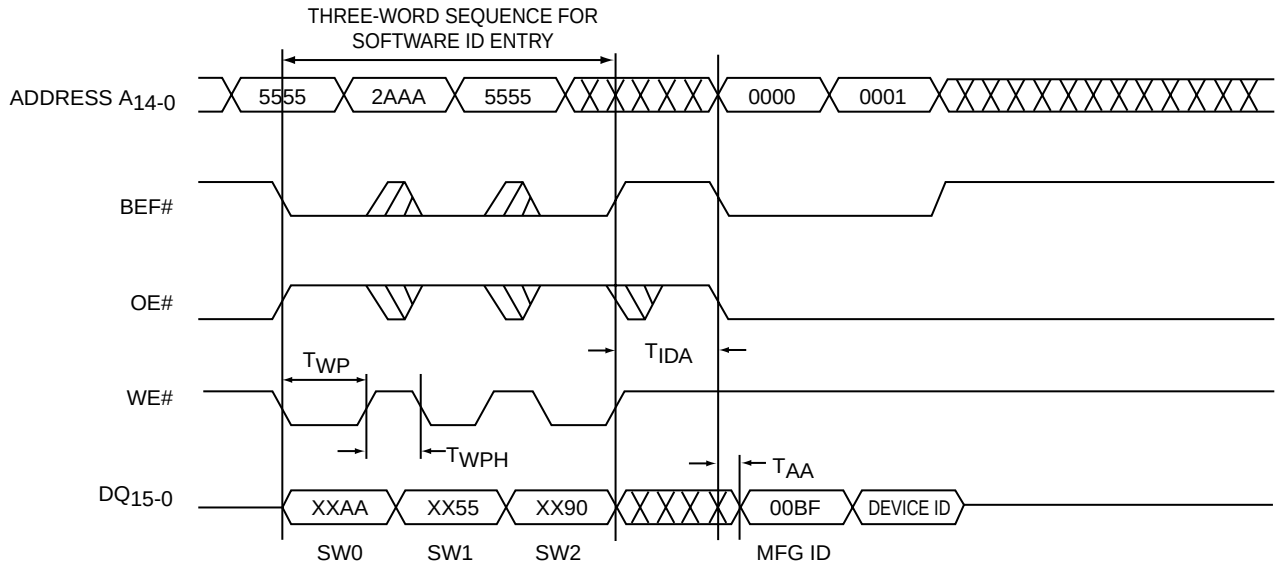
Note: The device also supports BEF# controlled Sector-Erase operation. The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See Table 12)
X can be V_{IL} or V_{IH}, but no other value
SA_X = Sector Address
A_{MSF} = Most Significant Flash Address

FIGURE 11: WE# CONTROLLED FLASH SECTOR-ERASE TIMING DIAGRAM



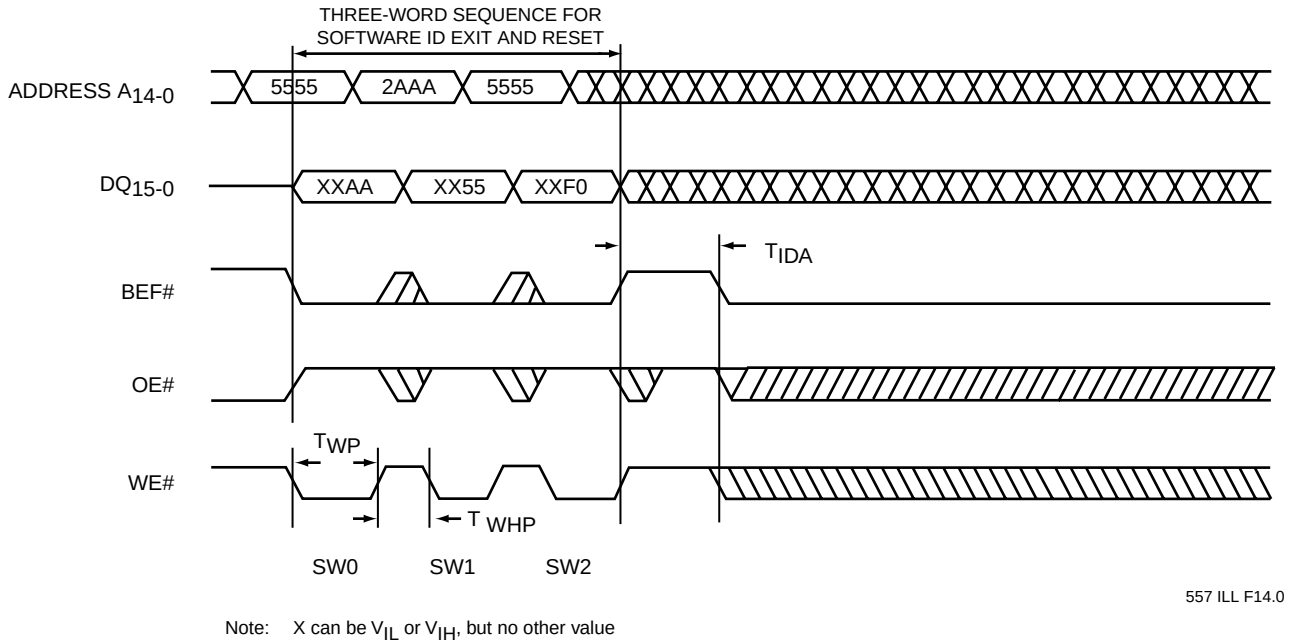
Note: The device also supports BEF# controlled Block-Erase operation. The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See Table 12)
X can be V_{IL} or V_{IH}, but no other value
BA_X = Block Address
A_{MSF} = Most Significant Flash Address

FIGURE 12: WE# CONTROLLED FLASH BLOCK-ERASE TIMING DIAGRAM



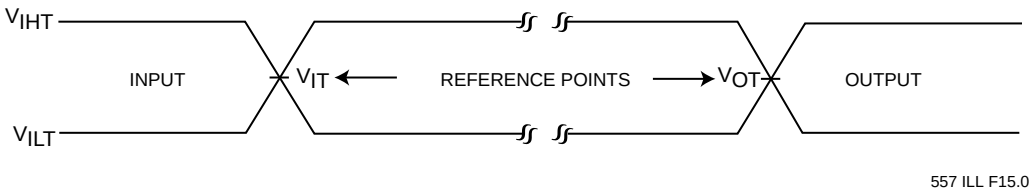
Note: X can be V_{IL} or V_{IH}, but no other value
Device ID = 2789H for SST32VF201/202 and
2780H for SST32VF401/402

FIGURE 13: SOFTWARE ID ENTRY AND READ



Note: X can be V_{IL} or V_{IH}, but no other value

FIGURE 14: SOFTWARE ID EXIT AND RESET



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 15: AC INPUT/OUTPUT REFERENCE WAVEFORMS

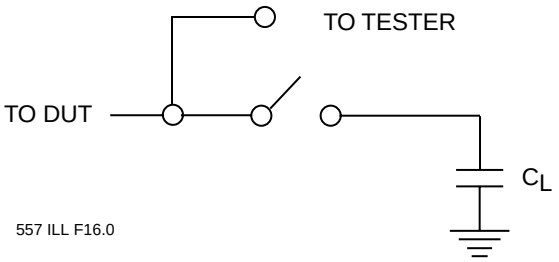
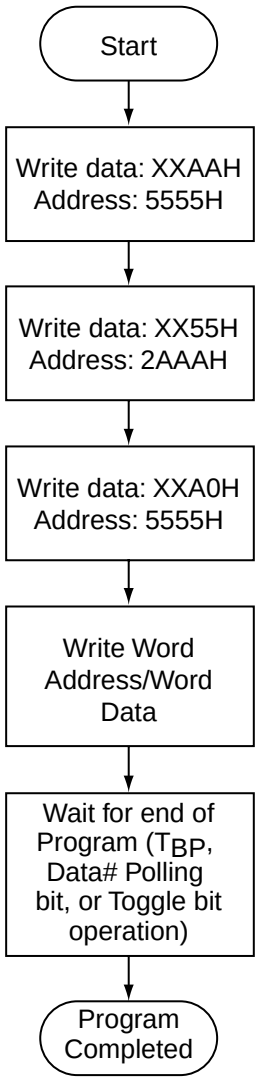


FIGURE 16: A TEST LOAD EXAMPLE



X can be V_{IL} or V_{IH}, but no other value.

FIGURE 17: WORD-PROGRAM ALGORITHM

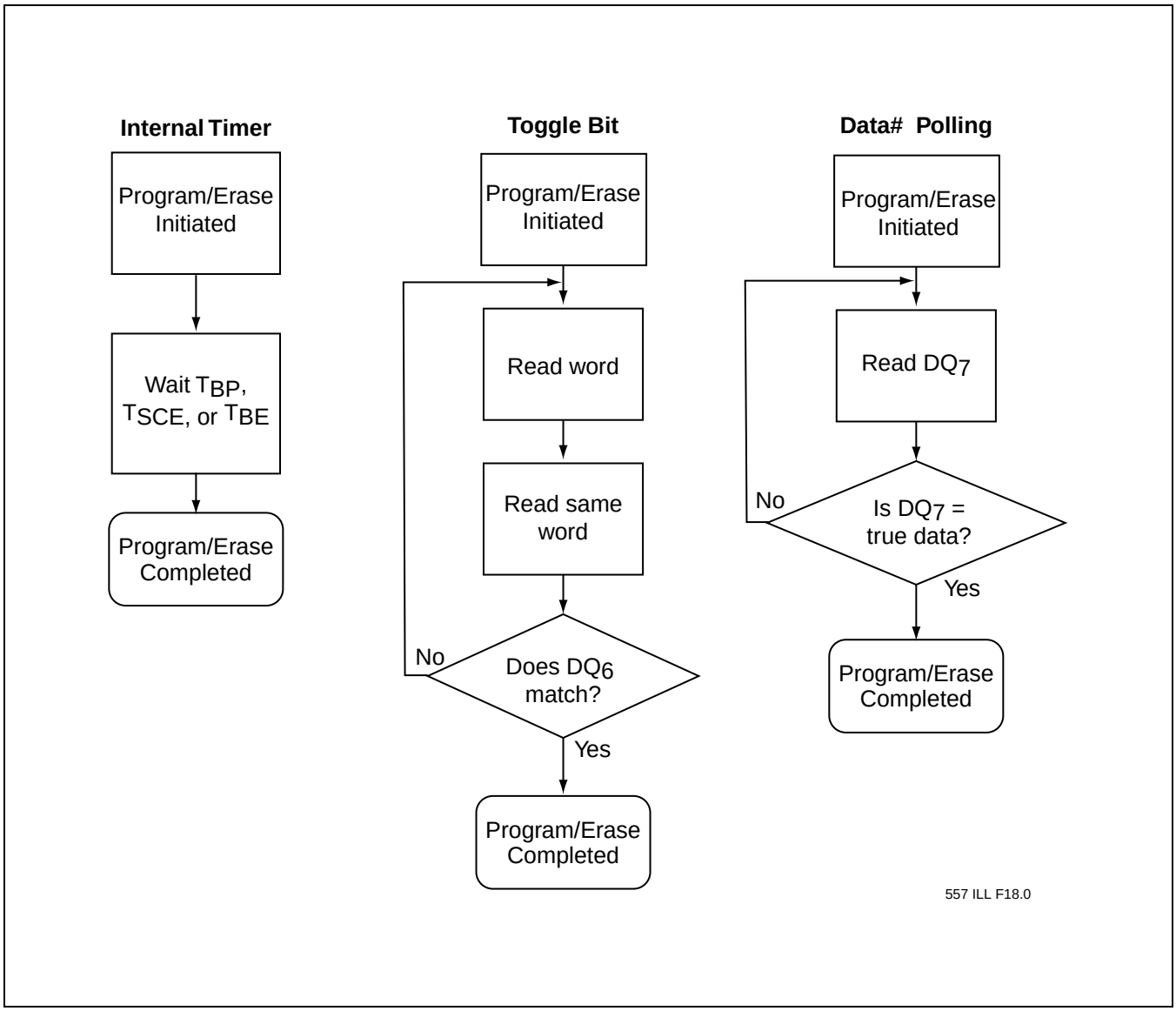


FIGURE 18: WAIT OPTIONS

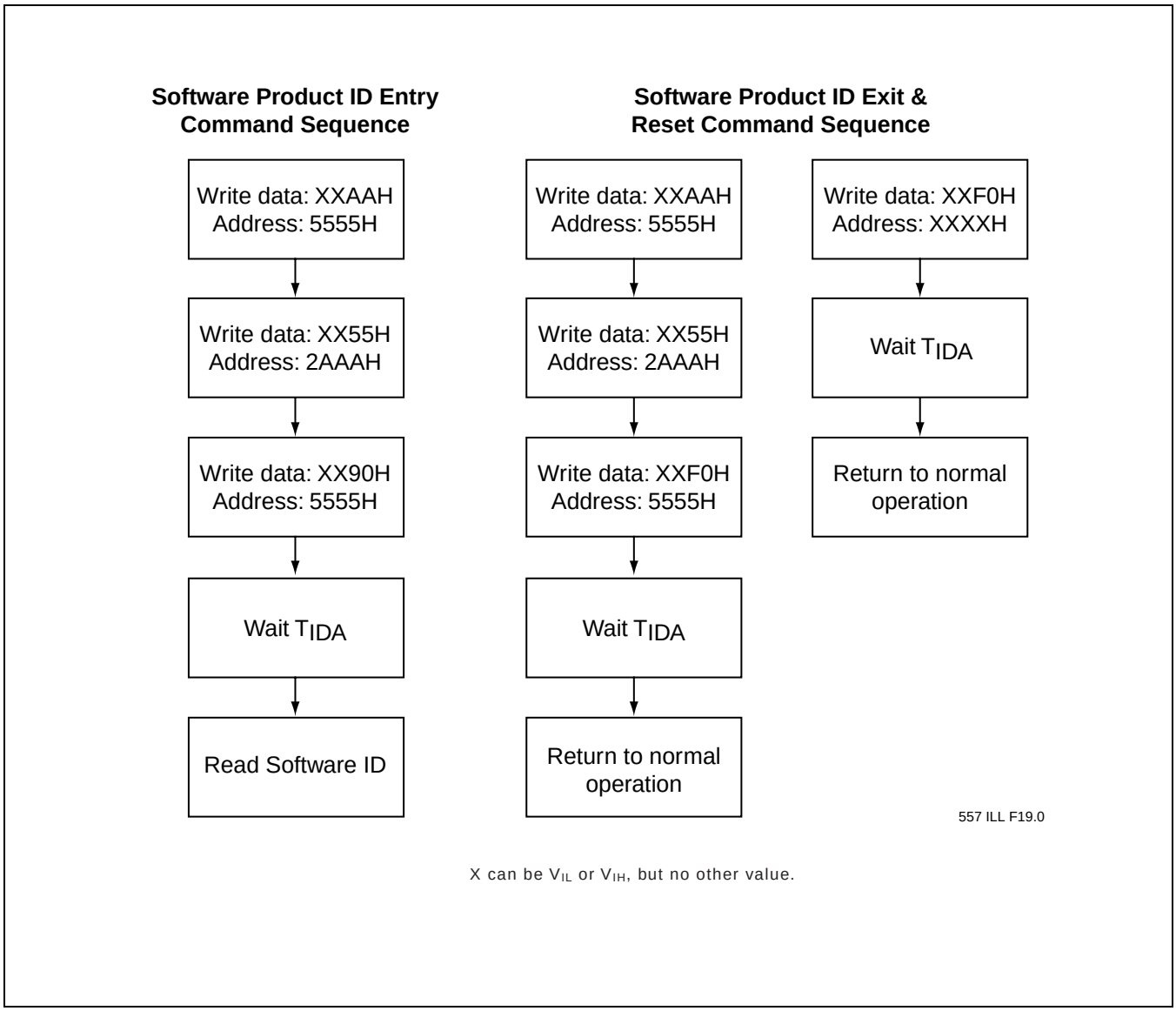


FIGURE 19: SOFTWARE PRODUCT COMMAND FLOWCHARTS

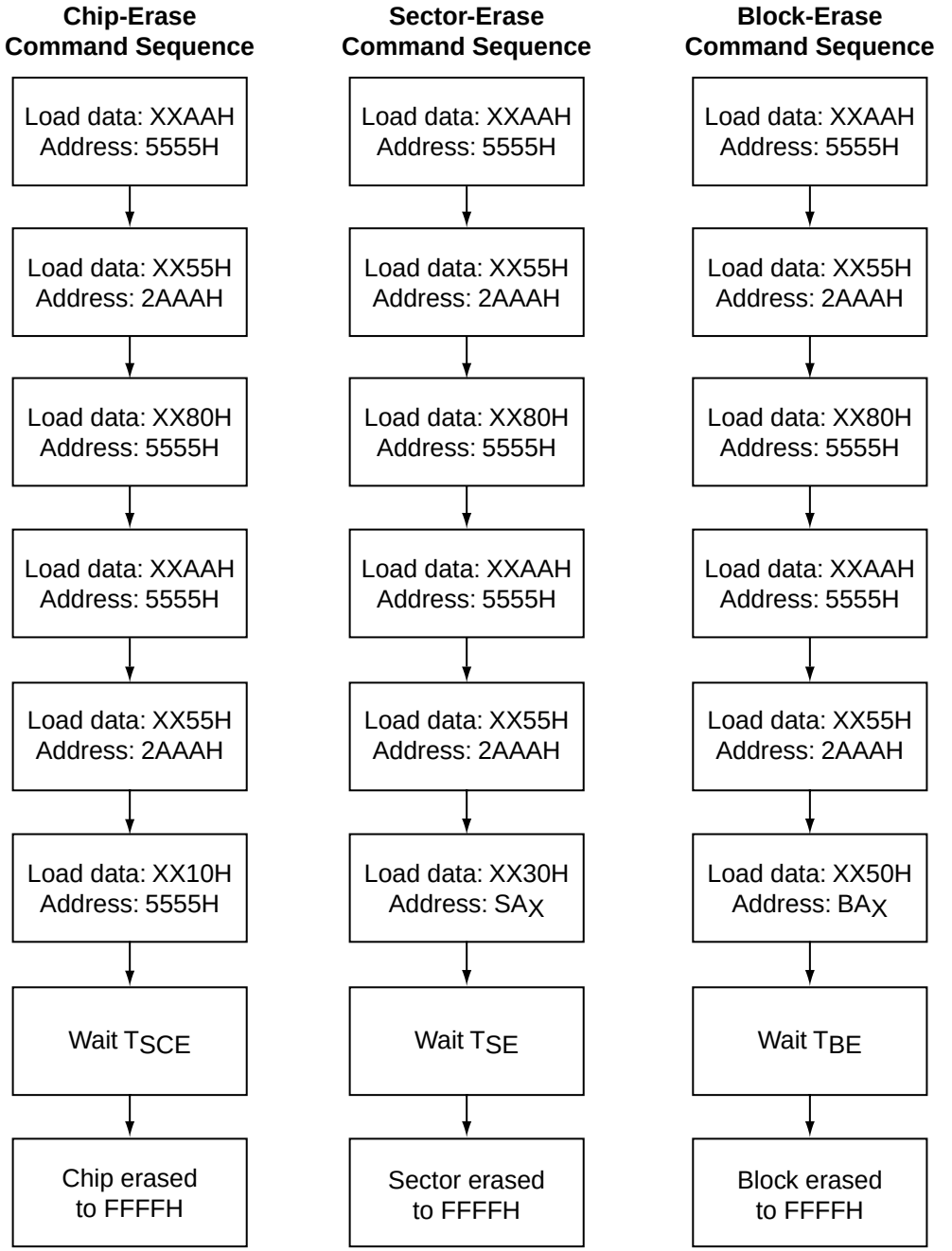


FIGURE 20: ERASE COMMAND SEQUENCE

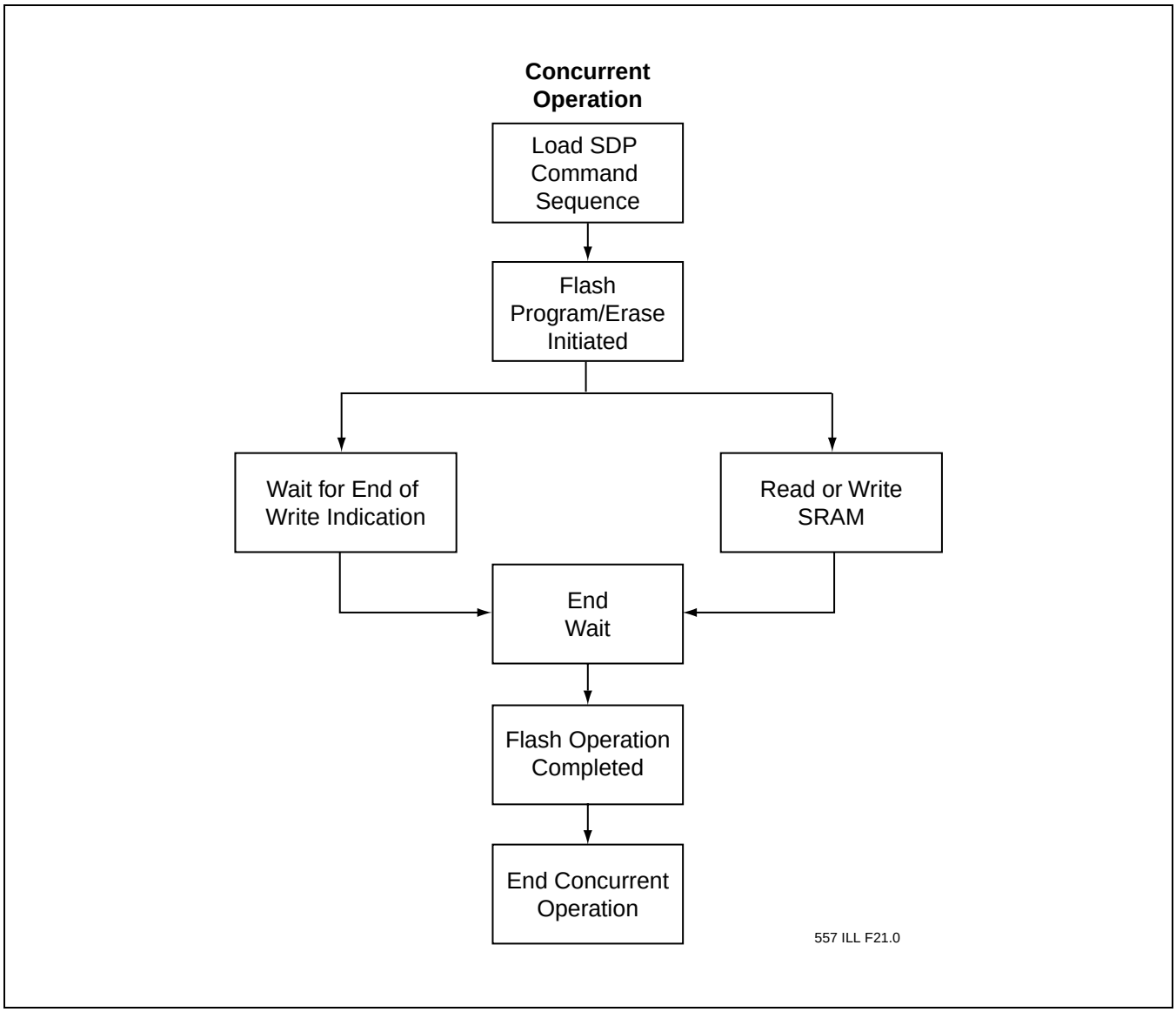
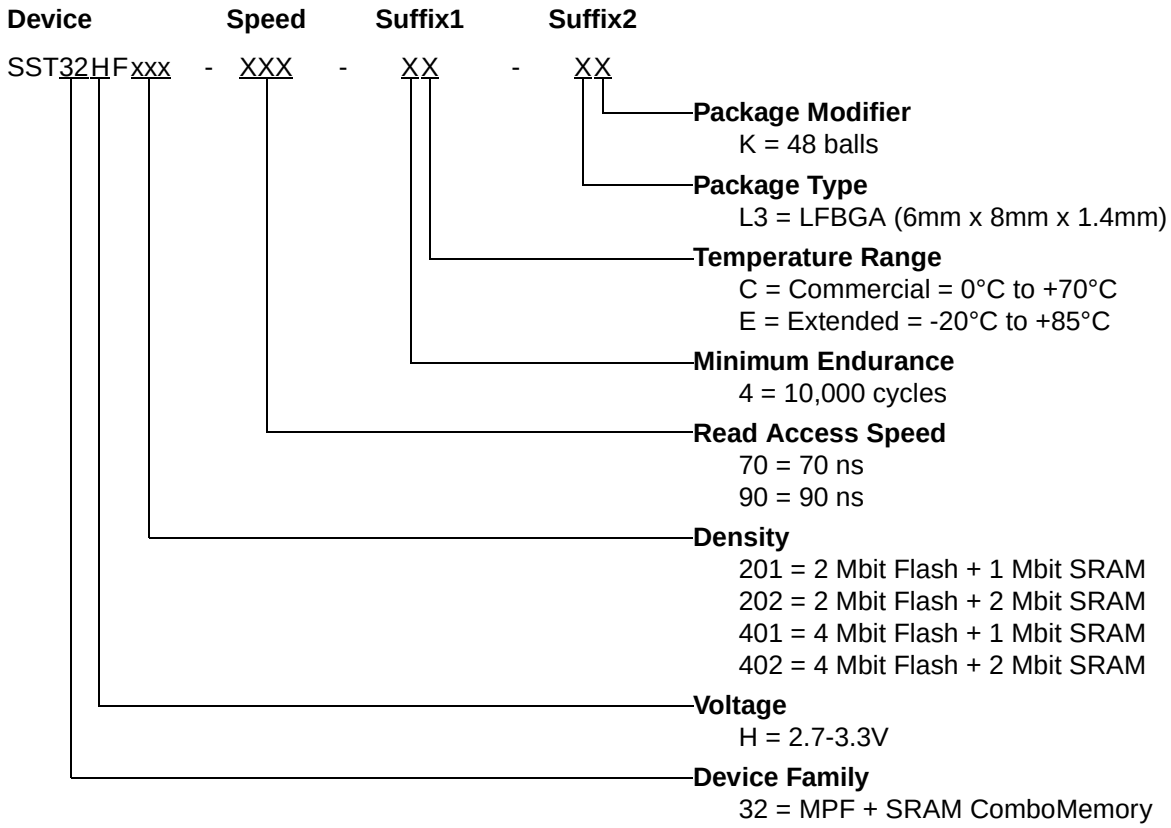


FIGURE 21: CONCURRENT OPERATION FLOWCHART

PRODUCT ORDERING INFORMATION



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Preliminary Specifications

Valid combinations for SST32HF201

SST32HF201-70-4C-L3K
SST32HF201-70-4E-L3K

SST32HF201-90-4C-L3K
SST32HF201-90-4E-L3K

Valid combinations for SST32HF202

SST32HF202-70-4C-L3K
SST32HF202-70-4E-L3K

SST32HF202-90-4C-L3K
SST32HF202-90-4E-L3K

Valid combinations for SST32HF401

SST32HF401-70-4C-L3K
SST32HF401-70-4E-L3K

SST32HF401-90-4C-L3K
SST32HF401-90-4E-L3K

Valid combinations for SST32HF402

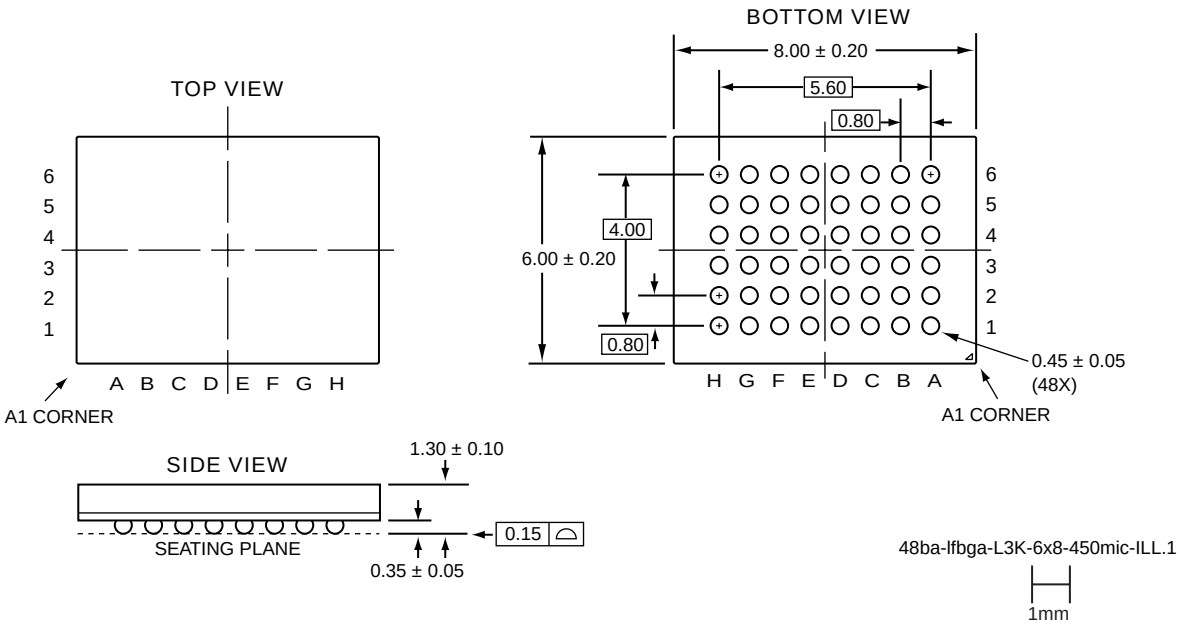
SST32HF402-70-4C-L3K
SST32HF402-70-4E-L3K

SST32HF402-90-4C-L3K
SST32HF402-90-4E-L3K

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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PACKAGING DIAGRAMS



Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-210, this specific package is not registered.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.1 (±.05) mm.
4. The actual shape of the corners may be slightly different than as portrayed in the drawing.

48-BALL LOW-PROFILE, FINE-PITCH BALL GRID ARRAY (LFBGA) 6MM X 8MM
SST PACKAGE CODE: L3K

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