ZL50110/11/14

128, 256 and 1024 Channel CESoP Processors

Data Sheet

October 2006

Features

General

- Circuit Emulation Services over Packet (CESoP) transport for MPLS, IP and Ethernet networks
- On chip timing & synchronization recovery across a packet network
- Grooming capability for Nx64 Kbps trunking

Circuit Emulation Services

- Complies with ITU-T recommendation Y.1413
- Complies with IETF PWE3 draft standards for CESoPSN and SAToP
- Complies with CESoP draft IAs for MEF and MFA
- Structured, synchronous CESoP with clock recovery
- Unstructured, asynchronous CESoP, with integral per stream clock recovery

TDM Interfaces

- Up to 32 T1/E1, 8 J2, 2 T3/E3 or 1 STS-1 ports
- H.110, H-MVIP, ST-BUS backplanes
- Up to 1024 bi-directional 64 Kbps channels

Ordering Information

ZL50110GAG	552 PBGA	Trays, Bake & Drypack
ZL50111GAG	552 PBGA	Trays, Bake & Drypack
ZL50114GAG	552 PBGA	Trays, Bake & Drypack
ZL50110GAG2	552 PBGA**	Trays, Bake & Drypack
ZL50111GAG2	552 PBGA**	Trays, Bake & Drypack
ZL50114GAG2	552 PBGA**	Trays, Bake & Drypack

**Pb Fee Tin Silver/Copper

-40°C to +85°C

- Direct connection to LIUs, framers, backplanes
- Dual reference Stratum 3, 4 and 4E DPLL for synchronous operation

Network Interfaces

- Up to 3 x 100 Mbps MII Fast Ethernet or Dual Redundant 1000 Mbps GMII/TBI Ethernet Interfaces

System Interfaces

- Flexible 32 bit host CPU interface (Motorola PowerQUICC™ compatible)
- On-chip packet memory for self-contained operation, with buffer depths of over 16 ms
- Up to 8 Mbytes of off-chip packet memory, supporting buffer depths of over 128 ms

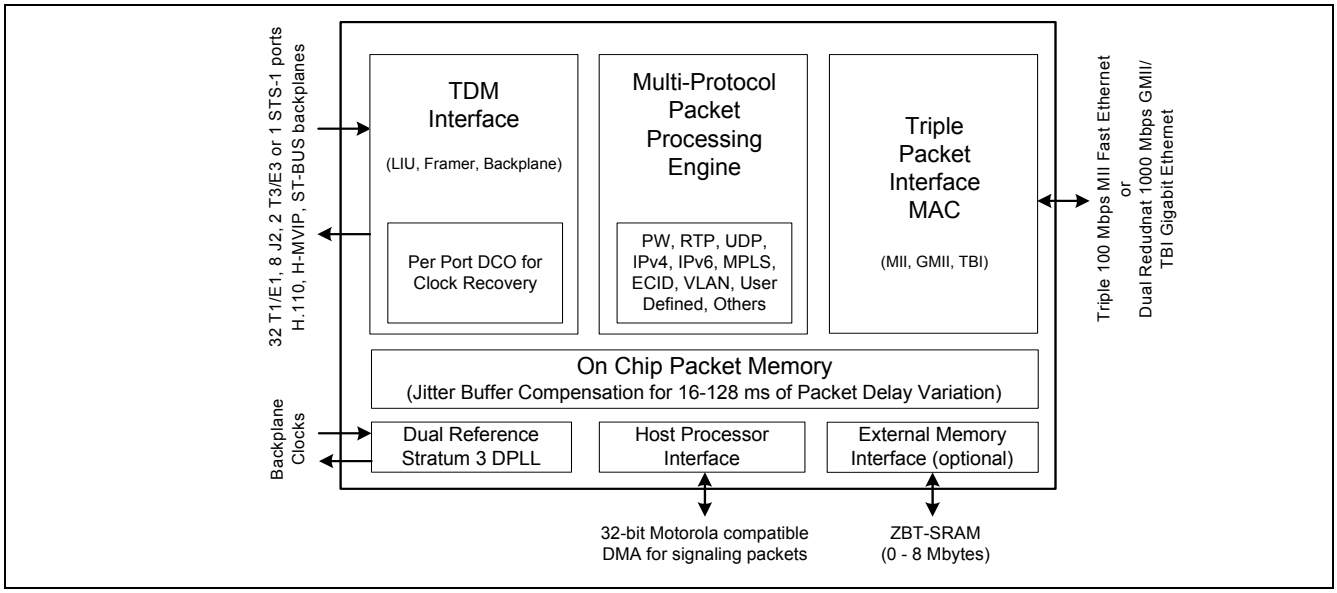


Figure 1 - ZL50110/11/14 High Level Overview

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Packet Processing Functions

- Flexible, multi-protocol packet encapsulation including IPv4, IPv6, RTP, MPLS, L2TPv3, ITU-T Y.1413., IETF CESoPSN, IETF SAToP and user programmable
- Packet re-sequencing to allow lost packet detection
- Four classes of service with programmable priority mechanisms (WFQ and SP) using egress queues
- Flexible classification of incoming packets at layers 2, 3, 4, and 5
- Supports up to 128 separate CESoP connections across the Packet Switched Network

Applications

- Circuit Emulation Services over Packet Networks
  - Leased Line support over packet networks
  - Multi-Tenant Unit access concentration
  - TDM over Cable
  - Fibre To The Premises G/E-PON
  - Layer 2 VPN services
- Customer-premise and Provider Edge Routers and Switches
- Packet switched backplane applications

Description

The ZL50110/11/14 family of CESoP processors are highly functional TDM to Packet bridging devices. The ZL50110/11/14 provides both structured and unstructured circuit emulation services over packet (CESoP) for up to 32 T1, 32 E1 and 8 J2 streams across a packet network based on MPLS, IP or Ethernet. The ZL50111 also supports unstructured T3, E3 and STS-1 streams.

The circuit emulation features in the ZL50110/11/14 family comply with the ITU Recommendation Y.1413, as well as the emerging CESoP standards from the Metro Ethernet Forum (MEF) and MPLS and Frame Relay Alliance (MFA). The ZL50110/11/14 also complies with the standards currently being developed within the IETF's PWE3 working group, listed below.

- Structure-Agnostic TDM over Packet (SAToP) - draft-ietf-pwe3-satop
- Structure-aware TDM Circuit Emulation Service over Packet Switched Network (CESoPSN) - draft-ietf-pwe3-cesopsn

The ZL50110/11/14 provides up to triple 100 Mbps MII ports or dual redundant 1000 Mbps GMII/TBI ports.

The ZL50110/11/14 incorporates a range of powerful clock recovery mechanisms for each TDM stream, allowing the frequency of the source clock to be faithfully generated at the destination, enabling greater system performance and quality. Timing is carried using RTP or similar protocols, and both adaptive and differential clock recovery schemes are included, allowing the customer to choose the correct scheme for the application. An externally supplied clock may also be used to drive the TDM interface of the ZL50110/11/14.

The ZL50110/11/14 incur very low latency for the data flow, thereby increasing QoS when carrying voice services across the Packet Switched Network. Voice, when carried using CESoP, which typically has latencies of less than 10 ms, does not require expensive processing such as compression and echo cancellation.

The ZL50110/11/14 is capable of assembling user-defined packets of TDM traffic from the TDM interface and transmitting them out the packet interfaces using a variety of protocols. The ZL50110/11/14 supports a range of different packet switched networks, including Ethernet VLANs, IP (both versions 4 and 6) and MPLS. The devices also supports four different classes of service on packet egress, allowing priority treatment of TDM-based traffic. This can be used to help minimize latency variation in the TDM data.

Packets received from the packet interfaces are parsed to determine the egress destination, and are appropriately queued to the TDM interface, they can also be forwarded to the host interface, or back toward the packet interface. Packets queued to the TDM interface can be re-ordered based on sequence number, and lost packets filled in to maintain timing integrity.

The ZL50110/11/14 family includes sufficient on-chip memory that external memory is not required in most applications. This reduces system costs and simplifies the design. For applications that do require more memory (e.g., high stream count or high latency), the device supports up to 8 Mbytes of SSRAM.

A comprehensive evaluation system is available upon request from your local Zarlink representative or distributor. This system includes the CESoP processor, various TDM interfaces and a fully featured evaluation software GUI that will run on a Windows PC.

Device Line Up

There are three products within the ZL50110/11/14 family, with capacity as shown in the following table:

Device	TDM Interfaces	Ethernet Packet I/F
ZL50114	4 T1, 4 E1, or 1 J2 streams or 4 MVIP/ST-BUS streams at 2.048 Mbps or 1 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps	Dual 100 Mbps MII or Dual Redundant 1000 Mbps GMII/TBI
ZL50110	8 T1, 8 E1 or 2 J2 streams or 8 MVIP/ST-BUS streams at 2.048 Mbps or 2 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps	Dual 100 Mbps MII or Dual Redundant 1000 Mbps GMII/TBI
ZL50111	32 T1, 32 E1, 8 J2, 2 T3, 2 E3 or 1 STS-1 streams or 32 MVIP/ST-BUS streams at 2.048 Mbps or 8 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps	Triple 100 Mbps MII or Dual Redundant 1000 Mbps GMII/TBI or Single 100 Mbps MII and Single 1000 Mbps GMII/TBI

Table 1 - Capacity of Devices in the ZL50110/11/14 Family

Table of Contents

1.0 Changes Summary . . . 11
2.0 Physical Specification . . . 12
3.0 External Interface Description . . . 21
3.1 TDM Interface . . . 21
3.1.1 ZL50111 Variant TDM Stream Connection . . . 21
3.1.2 ZL50110 Variant TDM stream connection . . . 24
3.1.3 ZL50114 Variant TDM Stream Connection . . . 25
3.1.4 TDM Signals Common to ZL50111, ZL50110 and ZL50114 . . . 26
3.2 PAC Interface . . . 27
3.3 Packet Interfaces . . . 28
3.4 External Memory Interface . . . 37
3.5 CPU Interface . . . 39
3.6 System Function Interface . . . 41
3.7 Test Facilities . . . 42
3.7.1 Administration, Control and Test Interface . . . 42
3.7.2 JTAG Interface . . . 42
3.8 Miscellaneous Inputs . . . 43
3.9 Power and Ground Connections . . . 43
3.10 Internal Connections . . . 44
4.0 Typical Applications . . . 44
4.1 Leased Line Provision . . . 44
4.2 Metropolitan Area Network Aggregation . . . 44
4.3 Digital Loop Carrier . . . 45
4.4 Remote Concentrator . . . 46
4.5 Cell Site Backhaul . . . 46
4.6 Metro Ethernet Equipment . . . 47
5.0 Functional Description . . . 48
5.1 Block Diagram . . . 49
5.2 Data and Control Flows . . . 49
5.3 TDM Interface . . . 50
5.3.1 TDM Interface Block . . . 50
5.3.2 Structured TDM Port Data Formats . . . 51
5.3.3 TDM Clock Structure . . . 52
5.3.3.1 Synchronous TDM Clock Generation . . . 52
5.3.3.2 Asynchronous TDM Clock Generation . . . 52
5.4 Payload Assembly . . . 52
5.4.1 Structured Payload Operation . . . 53
5.4.1.1 Structured Payload Order . . . 54
5.4.2 Unstructured Payload Operation . . . 54
5.5 Protocol Engine . . . 55
5.6 Packet Transmission . . . 55
5.7 TDM Formatter . . . 55
6.0 Clock Recovery . . . 56
6.1 Differential Clock Recovery . . . 56
6.2 Adaptive Clock Recovery . . . 57
6.3 SYSTEM_CLK Considerations . . . 57
7.0 System Features . . . 58
7.1 Latency . . . 58
7.2 Loopback Modes . . . 58
7.3 Host Packet Generation . . . 58
7.4 Loss of Service (LOS) . . . 59

Table of Contents

7.5 External Memory Requirement . . . 59
7.6 GIGABIT Ethernet - Recommended Configurations . . . 60
7.6.1 Central Ethernet Switch . . . 61
7.6.2 Redundant Ethernet Switch . . . 62
7.7 Power Up sequence . . . 62
7.8 JTAG Interface and Board Level Test Features . . . 63
7.9 External Component Requirements . . . 63
7.10 Miscellaneous Features . . . 63
7.11 Test Modes Operation . . . 64
7.11.1 Overview . . . 64
7.11.1.1 System Normal Mode . . . 64
7.11.1.2 System Tri-State Mode . . . 64
7.11.2 Test Mode Control . . . 64
7.11.3 System Normal Mode . . . 64
7.11.4 System Tri-state Mode . . . 64
8.0 DPLL Specification . . . 65
8.1 Modes of Operation . . . 65
8.1.1 Locking Mode (normal operation) . . . 65
8.1.2 Holdover Mode . . . 66
8.1.3 Freerun Mode . . . 66
8.1.4 Powerdown Mode . . . 66
8.2 Reference Monitor Circuit . . . 66
8.3 Locking Mode Reference Switching . . . 67
8.4 Locking Range . . . 67
8.5 Locking Time . . . 67
8.6 Lock Status . . . 68
8.7 Jitter . . . 68
8.7.1 Acceptance of Input Wander . . . 68
8.7.2 Intrinsic Jitter . . . 68
8.7.3 Jitter Tolerance . . . 68
8.7.4 Jitter Transfer . . . 69
8.8 Maximum Time Interval Error (MTIE) . . . 69
9.0 Memory Map and Register Definitions . . . 70
10.0 DC Characteristics . . . 71
11.0 AC Characteristics . . . 73
11.1 TDM Interface Timing - ST-BUS . . . 73
11.1.1 ST-BUS Slave Clock Mode . . . 73
11.1.2 ST-BUS Master Clock Mode . . . 75
11.2 TDM Interface Timing - H.110 Mode . . . 76
11.3 TDM Interface Timing - H-MVIP . . . 77
11.4 TDM LIU Interface Timing . . . 78
11.5 PAC Interface Timing . . . 79
11.6 Packet Interface Timing . . . 79
11.6.1 MII Transmit Timing . . . 79
11.6.2 MII Receive Timing . . . 80
11.6.3 GMII Transmit Timing . . . 82
11.6.4 GMII Receive Timing . . . 83
11.6.5 TBI Interface Timing . . . 84
11.6.6 Management Interface Timing . . . 85
11.7 External Memory Interface Timing . . . 86
11.8 CPU Interface Timing . . . 87
11.9 System Function Port . . . 90

Table of Contents

11.10 JTAG Interface Timing . . . 91
12.0 Power Characteristics . . . 93
13.0 Design and Layout Guidelines . . . 94
13.1 High Speed Clock & Data Interfaces . . . 94
13.1.1 External Memory Interface - special considerations during layout . . . 95
13.1.2 GMAC Interface - special considerations during layout . . . 95
13.1.3 TDM Interface - special considerations during layout . . . 95
13.1.4 Summary . . . 95
13.2 CPU TA Output . . . 95
13.3 Mx_LINKUP_LED Outputs . . . 96
14.0 Reference Documents . . . 99
14.1 External Standards/Specifications . . . 99
14.2 Zarlink Standards . . . 99
15.0 Glossary . . . 100

List of Figures

Figure 1 - ZL50110/11/14 High Level Overview . . . 1
Figure 2 - ZL50111 Package View and Ball Positions . . . 13
Figure 3 - ZL50110 Package View and Ball Positions . . . 14
Figure 4 - ZL50114 Package View and Ball Positions . . . 15
Figure 5 - Leased Line Services Over a Circuit Emulation Link . . . 44
Figure 6 - Metropolitan Area Network Aggregation using CESoP . . . 45
Figure 7 - Digital Loop Carrier using CESoP . . . 45
Figure 8 - Remote Concentrator using CESoP . . . 46
Figure 9 - Cell Site Backhaul using CESoP . . . 47
Figure 10 - Metro Ethernet Equipment using CESoP . . . 48
Figure 11 - ZL50110/11/14 Family Operation . . . 48
Figure 12 - ZL50110/11/14 Data and Control Flows . . . 49
Figure 13 - Synchronous TDM Clock Generation . . . 52
Figure 14 - ZL50110/11/14 Packet Format - Structured Mode . . . 53
Figure 15 - Channel Order for Packet Formation . . . 54
Figure 16 - ZL50110/11/14 Packet Format - Unstructured Mode . . . 54
Figure 17 - Differential Clock Recovery . . . 56
Figure 18 - Adaptive Clock Recovery . . . 57
Figure 19 - External Memory Requirement for ZL50111 . . . 59
Figure 20 - External Memory Requirement for ZL50110 . . . 60
Figure 21 - Gigabit Ethernet Connection - Central Ethernet Switch . . . 61
Figure 22 - Gigabit Ethernet Connection - Redundant Ethernet Switch . . . 62
Figure 23 - Powering Up the ZL50110/11/14 . . . 63
Figure 24 - Jitter Transfer Function . . . 69
Figure 25 - Jitter Transfer Function - Detail . . . 70
Figure 26 - TDM ST-BUS Slave Mode Timing at 8.192 Mbps . . . 74
Figure 27 - TDM ST-BUS Slave Mode Timing at 2.048 Mbps . . . 74
Figure 28 - TDM Bus Master Mode Timing at 8.192 Mbps . . . 75
Figure 29 - TDM Bus Master Mode Timing at 2.048 Mbps . . . 76
Figure 30 - H.110 Timing Diagram . . . 77
Figure 31 - TDM - H-MVIP Timing Diagram for 16 MHz Clock (8.192 Mbps) . . . 78
Figure 32 - TDM-LIU Structured Transmission/Reception . . . 79
Figure 33 - MII Transmit Timing Diagram . . . 80
Figure 34 - MII Receive Timing Diagram . . . 81
Figure 35 - GMII Transmit Timing Diagram . . . 82
Figure 36 - GMII Receive Timing Diagram . . . 83
Figure 37 - TBI Transmit Timing Diagram . . . 84
Figure 38 - TBI Receive Timing Diagram . . . 85
Figure 39 - Management Interface Timing for Ethernet Port - Read . . . 85
Figure 40 - Management Interface Timing for Ethernet Port - Write . . . 86
Figure 41 - External RAM Read and Write Timing . . . 86
Figure 42 - CPU Read - MPC8260 . . . 88
Figure 43 - CPU Write - MPC8260 . . . 88
Figure 44 - CPU DMA Read - MPC8260 . . . 89
Figure 45 - CPU DMA Write - MPC8260 . . . 89
Figure 46 - JTAG Signal Timing . . . 92
Figure 47 - JTAG Clock and Reset Timing . . . 92
Figure 48 - ZL50110/11/14 Power Consumption Plot . . . 93

List of Figures

Figure 49 - CPU_TA Board Circuit 96
Figure 50 - Mx_LINKUP_LED Stuffing Option 97

List of Tables

Table 1 - Capacity of Devices in the ZL50110/11/14 Family 4
Table 2 - TDM Interface ZL50111 Stream Pin Definition 21
Table 3 - TDM Interface ZL50110 Stream Pin Definition 24
Table 4 - TDM Interface ZL50114 Stream Pin Definition 25
Table 5 - TDM Interface Common Pin Definition 26
Table 6 - PAC Interface Package Ball Definition 27
Table 7 - Packet Interface Signal Mapping - MII to GMII/TBI 28
Table 8 - MII Management Interface Package Ball Definition 29
Table 9 - MII Port 0 Interface Package Ball Definition 29
Table 10 - MII Port 1 Interface Package Ball Definition 32
Table 11 - MII Port 2 Interface Package Ball Definition 34
Table 12 - MII Port 3 Interface Package Ball Definition 35
Table 13 - External Memory Interface Package Ball Definition 37
Table 14 - CPU Interface Package Ball Definition 39
Table 15 - System Function Interface Package Ball Definition. 41
Table 16 - Administration/Control Interface Package Ball Definition 42
Table 17 - JTAG Interface Package Ball Definition 42
Table 18 - Miscellaneous Inputs Package Ball Definitions 43
Table 19 - Power and Ground Package Ball Definition 43
Table 20 - No Connection Ball Definition 44
Table 21 - Standard Device Flows 49
Table 22 - TDM Services Offered by the ZL50110/11/14 Family 50
Table 23 - Some of the TDM Port Formats Accepted by the ZL50110/11/14 Family 51
Table 24 - DMA Maximum Bandwidths 58
Table 25 - Test Mode Control 64
Table 26 - DPLL Input Reference Frequencies 65
Table 27 - TDM ST-BUS Master Timing Specification 75
Table 28 - TDM H.110 Timing Specification 76
Table 29 - TDM H-MVIP Timing Specification 77
Table 30 - TDM - LIU Structured Transmission/Reception 78
Table 31 - PAC Timing Specification 79
Table 32 - MII Transmit Timing - 100 Mbps 79
Table 33 - MII Receive Timing - 100 Mbps 80
Table 34 - GMII Transmit Timing - 1000 Mbps 82
Table 35 - GMII Receive Timing - 1000 Mbps 83
Table 36 - TBI Timing - 1000 Mbps 84
Table 37 - MAC Management Timing Specification 85
Table 38 - External Memory Timing 86
Table 39 - CPU Timing Specification 87
Table 40 - System Clock Timing. 90
Table 41 - JTAG Interface Timing. 91
Table 42 - Mx_LINKUP_LED Pin Assignments 96
Table 43 - Mx_LINKUP_LED Stuffing Option 98

1.0 Changes Summary

The following table captures the changes from the February 2006 issue.

Page	Item	Change
86	Table 38, Table 38 - External Memory Timing	Added Minimum Values

The following table captures the changes from the April 2005 issue.

Page	Item	Change
		Clarified ZL50111 supports 3 MII ports, ZL50110/4 support 2 MII ports.
41, 42	Section 3.6 and Section 3.7.2	Added external pull-up/pull-down resistor recommendations for SYSTEM_RST, SYSTEM_DEBUG, JTAG_TRST, JTAG_TCK.
57	Section 6.3	Added Section 6.3 SYSTEM_CLK Considerations.

The following table captures the changes from the January 2005 issue.

Page	Item	Change
		Clarified data sheet to indicate ZL5011x supports clock recovery in both synchronous and asynchronous modes of operation.
89	Figure 44	Inverted polarity of $\overline{\text{CPU_DREQ0}}$ and $\overline{\text{CPU_DREQ1}}$ to conform with default MPC8260. Polarity of $\overline{\text{CPU_DREQ}}$ and $\overline{\text{CPU_SDACK}}$ remains programmable through API.
89	Figure 45	Inverted polarity of $\overline{\text{CPU_DREQ0}}$ and $\overline{\text{CPU_DREQ1}}$ to conform with default MPC8260. Polarity of $\overline{\text{CPU_DREQ}}$ and $\overline{\text{CPU_SDACK}}$ remains programmable through API.

The following table captures the changes from the October 2004 issue.

Page	Item	Change
42	Section 3.7.1	Added 5 kohm pulldown recommendation to GPIO signals.

The following table captures the changes from the September 2004 issue.

Page	Item	Change
12, 16, 19	Fig. 2 and Ball Signal Assignment Table	Corrected Mx_LINKUP_LED pin assignment.
73	DC Electrical Characteristics Table and Output Levels Table	Changed Electrical Characteristics to differentiate between 3.3 V and 5 V tolerant signals.
98	Section 13.3	New section added; Mx_LINKUP_LED Outputs.

2.0 Physical Specification

The ZL50111 will be packaged in a PBGA device.

Features:

- Body Size: 35 mm x 35 mm (typ)
- Ball Count: 552
- Ball Pitch: 1.27 mm (typ)
- Ball Matrix: 26 x 26
- Ball Diameter: 0.75 mm (typ)
- Total Package Thickness: 2.33 mm (typ)

The ZL50110 will be packaged in a PBGA device.

Features:

- Body Size: 35 mm x 35 mm (typ)
- Ball Count: 552
- Ball Pitch: 1.27 mm (typ)
- Ball Matrix: 26 x 26
- Ball Diameter: 0.75 mm (typ)
- Total Package Thickness: 2.33 mm (typ)

The ZL50114 will be packaged in a PBGA device.

Features:

- Body Size: 35 mm x 35 mm (typ)
- Ball Count: 552
- Ball Pitch: 1.27 mm (typ)
- Ball Matrix: 26 x 26
- Ball Diameter: 0.75 mm (typ)
- Total Package Thickness: 2.33 mm (typ)

ZL50111 Package view from TOP side. Note that ball A1 is non-chamfered corner

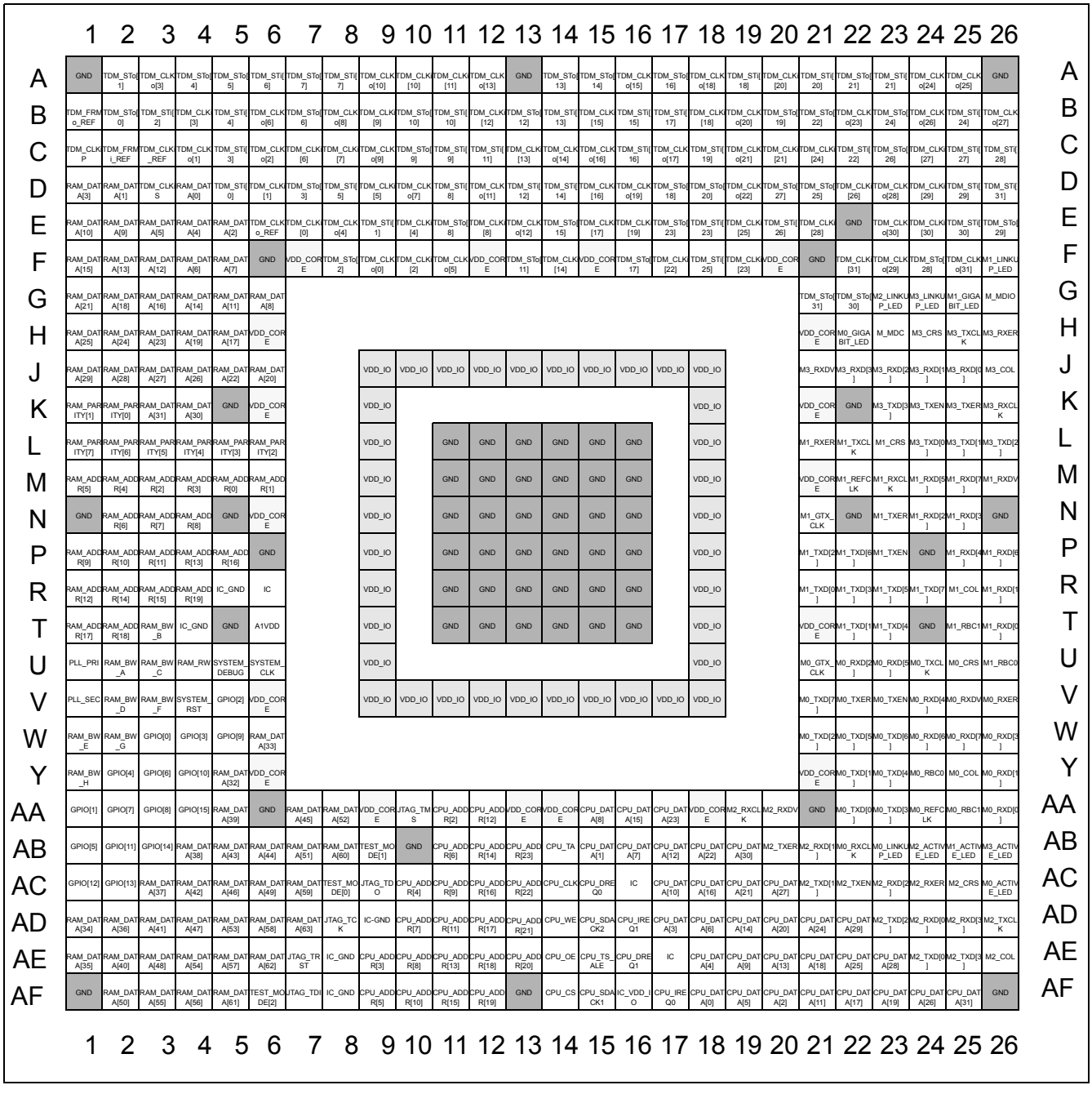
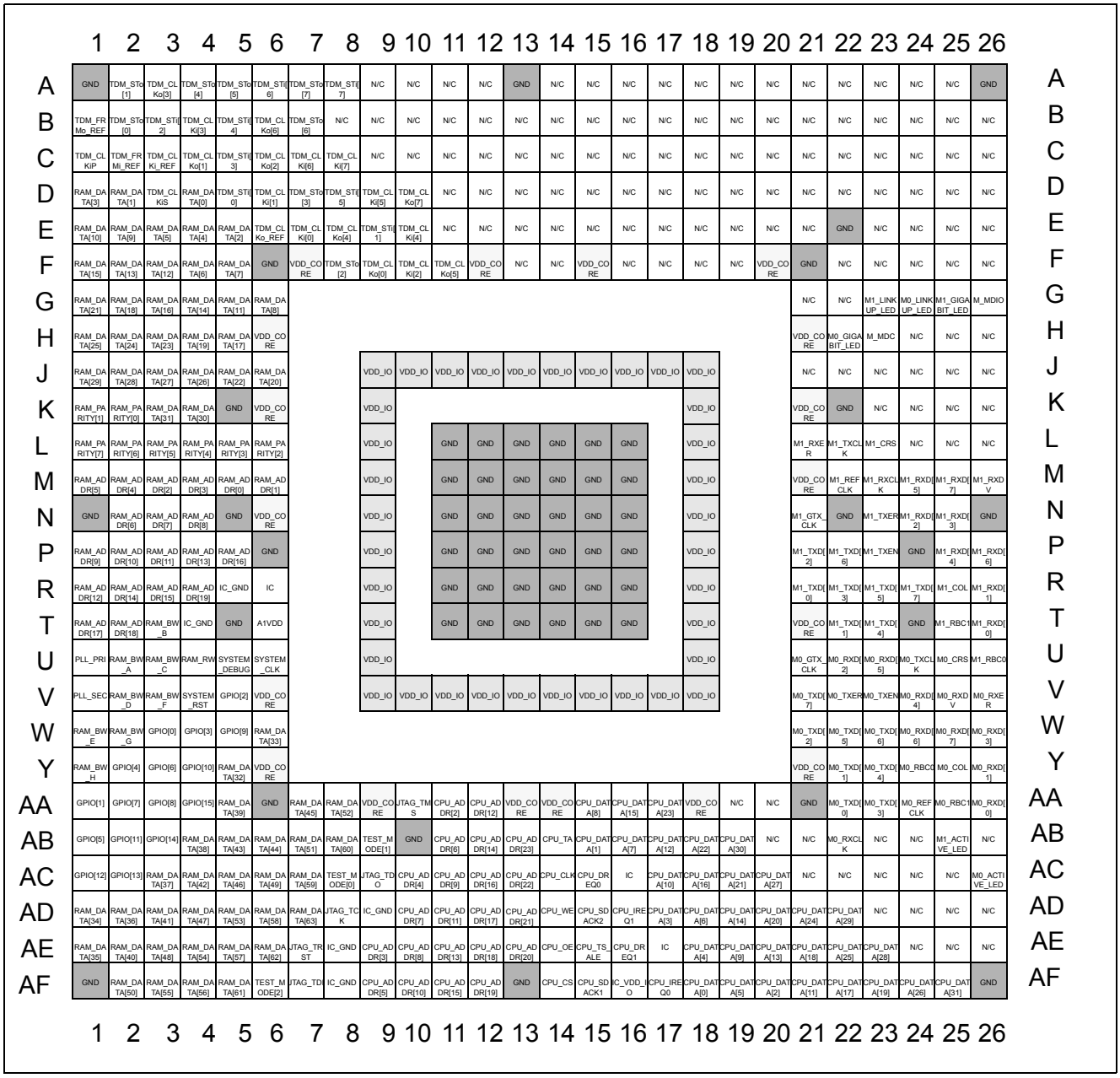


Figure 2 - ZL50111 Package View and Ball Positions

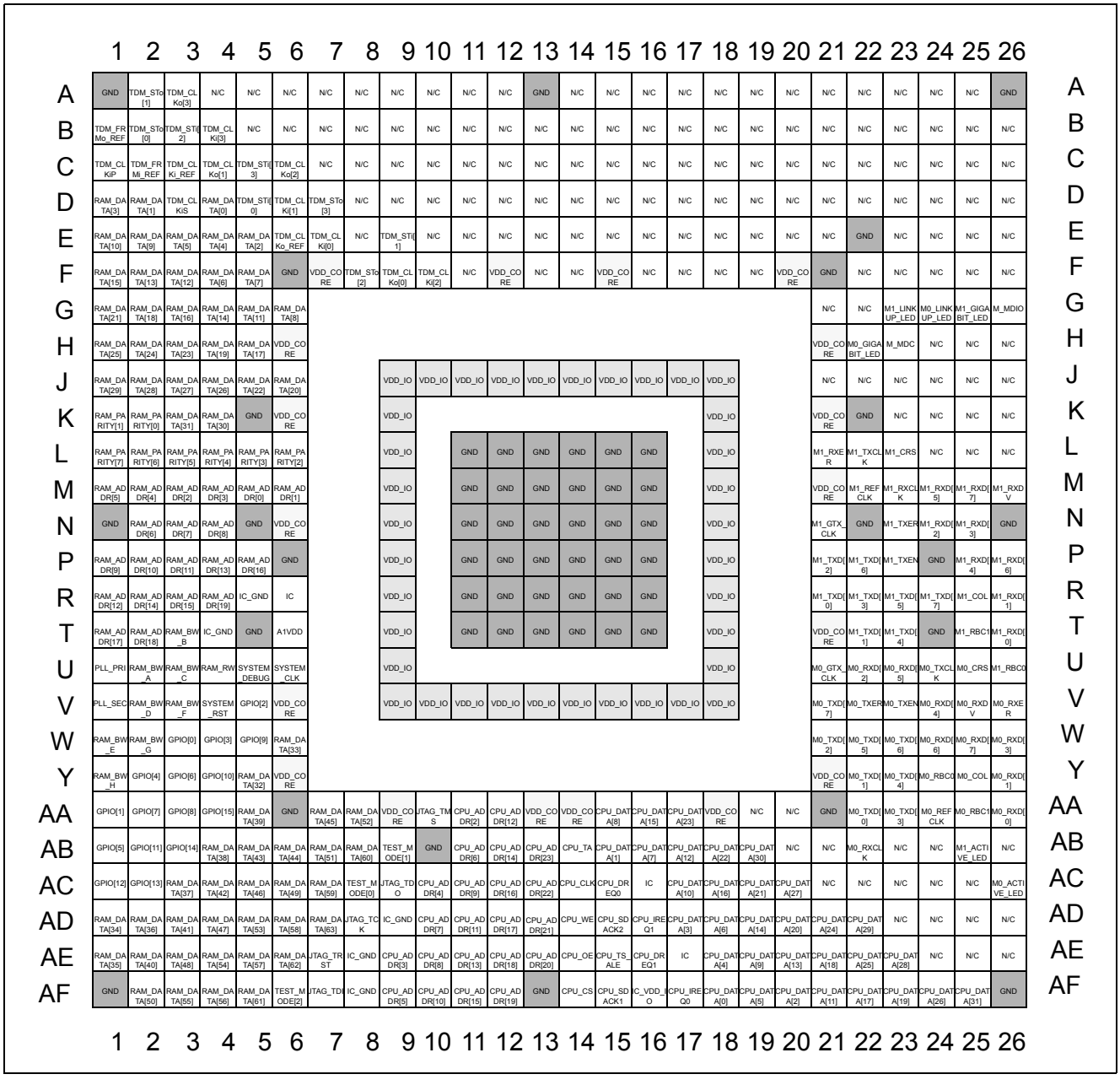
ZL50110 Package view from TOP side. Note that ball A1 is non-chamfered corner.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	GND	TDM_STo[1]	TDM_CLKo[3]	TDM_STo[4]	TDM_STo[5]	TDM_STi[6]	TDM_STo[7]	TDM_STi[7]	N/C	N/C	N/C	N/C	GND	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	GND	A
B	TDM_FRMo_REF	TDM_STo[0]	TDM_STi[2]	TDM_CLKi[3]	TDM_STi[4]	TDM_CLKo[6]	TDM_STo[6]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	B
C	TDM_CLKiP	TDM_FRMi_REF	TDM_CLKi_REF	TDM_CLKo[1]	TDM_STi[3]	TDM_CLKo[2]	TDM_CLKi[6]	TDM_CLKi[7]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	C
D	RAM_DATA[3]	RAM_DATA[1]	TDM_CLKiS	RAM_DATA[0]	TDM_STi[0]	TDM_CLKi[1]	TDM_STo[3]	TDM_STo[5]	TDM_CLKi[5]	TDM_CLKo[7]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	D
E	RAM_DATA[10]	RAM_DATA[9]	RAM_DATA[5]	RAM_DATA[4]	RAM_DATA[2]	TDM_CLKo_REF	TDM_CLKi[0]	TDM_CLKo[4]	TDM_STi[1]	TDM_CLKi[4]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	GND	N/C	N/C	N/C	N/C	E
F	RAM_DATA[15]	RAM_DATA[13]	RAM_DATA[12]	RAM_DATA[6]	RAM_DATA[7]	GND	VDD_CORE	TDM_STo[2]	TDM_CLKo[0]	TDM_CLKi[2]	TDM_CLKo[5]	VDD_CORE	N/C	N/C	VDD_CORE	N/C	N/C	N/C	N/C	VDD_CORE	GND	N/C	N/C	N/C	N/C	N/C	F
G	RAM_DATA[21]	RAM_DATA[18]	RAM_DATA[16]	RAM_DATA[14]	RAM_DATA[11]	RAM_DATA[8]															N/C	N/C	M1_LINKUP_LED	M0_LINKUP_LED	M1_GIGABIT_LED	M_MDIO	G
H	RAM_DATA[25]	RAM_DATA[24]	RAM_DATA[23]	RAM_DATA[19]	RAM_DATA[17]	VDD_CORE															VDD_CORE	M0_GIGABIT_LED	M_MDC	N/C	N/C	N/C	H
J	RAM_DATA[29]	RAM_DATA[28]	RAM_DATA[27]	RAM_DATA[26]	RAM_DATA[22]	RAM_DATA[20]			VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO			N/C	N/C	N/C	N/C	N/C	N/C	J
K	RAM_PARITY[1]	RAM_PARITY[0]	RAM_DATA[31]	RAM_DATA[30]	GND	VDD_CORE			VDD_IO									VDD_IO			VDD_CORE	GND	N/C	N/C	N/C	N/C	K
L	RAM_PARITY[7]	RAM_PARITY[6]	RAM_PARITY[5]	RAM_PARITY[4]	RAM_PARITY[3]	RAM_PARITY[2]			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_RXER	M1_TXCLK	M1_CRS	N/C	N/C	N/C	L
M	RAM_ADDR[5]	RAM_ADDR[4]	RAM_ADDR[2]	RAM_ADDR[3]	RAM_ADDR[0]	RAM_ADDR[1]			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			VDD_CORE	M1_REFCLK	M1_RXCLK	M1_RXD[5]	M1_RXD[7]	M1_RXDV	M
N	GND	RAM_ADDR[6]	RAM_ADDR[7]	RAM_ADDR[8]	GND	VDD_CORE			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_GTX_CLK	GND	M1_TXER	M1_RXD[2]	M1_RXD[3]	GND	N
P	RAM_ADDR[9]	RAM_ADDR[10]	RAM_ADDR[11]	RAM_ADDR[13]	RAM_ADDR[16]	GND			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_TXD[2]	M1_TXD[6]	M1_TXEN	GND	M1_RXD[4]	M1_RXD[6]	P
R	RAM_ADDR[12]	RAM_ADDR[14]	RAM_ADDR[15]	RAM_ADDR[19]	IC_GND	IC			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_TXD[0]	M1_TXD[3]	M1_TXD[5]	M1_TXD[7]	M1_COL	M1_RXD[1]	R
T	RAM_ADDR[17]	RAM_ADDR[18]	RAM_BW_B	IC_GND	GND	A1VDD			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			VDD_CORE	M1_TXD[1]	M1_TXD[4]	GND	M1_RBC1	M1_RXD[0]	T
U	PLL_PRI	RAM_BW_A	RAM_BW_C	RAM_RW	SYSTEM_DEBUG	SYSTEM_CLK			VDD_IO									VDD_IO			M0_GTX_CLK	M0_RXD[2]	M0_RXD[5]	M0_TXCLK	M0_CRS	M1_RBC0	U
V	PLL_SEC	RAM_BW_D	RAM_BW_F	SYSTEM_RST	GPIO[2]	VDD_CORE			VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO			M0_TXD[7]	M0_TXER	M0_TXEN	M0_RXD[4]	M0_RXDV	M0_RXER	V
W	RAM_BW_E	RAM_BW_G	GPIO[0]	GPIO[3]	GPIO[9]	RAM_DATA[33]															M0_TXD[2]	M0_TXD[5]	M0_TXD[6]	M0_RXD[6]	M0_RXD[7]	M0_RXD[3]	W
Y	RAM_BW_H	GPIO[4]	GPIO[6]	GPIO[10]	RAM_DATA[32]	VDD_CORE															VDD_CORE	M0_TXD[1]	M0_TXD[4]	M0_RBC0	M0_COL	M0_RXD[1]	Y
AA	GPIO[1]	GPIO[7]	GPIO[8]	GPIO[15]	RAM_DATA[39]	GND	RAM_DATA[45]	RAM_DATA[52]	VDD_CORE	JTAG_TMS	CPU_ADDR[2]	CPU_ADDR[12]	VDD_CORE	VDD_CORE	CPU_DATA[8]	CPU_DATA[15]	CPU_DATA[23]	VDD_CORE	N/C	N/C	GND	M0_TXD[0]	M0_TXD[3]	M0_REFCLK	M0_RBC1	M0_RXD[0]	AA
AB	GPIO[5]	GPIO[11]	GPIO[14]	RAM_DATA[38]	RAM_DATA[43]	RAM_DATA[44]	RAM_DATA[51]	RAM_DATA[60]	TEST_MODE[1]	GND	CPU_ADDR[6]	CPU_ADDR[14]	CPU_ADDR[23]	CPU_TA	CPU_DATA[1]	CPU_DATA[7]	CPU_DATA[12]	CPU_DATA[22]	CPU_DATA[30]	N/C	N/C	M0_RXCLK	N/C	N/C	M1_ACTIVE_LED	N/C	AB
AC	GPIO[12]	GPIO[13]	RAM_DATA[37]	RAM_DATA[42]	RAM_DATA[46]	RAM_DATA[49]	RAM_DATA[59]	TEST_MODE[0]	JTAG_TDO	CPU_ADDR[4]	CPU_ADDR[9]	CPU_ADDR[16]	CPU_ADDR[22]	CPU_CLK	CPU_DREQ0	IC	CPU_DATA[10]	CPU_DATA[16]	CPU_DATA[21]	CPU_DATA[27]	N/C	N/C	N/C	N/C	N/C	M0_ACTIVE_LED	AC
AD	RAM_DATA[34]	RAM_DATA[36]	RAM_DATA[41]	RAM_DATA[47]	RAM_DATA[53]	RAM_DATA[58]	RAM_DATA[63]	JTAG_TCK	IC_GND	CPU_ADDR[7]	CPU_ADDR[11]	CPU_ADDR[17]	CPU_ADDR[21]	CPU_WE	CPU_SDACK2	CPU_IREQ1	CPU_DATA[3]	CPU_DATA[6]	CPU_DATA[14]	CPU_DATA[20]	CPU_DATA[24]	CPU_DATA[29]	N/C	N/C	N/C	N/C	AD
AE	RAM_DATA[35]	RAM_DATA[40]	RAM_DATA[48]	RAM_DATA[54]	RAM_DATA[57]	RAM_DATA[62]	JTAG_TRST	IC_GND	CPU_ADDR[3]	CPU_ADDR[8]	CPU_ADDR[13]	CPU_ADDR[18]	CPU_ADDR[20]	CPU_OE	CPU_TSALE	CPU_DREQ1	IC	CPU_DATA[4]	CPU_DATA[9]	CPU_DATA[13]	CPU_DATA[18]	CPU_DATA[25]	CPU_DATA[28]	N/C	N/C	N/C	AE
AF	GND	RAM_DATA[50]	RAM_DATA[55]	RAM_DATA[56]	RAM_DATA[61]	TEST_MODE[2]	JTAG_TDI	IC_GND	CPU_ADDR[5]	CPU_ADDR[10]	CPU_ADDR[15]	CPU_ADDR[19]	GND	CPU_CS	CPU_SDACK1	IC_VDD_IO	CPU_IREQ0	CPU_DATA[0]	CPU_DATA[5]	CPU_DATA[2]	CPU_DATA[11]	CPU_DATA[17]	CPU_DATA[19]	CPU_DATA[26]	CPU_DATA[31]	GND	AF

Figure 3 - ZL50110 Package View and Ball Positions

ZL50114 Package view from TOP side. Note that ball A1 is non-chamfered corner



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	GND	TDM_STo[1]	TDM_CLKo[3]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	GND	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	GND	A
B	TDM_FRMo_REF	TDM_STo[0]	TDM_STi[2]	TDM_CLKi[3]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	B
C	TDM_CLKiP	TDM_FRMi_REF	TDM_CLKi_REF	TDM_CLKo[1]	TDM_STi[3]	TDM_CLKo[2]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	C
D	RAM_DATA[3]	RAM_DATA[1]	TDM_CLKiS	RAM_DATA[0]	TDM_STi[0]	TDM_CLKi[1]	TDM_STo[3]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	D
E	RAM_DATA[10]	RAM_DATA[9]	RAM_DATA[5]	RAM_DATA[4]	RAM_DATA[2]	TDM_CLKo_REF	TDM_CLKi[0]	N/C	TDM_STi[1]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	GND	N/C	N/C	N/C	N/C	E
F	RAM_DATA[15]	RAM_DATA[13]	RAM_DATA[12]	RAM_DATA[6]	RAM_DATA[7]	GND	VDD_CORE	TDM_STo[2]	TDM_CLKo[0]	TDM_CLKi[2]	N/C	VDD_CORE	N/C	N/C	VDD_CORE	N/C	N/C	N/C	N/C	VDD_CORE	GND	N/C	N/C	N/C	N/C	N/C	F
G	RAM_DATA[21]	RAM_DATA[18]	RAM_DATA[16]	RAM_DATA[14]	RAM_DATA[11]	RAM_DATA[8]															N/C	N/C	M1_LINK_UP_LED	M0_LINK_UP_LED	M1_GIGABIT_LED	M_MDIO	G
H	RAM_DATA[25]	RAM_DATA[24]	RAM_DATA[23]	RAM_DATA[19]	RAM_DATA[17]	VDD_CORE															VDD_CORE	M0_GIGABIT_LED	M_MDC	N/C	N/C	N/C	H
J	RAM_DATA[29]	RAM_DATA[28]	RAM_DATA[27]	RAM_DATA[26]	RAM_DATA[22]	RAM_DATA[20]			VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO			N/C	N/C	N/C	N/C	N/C	N/C	J
K	RAM_PARITY[1]	RAM_PARITY[0]	RAM_DATA[31]	RAM_DATA[30]	GND	VDD_CORE			VDD_IO									VDD_IO			VDD_CORE	GND	N/C	N/C	N/C	N/C	K
L	RAM_PARITY[7]	RAM_PARITY[6]	RAM_PARITY[5]	RAM_PARITY[4]	RAM_PARITY[3]	RAM_PARITY[2]			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_RXER	M1_TXCLK	M1_CRS	N/C	N/C	N/C	L
M	RAM_ADDR[5]	RAM_ADDR[4]	RAM_ADDR[2]	RAM_ADDR[3]	RAM_ADDR[0]	RAM_ADDR[1]			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			VDD_CORE	M1_REFCLK	M1_RXCLK	M1_RXD[5]	M1_RXD[7]	M1_RXDV	M
N	GND	RAM_ADDR[6]	RAM_ADDR[7]	RAM_ADDR[8]	GND	VDD_CORE			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_GTX_CLK	GND	M1_TXER	M1_RXD[2]	M1_RXD[3]	GND	N
P	RAM_ADDR[9]	RAM_ADDR[10]	RAM_ADDR[11]	RAM_ADDR[13]	RAM_ADDR[16]	GND			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_TXD[2]	M1_TXD[6]	M1_TXEN	GND	M1_RXD[4]	M1_RXD[6]	P
R	RAM_ADDR[12]	RAM_ADDR[14]	RAM_ADDR[15]	RAM_ADDR[19]	IC_GND	IC			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_TXD[0]	M1_TXD[3]	M1_TXD[5]	M1_TXD[7]	M1_COL	M1_RXD[1]	R
T	RAM_ADDR[17]	RAM_ADDR[18]	RAM_BW_B	IC_GND	GND	A1VDD			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			VDD_CORE	M1_TXD[1]	M1_TXD[4]	GND	M1_RBC1	M1_RXD[0]	T
U	PLL_PRI	RAM_BW_A	RAM_BW_C	RAM_RW	SYSTEM_DEBUG	SYSTEM_CLK			VDD_IO									VDD_IO			M0_GTX_CLK	M0_RXD[2]	M0_RXD[5]	M0_TXCLK	M0_CRS	M1_RBC0	U
V	PLL_SEC	RAM_BW_D	RAM_BW_F	SYSTEM_RST	GPIO[2]	VDD_CORE			VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO			M0_TXD[7]	M0_TXER	M0_TXEN	M0_RXD[4]	M0_RXDV	M0_RXER	V
W	RAM_BW_E	RAM_BW_G	GPIO[0]	GPIO[3]	GPIO[9]	RAM_DATA[33]															M0_TXD[2]	M0_TXD[5]	M0_TXD[6]	M0_RXD[6]	M0_RXD[7]	M0_RXD[3]	W
Y	RAM_BW_H	GPIO[4]	GPIO[6]	GPIO[10]	RAM_DATA[32]	VDD_CORE															VDD_CORE	M0_TXD[1]	M0_TXD[4]	M0_RBC0	M0_COL	M0_RXD[1]	Y
AA	GPIO[1]	GPIO[7]	GPIO[8]	GPIO[15]	RAM_DATA[39]	GND	RAM_DATA[45]	RAM_DATA[52]	VDD_CORE	JTAG_TMS	CPU_ADDR[2]	CPU_ADDR[12]	VDD_CORE	VDD_CORE	CPU_DATA[8]	CPU_DATA[15]	CPU_DATA[23]	VDD_CORE	N/C	N/C	GND	M0_TXD[0]	M0_TXD[3]	M0_REFCLK	M0_RBC1	M0_RXD[0]	AA
AB	GPIO[5]	GPIO[11]	GPIO[14]	RAM_DATA[38]	RAM_DATA[43]	RAM_DATA[44]	RAM_DATA[51]	RAM_DATA[60]	TEST_MODE[1]	GND	CPU_ADDR[6]	CPU_ADDR[14]	CPU_ADDR[23]	CPU_TA	CPU_DATA[1]	CPU_DATA[7]	CPU_DATA[12]	CPU_DATA[22]	CPU_DATA[30]	N/C	N/C	M0_RXCLK	N/C	N/C	M1_ACTIVE_LED	N/C	AB
AC	GPIO[12]	GPIO[13]	RAM_DATA[37]	RAM_DATA[42]	RAM_DATA[46]	RAM_DATA[49]	RAM_DATA[59]	TEST_MODE[0]	JTAG_TDO	CPU_ADDR[4]	CPU_ADDR[9]	CPU_ADDR[16]	CPU_ADDR[22]	CPU_CLK	CPU_DREQ0	IC	CPU_DATA[10]	CPU_DATA[16]	CPU_DATA[21]	CPU_DATA[27]	N/C	N/C	N/C	N/C	N/C	M0_ACTIVE_LED	AC
AD	RAM_DATA[34]	RAM_DATA[36]	RAM_DATA[41]	RAM_DATA[47]	RAM_DATA[53]	RAM_DATA[58]	RAM_DATA[63]	JTAG_TCK	IC_GND	CPU_ADDR[7]	CPU_ADDR[11]	CPU_ADDR[17]	CPU_ADDR[21]	CPU_WE	CPU_SDACK2	CPU_IREQ1	CPU_DATA[3]	CPU_DATA[6]	CPU_DATA[14]	CPU_DATA[20]	CPU_DATA[24]	CPU_DATA[29]	N/C	N/C	N/C	N/C	AD
AE	RAM_DATA[35]	RAM_DATA[40]	RAM_DATA[48]	RAM_DATA[54]	RAM_DATA[57]	RAM_DATA[62]	JTAG_TRST	IC_GND	CPU_ADDR[3]	CPU_ADDR[8]	CPU_ADDR[13]	CPU_ADDR[18]	CPU_ADDR[20]	CPU_OE	CPU_TSALE	CPU_DREQ1	IC	CPU_DATA[4]	CPU_DATA[9]	CPU_DATA[13]	CPU_DATA[18]	CPU_DATA[25]	CPU_DATA[28]	N/C	N/C	N/C	AE
AF	GND	RAM_DATA[50]	RAM_DATA[55]	RAM_DATA[56]	RAM_DATA[61]	TEST_MODE[2]	JTAG_TDI	IC_GND	CPU_ADDR[5]	CPU_ADDR[10]	CPU_ADDR[15]	CPU_ADDR[19]	GND	CPU_CS	CPU_SDACK1	IC_VDD_IO	CPU_IREQ0	CPU_DATA[0]	CPU_DATA[5]	CPU_DATA[2]	CPU_DATA[11]	CPU_DATA[17]	CPU_DATA[19]	CPU_DATA[26]	CPU_DATA[31]	GND	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 4 - ZL50114 Package View and Ball Positions

Ball Signal Assignment

Ball Number	Signal Name
A1	GND
A2	TDM_STo[1]
A3	TDM_CLKo[3]
A4‡	TDM_STo[4]
A5‡	TDM_STo[5]
A6‡	TDM_STi[6]
A7‡	TDM_STo[7]
A8‡	TDM_STi[7]
A9†	TDM_CLKo[10]
A10†	TDM_CLKi[10]
A11†	TDM_CLKi[11]
A12†	TDM_CLKo[13]
A13	GND
A14†	TDM_STo[13]
A15†	TDM_STo[14]
A16†	TDM_CLKo[15]
A17†	TDM_STo[16]
A18†	TDM_CLKo[18]
A19†	TDM_STi[18]
A20†	TDM_CLKi[20]
A21†	TDM_STi[20]
A22†	TDM_STo[21]
A23†	TDM_STi[21]
A24†	TDM_CLKo[24]
A25†	TDM_CLKo[25]
A26	GND
B1	TDM_FRMo_REF
B2	TDM_STo[0]
B3	TDM_STi[2]
B4	TDM_CLKi[3]
B5‡	TDM_STi[4]
B6‡	TDM_CLKo[6]
B7‡	TDM_STo[6]
B8†	TDM_CLKo[8]
B9†	TDM_CLKi[9]
B10†	TDM_STo[10]
B11†	TDM_STi[10]
B12†	TDM_CLKi[12]
B13†	TDM_STo[12]
B14†	TDM_STi[13]
B15†	TDM_CLKi[15]
B16†	TDM_STi[15]
B17†	TDM_STi[17]
B18†	TDM_CLKi[18]
B19†	TDM_CLKo[20]
B20†	TDM_STo[19]
B21†	TDM_STo[22]
B22†	TDM_CLKo[23]
B23†	TDM_STo[24]
B24†	TDM_CLKo[26]
B25†	TDM_STi[24]
B26†	TDM_CLKo[27]
C1	TDM_CLKiP
C2	TDM_FRMi_REF
C3	TDM_CLKi_REF
C4	TDM_CLKo[1]
C5	TDM_STi[3]
C6	TDM_CLKo[2]
C7‡	TDM_CLKi[6]
C8‡	TDM_CLKi[7]
C9†	TDM_CLKo[9]
C10†	TDM_STo[9]
C11†	TDM_STi[9]
C12†	TDM_STi[11]
C13†	TDM_CLKi[13]
C14†	TDM_CLKo[14]
C15†	TDM_CLKo[16]
C16†	TDM_STi[16]
C17†	TDM_CLKo[17]
C18†	TDM_STi[19]
C19†	TDM_CLKo[21]
C20†	TDM_CLKi[21]
C21†	TDM_CLKi[24]
C22†	TDM_STi[22]
C23†	TDM_STo[26]
C24†	TDM_CLKi[27]
C25†	TDM_STi[27]
C26†	TDM_STi[28]
D1	RAM_DATA[3]
D2	RAM_DATA[1]
D3	TDM_CLKiS
D4	RAM_DATA[0]
D5	TDM_STi[0]
D6	TDM_CLKi[1]
D7	TDM_STo[3]
D8‡	TDM_STi[5]
D9‡	TDM_CLKi[5]
D10‡	TDM_CLKo[7]
D11†	TDM_STi[8]
D12†	TDM_CLKo[11]
D13†	TDM_STi[12]
D14†	TDM_STi[14]
D15†	TDM_CLKi[16]
D16†	TDM_CLKo[19]
D17†	TDM_STo[18]
D18†	TDM_STo[20]
D19†	TDM_CLKo[22]
D20†	TDM_STo[27]
D21†	TDM_STo[25]
D22†	TDM_CLKi[26]
D23†	TDM_CLKo[28]
D24†	TDM_CLKi[29]
D25†	TDM_STi[29]
D26†	TDM_STi[31]
E1	RAM_DATA[10]
E2	RAM_DATA[9]
E3	RAM_DATA[5]
E4	RAM_DATA[4]
E5	RAM_DATA[2]
E6	TDM_CLKo_REF
E7	TDM_CLKi[0]
E8‡	TDM_CLKo[4]
E9	TDM_STi[1]
E10‡	TDM_CLKi[4]
E11†	TDM_STo[8]
E12†	TDM_CLKi[8]
E13†	TDM_CLKo[12]
E14†	TDM_STo[15]
E15†	TDM_CLKi[17]

Ball Number	Signal Name
E16†	TDM_CLKi[19]
E17†	TDM_STo[23]
E18†	TDM_STi[23]
E19†	TDM_CLKi[25]
E20†	TDM_STi[26]
E21†	TDM_CLKi[28]
E22	GND
E23†	TDM_CLKo[30]
E24†	TDM_CLKi[30]
E25†	TDM_STi[30]
E26†	TDM_STo[29]
F1	RAM_DATA[15]
F2	RAM_DATA[13]
F3	RAM_DATA[12]
F4	RAM_DATA[6]
F5	RAM_DATA[7]
F6	GND
F7	VDD_CORE
F8	TDM_STo[2]
F9	TDM_CLKo[0]
F10	TDM_CLKi[2]
F11‡	TDM_CLKo[5]
F12	VDD_CORE
F13†	TDM_STo[11]
F14†	TDM_CLKi[14]
F15	VDD_CORE
F16†	TDM_STo[17]
F17†	TDM_CLKi[22]
F18†	TDM_STi[25]
F19†	TDM_CLKi[23]
F20	VDD_CORE
F21	GND
F22†	TDM_CLKi[31]
F23†	TDM_CLKo[29]
F24†	TDM_STo[28]
F25†	TDM_CLKo[31]
F26†	M1_LINKUP_LED
G1	RAM_DATA[21]
G2	RAM_DATA[18]
G3	RAM_DATA[16]
G4	RAM_DATA[14]
G5	RAM_DATA[11]
G6	RAM_DATA[8]
G21†	TDM_STo[31]
G22†	TDM_STo[30]
G23	M1/2_LINKUP_LED
G24	M0/3_LINKUP_LED
G25	M1_GIGABIT_LED
G26	M_MDIO
H1	RAM_DATA[25]
H2	RAM_DATA[24]
H3	RAM_DATA[23]
H4	RAM_DATA[19]
H5	RAM_DATA[17]
H6	VDD_CORE
H21	VDD_CORE
H22	M0_GIGABIT_LED
H23	M_MDC
H24†	M3_CRS
H25†	M3_TXCLK
H26†	M3_RXER
J1	RAM_DATA[29]
J2	RAM_DATA[28]
J3	RAM_DATA[27]
J4	RAM_DATA[26]
J5	RAM_DATA[22]
J6	RAM_DATA[20]
J9	VDD_IO
J10	VDD_IO
J11	VDD_IO
J12	VDD_IO
J13	VDD_IO
J14	VDD_IO
J15	VDD_IO
J16	VDD_IO
J17	VDD_IO
J18	VDD_IO
J21†	M3_RXDV
J22†	M3_RXD[3]
J23†	M3_RXD[2]
J24†	M3_RXD[1]
J25†	M3_RXD[0]
J26†	M3_COL
K1	RAM_PARITY[1]
K2	RAM_PARITY[0]
K3	RAM_DATA[31]
K4	RAM_DATA[30]
K5	GND
K6	VDD_CORE
K9	VDD_IO
K18	VDD_IO
K21	VDD_CORE
K22	GND
K23†	M3_TXD[3]
K24†	M3_TXEN
K25†	M3_TXER
K26†	M3_RXCLK
L1	RAM_PARITY[7]
L2	RAM_PARITY[6]
L3	RAM_PARITY[5]
L4	RAM_PARITY[4]
L5	RAM_PARITY[3]
L6	RAM_PARITY[2]
L9	VDD_IO
L11	GND
L12	GND
L13	GND
L14	GND
L15	GND
L16	GND
L18	VDD_IO
L21	M1_RXER
L22	M1_TXCLK
L23	M1_CRS
L24†	M3_TXD[0]
L25†	M3_TXD[1]
L26†	M3_TXD[2]
M1	RAM_ADDR[5]
M2	RAM_ADDR[4]
M3	RAM_ADDR[2]

Ball Number	Signal Name
M4	RAM_ADDR[3]
M5	RAM_ADDR[0]
M6	RAM_ADDR[1]
M9	VDD_IO
M11	GND
M12	GND
M13	GND
M14	GND
M15	GND
M16	GND
M18	VDD_IO
M21	VDD_CORE
M22	M1_REFCLK
M23	M1_RXCLK
M24	M1_RXD[5]
M25	M1_RXD[7]
M26	M1_RXDV
N1	GND
N2	RAM_ADDR[6]
N3	RAM_ADDR[7]
N4	RAM_ADDR[8]
N5	GND
N6	VDD_CORE
N9	VDD_IO
N11	GND
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N18	VDD_IO
N21	M1_GTX_CLK
N22	GND
N23	M1_TXER
N24	M1_RXD[2]
N25	M1_RXD[3]
N26	GND
P1	RAM_ADDR[9]
P2	RAM_ADDR[10]
P3	RAM_ADDR[11]

Ball Number	Signal Name
P4	RAM_ADDR[13]
P5	RAM_ADDR[16]
P6	GND
P9	VDD_IO
P11	GND
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P18	VDD_IO
P21	M1_TXD[2]
P22	M1_TXD[6]
P23	M1_TXEN
P24	GND
P25	M1_RXD[4]
P26	M1_RXD[6]
R1	RAM_ADDR[12]
R2	RAM_ADDR[14]
R3	RAM_ADDR[15]
R4	RAM_ADDR[19]
R5	IC_GND
R6	IC
R9	VDD_IO
R11	GND
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R18	VDD_IO
R21	M1_TXD[0]
R22	M1_TXD[3]
R23	M1_TXD[5]
R24	M1_TXD[7]
R25	M1_COL
R26	M1_RXD[1]
T1	RAM_ADDR[17]
T2	RAM_ADDR[18]
T3	RAM_BW_B

Ball Number	Signal Name
T4	IC_GND
T5	GND
T6	A1VDD
T9	VDD_IO
T11	GND
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND
T18	VDD_IO
T21	VDD_CORE
T22	M1_TXD[1]
T23	M1_TXD[4]
T24	GND
T25	M1_RBC1
T26	M1_RXD[0]
U1	PLL_PRI
U2	RAM_BW_A
U3	RAM_BW_C
U4	RAM_RW
U5	SYSTEM_DEBUG
U6	SYSTEM_CLK
U9	VDD_IO
U18	VDD_IO
U21	M0_GTX_CLK
U22	M0_RXD[2]
U23	M0_RXD[5]
U24	M0_TXCLK
U25	M0_CRS
U26	M1_RBC0
V1	PLL_SEC
V2	RAM_BW_D
V3	RAM_BW_F
V4	SYSTEM_RST
V5	GPIO[2]
V6	VDD_CORE
V9	VDD_IO
V10	VDD_IO
V11	VDD_IO

Ball Number	Signal Name
V12	VDD_IO
V13	VDD_IO
V14	VDD_IO
V15	VDD_IO
V16	VDD_IO
V17	VDD_IO
V18	VDD_IO
V21	M0_TXD[7]
V22	M0_TXER
V23	M0_TXEN
V24	M0_RXD[4]
V25	M0_RXDV
V26	M0_RXER
W1	RAM_BW_E
W2	RAM_BW_G
W3	GPIO[0]
W4	GPIO[3]
W5	GPIO[9]
W6	RAM_DATA[33]
W21	M0_TXD[2]
W22	M0_TXD[5]
W23	M0_TXD[6]
W24	M0_RXD[6]
W25	M0_RXD[7]
W26	M0_RXD[3]
Y1	RAM_BW_H
Y2	GPIO[4]
Y3	GPIO[6]
Y4	GPIO[10]
Y5	RAM_DATA[32]
Y6	VDD_CORE
Y21	VDD_CORE
Y22	M0_TXD[1]
Y23	M0_TXD[4]
Y24	M0_RBC0
Y25	M0_COL
Y26	M0_RXD[1]
AA1	GPIO[1]
AA2	GPIO[7]
AA3	GPIO[8]

Ball Number	Signal Name
AA4	GPIO[15]
AA5	RAM_DATA[39]
AA6	GND
AA7	RAM_DATA[45]
AA8	RAM_DATA[52]
AA9	VDD_CORE
AA10	JTAG_TMS
AA11	CPU_ADDR[2]
AA12	CPU_ADDR[12]
AA13	VDD_CORE
AA14	VDD_CORE
AA15	CPU_DATA[8]
AA16	CPU_DATA[15]
AA17	CPU_DATA[23]
AA18	VDD_CORE
AA19†	M2_RXCLK
AA20†	M2_RXDV
AA21	GND
AA22	M0_TXD[0]
AA23	M0_TXD[3]
AA24	M0_REFCLK
AA25	M0_RBC1
AA26	M0_RXD[0]
AB1	GPIO[5]
AB2	GPIO[11]
AB3	GPIO[14]
AB4	RAM_DATA[38]
AB5	RAM_DATA[43]
AB6	RAM_DATA[44]
AB7	RAM_DATA[51]
AB8	RAM_DATA[60]
AB9	TEST_MODE[1]
AB10	GND
AB11	CPU_ADDR[6]
AB12	CPU_ADDR[14]
AB13	CPU_ADDR[23]
AB14	CPU_TA
AB15	CPU_DATA[1]
AB16	CPU_DATA[7]
AB17	CPU_DATA[12]

Ball Number	Signal Name
AB18	CPU_DATA[22]
AB19	CPU_DATA[30]
AB20†	M2_TXER
AB21†	M2_RXD[1]
AB22	M0_RXCLK
AB23†	M0_LINKUP_LED
AB24†	M2_ACTIVE_LED
AB25	M1_ACTIVE_LED
AB26†	M3_ACTIVE_LED
AC1	GPIO[12]
AC2	GPIO[13]
AC3	RAM_DATA[37]
AC4	RAM_DATA[42]
AC5	RAM_DATA[46]
AC6	RAM_DATA[49]
AC7	RAM_DATA[59]
AC8	TEST_MODE[0]
AC9	JTAG_TDO
AC10	CPU_ADDR[4]
AC11	CPU_ADDR[9]
AC12	CPU_ADDR[16]
AC13	CPU_ADDR[22]
AC14	CPU_CLK
AC15	CPU_DREQ0
AC16	IC
AC17	CPU_DATA[10]
AC18	CPU_DATA[16]
AC19	CPU_DATA[21]
AC20	CPU_DATA[27]
AC21†	M2_TXD[1]
AC22†	M2_TXEN
AC23†	M2_RXD[2]
AC24†	M2_RXER
AC25†	M2_CRS
AC26	M0_ACTIVE_LED
AD1	RAM_DATA[34]
AD2	RAM_DATA[36]
AD3	RAM_DATA[41]
AD4	RAM_DATA[47]
AD5	RAM_DATA[53]

Ball Number	Signal Name
AD6	RAM_DATA[58]
AD7	RAM_DATA[63]
AD8	JTAG_TCK
AD9	IC_GND
AD10	CPU_ADDR[7]
AD11	CPU_ADDR[11]
AD12	CPU_ADDR[17]
AD13	CPU_ADDR[21]
AD14	CPU_WE
AD15	CPU_SDACK2
AD16	CPU_IREQ1
AD17	CPU_DATA[3]
AD18	CPU_DATA[6]
AD19	CPU_DATA[14]
AD20	CPU_DATA[20]
AD21	CPU_DATA[24]
AD22	CPU_DATA[29]
AD23†	M2_TXD[2]
AD24†	M2_RXD[0]
AD25†	M2_RXD[3]
AD26†	M2_TXCLK
AE1	RAM_DATA[35]
AE2	RAM_DATA[40]
AE3	RAM_DATA[48]
AE4	RAM_DATA[54]
AE5	RAM_DATA[57]
AE6	RAM_DATA[62]
AE7	JTAG_TRST
AE8	IC_GND
AE9	CPU_ADDR[3]
AE10	CPU_ADDR[8]
AE11	CPU_ADDR[13]
AE12	CPU_ADDR[18]
AE13	CPU_ADDR[20]
AE14	CPU_OE
AE15	CPU_TS_ALE
AE16	CPU_DREQ1
AE17	IC
AE18	CPU_DATA[4]
AE19	CPU_DATA[9]
AE20	CPU_DATA[13]
AE21	CPU_DATA[18]
AE22	CPU_DATA[25]
AE23	CPU_DATA[28]
AE24†	M2_TXD[0]
AE25†	M2_TXD[3]
AE26†	M2_COL
AF1	GND
AF2	RAM_DATA[50]
AF3	RAM_DATA[55]
AF4	RAM_DATA[56]
AF5	RAM_DATA[61]
AF6	TEST_MODE[2]
AF7	JTAG_TDI
AF8	IC_GND
AF9	CPU_ADDR[5]
AF10	CPU_ADDR[10]
AF11	CPU_ADDR[15]
AF12	CPU_ADDR[19]
AF13	GND
AF14	CPU_CS
AF15	CPU_SDACK1
AF16	IC_VDD_IO
AF17	CPU_IREQ0
AF18	CPU_DATA[0]
AF19	CPU_DATA[5]
AF20	CPU_DATA[2]
AF21	CPU_DATA[11]
AF22	CPU_DATA[17]
AF23	CPU_DATA[19]
AF24	CPU_DATA[26]
AF25	CPU_DATA[31]
AF26	GND

† Not Connected on ZL50110 and ZL50114 - leave open circuit.

‡ Not Connected on ZL50114 - leave open circuit.

N/C - Not Connected - leave open circuit.

IC - Internally Connected - leave open circuit.

IC_GND - tie to ground

IC_VDD_IO - tie to VDD_IO

3.0 External Interface Description

The following key applies to all tables:

I	Input
O	Output
D	Internal 100 kΩ pull-down resistor present
U	Internal 100 kΩ pull-up resistor present
T	Tri-state Output

3.1 TDM Interface

All TDM Interface signals are 5 V tolerant.

All TDM Interface outputs are high impedance while System Reset is LOW.

All TDM Interface inputs (including data, clock and frame pulse) have internal pull-down resistors so they can be safely left unconnected if not used.

3.1.1 ZL50111 Variant TDM Stream Connection

Signal	I/O	Package Balls				Description
TDM_STi[31:0]	I D	[31]	D26	[15]	B16	TDM port serial data input streams. For different standards these pins are given different identities: ST-BUS: TDM_STi[31:0] H.110: TDM_D[31:0] H-MVIP: TDM_HDS[31:0] Triggered on rising edge or falling edge depending on standard. At 8.192 Mbps only streams [7:0] are used, with 128 channels per stream. Streams [7:0] are used for J2, and streams [1:0] are used for T3, E3 pr STS-1.
		[30]	E25	[14]	D14	
		[29]	D25	[13]	B14	
		[28]	C26	[12]	D13	
		[27]	C25	[11]	C12	
		[26]	E20	[10]	B11	
		[25]	F18	[9]	C11	
		[24]	B25	[8]	D11	
		[23]	E18	[7]	A8	
		[22]	C22	[6]	A6	
		[21]	A23	[5]	D8	
		[20]	A21	[4]	B5	
		[19]	C18	[3]	C5	
		[18]	A19	[2]	B3	
		[17]	B17	[1]	E9	
		[16]	C16	[0]	D5	

Table 2 - TDM Interface ZL50111 Stream Pin Definition

Signal	I/O	Package Balls				Description
TDM_STo[31:0]	OT	[31] G21 [30] G22 [29] E26 [28] F24 [27] D20 [26] C23 [25] D21 [24] B23 [23] E17 [22] B21 [21] A22 [20] D18 [19] B20 [18] D17 [17] F16 [16] A17		[15] E14 [14] A15 [13] A14 [12] B13 [11] F13 [10] B10 [9] C10 [8] E11 [7] A7 [6] B7 [5] A5 [4] A4 [3] D7 [2] F8 [1] A2 [0] B2		TDM port serial data output streams. For different standards these pins are given different identities: ST-BUS: TDM_STo[31:0] H.110: TDM_D[31:0] H-MVIP: TDM_HDS[31:0] Triggered on rising edge or falling edge depending on standard. At 8.192 Mbps only streams [7:0] are used, with 128 channels per stream. Streams [7:0] are used for J2, and streams [1:0] are used for T3, E3 or STS-1.
TDM_CLKi[31:0]	I D	[31] F22 [30] E24 [29] D24 [28] E21 [27] C24 [26] D22 [25] E19 [24] C21 [23] F19 [22] F17 [21] C20 [20] A20 [19] E16 [18] B18 [17] E15 [16] D15		[15] B15 [14] F14 [13] C13 [12] B12 [11] A11 [10] A10 [9] B9 [8] E12 [7] C8 [6] C7 [5] D9 [4] E10 [3] B4 [2] F10 [1] D6 [0] E7		TDM port clock inputs. Programmable as active high or low. Can accept frequencies of 1.544 MHz, 2.048 MHz, 4.096 MHz, 6.312 MHz, 8.192 MHz, 16.384 MHz, 34.368 MHz or 44.736 MHz depending on standard used. At 8.192 Mbps only streams [7:0] are used. Streams [7:0] are used for J2, and streams [1:0] are used for T3, E3 or STS-1.

Table 2 - TDM Interface ZL50111 Stream Pin Definition (continued)

Signal	I/O	Package Balls				Description
TDM_CLKo[31:0]	O	[31]	F25	[15]	A16	TDM port clock outputs. Will generate 1.544 MHz, 2.048 MHz, 4.096 MHz, 6.312 MHz, 8.192 MHz, 16.384 MHz, 34.368 MHz or 44.736 MHz depending on standard used. At 8.192 Mbps only streams [7:0] are used. Streams [7:0] are used for J2, and streams [1:0] are used for T3, E3 or STS-1.
		[30]	E23	[14]	C14	
		[29]	F23	[13]	A12	
		[28]	D23	[12]	E13	
		[27]	B26	[11]	D12	
		[26]	B24	[10]	A9	
		[25]	A25	[9]	C9	
		[24]	A24	[8]	B8	
		[23]	B22	[7]	D10	
		[22]	D19	[6]	B6	
		[21]	C19	[5]	F11	
		[20]	B19	[4]	E8	
		[19]	D16	[3]	A3	
		[18]	A18	[2]	C6	
		[17]	C17	[1]	C4	
		[16]	C15	[0]	F9	

Table 2 - TDM Interface ZL50111 Stream Pin Definition (continued)

Note: Speed modes:
2.048 Mbps - all 32 streams active (bits [31:0]), with 32 channels per stream - 1024 total channels.
8.192 Mbps - 8 streams active (bits [7:0]), with 128 channels per stream - 1024 total channels.
J2 - 8 streams active (bits [7:0]), with 98 channels per stream - 784 total channels.
E3 - 2 streams active (bits [1:0]), with 537 channels per stream - 1074 total channels.
T3 - 2 streams active (bits [1:0]), with 699 channels per stream - 1398 total channels.

Note: All TDM Interface inputs (including data, clock and frame pulse) have internal pull-down resistors so they can be safely left unconnected if not used.

3.1.2 ZL50110 Variant TDM stream connection

Signal	I/O	Package Balls	Description
TDM_STi[7:0]	I D	[7] A8 [6] A6 [5] D8 [4] B5 [3] C5 [2] B3 [1] E9 [0] D5	TDM port serial data input streams. For different standards these pins are given different identities: ST-BUS: TDM_STi[7:0] H.110: TDM_D[7:0] H-MVIP: TDM_HDS[7:0] Triggered on rising edge or falling edge depending on standard. At 8.192 Mbps only streams [1:0] are used. Streams [1:0] are used for J2.
TDM_STo[7:0]	OT	[7] A7 [6] B7 [5] A5 [4] A4 [3] D7 [2] F8 [1] A2 [0] B2	TDM port serial data output streams. For different standards these pins are given different identities: ST-BUS: TDM_STo[7:0] H.110: TDM_D[7:0] H-MVIP: TDM_HDS[7:0] Triggered on rising edge or falling edge depending on standard. At 8.192 Mbps only streams [1:0] are used. Streams [1:0] are used for J2.
TDM_CLKi[7:0]	I D	[7] C8 [6] C7 [5] D9 [4] E10 [3] B4 [2] F10 [1] D6 [0] E7	TDM port clock inputs programmable as active high or low. Can accept frequencies of 1.544 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 6.312 MHz or 16.384 MHz depending on standard used. At 8.192 Mbps only streams [1:0] are used. Streams [1:0] are used for J2.
TDM_CLKo[7:0]	OT	[7] D10 [6] B6 [5] F11 [4] E8 [3] A3 [2] C6 [1] C4 [0] F9	TDM port clock outputs. Will generate 1.544 MHz, 2.048 MHz, 4.096 MHz, 6.312 MHz, 8.192 MHz or 16.384 MHz depending on standard used. At 8.192 Mbps only streams [1:0] are used. Streams [1:0] are used for J2.

Table 3 - TDM Interface ZL50110 Stream Pin Definition

Note: Speed modes:
2.048 Mbps - all 8 streams active (bits [7:0]), with 32 channels per stream - 256 total channels.
8.192 Mbps - 2 streams active (bits [1:0]), with 128 channels per stream - 256 total channels.
J2 - 2 streams active (bits [1:0]), with 98 channels per stream - 196 total channels.

Note: All TDM Interface inputs (including data, clock and frame pulse) have internal pull-down resistors so they can be safely left unconnected if not used.

3.1.3 ZL50114 Variant TDM Stream Connection

Signal	I/O	Package Balls	Description
TDM_STi[3:0]	I D	[3] C5 [2] B3 [1] E9 [0] D5	TDM port serial data input streams. For different standards these pins are given different identities: ST-BUS: TDM_STi[3:0] H.110: TDM_D[3:0] H-MVIP: TDM_HDS[3:0] Triggered on rising edge or falling edge depending on standard. At 8.192 Mbps only streams [1:0] are used. Streams [1:0] are used for J2.
TDM_STo[3:0]	OT	[3] D7 [2] F8 [1] A2 [0] B2	TDM port serial data output streams. For different standards these pins are given different identities: ST-BUS: TDM_STo[3:0] H.110: TDM_D[3:0] H-MVIP: TDM_HDS[3:0] Triggered on rising edge or falling edge depending on standard. At 8.192 Mbps only streams [1:0] are used. Streams [1:0] are used for J2.
TDM_CLKi[3:0]	I D	[3] B4 [2] F10 [1] D6 [0] E7	TDM port clock inputs programmable as active high or low. Can accept frequencies of 1.544 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 6.312 MHz or 16.384 MHz depending on standard used. At 8.192 Mbps only streams [1:0] are used. Streams [1:0] are used for J2.
TDM_CLKo[3:0]	OT	[3] A3 [2] C6 [1] C4 [0] F9	TDM port clock outputs. Will generate 1.544 MHz, 2.048 MHz, 4.096 MHz, 6.312 MHz, 8.192 MHz or 16.384 MHz depending on standard used. At 8.192 Mbps only streams [1:0] are used. Streams [1:0] are used for J2.

Table 4 - TDM Interface ZL50114 Stream Pin Definition

Note: Speed modes:
2.048 Mbps - all 4 streams active (bits [3:0]), with 32 channels per stream - 128 total channels.
8.192 Mbps - 2 streams active (bits [1:0]), with 128 channels per stream - 256 total channels.
J2 - 2 streams active (bits [1:0]), with 98 channels per stream - 196 total channels.

Note: All TDM Interface inputs (including data, clock and frame pulse) have internal pull-down resistors so they can be safely left unconnected if not used.

3.1.4 TDM Signals Common to ZL50111, ZL50110 and ZL50114

Signal	I/O	Package Balls	Description
TDM_CLKi_REF	I D	C3	TDM port reference clock input for backplane operation
TDM_CLKo_REF	O	E6	TDM port reference clock output for backplane operation
TDM_FRMi_REF	I D	C2	TDM port reference frame input. For different standards this pin is given a different identity: ST-BUS: TDM_F0i H.110: TDM_FRAME H-MVIP: TDM_F0 Signal is normally active low, but can be active high depending on standard. Indicates the start of a TDM frame by pulsing every 125 µs. Normally will straddle rising edge or falling edge of clock pulse, depending on standard and clock frequency.
TDM_FRMo_REF	O	B1	TDM port reference frame output. For different standards this pin is given a different identity: ST-BUS: TDM_F0o H.110: TDM_FRAME H-MVIP: TDM_F0 Signal is normally active low, but can be active high depending on standard. Indicates the start of a TDM frame by pulsing every 125 µs. Normally will straddle rising edge or falling edge of clock pulse, depending on standard and clock frequency.

Table 5 - TDM Interface Common Pin Definition

3.2 PAC Interface

All PAC Interface signals are 5 V tolerant

All PAC Interface outputs are high impedance while System Reset is LOW.

Signal	I/O	Package Balls	Description
TDM_CLKiP	I D	C1	Primary reference clock input. Should be driven by external clock source to provide locking reference to internal / optional external DPLL in TDM master mode. Also provides PRS clock for RTP timestamps in synchronous modes. Acceptable frequency range: 8 kHz - 34.368 MHz.
TDM_CLKiS	I D	D3	Secondary reference clock input. Backup external reference for automatic switch-over in case of failure of TDM_CLKiP source.
PLL_PRI	OT	U1	Primary reference output to optional external DPLL. Multiplexed & frequency divided reference output for support of optional external DPLL. Expected frequency range: 8 kHz - 16.384 MHz.
PLL_SEC	OT	V1	Secondary reference output to optional external DPLL Multiplexed & frequency divided reference output for support of optional external DPLL. Expected frequency range: 8 kHz - 16.384 MHz.

Table 6 - PAC Interface Package Ball Definition

3.3 Packet Interfaces

For the ZL50111 variant the packet interface is capable of either 3 MII interfaces, 2 GMII interfaces or 2 TBI (1000 Mbps) interfaces. The TBI interface is a PCS interface supported by an integrated 1000BASE-X PCS module. The ZL50110 variant has either 2 MII interfaces, 2 GMII interfaces or 2 TBI (1000 Mbps) interfaces. Ports 2 and 3 are not available on the ZL50110 device.

NOTE: In GMII/TBI mode only 1 GMAC port may be used to receive data. The second GMAC port is for redundancy purposes only.

Data for all three types of packet switching is based on Specification IEEE Std. 802.3 - 2000. For the ZL50111 variant, only Ports 0 and 1 have the 1000 Mbps capability necessary for the GMII/TBI interface. In either GMII or TBI mode Ports 2 and 3 are disabled. Alternatively 3 ports can be used as 100 Mbps MII interfaces, either Ports 0, 1 and 2 or Ports 0, 1 and 3.

Note: Port 2 and Port 3 can not be used to receive data simultaneously, they are mutually exclusive for packet reception. They may both be used for packet transmission if required.

Table 7 maps the signal pins used in the MII interface to those used in the GMII and TBI interface. Table 8 shows all the pins and their related package ball, but is based on the GMII/MII configuration.

All Packet Interface signals are 5V tolerant, and all outputs are high impedance while System Reset is LOW.

MII	GMII	TBI (PCS)
M*n*_LINKUP_LED	M*n*_LINKUP_LED	M*n*_LINKUP_LED
M*n*_ACTIVE_LED	M*n*_ACTIVE_LED	M*n*_ACTIVE_LED
-	M*n*_GIGABIT_LED	M*n*_GIGABIT_LED
-	M*n*_REFCLK	M*n*_REFCLK
M*n*_RXCLK	M*n*_RXCLK	M*n*_RBC0
M*n*_COL	M*n*_COL	M*n*_RBC1
M*n*_RXD[3:0]	M*n*_RXD[7:0]	M*n*_RXD[7:0]
M*n*_RXDV	M*n*_RXDV	M*n*_RXD[8]
M*n*_RXER	M*n*_RXER	M*n*_RXD[9]
M*n*_CRS	M*n*_CRS	M*n*_Signal_Detect
M*n*_TXCLK	-	-
M*n*_TXD[3:0]	M*n*_TXD[7:0]	M*n*_TXD[7:0]
M*n*_TXEN	M*n*_TXEN	M*n*_TXD[8]
M*n*_TXER	M*n*_TXER	M*n*_TXD[9]
-	M*n*_GTX_CLK	M*n*_GTX_CLK

Table 7 - Packet Interface Signal Mapping - MII to GMII/TBI

Note: M*n* can be either M0, M1, M2, or M3 for ZL50111 variant; and M0 or M1 for ZL50110 variant.

Signal	I/O	Package Balls	Description
M_MDC	O	H23	MII management data clock. Common for all four MII ports. It has a minimum period of 400ns (maximum freq. 2.5 MHz), and is independent of the TXCLK and RXCLK.
M_MDIO	ID/ OT	G26	MII management data I/O. Common for all four MII ports at up to 2.5 MHz. It is bi-directional between the ZL50110/11/14 and the Ethernet station management entity. Data is passed synchronously with respect to M_MDC.

Table 8 - MII Management Interface Package Ball Definition

MII Port 0			
Signal	**I/O**	**Package Balls**	**Description**
M0_LINKUP_LED	O	G24 on ZL50110/4 AB23 on ZL50111	LED drive for MAC 0 to indicate port is linked up. Logic 0 output = LED on Logic 1 output = LED off
M0_ACTIVE_LED	O	AC26	LED drive for MAC 0 to indicate port is transmitting or receiving packet data. Logic 0 output = LED on Logic 1 output = LED off
M0_GIGABIT_LED	O	H22	LED drive for MAC 0 to indicate operation at Gbps Logic 0 output = LED on Logic 1 output = LED off
M0_REFCLK	I D	AA24	**GMII/TBI** - Reference Clock input at 125 MHz. Can be used to lock receive circuitry (RX) to M0_GTXCLK rather than recovering the RXCLK (or RBC0 and RBC1). Useful, for example, in the absence of valid serial data. **NOTE:** In **MII** mode this pin must be driven with the same clock as M0_RXCLK.
M0_RXCLK	I U	AB22	GMII/MII - M0_RXCLK. Accepts the following frequencies: 25.0 MHz MII 100 Mbps 125.0 MHz GMII 1 Gbps

Table 9 - MII Port 0 Interface Package Ball Definition

MII Port 0			
Signal	**I/O**	**Package Balls**	**Description**
M0_RBC0	I U	Y24	TBI - M0_RBC0. Used as a clock when in TBI mode. Accepts 62.5 MHz, and is 180°C out of phase with M0_RBC1. Receive data is clocked at each rising edge of M1_RBC1 and M1_RBC0, resulting in 125 MHz sample rate.
M0_RBC1	I U	AA25	TBI - M0_RBC1 Used as a clock when in TBI mode. Accepts 62.5 MHz, and is 180°C out of phase with M0_RBC0. Receive data is clocked at each rising edge of M0_RBC1 and M0_RBC0, resulting in 125 MHz sample rate.
M0_COL	I D	Y25	GMII/MII - M0_COL. Collision Detection. This signal is independent of M0_TXCLK and M0_RXCLK, and is asserted when a collision is detected on an attempted transmission. It is active high, and only specified for half-duplex operation.
M0_RXD[7:0]	I U	[7] W25 [3] W26 [6] W24 [2] U22 [5] U23 [1] Y26 [4] V24 [0] AA26	Receive Data. Only half the bus (bits [3:0]) are used in MII mode. Clocked on rising edge of M0_RXCLK (GMII/MII) or the rising edges of M0_RBC0 and M0_RBC1 (TBI).
M0_RXDV / M0_RXD[8]	I D	V25	GMII/MII - M0_RXDV Receive Data Valid. Active high. This signal is clocked on the rising edge of M0_RXCLK. It is asserted when valid data is on the M0_RXD bus. TBI - M0_RXD[8] Receive Data. Clocked on the rising edges of M0_RBC0 and M0_RBC1.
M0_RXER / M0_RXD[9]	I D	V26	GMII/MII - M0_RXER Receive Error. Active high signal indicating an error has been detected. Normally valid when M0_RXDV is asserted. Can be used in conjunction with M0_RXD when M0_RXDV signal is de-asserted to indicate a False Carrier. TBI - M0_RXD[9] Receive Data. Clocked on the rising edges of M0_RBC0 and M0_RBC1.

Table 9 - MII Port 0 Interface Package Ball Definition (continued)

MII Port 0			
Signal	**I/O**	**Package Balls**	**Description**
M0_CRS / M0_Signal_Detect	I D	U25	GMII/MII - M0_CRS Carrier Sense. This asynchronous signal is asserted when either the transmission or reception device is non-idle. It is active high. TBI - M0_Signal Detect Similar function to M0_CRS.
M0_TXCLK	I U	U24	**MII only** - Transmit Clock Accepts the following frequencies: 25.0 MHz MII 100 Mbps
M0_TXD[7:0]	O	[7] V21 [3] AA23 [6] W23 [2] W21 [5] W22 [1] Y22 [4] Y23 [0] AA22	Transmit Data. Only half the bus (bits [3:0]) are used in MII mode. Clocked on rising edge of M0_TXCLK (MII) or the rising edge of M0_GTXCLK (GMII/TBI).
M0_TXEN / M0_TXD[8]	O	V23	GMII/MII - M0_TXEN Transmit Enable. Asserted when the MAC has data to transmit, synchronously to M0_TXCLK with the first pre-amble of the packet to be sent. Remains asserted until the end of the packet transmission. Active high. TBI - M0_TXD[8] Transmit Data. Clocked on rising edge of M0_GTXCLK.
M0_TXER / M0_TXD[9]	O	V22	GMII/MII - M0_TXER Transmit Error. Transmitted synchronously with respect to M0_TXCLK, and active high. When asserted (with M0_TXEN also asserted) the ZL50110/11/14 will transmit a non-valid symbol, somewhere in the transmitted frame. TBI - M0_TXD[9] Transmit Data. Clocked on rising edge of M0_GTXCLK.
M0_GTX_CLK	O	U21	**GMII/TBI only** - Gigabit Transmit Clock Output of a clock for Gigabit operation at 125 MHz.

Table 9 - MII Port 0 Interface Package Ball Definition (continued)

MII Port 1			
Signal	**I/O**	**Package Balls**	**Description**
M1_LINKUP_LED	O	G23 on ZL50110/4 F26 on ZL50111	LED drive for MAC 1 to indicate port is linked up. Logic 0 output = LED on Logic 1 output = LED off
M1_ACTIVE_LED	O	AB25	LED drive for MAC 1 to indicate port is transmitting or receiving packet data. Logic 0 output = LED on Logic 1 output = LED off
M1_GIGABIT_LED	O	G25	LED drive for MAC 1 to indicate operation at Gbps. Logic 0 output = LED on Logic 1 output = LED off
M1_REFCLK	I D	M22	**GMII/TBI** - Reference Clock input at 125 MHz. Can be used to lock receive circuitry (RX) to M1_GTXCLK rather than recovering the RXCLK (or RBC0 and RBC1). Useful, for example, in the absence of valid serial data. **NOTE:** In **MII** mode this pin must be driven with the same clock as M1_RXCLK.
M1_RXCLK	I U	M23	GMII/MII - M1_RXCLK. Accepts the following frequencies: 25.0 MHz MII 100 Mbps 125.0 MHz GMII 1 Gbps
M1_RBC0	I U	U26	TBI - M1_RBC0. Used as a clock when in TBI mode. Accepts 62.5 MHz and is 180°C out of phase with M1_RBC1. Receive data is clocked at each rising edge of M1_RBC1 and M1_RBC0, resulting in 125 MHz sample rate.
M1_RBC1	I U	T25	TBI - M1_RBC1 Used as a clock when in TBI mode. Accepts 62.5 MHz, and is 180° out of phase with M1_RBC0. Receive data is clocked at each rising edge of M1_RBC1 and M1_RBC0, resulting in 125 MHz sample rate.
M1_COL	I D	R25	GMII/MII - M1_COL. Collision Detection. This signal is independent of M1_TXCLK and M1_RXCLK, and is asserted when a collision is detected on an attempted transmission. It is active high, and only specified for half-duplex operation.

Table 10 - MII Port 1 Interface Package Ball Definition

MII Port 1			
Signal	**I/O**	**Package Balls**	**Description**
M1_RXD[7:0]	I U	[7] M25 [3] N25 [6] P26 [2] N24 [5] M24 [1] R26 [4] P25 [0] T26	Receive Data. Only half the bus (bits [3:0]) are used in MII mode. Clocked on rising edge of M1_RXCLK (GMII/MII) or the rising edges of M1_RBC0 and M1_RBC1 (TBI).
M1_RXDV / M1_RXD[8]	I D	M26	GMII/MII - M1_RXDV Receive Data Valid. Active high. This signal is clocked on the rising edge of M1_RXCLK. It is asserted when valid data is on the M1_RXD bus. TBI - M1_RXD[8] Receive Data. Clocked on the rising edges of M1_RBC0 and M1_RBC1.
M1_RXER / M1_RXD[9]	I D	L21	GMII/MII - M1_RXER Receive Error. Active high signal indicating an error has been detected. Normally valid when M1_RXDV is asserted. Can be used in conjunction with M1_RXD when M1_RXDV signal is de-asserted to indicate a False Carrier. TBI - M1_RXD[9] Receive Data. Clocked on the rising edges of M1_RBC0 and M1_RBC1.
M1_CRS / M1_Signal_Detect	I D	L23	GMII/MII - M1_CRS Carrier Sense. This asynchronous signal is asserted when either the transmission or reception device is non-idle. It is active high. TBI - M1_Signal Detect Similar function to M1_CRS.
M1_TXCLK	I U	L22	**MII only** - Transmit Clock Accepts the following frequencies: 25.0 MHz MII 100 Mbps
M1_TXD[7:0]	O	[7] R24 [3] R22 [6] P22 [2] P21 [5] R23 [1] T22 [4] T23 [0] R21	Transmit Data. Only half the bus (bits [3:0]) are used in MII mode. Clocked on rising edge of M1_TXCLK (MII) or the rising edge of M1_GTXCLK (GMII/TBI).
M1_TXEN / M1_TXD[8]	O	P23	GMII/MII - M1_TXEN Transmit Enable. Asserted when the MAC has data to transmit, synchronously to M1_TXCLK with the first pre-amble of the packet to be sent. Remains asserted until the end of the packet transmission. Active high. TBI - M1_TXD[8] Transmit Data. Clocked on rising edge of M1_GTXCLK.

Table 10 - MII Port 1 Interface Package Ball Definition (continued)

MII Port 1			
Signal	**I/O**	**Package Balls**	**Description**
M1_TXER / M1_TXD[9]	O	N23	GMII/MII - M1_TXER Transmit Error. Transmitted synchronously with respect to M1_TXCLK, and active high. When asserted (with M1_TXEN also asserted) the ZL50110/11/14 will transmit a non-valid symbol, somewhere in the transmitted frame. TBI - M1_TXD[9] Transmit Data. Clocked on rising edge of M1_GTXCLK.
M1_GTX_CLK	O	N21	**GMII/TBI only** - Gigabit Transmit Clock Output of a clock for Gigabit operation at 125 MHz.

Table 10 - MII Port 1 Interface Package Ball Definition (continued)

MII Port 2 - ZL50111 variant only. Note: This port must not be used to receive data at the same time as port 3, they are mutually exclusive.			
Signal	**I/O**	**Package Balls**	**Description**
M2_LINKUP_LED	O	G23	LED drive for MAC 2 to indicate port is linked up. Logic 0 output = LED on Logic 1 output = LED off
M2_ACTIVE_LED	O	AB24	LED drive for MAC 2 to indicate port is transmitting or receiving packet data. Logic 0 output = LED on Logic 1 output = LED off
M2_RXCLK	I U	AA19	MII only - Receive Clock. Accepts the following frequencies: 25.0 MHz MII 100 Mbps
M2_COL	I D	AE26	Collision Detection. This signal is independent of M2_TXCLK and M2_RXCLK, and is asserted when a collision is detected on an attempted transmission. It is active high, and only specified for half-duplex operation.
M2_RXD[3:0]	I U	[3] AD25 [1] AB21 [2] AC23 [0] AD24	Receive Data. Clocked on rising edge of M2_RXCLK.
M2_RXDV	I D	AA20	Receive Data Valid. Active high. This signal is clocked on the rising edge of M2_RXCLK. It is asserted when valid data is on the M2_RXD bus.

Table 11 - MII Port 2 Interface Package Ball Definition

MII Port 2 - ZL50111 variant only. Note: This port must not be used to receive data at the same time as port 3, they are mutually exclusive.			
Signal	**I/O**	**Package Balls**	**Description**
M2_RXER	I D	AC24	Receive Error. Active high signal indicating an error has been detected. Normally valid when M2_RXDV is asserted. Can be used in conjunction with M2_RXD when M2_RXDV signal is de-asserted to indicate a False Carrier.
M2_CRS	I D	AC25	Carrier Sense. This asynchronous signal is asserted when either the transmission or reception device is non-idle. It is active high.
M2_TXCLK	I U	AD26	MII only - Transmit Clock Accepts the following frequencies: 25.0 MHz MII 100 Mbps
M2_TXD[3:0]	O	[3] AE25 [1] AC21 [2] AD23 [0] AE24	Transmit Data. Clocked on rising edge of M2_TXCLK.
M2_TXEN	O	AC22	Transmit Enable. Asserted when the MAC has data to transmit, synchronously to M2_TXCLK with the first pre-amble of the packet to be sent. Remains asserted until the end of the packet transmission. Active high.
M2_TXER	O	AB20	Transmit Error. Transmitted synchronously with respect to M2_TXCLK, and active high. When asserted (with M2_TXEN also asserted) the ZL50110/11/14 will transmit a non-valid symbol, somewhere in the transmitted frame.

Table 11 - MII Port 2 Interface Package Ball Definition (continued)

MII Port 3 - ZL50111 variant only Note: This port must not be used to receive data at the same time as port 2, they are mutually exclusive.			
Signal	**I/O**	**Package Balls**	**Description**
M3_LINKUP_LED	O	G24	LED drive for MAC 3 to indicate port is linked up. Logic 0 output = LED on Logic 1 output = LED off
M3_ACTIVE_LED	O	AB26	LED drive for MAC 3 to indicate port is transmitting or receiving packet data. Logic 0 output = LED on Logic 1 output = LED off

Table 12 - MII Port 3 Interface Package Ball Definition

MII Port 3 - ZL50111 variant only Note: This port must not be used to receive data at the same time as port 2, they are mutually exclusive.			
Signal	**I/O**	**Package Balls**	**Description**
M3_RXCLK	I U	K26	MII only - Receive Clock. Accepts the following frequencies: 25.0 MHz MII 100 Mbps
M3_COL	I D	J26	Collision Detection. This signal is independent of M3_TXCLK and M3_RXCLK, and is asserted when a collision is detected on an attempted transmission. It is active high, and only specified for half-duplex operation.
M3_RXD[3:0]	I U	[3] J22 [1] J24 [2] J23 [0] J25	Receive Data. Clocked on rising edge of M3_RXCLK.
M3_RXDV	I D	J21	Receive Data Valid. Active high. This signal is clocked on the rising edge of M3_RXCLK. It is asserted when valid data is on the M3_RXD bus.
M3_RXER	I D	H26	Receive Error. Active high signal indicating an error has been detected. Normally valid when M3_RXDV is asserted. Can be used in conjunction with M3_RXD when M3_RXDV signal is de-asserted to indicate a False Carrier.
M3_CRS	I D	H24	Carrier Sense. This asynchronous signal is asserted when either the transmission or reception device is non-idle. It is active high.
M3_TXCLK	I U	H25	MII only - Transmit Clock Accepts the following frequencies: 25.0 MHz MII 100 Mbps
M3_TXD[3:0]	O	[3] K23 [1] L25 [2] L26 [0] L24	Transmit Data. Clocked on rising edge of M3_TXCLK.
M3_TXEN	O	K24	Transmit Enable. Asserted when the MAC has data to transmit, synchronously to M3_TXCLK with the first pre-amble of the packet to be sent. Remains asserted until the end of the packet transmission. Active high.
M3_TXER	O	K25	Transmit Error. Transmitted synchronously with respect to M3_TXCLK, and active high. When asserted (with M3_TXEN also asserted) the ZL50110/11/14 will transmit a non-valid symbol, somewhere in the transmitted frame.

Table 12 - MII Port 3 Interface Package Ball Definition (continued)

3.4 External Memory Interface

All External Memory Interface signals are 5 V tolerant.

All External Memory Interface outputs are high impedance while System Reset is LOW.

If the External Memory Interface is unused, all input pins may be left unconnected.

Active low signals are designated by a # suffix, in accordance with the convention used in common memory data sheets.

Signal	I/O	Package Balls				Description
RAM_DATA[63:0]	IU/ OT	[63]	AD7	[31]	K3	Buffer memory data. Synchronous to rising edge of SYSTEM_CLK.
		[62]	AE6	[30]	K4	
		[61]	AF5	[29]	J1	
		[60]	AB8	[28]	J2	
		[59]	AC7	[27]	J3	
		[58]	AD6	[26]	J4	
		[57]	AE5	[25]	H1	
		[56]	AF4	[24]	H2	
		[55]	AF3	[23]	H3	
		[54]	AE4	[22]	J5	
		[53]	AD5	[21]	G1	
		[52]	AA8	[20]	J6	
		[51]	AB7	[19]	H4	
		[50]	AF2	[18]	G2	
		[49]	AC6	[17]	H5	
		[48]	AE3	[16]	G3	
		[47]	AD4	[15]	F1	
		[46]	AC5	[14]	G4	
		[45]	AA7	[13]	F2	
		[44]	AB6	[12]	F3	
		[43]	AB5	[11]	G5	
		[42]	AC4	[10]	E1	
		[41]	AD3	[9]	E2	
		[40]	AE2	[8]	G6	
		[39]	AA5	[7]	F5	
		[38]	AB4	[6]	F4	
		[37]	AC3	[5]	E3	
		[36]	AD2	[4]	E4	
		[35	AE1	[3]	D1	
		[34]	AD1	[2]	E5	
		[33]	W6	[1]	D2	
		[32]	Y5	[0]	D4	
RAM_PARITY[7:0]	IU/ OT	[7]	L1	[3]	L5	Buffer memory parity. Synchronous to rising edge of SYSTEM_CLK. Bit [7] is parity for data byte [63:56], bit [0] is parity for data byte [7:0].
		[6]	L2	[2]	L6	
		[5]	L3	[1]	K1	
		[4]	L4	[0]	K2	

Table 13 - External Memory Interface Package Ball Definition

Signal	I/O	Package Balls	Description
RAM_ADDR[19:0]	O	[19] R4 [18] T2 [17] T1 [16] P5 [15] R3 [14] R2 [13] P4 [12] R1 [11] P3 [10] P2 [9] P1 [8] N4 [7] N3 [6] N2 [5] M1 [4] M2 [3] M4 [2] M3 [1] M6 [0] M5	Buffer memory address output. Synchronous to rising edge of SYSTEM_CLK.
RAM_BW_A#	O	U2	Synchronous Byte Write Enable A (Active Low). Must be asserted same clock cycle as RAM_ADDR. Enables RAM_DATA[7:0].
RAM_BW_B#	O	T3	Synchronous Byte Write Enable B (Active Low). Must be asserted same clock cycle as RAM_ADDR. Enables RAM_DATA[15:8].
RAM_BW_C#	O	U3	Synchronous Byte Write Enable C (Active Low). Must be asserted same clock cycle as RAM_ADDR. Enables RAM_DATA[23:16].
RAM_BW_D#	O	V2	Synchronous Byte Write Enable D (Active Low). Must be asserted same clock cycle as RAM_ADDR. Enables RAM_DATA[31:24].
RAM_BW_E#	O	W1	Synchronous Byte Write Enable E (Active Low). Must be asserted same clock cycle as RAM_ADDR. Enables RAM_DATA[39:32].
RAM_BW_F#	O	V3	Synchronous Byte Write Enable F (Active Low). Must be asserted same clock cycle as RAM_ADDR. Enables RAM_DATA[47:40].
RAM_BW_G#	O	W2	Synchronous Byte Write Enable G (Active Low). Must be asserted same clock cycle as RAM_ADDR. Enables RAM_DATA[55:48].
RAM_BW_H#	O	Y1	Synchronous Byte Write Enable H (Active Low). Must be asserted same clock cycle as RAM_ADDR. Enables RAM_DATA[63:56].
RAM_RW#	O	U4	Read/Write Enable output Read = high Write = low

Table 13 - External Memory Interface Package Ball Definition (continued)

3.5 CPU Interface

All CPU Interface signals are 5 V tolerant.

All CPU Interface outputs are high impedance while System Reset is LOW.

Signal	I/O	Package Balls	Description
CPU_DATA[31:0]	I/ OT	[31] AF25 [30] AB19 [29] AD22 [28] AE23 [27] AC20 [26] AF24 [25] AE22 [24] AD21 [23] AA17 [22] AB18 [21] AC19 [20] AD20 [19] AF23 [18] AE21 [17] AF22 [16] AC18 [15] AA16 [14] AD19 [13] AE20 [12] AB17 [11] AF21 [10] AC17 [9] AE19 [8] AA15 [7] AB16 [6] AD18 [5] AF19 [4] AE18 [3] AD17 [2] AF20 [1] AB15 [0] AF18	CPU Data Bus. Bi-directional data bus, synchronously transmitted with CPU_CLK rising edge. NOTE: as with all ports in the ZL50110/11/14 device, CPU_DATA[0] is the least significant bit (lsb).
CPU_ADDR[23:2]	I	[23] AB13 [22] AC13 [21] AD13 [20] AE13 [19] AF12 [18] AE12 [17] AD12 [16] AC12 [15] AF11 [14] AB12 [13] AE11 [12] AA12 [11] AD11 [10] AF10 [9] AC11 [8] AE10 [7] AD10 [6] AB11 [5] AF9 [4] AC10 [3] AE9 [2] AA11	CPU Address Bus. Address input from processor to ZL50110/11/14, synchronously transmitted with CPU_CLK rising edge. NOTE: as with all ports in the ZL50110/11/14 device, CPU_ADDR[2] is the least significant bit (lsb).
$\overline{\text{CPU_CS}}$	I U	AF14	CPU Chip Select. Synchronous to rising edge of CPU_CLK and active low. Is asserted with CPU_$\overline{\text{TS}}$_ALE. Must be asserted with $\overline{\text{CPU_OE}}$ to asynchronously enable the CPU_DATA output during a read, including DMA read.
$\overline{\text{CPU_WE}}$	I	AD14	CPU Write Enable. Synchronously asserted with respect to CPU_CLK rising edge, and active low. Used for CPU writes from the processor to registers within the ZL50110/11/14. Asserted one clock cycle after CPU_$\overline{\text{TS}}$_ALE.

Table 14 - CPU Interface Package Ball Definition

Signal	I/O	Package Balls	Description
CPU_OE	I	AE14	CPU Output Enable. Synchronously asserted with respect to CPU_CLK rising edge, and active low. Used for CPU reads from the processor to registers within the ZL50110/11/14. Asserted one clock cycle after CPU_TS_ALE. Must be asserted with CPU_CS to asynchronously enable the CPU_DATA output during a read, including DMA read.
CPU_TS_ALE	I	AE15	Synchronous input with rising edge of CPU_CLK. Latch Enable (ALE), active high signal. Asserted with CPU_CS, for a single clock cycle.
CPU_SDACK1	I	AF15	CPU/DMA 1 Acknowledge Input. Active low synchronous to CPU_CLK rising edge. Used to acknowledge request from ZL50110/11/14 for a DMA write transaction. Only used for DMA transfers, not for normal register access.
CPU_SDACK2	I	AD15	CPU/DMA 2 Acknowledge Input Active low synchronous to CPU_CLK rising edge. Used to acknowledge request from ZL50110/11/14 for a DMA read transaction. Only used for DMA transfers, not for normal register access.
CPU_CLK	I	AC14	CPU PowerQUICC™ II Bus Interface clock input. 66 MHz clock, with minimum of 6 ns high/low time. Used to time all host interface signals into and out of ZL50110/11/14 device.
CPU_TA	OT	AB14	CPU Transfer Acknowledge. Driven from tri-state condition on the negative clock edge of CPU_CLK following the assertion of CPU_CS. Active low, asserted from the rising edge of CPU_CLK. For a read, asserted when valid data is available at CPU_DATA. The data is then read by the host on the following rising edge of CPU_CLK. For a write, is asserted when the ZL50110/11/14 is ready to accept data from the host. The data is written on the rising edge of CPU_CLK following the assertion. Returns to tri-state from the negative clock edge of CPU_CLK following the de-assertion of CPU_CS.

Table 14 - CPU Interface Package Ball Definition (continued)

Signal	I/O	Package Balls	Description
$\overline{\text{CPU_DREQ0}}$	OT	AC15	CPU DMA 0 Request Output Active low synchronous to CPU_CLK rising edge. Asserted by ZL50110/11/14 to request the host initiates a DMA write. Only used for DMA transfers, not for normal register access.
$\overline{\text{CPU_DREQ1}}$	OT	AE16	CPU DMA 1 Request Active low synchronous to CPU_CLK rising edge. Asserted by ZL50110/11/14 to indicate packet data is ready for transmission to the CPU, and request the host initiates a DMA read. Only used for DMA transfers, not for normal register access.
$\overline{\text{CPU_IREQO}}$	O	AF17	CPU Interrupt 0 Request (Active Low)
$\overline{\text{CPU_IREQ1}}$	O	AD16	CPU Interrupt 1 Request (Active Low)

Table 14 - CPU Interface Package Ball Definition (continued)

3.6 System Function Interface

All System Function Interface signals are 5 V tolerant.

The core of the chip will be held in reset for 16383 SYSTEM_CLK cycles after SYSTEM_RST has gone HIGH to allow the PLL's to lock.

Signal	I/O	Package Balls	Description
SYSTEM_CLK	I	U6	System Clock Input. The system clock frequency is 100 MHz. The frequency must be accurate to within ±32 ppm in synchronous mode. The quality of SYSTEM_CLK, or the oscillator that drives SYSTEM_CLK directly impacts the adaptive clock recovery performance. See Section 6.3.
SYSTEM_RST	I	V4	System Reset Input. Active low. The system reset is asynchronous, and causes all registers within the ZL50110/11/14 to be reset to their default state. Recommend external pull-up.
SYSTEM_DEBUG	I	U5	System Debug Enable. This is an asynchronous signal that, when de-asserted, prevents the software assertion of the debug-freeze command, regardless of the internal state of registers, or any error conditions. Active high. Recommend external pull-down.

Table 15 - System Function Interface Package Ball Definition

3.7 Test Facilities

3.7.1 Administration, Control and Test Interface

All Administration, Control and Test Interface signals are 5 V tolerant.

Signal	I/O	Package Balls	Description
GPIO[15:0]	ID/ OT	[15] AA4 [14] AB3 [13] AC2 [12] AC1 [11] AB2 [10] Y4 [9] W5 [8] AA3 [7] AA2 [6] Y3 [5] AB1 [4] Y2 [3] W4 [2] V5 [1] AA1 [0] W3	General Purpose I/O pins. Connected to an internal register, so customer can set user-defined parameters. Bits [4:0] reserved at startup or reset for memory TDL setup. See the ZL50110/11/14 Programmers Model for more details. Recommend 5 kohm pulldown on these signals.
TEST_MODE[2:0]	I D	[2] AF6 [1] AB9 [0] AC8	Test Mode input - ensure these pins are tied to ground for normal operation. 000 SYS_NORMAL_MODE 001-010 RESERVED 011 SYS_TRISTATE_MODE 100-111 RESERVED

Table 16 - Administration/Control Interface Package Ball Definition

3.7.2 JTAG Interface

All JTAG Interface signals are 5 V tolerant, and conform to the requirements of IEEE1149.1 (2001).

Signal	I/O	Package Balls	Description
$\overline{\text{JTAG_TRST}}$	I U	AE7	JTAG Reset. Asynchronous reset. In normal operation this pin should be pulled low. Recommend external pull-down.
JTAG_TCK	I	AD8	JTAG Clock - maximum frequency is 25MHz, typically run at 10 MHz. In normal operation this pin should be pulled either high or low. Recommend external pull-down.
JTAG_TMS	I U	AA10	JTAG test mode select. Synchronous to JTAG_TCK rising edge. Used by the Test Access Port controller to set certain test modes.
JTAG_TDI	I U	AF7	JTAG test data input. Synchronous to JTAG_TCK.
JTAG_TDO	O	AC9	JTAG test data output. Synchronous to JTAG_TCK.

Table 17 - JTAG Interface Package Ball Definition

3.8 Miscellaneous Inputs

Signal	Package Balls	Description
IC_GND	AD9, AF8, R5, T4, AE8	Internally Connected. Tie to GND.
IC_VDD_IO	AF16	Internally Connected. Tie to VDD_IO.

Table 18 - Miscellaneous Inputs Package Ball Definitions

3.9 Power and Ground Connections

Signal	Package Balls				Description
VDD_IO	J9	J10	J11	J12	3.3 V VDD Power Supply for IO Ring
	J13	J14	J15	J16	
	J17	J18	K9	K18	
	L9	L18	M9	M18	
	N9	N18	P9	P18	
	R9	R18	T9	T18	
	U9	U18	V9	V10	
	V11	V12	V13	V14	
	V15	V16	V17	V18	
GND	A1	A13	A26	E22	0 V Ground Supply
	F6	F21	K5	K22	
	L11	L12	L13	L14	
	L15	L16	M11	M12	
	M13	M14	M15	M16	
	N1	N5	N11	N12	
	N13	N14	N15	N16	
	N22	N26	P6	P11	
	P12	P13	P14	P15	
	P16	P24	R11	R12	
	R13	R14	R15	R16	
	T5	T11	T12	T13	
	T14	T15	T16	T24	
	AA6	AA21	AB10	AF1	
	AF13	AF26			
VDD_CORE	F7	F12	F15		1.8 V VDD Power Supply for Core Region
	F20	H6	H21		
	K6	K21	M21		
	N6	T21	V6		
	Y6	Y21	AA9		
	AA13	AA14	AA18		
A1VDD	T6				1.8 V PLL Power Supply

Table 19 - Power and Ground Package Ball Definition

3.10 Internal Connections

Signal	Package Balls	Description
IC	R6, AC16, AE17	Internally Connected. Must leave open circuit.

Table 20 - No Connection Ball Definition

4.0 Typical Applications

4.1 Leased Line Provision

Circuit emulation is typically used to support the provision of leased line services to customers using legacy TDM equipment. For example, Figure 5 shows a leased line TDM service being carried across a packet network. The advantages are that a carrier can upgrade to a packet switched network, whilst still maintaining their existing TDM business.

The ZL50110/11/14 is capable of handling circuit emulation of both structured T1, E1, and J2 links (e.g., for support of fractional circuits) and unstructured (or clear channel) T1, E1, J2, T3, E3 and STS-1 links. The device handles the data-plane requirements of the provider edge inter-working function (with the exception of the physical interfaces and line interface units). Control plane functions are forwarded to the host processor controlling the ZL50110/11/14 device.

The ZL50110/11/14 provides a per-stream clock recovery function to reproduce the TDM service frequency at the egress of the packet network. This is required otherwise the queue at the egress of the packet network will either fill up or empty, depending on whether the regenerated clock is slower or faster than the original.

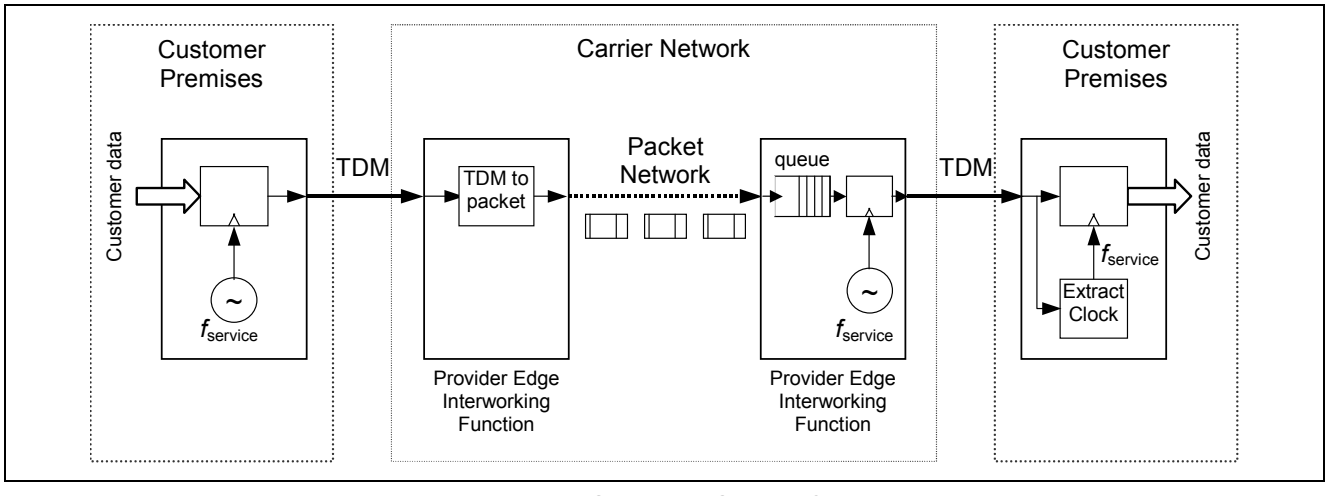


Figure 5 - Leased Line Services Over a Circuit Emulation Link

4.2 Metropolitan Area Network Aggregation

The metro Ethernet application, shown in Figure 6, consists of the metro Ethernet service modules sitting on the edge of the Metro Ethernet ring. The modules will connect Ethernet circuits and TDM circuits to the metro ring.

The ZL50110/11/14 is used to emulate leased line TDM circuits over Ethernet by establishing CESoP connections over the Metro Ethernet ring between the MTUs/MDUs and the PSTN. The use of CESoP eliminates the need for a separate TDM network in the metro core, thereby enabled convergence on a unified Ethernet network.

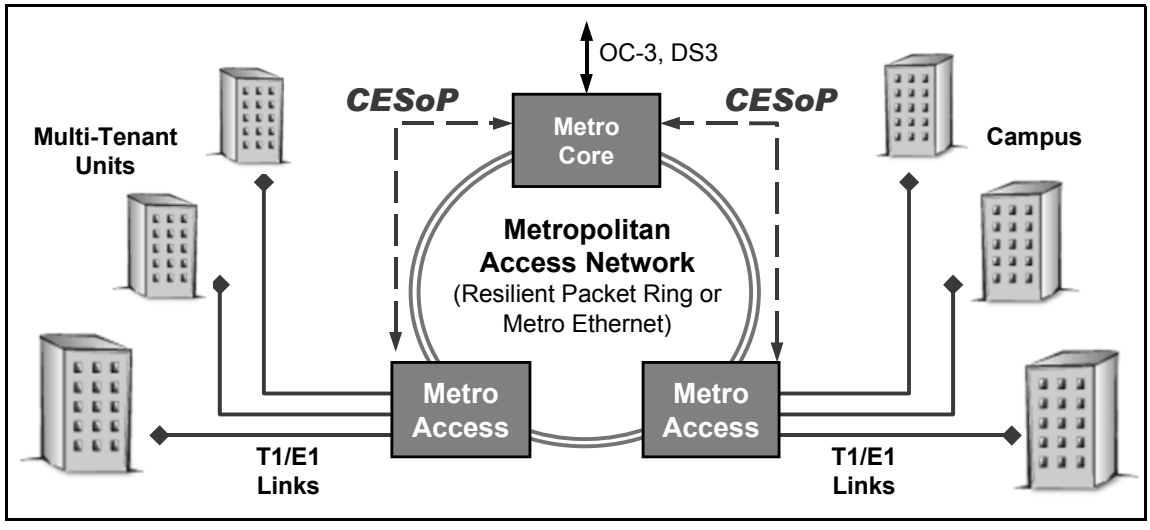


Figure 6 - Metropolitan Area Network Aggregation using CESoP

4.3 Digital Loop Carrier

The Broadband Digital Loop Carrier (BBDLC) application, shown in Figure 7, consists of a BBDLC connected to the Central Office (CO) by a dedicated fiber link running Gigabit Ethernet (GE) rather than by NxT1/E1 or DS3/E3.

The ZL50110/11/14 is used to emulate TDM circuits over Ethernet by establishing CESoP connections between the BBDLC and the CO. At the CO the native IP or Ethernet traffic is split from the CESoP connections at sent towards the packet network. Multiple T1/E1 CESoP connections from several BBDLC are aggregated in the CO using a larger ZL50110/11/14 variant, converted back to TDM circuits, and connected to a class 5 switch destined towards the PSTN.

In this configuration T3/E3 services can also be provided. Using CESoP allows voice and data traffic to be converged onto a single link.

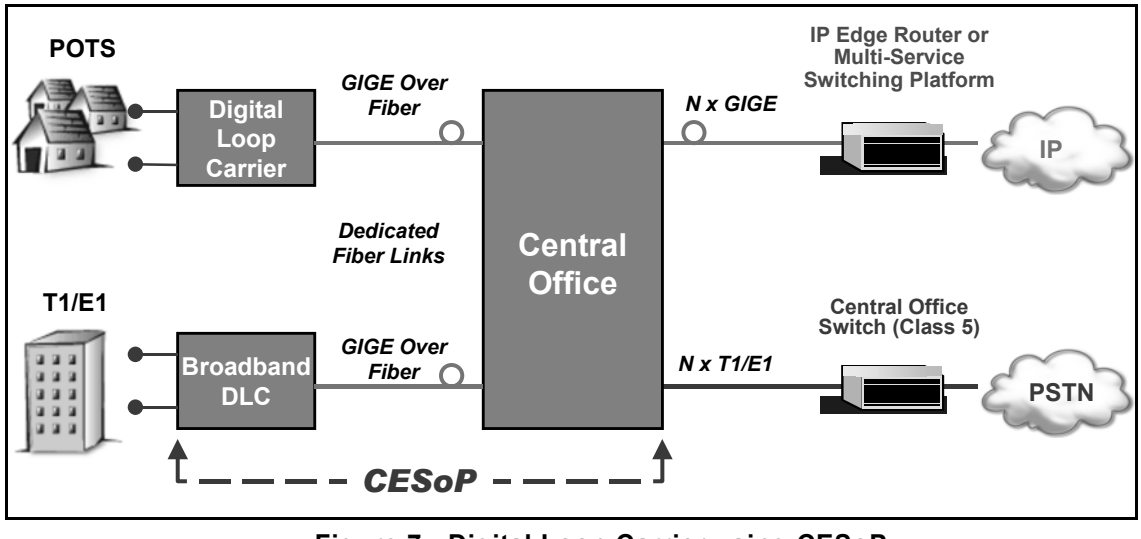


Figure 7 - Digital Loop Carrier using CESoP

4.4 Remote Concentrator

The remote concentrator application, shown in Figure 8, consists of a remote concentrators connected to the Central Office (CO) by a dedicated fiber link running Gigabit Ethernet (GE) or Ethernet over SONET (EoS) rather than by NxT1/E1 or DS3/E3. The remote concentrators provide both TDM service and native Ethernet service to the MTU/MDU.

The ZL50110/11/14 is used to emulate TDM circuits over Ethernet by establishing CESoP connections between the remote concentrator and the CO. The native IP or Ethernet traffic is multiplexed with the CESoP traffic inside the remote concentrator and sent across the same GE connection to the CO. At the CO the native IP or Ethernet traffic is split from the CESoP connections at sent towards the packet network. Multiple T1/E1 CESoP connections from several remote concentrators are aggregated in the CO using a larger ZL50110/11/14 variant, converted back to TDM circuits, and connected to the PSTN through a higher bandwidth TDM circuit such as OC-3 or STM-1.

The use of CESoP here allows the convergence of voice and data on a single access network based on Ethernet. This convergence on Ethernet, a packet technology, rather than SONET/SDH, a switched circuit technology, provides cost and operational savings.

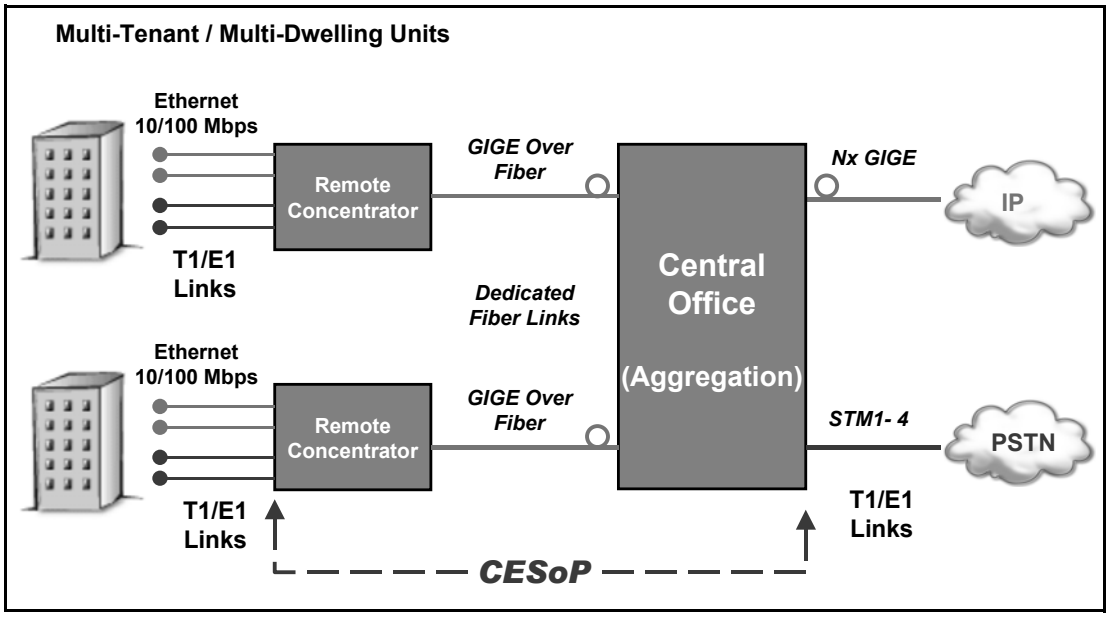


Figure 8 - Remote Concentrator using CESoP

4.5 Cell Site Backhaul

The cell site backhaul application, shown in Figure 9, consists of 2G, 2.5G and 3G base stations, co-located at a cell site, connected to their respective 2G, 2.5G base station controllers and 3G radio network controller. The traditional leased T1/E1 lines between the cell site and the base station controllers is now replaced by a packet network such as fixed wireless or Gigabit Ethernet (GE) fiber, that may be owned by the carrier or accessed through a service provider.

The ZL50110/11/14 would sit in a box either external to the base stations, or integrated in them, and would transparently carry multiple T1/E1s to the base station controllers using CESoP connections. At the base station controller location another ZL50110/11/14 would terminate the CESoP connection and provide the T1/E1 line to the controllers.

The use of the ZL50110/11/14 would allow for lower cost transport between the two locations, due to the replacement of the leased T1/E1 line cost. The CESoP connection would allow the T1/E1 to meet the strict timing

requirements for 3G base stations. Each T1/E1 may be asynchronous should a service provider be backhauling T1/E1s from multiple carriers.

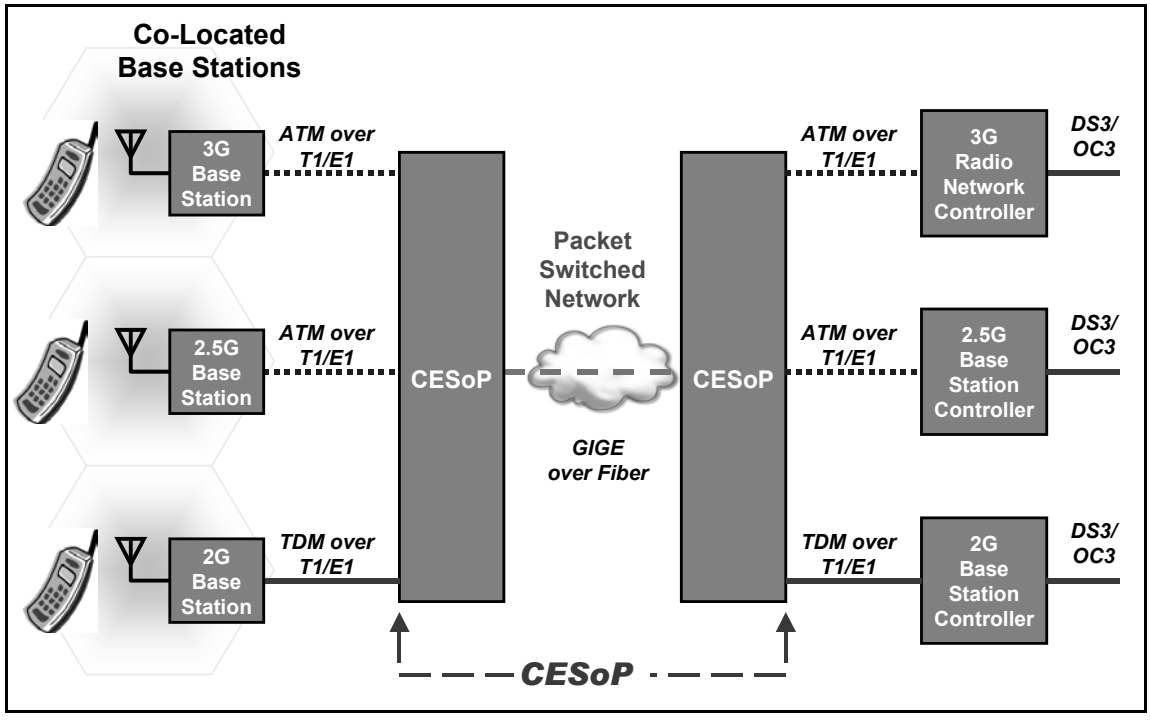


Figure 9 - Cell Site Backhaul using CESoP

4.6 Metro Ethernet Equipment

A Metro Ethernet service module, shown in Figure 10, supporting T1/E1 ports is shown at the board level using Zarlink's CESoP processors. The service module consists of three line cards and an uplink card connected to a packet backplane.

The first line card supports up to 32 T1/E1 lines, containing up to 1024 DS0, for Nx64 kbps structured data transfer (SDT) CESoP connections. The T1/E1 lines are broken down into DS0 channels on an H.110 bus. The ZL50110/11/14 establishes CESoP connections, with each connection taking a number of DS0 channels from the H.110 bus.

The third line card support up to 32 T1/E1 or 2 T3/E3 lines for private line unstructured data transfer (UDT) CESoP connections. The T1/E1 lines are not terminated on the card by are transparently packetized into individual CESoP connections by the ZL50110/11/14.

The second line card support multiple 10/100/1000 Mbps Ethernet ports for native Internet, video and data service.

The uplink card multiplexes the Ethernet traffic from the three cards, and uplinks the CESoP, Internet, video and data traffic to the packet switched network (PSN.)

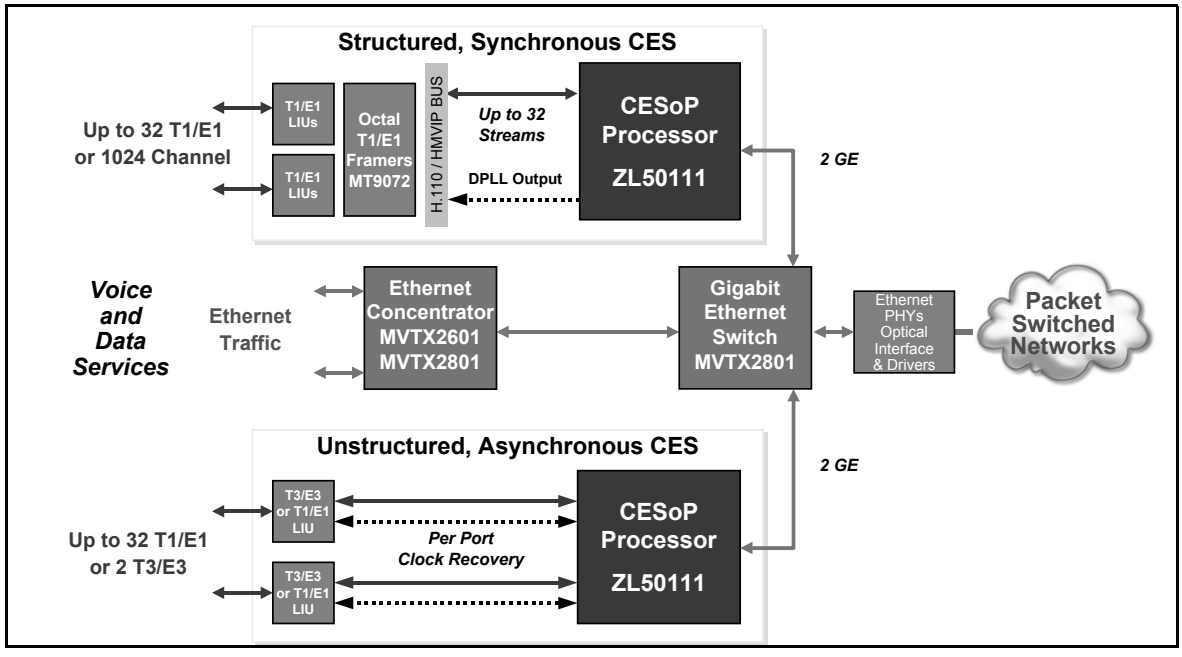


Figure 10 - Metro Ethernet Equipment using CESoP

5.0 Functional Description

The ZL50110/11/14 family provides the data-plane processing to enable constant bit rate TDM services to be carried over a packet switched network, such as an Ethernet, IP or MPLS network. The device segments the TDM data into user-defined packets, and passes it transparently over the packet network to be reconstructed at the far end. This has a number of applications, including emulation of TDM circuits and packet backplanes for TDM-based equipment.

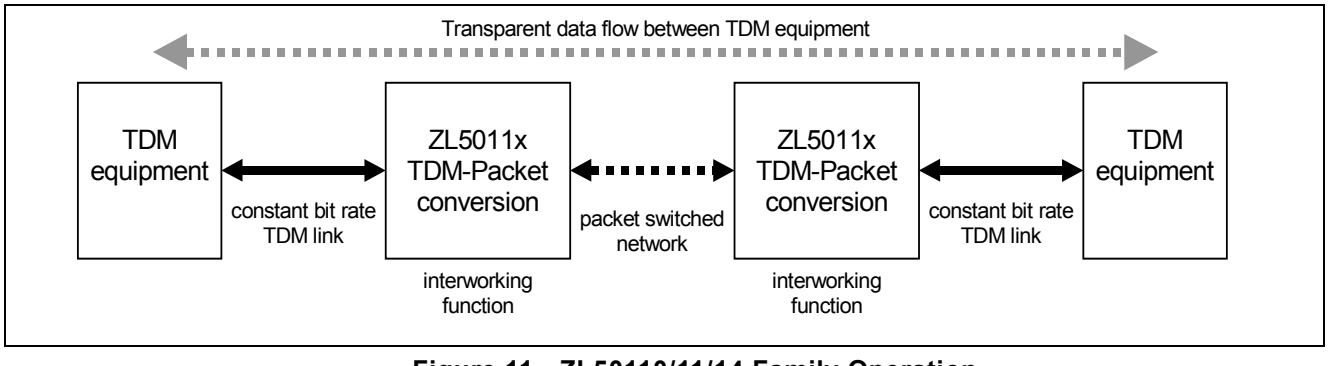


Figure 11 - ZL50110/11/14 Family Operation

5.1 Block Diagram

A diagram of the ZL50110/11/14 device is given in Figure 12, which shows the major data flows between functional components.

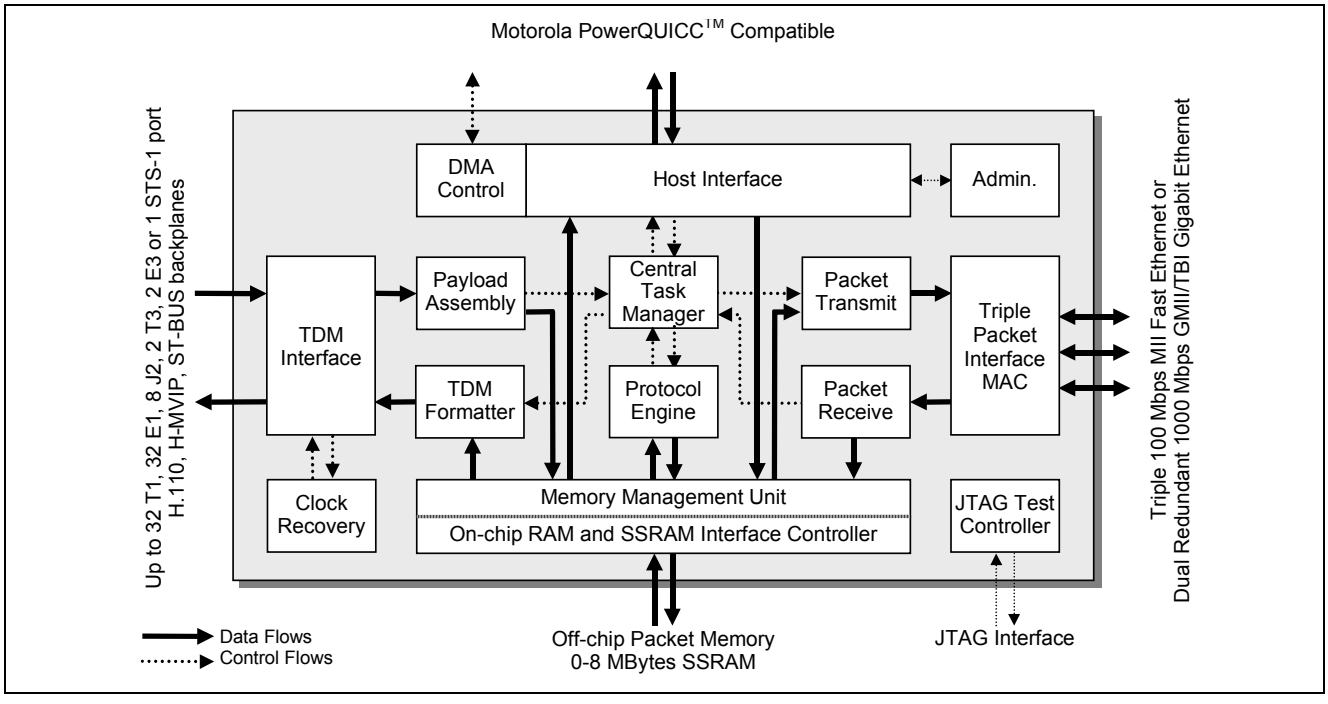


Figure 12 - ZL50110/11/14 Data and Control Flows

5.2 Data and Control Flows

There are numerous combinations that can be implemented to pass data through the ZL50110/11/14 device depending on the application requirements. The Task Manager can be considered the central pivot, through which all flows must operate.

The flow is determined by the Type field in the Task Message (see ZL50110/11/14 Programmers Model).

Flow Number	Flow Through Device
1	TDM to (TM) to PE to (TM) to PKT
2	PKT to (TM) to PE to (TM) to TDM
3	TDM to (TM) to PKT
4	PKT to (TM) to TDM
5	TDM to (TM) to CPU
6	TDM to (TM) to PE to (TM) to CPU
7	CPU to (TM) to TDM
8	PKT to (TM) to CPU
9	CPU to (TM) to PKT

Table 21 - Standard Device Flows

Flow Number	Flow Through Device
10[1]	TDM to (TM) to TDM
11[1]	PKT to (TM) to PKT

Table 21 - Standard Device Flows

1. This flow is for loopback test purposes only

Each of the 11 data flows uses the Task Manager to route packet information to the next block or interface for onward transmission. This section describes the flows between the TDM interface, the packet interface and the Task Manager which are the main flow routes used in the ZL50110/11/14 family. For example, the TDM->TM flow is used in flow types 1, 3, 5, and 6, and the TM->PKT flow is used in flow types 1, 3, and 9.

5.3 TDM Interface

The ZL50110/11/14 family offers the following types of TDM service across the packet network:

Service type	TDM interface	Interface type	Interfaces to
Unstructured asynchronous	T1, E1, J2, E3, T3 and STS-1	Bit clock in and out Data in and out	Line interface unit
Structured synchronous (N x 64 Kbps)	T1, E1 and J2 Framed TDM data streams at 2.048 and 8.192 Mbps	Bit clock out Frame pulse out Data in and out	Framers TDM backplane (master)
		Bit clock in Frame in Data in and out	Framers TDM backplane (slave)

Table 22 - TDM Services Offered by the ZL50110/11/14 Family

Unstructured services are fully asynchronous, and include full support for clock recovery on a per stream basis. Both adaptive and differential clock recovery mechanisms can be used. Structured services are synchronous, with all streams driven by a common clock and frame reference. These services can be offered in two ways:

- **Synchronous master mode** - the ZL50110/11/14 provides a common clock and frame pulse to all streams, which may be locked to an incoming clock or frame reference
- **Synchronous slave mode** - the ZL50110/11/14 accepts a common external clock and frame pulse to be used by all streams

In either mode, N x 64 Kbps trunking is supported as detailed in “Structured Payload Order” on page 55.

In addition, it can be used with a variety of different protocols. It includes full support for the CESoPSN (Circuit Emulation Services over Packet Switched Networks) and SAToP (Structure-Agnostic Transport over Packet) protocols currently in development by the IETF's PWE3 (Pseudo-Wire Emulation Edge to Edge) working group.

5.3.1 TDM Interface Block

The TDM Access Interface consists of up to 32 streams (depending on variant), each with an input and an output data stream operating at either 1.544 Mbps or 2.048 Mbps. It contains two basic types of interface: unstructured clock and data, for interfacing directly to a line interface unit; or structured, framed data, for interfacing to a framer or TDM backplane.

Unstructured data is treated asynchronously, with every stream using its own clock. Clock recovery is provided on each output stream, to reproduce the TDM service frequency at the egress of the packet network. Structured data is treated synchronously, i.e., all data streams are timed by the same clock and frame references. These can either be supplied from an external source (slave mode) or generated internally using the on-chip stratum 3/4/4E DPLL (master mode).

5.3.2 Structured TDM Port Data Formats

The ZL50110/11/14 is programmable such that the frame/clock polarity and clock alignment can be set to any desired combination. Table 23 shows a brief summary of four different TDM formats; ST-BUS, H.110, H-MVIP, and Generic (synchronous mode only), for more information see the relevant specifications shown. There are many additional formats for TDM transmission not depicted in Table 23, but the flexibility of the port will cover almost any scenario. The overall data format is set for the entire TDM Interface device, rather than on a per stream basis. It is possible to control the polarity of the master clock and frame pulse outputs, independent of the chosen data format (used when operating in synchronous master mode).

Data Format	Data Rate (Mbps)	Number of channels per frame	Clock Freq. (MHz)	Nominal Frame Pulse Width (ns)	Frame Pulse Polarity	Frame Boundary Alignment		Standard
						clock	frame pulse	
ST-bus	2.048	32	2.048	244	Negative	Rising Edge	Straddles boundary	MSAN-126 Rev B (Issue 4) Zarlink
	2.048	32	4.096	244	Negative	Falling Edge	Straddles boundary	
	8.192	128	16.384	61	Negative	Falling Edge	Straddles boundary	
H.110	8.192	128	8.192	122	Negative	Rising edge	Straddles boundary	ECTF H.110
H-MVIP	2.048	32	2.048	244	Negative	Rising Edge	Straddles boundary	H-MVIP Release 1.1a
	2.048	32	4.096	244	Negative	Falling Edge	Straddles boundary	
	8.192	128	16.384	244	Negative	Falling Edge	Straddles boundary	
Generic	2.048	32	2.048	488	Positive	Rising Edge	Rising edge of clock	
	8.192	128	8.192	122	Positive	Rising Edge	Rising edge of clock	

Table 23 - Some of the TDM Port Formats Accepted by the ZL50110/11/14 Family

5.3.3 TDM Clock Structure

The TDM interface can operate in two modes, synchronous for structured TDM data, and asynchronous for unstructured TDM data. The ZL50110/11/14 is capable of providing the TDM clock for either of the modes. The ZL50110/11/14 supports clock recovery in both synchronous and asynchronous modes of operation. In asynchronous operation each stream may have independent clock recovery.

5.3.3.1 Synchronous TDM Clock Generation

In synchronous mode all 32 streams will be driven by a common clock source. When the ZL50110/11/14 is acting as a master device, the source can either be the internal DPLL or an external PLL. In both cases, the primary and secondary reference clocks are taken from either two TDM input clocks, or two external clock sources driven to the chip. The input clocks are then divided down where necessary and sent either to the internal DPLL or to the output pins for connection to an external DPLL. The DPLL then provides the common clock and frame pulse required to drive the TDM streams. See “DPLL Specification” on page 66 for further details.

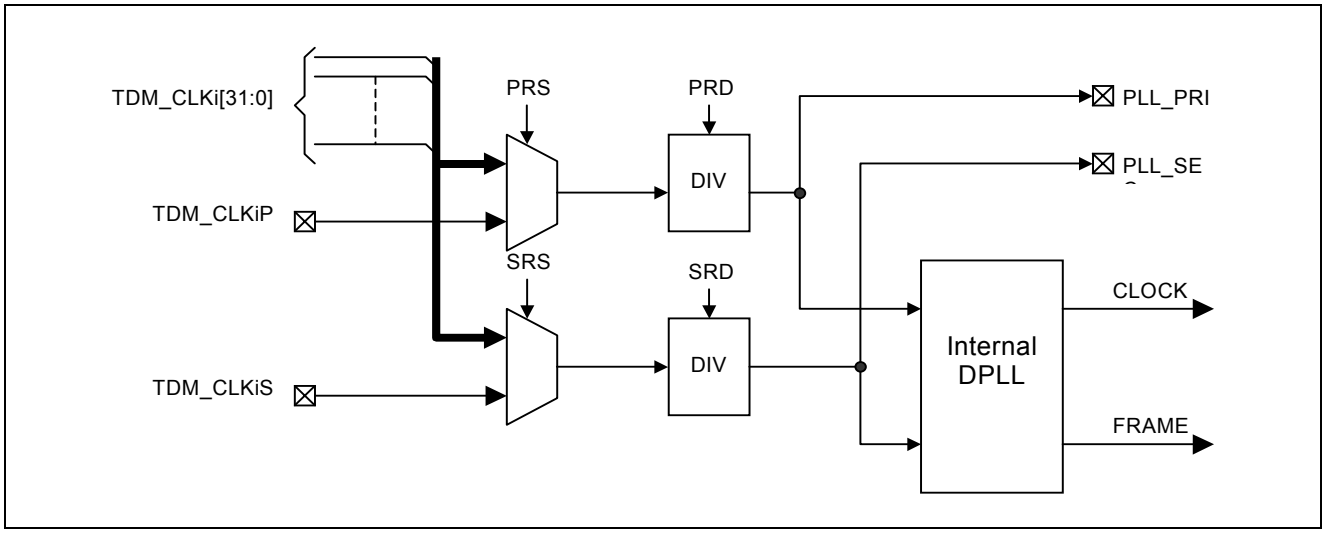


Figure 13 - Synchronous TDM Clock Generation

When the ZL50110/11/14 is acting as a slave device, the common clock and frame pulse signals are taken from an external device providing the TDM master function.

5.3.3.2 Asynchronous TDM Clock Generation

Each stream uses a separate internal DCO to provide an asynchronous TDM clock output. The DCO can be controlled to recover the clock from the original TDM source depending on the timing algorithm used.

5.4 Payload Assembly

Data traffic received on the TDM Access Interface is sampled in the TDM Interface block, and synchronized to the internal clock. It is then forwarded to the payload assembly process. The ZL50110/11/14 Payload Assembler can handle up to 128 active packet streams or “contexts” simultaneously. Packet payloads are assembled in the format shown in Figure 14 on page 54. This meets the requirements of the CESoPSN standard under development in the IETF. Alternatively, packet payloads are assembled in the format shown in Figure 16 on page 56. This meets the requirements of the SAToP standard under development in the IETF

When the payload has been assembled it is written into the centrally managed memory, and a task message is passed to the Task Manager.

5.4.1 Structured Payload Operation

In structured mode a context may contain any number of 64 kbps channels. These channels need not be contiguous and they may be selected from any input stream.

Channels may be added or deleted dynamically from a context. This feature can be used to optimize bandwidth utilisation. Modifications to the context are synchronised with the start of a new packet.

The fixed header at the start of each packet is added by the Packet Transmit block. This consists of up to 64 bytes, containing the Ethernet header, any upper layer protocol headers, and the two byte context descriptor field (see section below). The header is entirely user programmable, enabling the use of any protocol.

The payload header and size must be chosen so that the overall packet size is not less than 64 bytes, the Ethernet standard minimum packet size. Where this is likely to be the case, the header or data must be padded (as shown in Figure 14 and Figure 16) to ensure the packet is large enough. This padding is added by the ZL50110/11/14 for most applications.

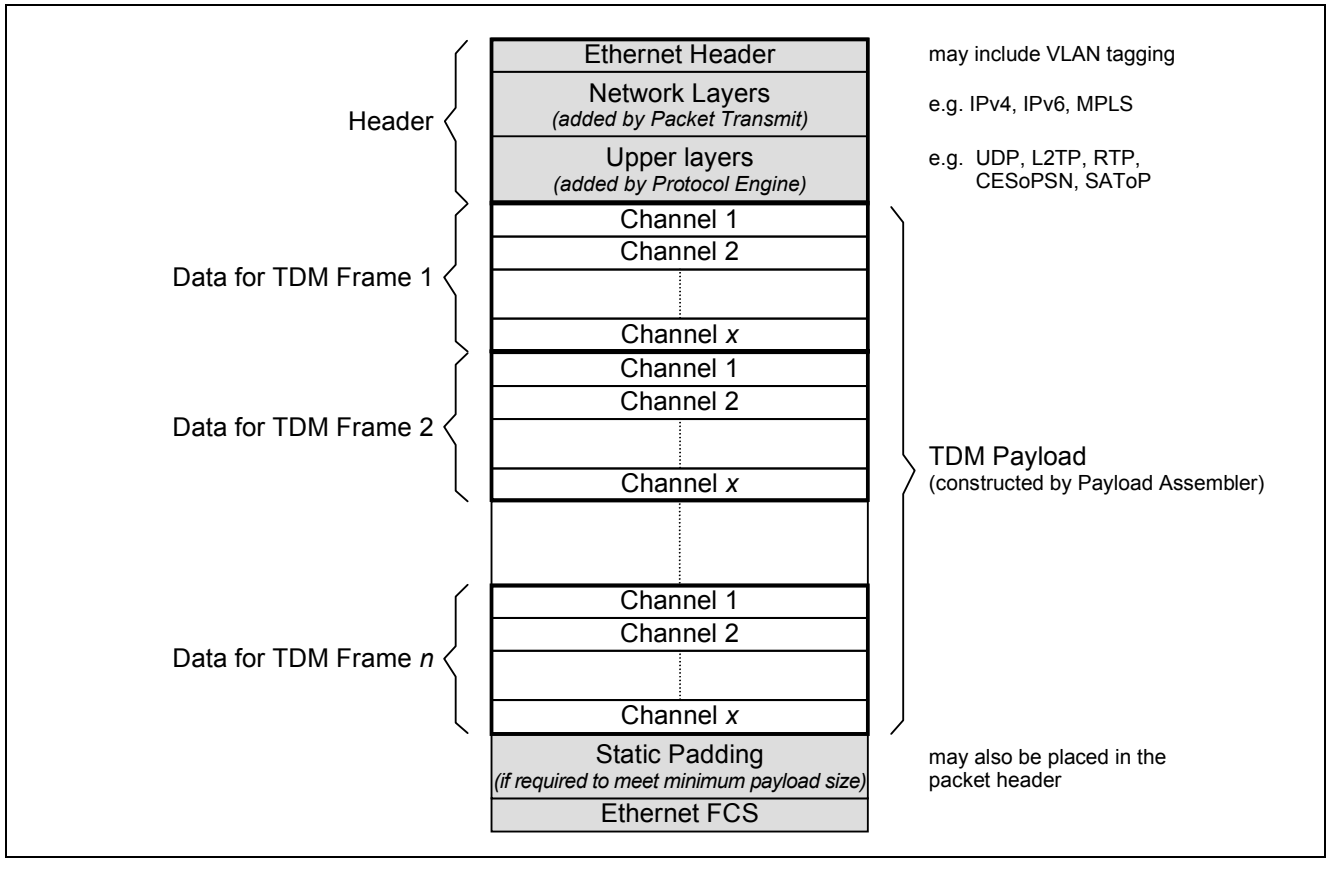


Figure 14 - ZL50110/11/14 Packet Format - Structured Mode

In applications where large payloads are being used, the payload size must be chosen such that the overall packet size does not exceed the maximum Ethernet packet size of 1518 bytes (1522 bytes with VLAN tags). Figure 14 shows the packet format for structured TDM data, where the payload is split into frames, and each frame concatenated to form the packet.

5.4.1.1 Structured Payload Order

Packets are assembled sequentially, with each channel placed into the packet as it arrives at the TDM Access Interface. A fixed order of channels is maintained (see Figure 15), with channel 0 placed before channel 1, which is placed before channel 2. It is this order that allows the packet to be correctly disassembled at the far end. A context must contain only unique channel numbers. As such a context that contains the same channel from different streams, for example channel 1 from stream 2 and channel 1 from stream 5, would not be permitted.

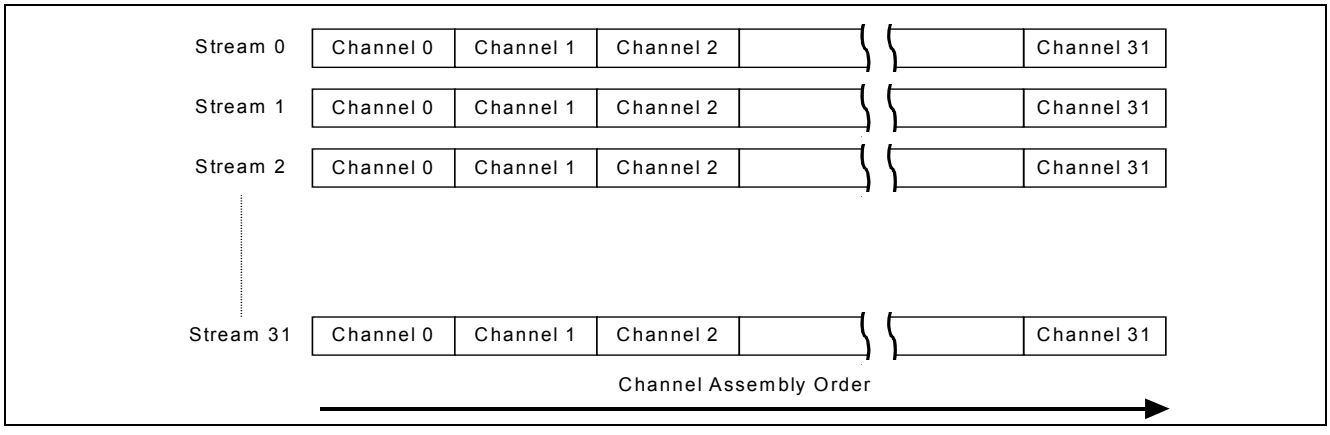


Figure 15 - Channel Order for Packet Formation

Each packet contains one or more frames of TDM data, in sequential order. This groups the selected channels for the first frame, followed by the same set of channels for the subsequent frame, and so on.

5.4.2 Unstructured Payload Operation

In unstructured mode, the payload is not split by defined frames or timeslots, so the packet consists of a continuous stream of data. Each packet contains a programmable number of octets, as shown in Figure 16. The number of octets in a packet need not be an integer number of frames. A typical value for N may be 192, as defined in the IETF PWE3 standard. For example, consider mapping the unstructured data of a 25 timeslot DS0 stream. The data for each T1 frame would normally consist of 193 bits, 192 data bits and 1 framing bit. If the payload consists of 24 octets it will be 1 bit short of a complete frames worth of data, if the payload consists of 25 octets it will be 7 bits over a complete frames worth of data. **NOTE:** No alignment of the octets with the T1 framing structure can be assumed.

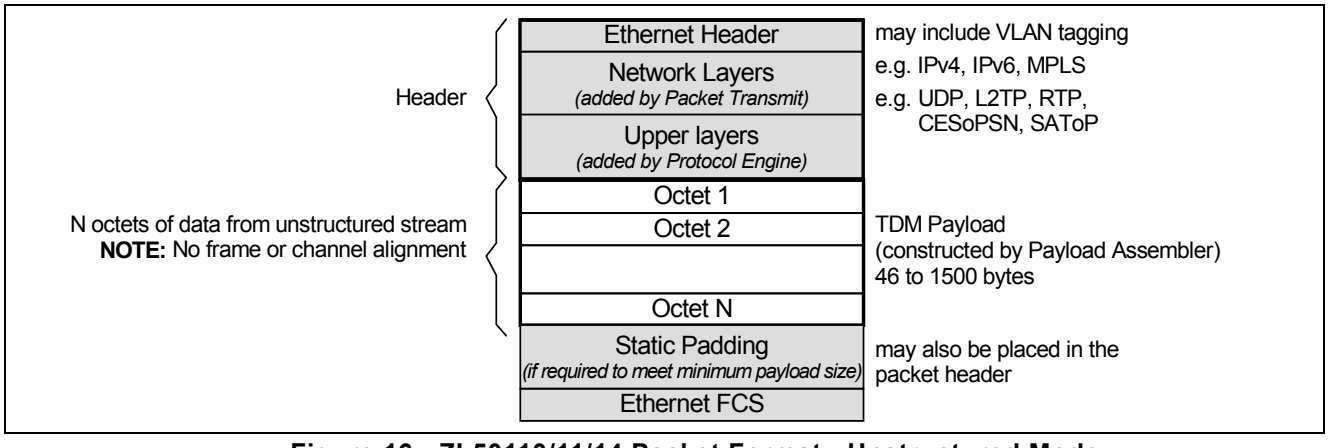


Figure 16 - ZL50110/11/14 Packet Format - Unstructured Mode

5.5 Protocol Engine

In general, the next processing block for TDM packets is the Protocol Engine. This handles the data-plane requirements of the main higher level protocols (layers 4 and 5) expected to be used in typical applications of the ZL50110/11/14 family: UDP, RTP, L2TP, CESoPSN and SAToP. The Protocol Engine can add a header to the datagram containing up to 24 bytes. This header is largely static information, and is programmed directly by the CPU. It may contain a number of dynamic fields, including a length field, checksum, sequence number and a timestamp. The location, and in some cases the length of these fields is also programmable, allowing the various protocols to be placed at variable locations within the header.

5.6 Packet Transmission

Packets ready for transmission are queued to the switch fabric interface by the Queue Manager. Four classes of service are provided, allowing some packet streams to be prioritized over others. On transmission, the Packet Transmit block appends a programmable header, which has been set up in advance by the control processor. Typically this contains the data-link and network layer headers (layers 2 and 3), such as Ethernet, IP (versions 4 and 6) and MPLS. Packet Reception

Incoming data traffic on the packet interface is received by the MACs. The well-formed packets are forwarded to a packet classifier to determine the destination. When a packet is successfully classified the destination can be the TDM interface, the LAN interface or the host interface. TDM traffic is then further classified to determine the context it is intended for.

Each TDM interface context has an individual queue, and the TDM re-formatting process re-creates the TDM streams from the incoming packet streams. This queue is used as a jitter buffer, to absorb variation in packet delay across the network. The size of the jitter buffer can be programmed in units of TDM frames (i.e. steps of 125 μs).

There is also a queue to the host interface, allowing a traffic flow to the host CPU for processing. Again the host's DMA controller can be used to retrieve packet data and write it out into the CPU's own memory.

5.7 TDM Formatter

At the receiving end of the packet network, the original TDM data must be re-constructed from the packets received. This is known as re-formatting, and follows the reverse process from the Payload Assembler. The TDM Formatter plays out the packets in the correct sequence, directing each octet to the selected timeslot on the output TDM interface.

When lost or late packets are detected, the TDM Formatter plays out underrun data for the same number of TDM frames as were included in the missing packet. Underrun data can either be the last value played out on that timeslot, or a pre-programmed value (e.g. 0xFF). If the packet subsequently turns up it is discarded. In this way, the end-to-end latency through the system is maintained at a constant value.

6.0 Clock Recovery

One of the main issues with circuit emulation is that the clock used to drive the TDM link is not necessarily linked into the central office reference clock, and hence may be any value within the tolerance defined for that service. The reverse link may also be independently timed, and operating at a slightly different frequency. In the plesiochronous digital hierarchy the difference in clock frequencies between TDM links is compensated for using bit stuffing techniques, allowing the clock to be accurately regenerated at the remote end of the carrier network.

With a packet network, that connection between the ingress and egress frequency is broken, since packets are discontinuous in time. From Figure 5, the TDM service frequency $f_{service}$ at the customer premises must be exactly reproduced at the egress of the packet network. The consequence of a long-term mismatch in frequency is that the queue at the egress of the packet network will either fill up or empty, depending on whether the regenerated clock is slower or faster than the original. This will cause loss of data and degradation of the service.

The ZL50110/11/14 provides a per-stream clock recovery function to reproduce the TDM service frequency at the egress of the packet network. Two schemes are employed, depending on the availability of a common reference clock at each provider edge unit, within the ZL50110/11/14 - differential and adaptive. The clock recovery itself is performed by software in the external processor, with support from on-chip hardware to gather the required statistics.

6.1 Differential Clock Recovery

For applications where the wander characteristics of the recovered clock are very important, such as when the emulated circuit must be connected into the plesiochronous digital hierarchy (PDH), the ZL50110/11/14 also offers a differential clock recovery technique. This relies on having a common reference clock available at each provider edge point.

In a differential technique, the timing of data packet formation is sent relative to the common reference clock. Since the same reference is available at the packet egress point and the packet size is fixed, the original service clock frequency can be recovered. This technique is unaffected by any low frequency components in the packet delay variation. The disadvantage is the requirement for a common reference clock at each end of the packet network, which could either be the central office TDM clock, or provided by a global position system (GPS) receiver.

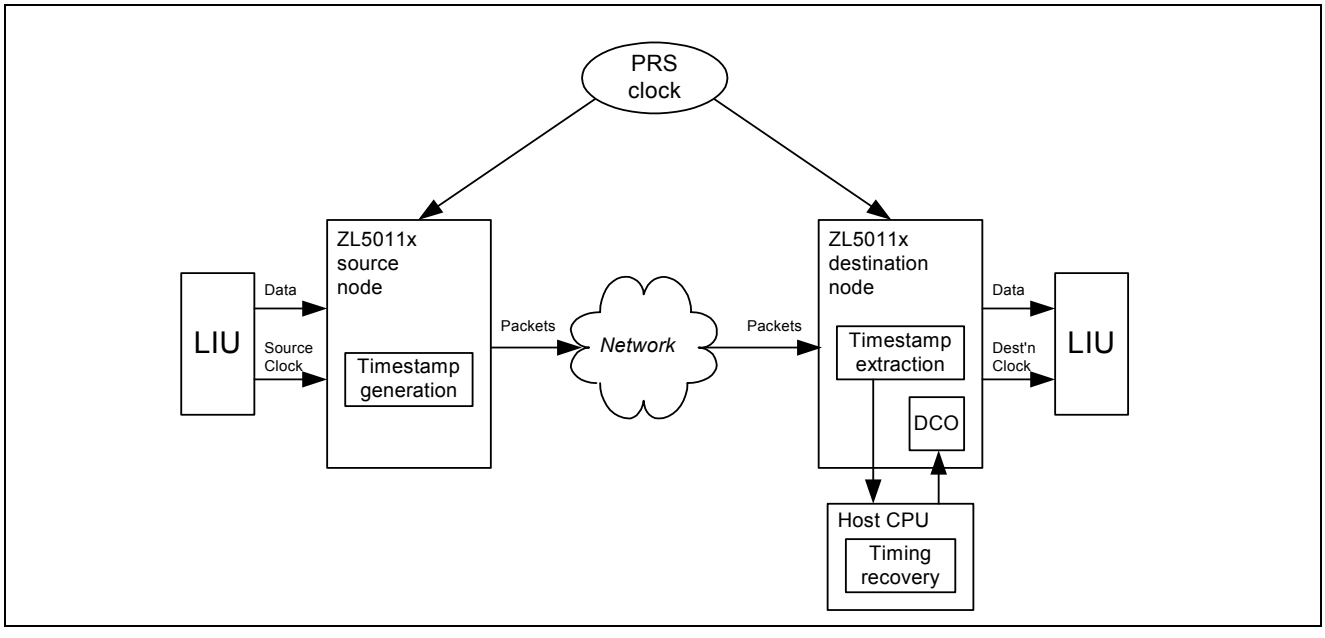


Figure 17 - Differential Clock Recovery

6.2 Adaptive Clock Recovery

For applications where there is no common reference clock between provider edge units, an adaptive clock recovery technique is provided. This infers the clock rate of the original TDM service clock from the mean arrival rate of packets at the packet egress point.

The disadvantage of this type of scheme is that, depending on the characteristics of the packet network, it may prove difficult to regenerate a clock that stays within the wander requirements of the plesiochronous digital hierarchy (specifically MTIE). The reason for this is that any variation in delay between packets will feed through as a variation in the frequency of the recovered clock. High frequency jitter can be filtered out, but any low frequency variation or wander is more difficult to remove without a very long time constant. This will in turn affect the ability of the system to lock to the original clock within an acceptable time.

With no PRS clock the only information available to determine the TDM transmission speed is the average arrival rate of the packets, as shown in Figure 18. Timestamps representing the number of elapsed source clock periods may be included in the packet header, or information can be inferred from a known payload size at the destination. It is possible to maintain average buffer-fill levels at the destination, where an increase or decrease in the fill level of the buffer would require a change in transmission clock speed to maintain the average. Additionally, the buffer-fill depth can be altered independently, with no relation to the recovered clock frequency, to control TDM transmission latency.

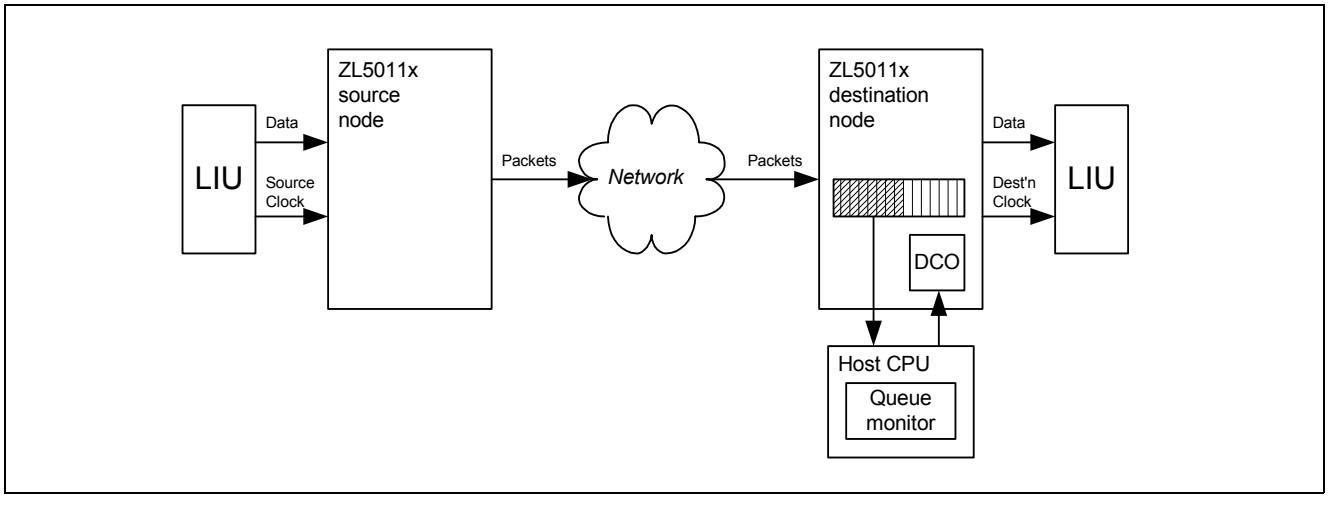


Figure 18 - Adaptive Clock Recovery

6.3 SYSTEM_CLK Considerations

The qualitiy of the 100 MHz SYSTEM_CLK or the oscillator that drives SYSTEM_CLK directly impacts the adaptive clock recovery performance. Zarlink has a recommended oscillator and guidelines for the selection of an oscillator. Please review application note ZLAN-159 “External Component Selection” before choosing an oscillator.

7.0 System Features

7.1 Latency

The following lists the intrinsic processing latency of the ZL50110/11/14, regardless of the number of active channels or contexts.

- TDM to Packet transmission processing latency less than 125 μs
- Packet to TDM transmission processing latency less than 250 μs (unstructured)
- Packet to TDM transmission processing latency less than 250 μs (structured, more than 16 channels in context)
- Packet to TDM transmission processing latency less than 375 μs (structured, 16 or less channels in context)

End-to-end latency may be estimated as the transmit latency + packet network latency + receive latency. The transmit latency is the sum of the transmit processing and the number of frames per packet x 125 μs. The receive latency is the sum of the receive processing and the delay through the jitter buffer which is programmed to compensate for packet network PDV.

The ZL50110/11/14 is capable of creating an extremely low latency connection, with end to end delays of less than 0.5 ms, depending on user configuration.

7.2 Loopback Modes

The ZL50110/11/14 devices support loopback of the TDM circuits and the circuit emulation packets.

TDM loopback is achieved by first packetizing the TDM circuit as normal via the TDM Interface and Payload Assembly blocks. The packetized data is then routed by the Task Manager back to the same TDM port via the TDM Formatter and TDM Interface.

Loopback of the emulated services is achieved by redirecting classified packets from the Packet Receive blocks, back to the packet network. The Packet Transmit blocks are setup to strip the original header and add a new header directing the packets back to the source.

7.3 Host Packet Generation

The control processor can generate packets directly, allowing it to use the network for out-of-band communications. This can be used for transmission of control data or network setup information, e.g. routing information. The host interface can also be used by a local resource for network transmission of processed data.

The device supports dual address DMA transfers of packets to and from the CPU memory, using the host's own DMA controller. Table 24 illustrates the maximum bandwidths achievable by an external DMA master.

DMA Path	Packet Size	Max Bandwidth Mbps[1]
ZL50110/11/14 to CPU only	>1000 bytes	50
ZL50110/11/14 to CPU only	60 bytes	6.7
CPU to ZL50110/11/14 only	>1000 bytes	60
CPU to ZL50110/11/14 only	60 bytes	43
Combined[2]	>1000 bytes	58 (29 each way)
Combined[2]	60 bytes	11 (5.5 each way)

Table 24 - DMA Maximum Bandwidths

Note 1: Maximum bandwidths are the maximum the ZL50110/11/14 devices can transfer under host control, and assumes only minimal packet processing by the host.

Note 2: Combined figures assume the same amount of data is to be transferred each way.

7.4 Loss of Service (LOS)

During normal operation, a situation may arise where a Loss of Service occurs. This may be caused by a disruption in the transmission line due to engineering works or cable disconnection, for example. The locally detected LOS should be transferred across the emulated T1/E1 to the far end. The far end, in turn, should propagate AIS downstream.

The handling of LOS over a CESoP connection is typically performed using (setting/clearing) the L bit in the CESoPSN or SAToP control word of the packet header.

Refer to Application Note ZLAN-159, section 4.1 for details on a variety of different ways that LOS may be handled in an application.

7.5 External Memory Requirement

The ZL50110/11/14 family includes a large amount of on-chip memory, such that for most applications, external memory will not be required. However, for certain combinations of header size, packet size and jitter buffer size, there may be a requirement for external memory. Therefore the device allows the connection of up to 8 Mbytes of synchronous ZBT-SRAM.

The following charts show how much memory is required by the ZL50111 (32 T1 streams) and the ZL50110 (8 T1 streams) for a variety of packet sizes (expressed in number of frames of TDM data) and jitter buffer sizes. It is assumed that each packet contains a full Ethernet/MPLS/MPLS/RTP/CESoPSN header.

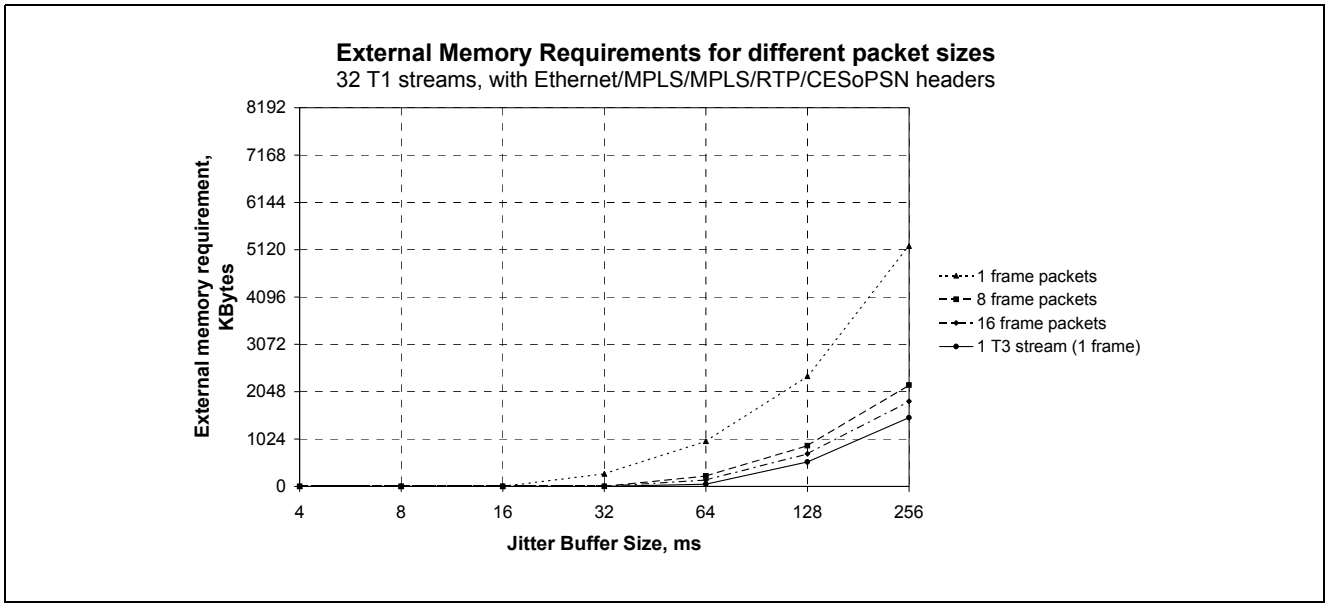


Figure 19 - External Memory Requirement for ZL50111

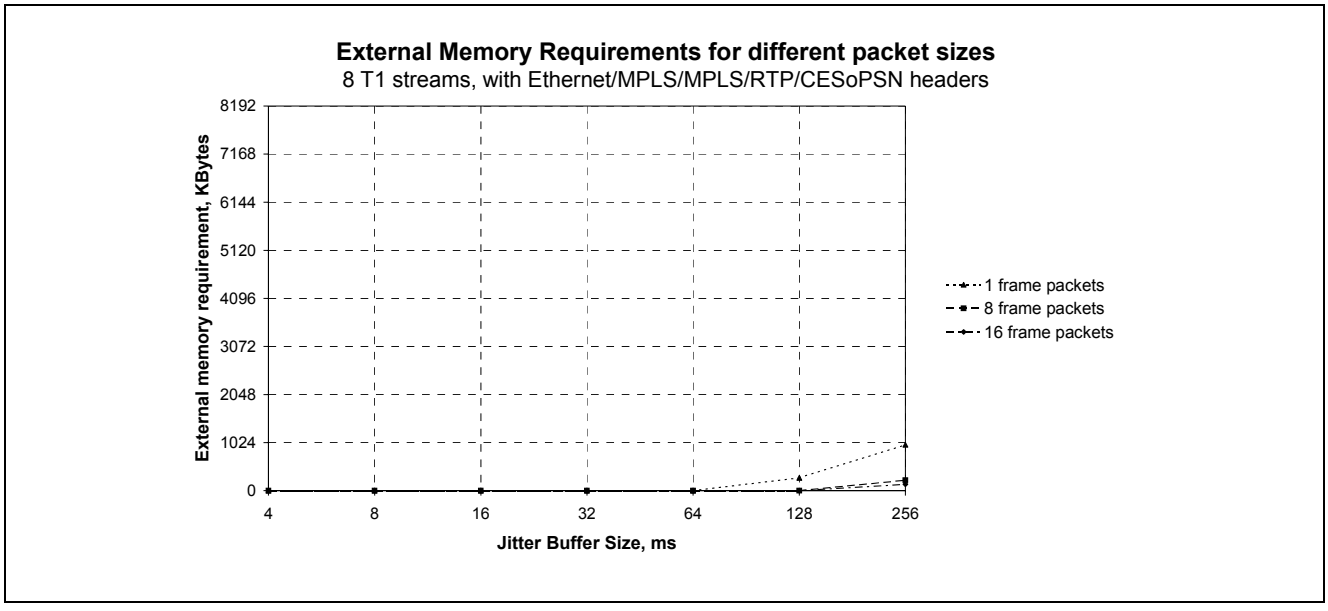


Figure 20 - External Memory Requirement for ZL50110

7.6 GIGABIT Ethernet - Recommended Configurations

NOTE: In GMII/TBI mode only 1 GMAC port may be used. The second GMAC port is for redundancy purposes only.

This section outlines connection methods for the ZL50110/11/14 in a Gigabit Ethernet environment recommended to ensure optimum performance. Two areas are covered:

- Central Ethernet Switch
- Redundant Ethernet Switch

7.6.1 Central Ethernet Switch

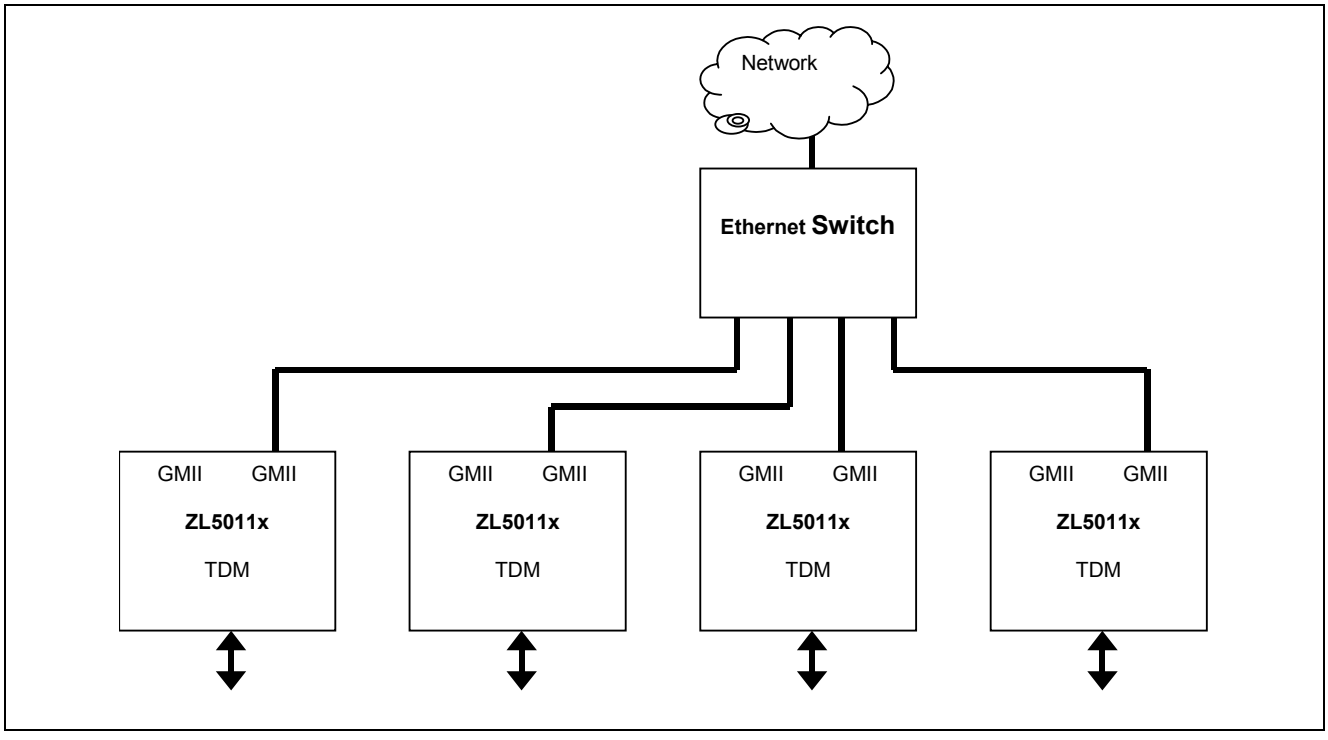


Figure 21 - Gigabit Ethernet Connection - Central Ethernet Switch

TDM data and control packets are directed to the appropriate ZL50110/11/14 device through the Ethernet Switch. There is no limit on the number of ZL50110/11/14 devices that can be connected in this configuration.

7.6.2 Redundant Ethernet Switch

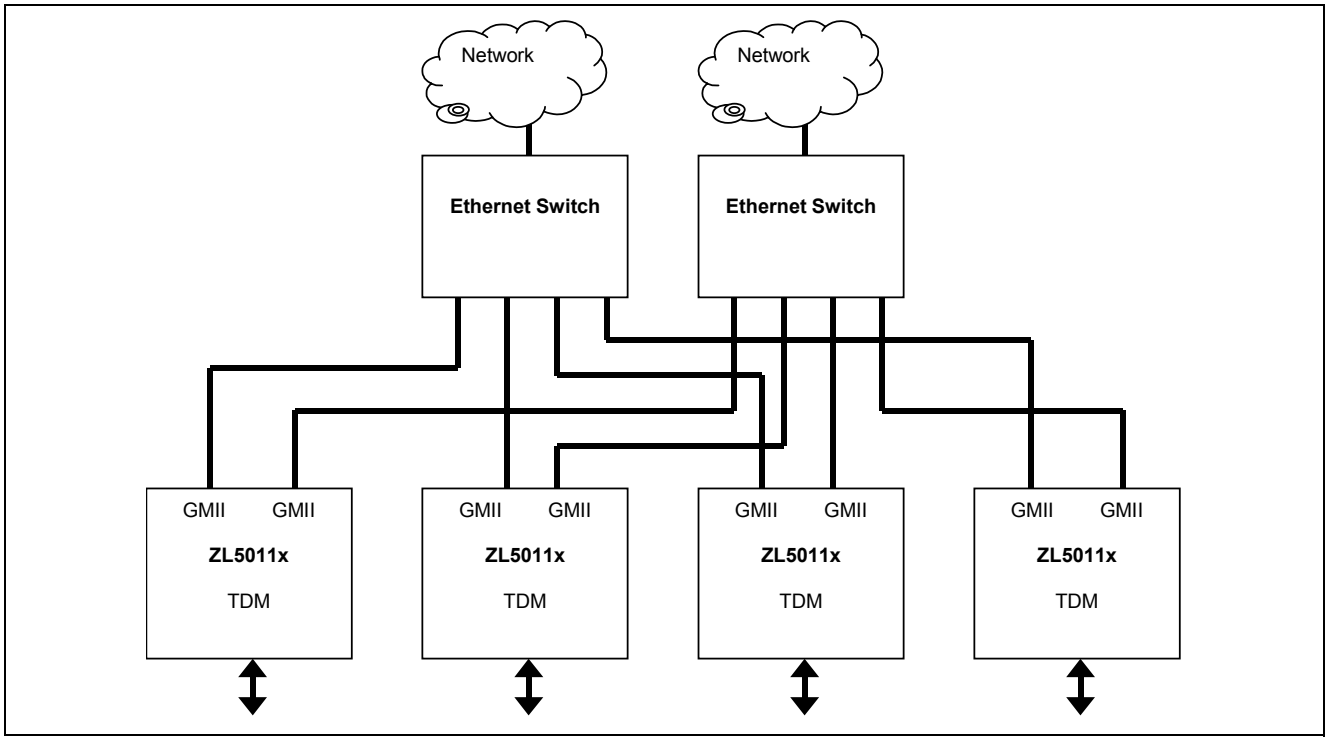


Figure 22 - Gigabit Ethernet Connection - Redundant Ethernet Switch

The central Ethernet Switch configuration can be extended to include a redundant switch connected to the second ZL50110/11/14 GMII port. One port should be used for all the TDM-to-Packet and Packet-to-TDM data with the other port idle. If the current port fails then data must be transferred to the spare port.

7.7 Power Up sequence

To power up the ZL50110/11/14 the following procedure must be used:

- The Core supply must never exceed the I/O supply by more than $0.5V_{DC}$
- Both the Core supply and the I/O supply must be brought up together
- The System Reset and, if used, the JTAG Reset must remain low until at least 100µs after the 100 MHz system clock has stabilised. Note that if JTAG Reset is not used it must be tied low

This is illustrated in the diagram shown in Figure 23.

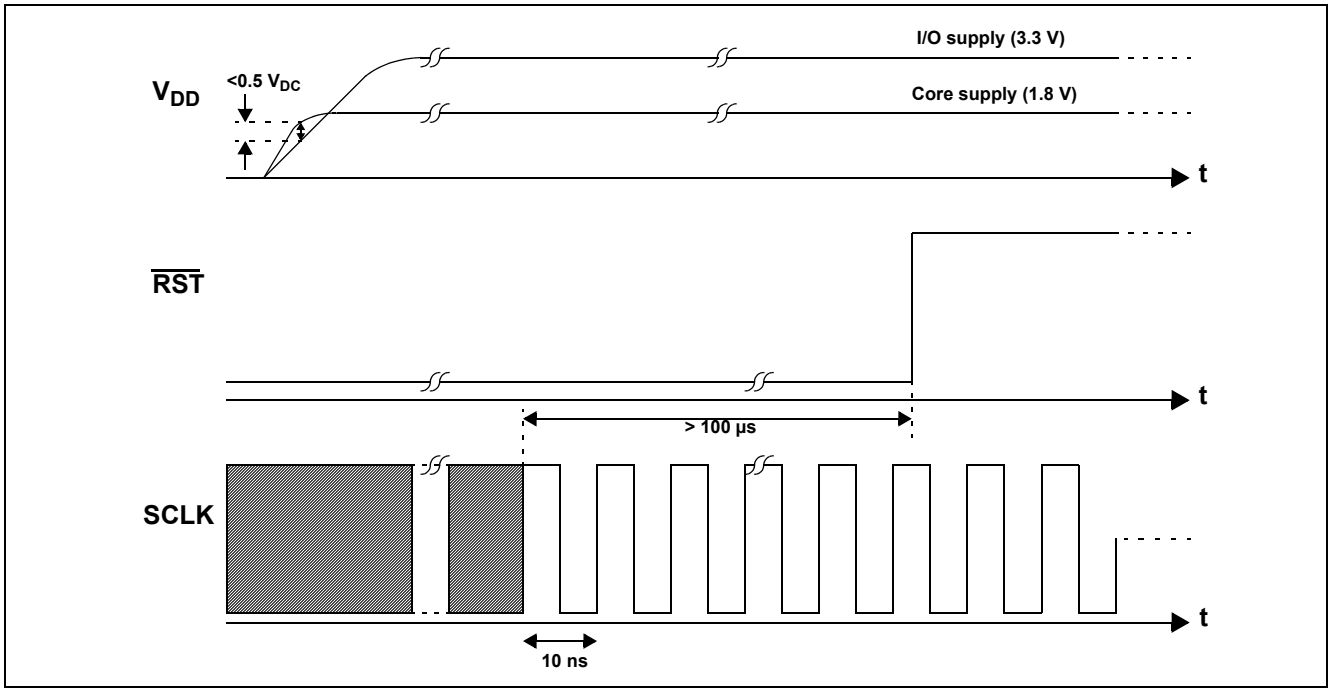


Figure 23 - Powering Up the ZL50110/11/14

7.8 JTAG Interface and Board Level Test Features

The JTAG interface is used to access the boundary scan logic for board level production testing.

7.9 External Component Requirements

- Direct connection to PowerQUICC™ II (MPC8260) host processor and associated memory, but can support other processors with appropriate glue logic
- TDM Framers and/or Line Interface Units
- Ethernet PHY for each MAC port
- Optional ZBT-SRAM for extended packet memory buffer depth

7.10 Miscellaneous Features

- System clock speed of 100 MHz
- Host clock speed of up to 66 MHz
- Debug option to freeze all internal state machines
- JTAG (IEEE1149) Test Access Port
- 3.3 V I/O Supply rail with 5 V tolerance
- 1.8 V Core Supply rail
- Fully compatible with MT90880/1/2/3 Zarlink product line

7.11 Test Modes Operation

7.11.1 Overview

The ZL50110/11/14 family supports the following modes of operation.

7.11.1.1 System Normal Mode

This mode is the device's normal operating mode. Boundary scan testing of the peripheral ring is accessible in this mode via the dedicated JTAG pins. The JTAG interface is compliant with the IEEE Std. 1149.1-2001; Test Access Port and Boundary Scan Architecture.

Each variant has it's own dedicated.bsdl file which fully describes it's boundary scan architecture.

7.11.1.2 System Tri-State Mode

All output and I/O output drivers are tri-stated allowing the device to be isolated when testing or debugging the development board.

7.11.2 Test Mode Control

The System Test Mode is selected using the dedicated device input bus TEST_MODE[2:0] as follows in Table 25.

System Test Mode	test_mode[2:0]
SYS_NORMAL_MODE	3’b000
SYS_TRI_STATE_MODE	3’b011

Table 25 - Test Mode Control

7.11.3 System Normal Mode

Selected by TEST_MODE[2:0] = 3'b000. As the test_mode[2:0] inputs have internal pull-downs this is the default mode of operation if no external pull-up/downs are connected. The GPIO[15:0] bus is captured on the rising edge of the external reset to provide internal bootstrap options. After the internal reset has been de-asserted the GPIO pins may be configured by the ADM module as either inputs or outputs.

7.11.4 System Tri-state Mode

Selected by TEST_MODE[2:0] = 3'b011. All device output and I/O output drivers are tri-stated.

8.0 DPLL Specification

The ZL50110/11/14 family incorporates an internal DPLL that meets Telcordia GR-1244-CORE Stratum 3 and Stratum 4/4E requirements, assuming an appropriate clock oscillator is connected to the system clock pin. It will meet the jitter/wander tolerance, jitter/wander transfer, intrinsic jitter/wander, frequency accuracy, capture range, phase change slope, holdover frequency and MTIE requirements for these specifications. In structured mode with the ZL50110/11/14 device operating as a master the DPLL is used to provide clock and frame reference signals to the internal and external TDM infrastructure. In structured mode, with the ZL50110/11/14 device operating as a slave, the DPLL is not used. All TDM clock generation is performed externally and the input streams are synchronised to the system clock by the TDM interface. The DPLL is not required in unstructured mode, where TDM clock and frame signals are generated by internal DCO's assigned to each individual stream.

8.1 Modes of Operation

It can be set into one of four operating modes: Locking mode, Holdover mode, Freerun mode and Powerdown mode.

8.1.1 Locking Mode (normal operation)

The DPLL accepts a reference signal from either a primary or secondary source, providing redundancy in the event of a failure. These references should have the same nominal frequencies but do not need to be identical as long as their frequency offsets meet the appropriate Stratum requirements. Each source is selected from any one of the available TDM input stream clocks (up to 32 on the ZL50111 variant), or from the external TDM_CLKiP (primary) or TDM_CLKiS (secondary) input pins, as illustrated in Figure 13 - on page 53. It is possible to supply a range of input frequencies as the DPLL reference source, depicted in Table 26. The PRD register Value is the number (in hexadecimal) that must be programmed into the PRD register within the DPLL to obtain the divided down frequency at PLL_PRI or PLL_SEC.

Source Input Frequency (MHz)	Tolerance (±ppm)	Divider Ratio	PRD/SRD Register Value (Hex) (Note 1)	Frequency at PLL_PRI or PLL_SEC (MHz)	Maximum Acceptable Input Wander tolerance (UI) (Note 2)
0.008	30	1	1	0.008	±1
1.544	130	1	1	1.544	±1023
2.048	50	1	1	2.048	±1023
4.096	50	1	1	4.096	±1023
8.192	50	1	1	8.192	±1023
16.384	50	1	1	16.384	±1023
6.312	30	1	1	6.312	±1023
22.368	20	2796	AEC	0.008	±1 (on 64k Hz)
34.368	20	537	219	0.064	±1 (on 64 kHz)
44.736 (Note 3)	20	699	2BB	0.064	±1 (on 64 kHz)

Table 26 - DPLL Input Reference Frequencies

Note 1: A PRD/SRD value of 0 will suppress the clock, and prevent it from reaching the DPLL.

Note 2: UI means Unit Interval - in this case periods of the time signal. So ±1UI on a 64 kHz signal means ±15.625 µs, the period of the reference frequency. Similarly ±1023UI on a 4.096 MHz signal means ±250 µs.

Note 3: This input frequency is supported with the use of an external divide by 2.

The maximum lock-in range can be programmed up to ±372 ppm regardless of the input frequency. The DPLL will fail to lock if the source input frequency is absent, if it is not of approximately the correct frequency or if it is too jittery. See Section 8.7 for further details. Limitations depend on the users programmed values, so the DPLL must be programmed properly to meet Stratum 3, or Stratum 4/4E. The Application Program Interface (API) software that accompanies the ZL50110/11/14 family can be used to automatically set up the DPLL for the appropriate standard requirement.

The DPLL lock-in range can be programmed using the Lock Range register (see ZL50110/11/14 Programmers Model document) in order to extend or reduce the capture envelope. The DPLL provides bit-error-free reference switching, meeting the specification limits in the Telcordia GR-1244-CORE standard. If Stratum 3 or Stratum 4/4E accuracy is not required, it is possible to use a more relaxed system clock tolerance.

The DPLL output consists of three signals; a common clock (comclk), a double-rate common clock (comclkx2), and a frame reference (8 kHz). These are used to time the internal TDM Interface, and hence the corresponding TDM infrastructure attached to the interface. The output clock options are either 2.048 Mbps (comclkx2 at 4.096 Mbps) or 8.192 Mbps (comclkx2 at 16.384 Mbps), determined by setup in the DPLL control register. The frame pulse is programmable for polarity and width.

8.1.2 Holdover Mode

In the event of a reference failure resulting in an absence of both the primary and secondary source, the DPLL automatically reverts to Holdover mode. The last valid frequency value recorded before failure can be maintained within the Stratum 3 limits of ±0.05 ppm. The hold value is wholly dependent on the drift and temperature performance of the system clock. For example, a ±32 ppm oscillator may have a temperature coefficient of ±0.1 ppm/°C. Thus a 10°C ambient change since the DPLL was last in the Locking mode will change the holdover frequency by an additional ±1 ppm, which is much greater than the ±0.05 ppm Stratum 3 specification. If the strict target of Stratum 3 is not required, a less restrictive oscillator can be used for the system clock.

Holdover mode is typically used for a short period of time until network synchronisation is re-established.

8.1.3 Freerun Mode

In freerun mode the DPLL is programmed with a centre frequency, and can output that frequency within the Stratum 3 limits of ±4.6 ppm. To achieve this the 100 MHz system clock must have an absolute frequency accuracy of ±4.6 ppm. The centre frequency is programmed as a fraction of the system clock frequency.

8.1.4 Powerdown Mode

It is possible to “power down” the DPLL when it is not in use. For example, an unstructured TDM system, or use of an external DPLL would mean the internal DPLL could be switched off, saving power. The internal registers can still be accessed while the DPLL is powered down.

8.2 Reference Monitor Circuit

There are two identical reference monitor circuits, one for the primary and one for the secondary source. Each circuit will continually monitor its reference, and report the references validity. The validity criteria depends on the frequency programmed for the reference. A reference must meet all the following criteria to maintain validity:

- The “period in specified range” check is performed regardless of the programmed frequency. Each period must be within a range, which is programmable for the application. Refer to the ZL50110/11/14 programmers model for details.
- If the programmed frequency is 1.544 MHz or 2.048 MHz, the “n periods in specified range” check will be performed. The time taken for n cycles must be within a programmed range, typically with n at 64, the time taken for consecutive cycles must be between 62 and 66 periods of the programmed frequency.

The fail flags are independent of the preferred option for primary or secondary operation, will be asserted in the event of an invalid signal regardless of mode.

8.3 Locking Mode Reference Switching

When the reference source the DPLL is currently locking to becomes invalid, the DPLL's response depends on which one of the failure detect modes has been chosen: autodetect, forced primary, or forced secondary. One of these failure detect modes must be chosen via the FDM1:0 bits of the DOM register. After a device reset via the SYSTEM_RESET pin, the autodetect mode is selected.

In autodetect mode (automatic reference switching) if both references are valid the DPLL will synchronise to the preferred reference. If the preferred reference becomes unreliable, the DPLL continues driving its output clock in a stable holdover state until it makes a switch to the backup reference. If the preferred reference recovers, the DPLL makes a switch back to the preferred reference. If necessary, the switch back can be prevented by changing the preferred reference using the REFSEL bit in the DOM register, after the switch to the backup reference has occurred.

If both references are unreliable, the DPLL will drive its output clock using the stable holdover values until one of the references becomes valid.

In forced primary mode, the DPLL will synchronise to the primary reference only. The DPLL will not switch to the secondary reference under any circumstances including the loss of the primary reference. In this condition, the DPLL remains in holdover mode until the primary reference recovers. Similarly in forced secondary mode, the DPLL will synchronise to the secondary reference only, and will not switch to the primary reference. Again, a failure of the secondary reference will cause the DPLL to enter holdover mode, until such time as the secondary reference recovers. The choice of preferred reference has no effect in these modes.

When a conventional PLL is locked to its reference, there is no phase difference between the input reference and the PLL output. For the DPLL, the input references can have any phase relationship between them. During a reference switch, if the DPLL output follows the phase of the new reference, a large phase jump could occur. The phase jump would be transferred to the TDM outputs. The DPLL's MTIE (Maximum Time Interval Error) feature preserves the continuity of the DPLL output so that it appears no reference switch had occurred. The MTIE circuit is not perfect however, and a small Time Interval Error is still incurred per reference switch. To align the DPLL output clock to the nearest edge of the selected input reference, the MTIE reset bit (MRST bit in the DOM register) can be used.

Unlike some designs, switching between references which are at different nominal frequencies do not require intervention such as a system reset.

8.4 Locking Range

The locking range is the input frequency range over which the DPLL must be able to pull into synchronization and to maintain the synchronization. The locking range is programmable up to ±372 ppm.

Note that the locking range relates to the system clock frequency. If the external oscillator has a tolerance of -100 ppm, and the locking range is programmed to ±200 ppm, the actual locking range is the programmed value shifted by the system clock tolerance to become -300 ppm to +100 ppm.

8.5 Locking Time

The Locking Time is the time it takes the synchroniser to phase lock to the input signal. Phase lock occurs when the input and output signals are not changing in phase with respect to each other (not including jitter).

Locking time is very difficult to determine because it is affected by many factors including:

- initial input to output phase difference
- initial input to output frequency difference

- DPLL Loop Filter
- DPLL Limiter (phase slope)

Although a short phase lock time is desirable, it is not always achievable due to other synchroniser requirements. For instance, better jitter transfer performance is obtained with a lower frequency loop filter which increases locking time; and a better (smaller) phase slope performance will increase locking time. Additionally, the locking time is dependent on the p_shift value.

The DPLL Loop Filter and Limiter have been optimised to meet the Telcordia GR-1244-CORE jitter transfer and phase alignment speed requirements. The phase lock time is guaranteed to be no greater than 30 seconds when using the recommended Stratum 3 and Stratum 4/4E register settings.

8.6 Lock Status

The DPLL has a Lock Status Indicator and a corresponding Lock Change Interrupt. The response of the Lock Status Indicator is a function of the programmed Lock Detect Interval (LDI) and Lock Detect Threshold (LDT) values in the dpll_ldetect register. The LDT register can be programmed to set the jitter tolerance level of the Lock Status Indicator. To determine if the DPLL has achieved lock the Lock Status Indicator must be high for a period of at least 30 seconds. When the DPLL loses lock the Lock Status Indicator will go low after LDI x 125 μs.

8.7 Jitter

The DPLL is designed to withstand, and improve inherent jitter in the TDM clock domain.

8.7.1 Acceptance of Input Wander

For T1(1.544 MHz), E1(2.048 MHz) and J2(6.312 MHz) input frequencies, the DPLL will accept a wander of up to ±1023UI_{pp} at 0.1 Hz to conform with the relevant specifications. For the 8 kHz (frame rate) and 64 kHz (the divided down output for T3/E3) input frequencies, the wander acceptance is limited to ±1 UI (0.1 Hz). This principle is illustrated in Table 26.

8.7.2 Intrinsic Jitter

Intrinsic jitter is the jitter produced by a synchronizer and measured at its output. It is measured by applying a jitter free reference signal to the input of the device, and measuring its output jitter. Intrinsic jitter may also be measured when the device is in a non synchronizing mode such as free running or holdover, by measuring the output jitter of the device. Intrinsic jitter is usually measured with various band-limiting filters, depending on the applicable standards.

The intrinsic jitter in the DPLL is reduced to less than 1 ns p-p[1] by an internal Tapped Delay Line (TDL). The DPLL can be programmed so that the output clock meets all the Stratum 3 requirements of Telcordia GR-1244-CORE. Stratum 4/4E is also supported.

8.7.3 Jitter Tolerance

Jitter tolerance is a measure of the ability of a PLL to operate properly without cycle slips (i.e. remain in lock and/or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and the jitter frequency depends on the applicable standards.

The DPLL's jitter tolerance can be programmed to meet Telcordia GR-1244-CORE DS1 reference input jitter tolerance requirements.

1. There are 2 exceptions to this. a) When reference is 8 kHz, and reference frequency offset relative to the master is small, jitter up to 1 master clock period is possible, i.e. 10 ns p-p. b) In holdover mode, if a huge amount of jitter had been present prior to entering holdover, then an additional 2 ns p-p is possible.

8.7.4 Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

Since intrinsic jitter is always present, jitter attenuation will appear to be lower for small input jitter signals than larger ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (e.g. 75% of the specified maximum jitter tolerance).

The internal DPLL is a first order type 2 component, so a frequency offset doesn't result in a phase offset. Stratum 3 requires a -3 dB frequency of less than 3 Hz. The nature of the filter results in some peaking, resulting in a -3dB frequency of 1.9 Hz and a 0.08 dB peak with a system clock frequency of 100 MHz assuming a p_shift value of 2. The transfer function is illustrated in Figure 24 and in more detail in Figure 25. Increasing the p_shift value increases the speed the DPLL will lock to the required frequency and reduces the peak, but also reduces the tolerance to jitter - so the p_shift value must be programmed correctly to meet Stratum 3 or Stratum 4/4E jitter transfer characteristics. This is done automatically in the API.

8.8 Maximum Time Interval Error (MTIE)

In order to meet several standards requirements, the phase shift of the DPLL output must be controlled. A potential phase shift occurs every time the DPLL is re-arranged by changing reference source signal, or the mode. In order to meet the requirements of Stratum 3, the DPLL will shift phase by no more than 20 ns per re-arrangement.

Additionally the speed at which the change occurs is also critical. A large step change in output frequency is undesirable. The rate of change is programmable using the skew register, up to a maximum of 15.4 ns / 125 µs (124 ppm).

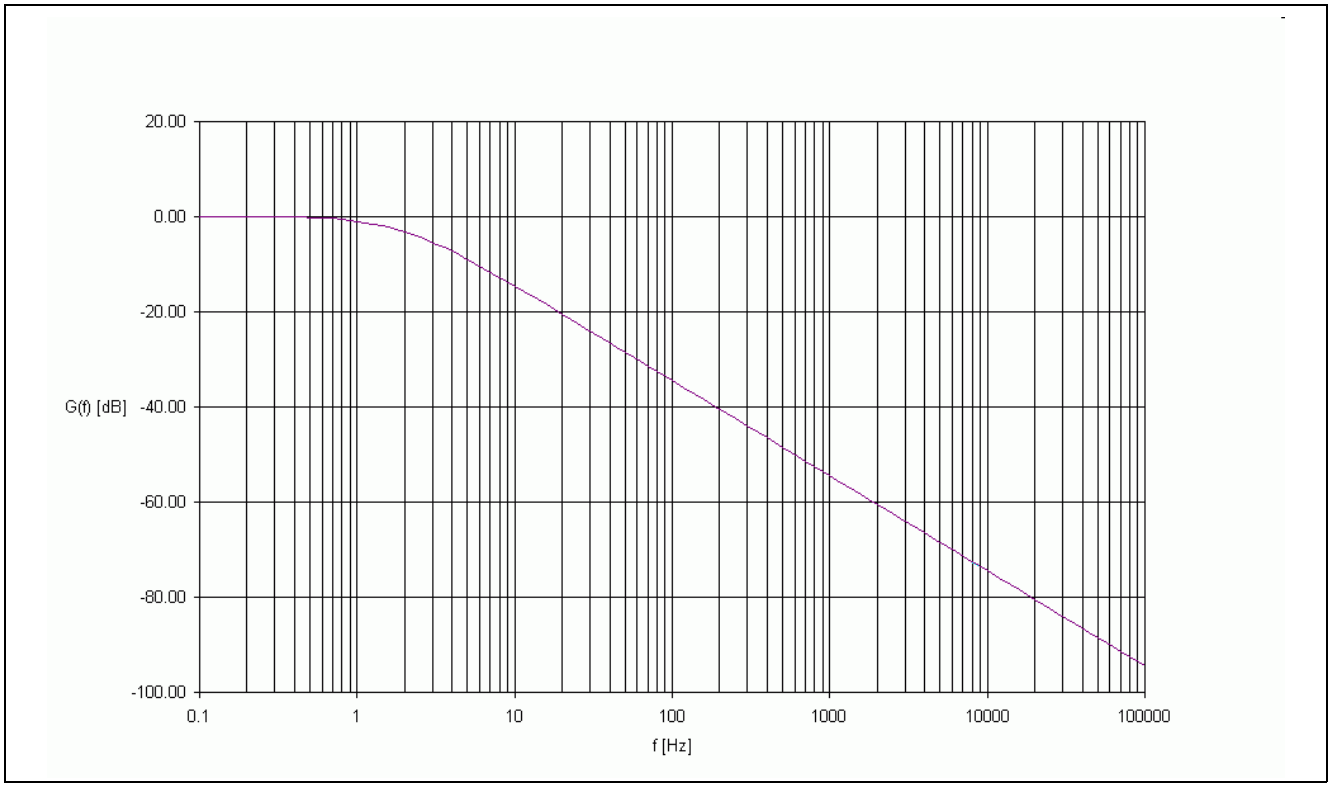


Figure 24 - Jitter Transfer Function

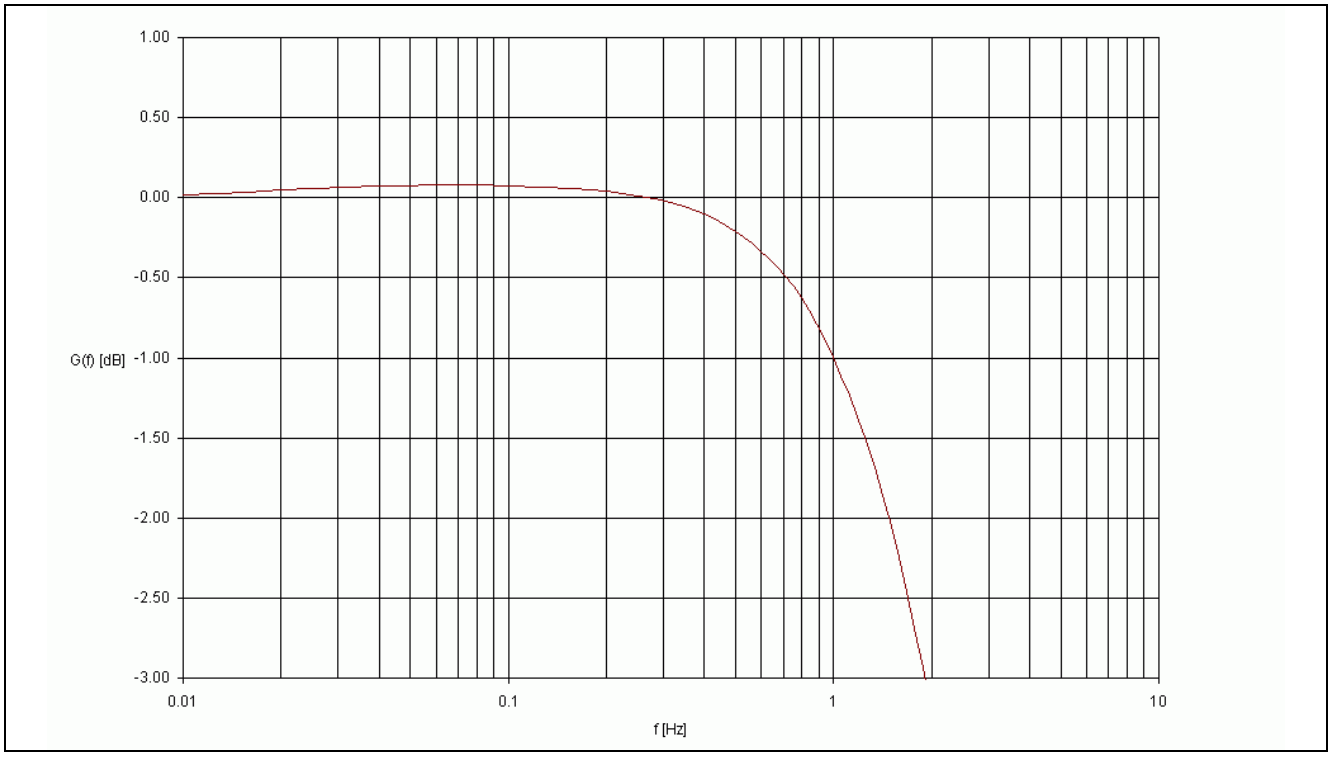


Figure 25 - Jitter Transfer Function - Detail

9.0 Memory Map and Register Definitions

All memory map and register definitions are included in the ZL50110/11/14 Programmers Model document.

10.0 DC Characteristics

Absolute Maximum Ratings*

Parameter	Symbol	Min.	Max.	Units
I/O Supply Voltage	V_{DD_IO}	-0.5	5.0	V
Core Supply Voltage	V_{DD_CORE}	-0.5	2.5	V
PLL Supply Voltage	V_{DD_PLL}	-0.5	2.5	V
Input Voltage	V_I	-0.5	V_{DD} + 0.5	V
Input Voltage (5 V tolerant inputs)	V_{I_5V}	-0.5	7.0	V
Continuous current at digital inputs	I_{IN}	-	±10	mA
Continuous current at digital outputs	I_O	-	±15	mA
Package power dissipation	PD	-	3	W
Storage Temperature	TS	-55	+125	°C

* Exceeding these figures may cause permanent damage. Functional operation under these conditions is not guaranteed. Voltage measurements are with respect to ground (V_{SS}) unless otherwise stated.

* The core and PLL supply voltages must never be allowed to exceed the I/O supply voltage by more than 0.5 V during power-up. Failure to observe this rule could lead to a high-current latch-up state, possibly leading to chip failure, if sufficient cross-supply current is available. To be safe ensure the I/O supply voltage supply always rises earlier than the core and PLL supply voltages.

Recommended Operating Conditions

Characteristics	Symbol	Min.	Typ.	Max.	Units	Test Condition
Operating Temperature	T_{OP}	-40	25	+85	°C	
Junction temperature	T_J	-40	-	125	°C	
Positive Supply Voltage, I/O	V_{DD_IO}	3.0	3.3	3.6	V	
Positive Supply Voltage, Core	V_{DD_CORE}	1.65	1.8	1.95	V	
Positive Supply Voltage, Core	V_{DD_PLL}	1.65	1.8	1.95	V	
Input Voltage Low - all inputs	V_{IL}	-	-	0.8	V	
Input Voltage High	V_{IH}	2.0	-	V_{DD_IO}	V	
Input Voltage High, 5V tolerant inputs	V_{IH_5V}	2.0	-	5.5	V	

Typical figures are at 25°C and are for design aid only, they are not guaranteed and not subject to production testing. Voltage measurements are with respect to ground (V_{SS}) unless otherwise stated.

DC Electrical Characteristics - Typical characteristics are at 1.8 V core, 3.3 V I/O, 25°C and typical processing. The min. and max. values are defined over all process conditions, from -40 to 125°C junction temperature, core voltage 1.65 to 1.95 V and I/O voltage 3.0 and 3.6 V unless otherwise stated.

Characteristics	Symbol	Min.	Typ.	Max.	Units.	Test Condition
Input Leakage	I_{LEIP}			±1	µA	No pull up/down V_{DD_IO} = 3.6 V
Output (High impedance) Leakage	I_{LEOP}			2	µA	No pull up/down V_{DD_IO} = 3.6 V
Input Capacitance	C_{IP}		1		pF	
Output Capacitance	C_{OP}		4		pF	
Pullup Current	I_{PU}		-27		µA	Input at 0 V
Pullup Current, 5 V tolerant inputs	I_{PU_5V}		-110		µA	Input at 0 V
Pulldown Current	I_{PD}		27		µA	Input at V_{DD_IO}
Pulldown Current, 5 V tolerant inputs	I_{PD_5V}		110		µA	Input at V_{DD_IO}
Core 1.8 V supply current	I_{DD_CORE}			950	mA	Note 1,2
PLL 1.8 V supply current	I_{DD_PLL}			1.30	mA	
I/O 3.3 V supply current	I_{DD_IO}			120	mA	Note 1,2

Note 1: The IO and Core supply current worst case figures apply to different scenarios, e.g., internal or external memory and can not simply be summed for a total figure. For a clearer indication of power consumption, please refer to Section 12.0.

Note 2: Worst case assumes the maximum number of active contexts and channels, i.e., 128 contexts/1024 channels. Figures are for the ZL50111. For an indication of power consumption by the ZL50110 and ZL50114, please refer to Section 12.0 and choose the appropriate memory configuration and number of contexts.

Input Levels

Characteristics	Symbol	Min.	Typ.	Max.	Units	Test Condition
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Positive Schmitt Threshold	V_{T+}		1.6		V	
Negative Schmitt Threshold	V_{T-}		1.2		V	

Output Levels

Characteristics	Symbol	Min.	Typ.	Max.	Units	Test Condition
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 6 mA. I_{OL} = 12 mA for packet interface (m*) pins and GPIO pins. I_{OL} = 24 mA for LED pins.
Output High Voltage	V_{OH}	2.4			V	I_{OH} = 6 mA. I_{OH} = 12 mA for packet interface (m*) pins and GPIO pins. I_{OH} = 24 mA for LED pins.

11.0 AC Characteristics

11.1 TDM Interface Timing - ST-BUS

The TDM Bus either operates in Slave mode, where the TDM clocks for each stream are provided by the device sourcing the data, or Master mode, where the TDM clocks are generated from the ZL50110/11/14.

11.1.1 ST-BUS Slave Clock Mode

TDM ST-BUS Slave Timing Specification

Data Format	Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
ST-BUS 8.192 Mbps mode	TDM_CLKi Period	t_{C16IP}	54	60	66	ns	
	TDM_CLKi High	t_{C16IH}	27	-	33	ns	
	TDM_CLKi Low	t_{C16IL}	27	-	33	ns	
ST-BUS 2.048 Mbps mode	TDM_CLKi Period	t_{C4IP}	-	244.1	-	ns	
	TDM_CLKi High	t_{C4IH}	110	-	134	ns	
	TDM_CLKi Low	t_{C4IL}	110	-	134	ns	
All Modes	$\overline{\text{TDM_F0i}}$ Width 8.192 Mbps 2.048 Mbps	t_{FOIW}	 50 200	 - -	 - 300	ns	
	$\overline{\text{TDM_F0i}}$ Setup Time	t_{FOIS}	5	-	-	ns	With respect to TDM_CLKi falling edge
	$\overline{\text{TDM_F0i}}$ Hold Time	t_{FOIH}	5	-	-	ns	With respect to TDM_CLKi falling edge
	TDM_STo Delay	t_{STOD}	1	-	20	ns	With respect to TDM_CLKi Load C_L = 50 pF
	TDM_STi Setup Time	t_{STIS}	5	-	-	ns	With respect to TDM_CLKi
	TDM_STi Hold Time	t_{STIH}	5	-	-	ns	With respect to TDM_CLKi

In synchronous mode the clock must be within the locking range of the DPLL to function correctly (± 245 ppm). In asynchronous mode, the clock may be any frequency.

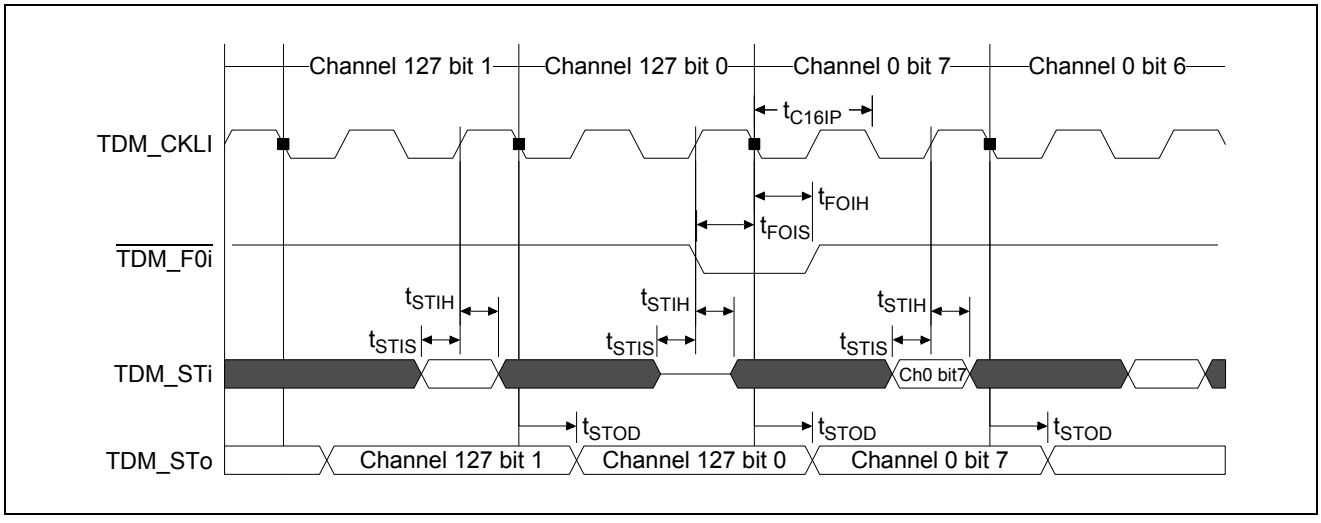


Figure 26 - TDM ST-BUS Slave Mode Timing at 8.192 Mbps

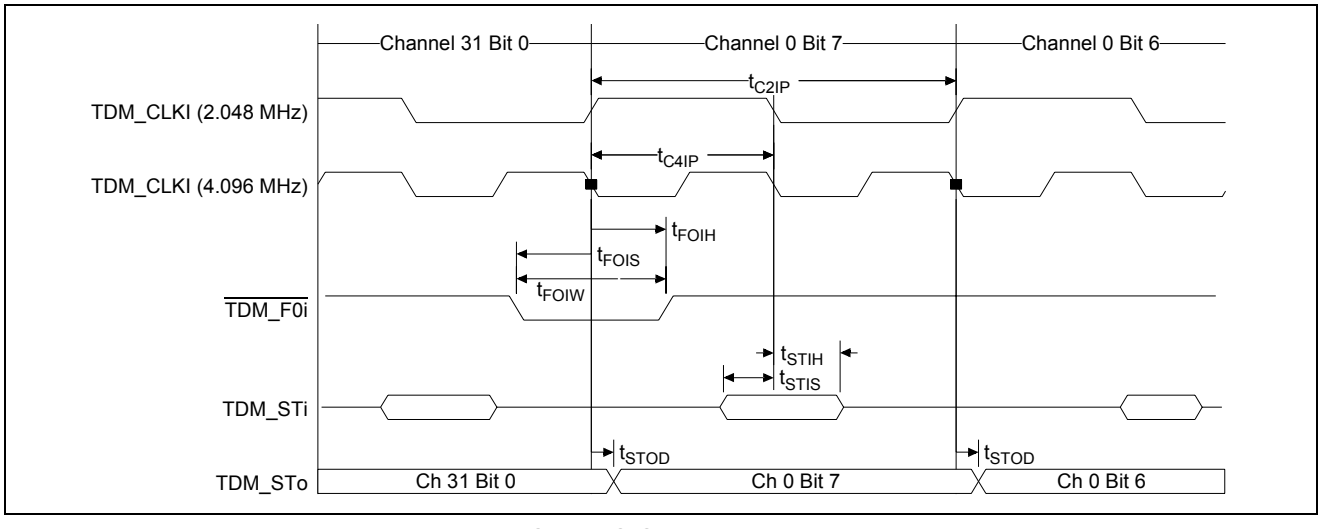


Figure 27 - TDM ST-BUS Slave Mode Timing at 2.048 Mbps

11.1.2 ST-BUS Master Clock Mode

Data Format	Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
ST-BUS 8.192 Mbps mode	TDM_CLKo Period	t_{C16OP}	54.0	61.0	68.0	ns	
	TDM_CLKo High	t_{C16OH}	23.0	-	37.0	ns	
	TDM_CLKo Low	t_{C16OL}	23.0	-	37.0	ns	
ST-BUS 2.048 Mbps mode	TDM_CLKo Period	t_{C4OP}	237.0	244.1	251.0	ns	
	TDM_CLKo High	t_{C4OH}	115.0	-	129.0	ns	
	TDM_CLKo Low	t_{C4OL}	115.0	-	129.0	ns	
All Modes	$\overline{\text{TDM_F0o}}$ Delay	t_{FOD}	-	-	25	ns	With respect to TDM_CLKo falling edge
	TDM_STo Delay Active-Active	t_{STOD}	-	-	5	ns	With respect to TDM_CLKo falling edge
	TDM_STo Delay Active to HiZ and HiZ to Active	t_{DZ}, t_{ZD}	-	-	33	ns	With respect to TDM_CLKo falling edge
	TDM_STi Setup Time	t_{STIS}	5	-	-	ns	With respect to TDM_CLKo
	TDM_STi Hold Time	t_{STIH}	5	-	-	ns	With respect to TDM_CLKo

Table 27 - TDM ST-BUS Master Timing Specification

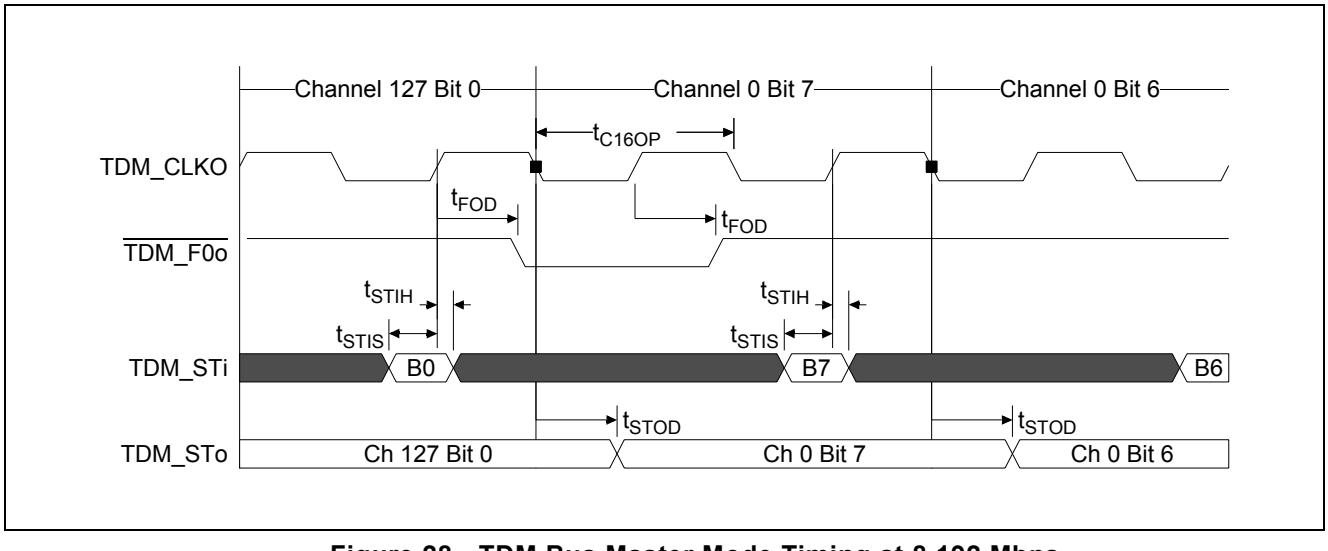


Figure 28 - TDM Bus Master Mode Timing at 8.192 Mbps

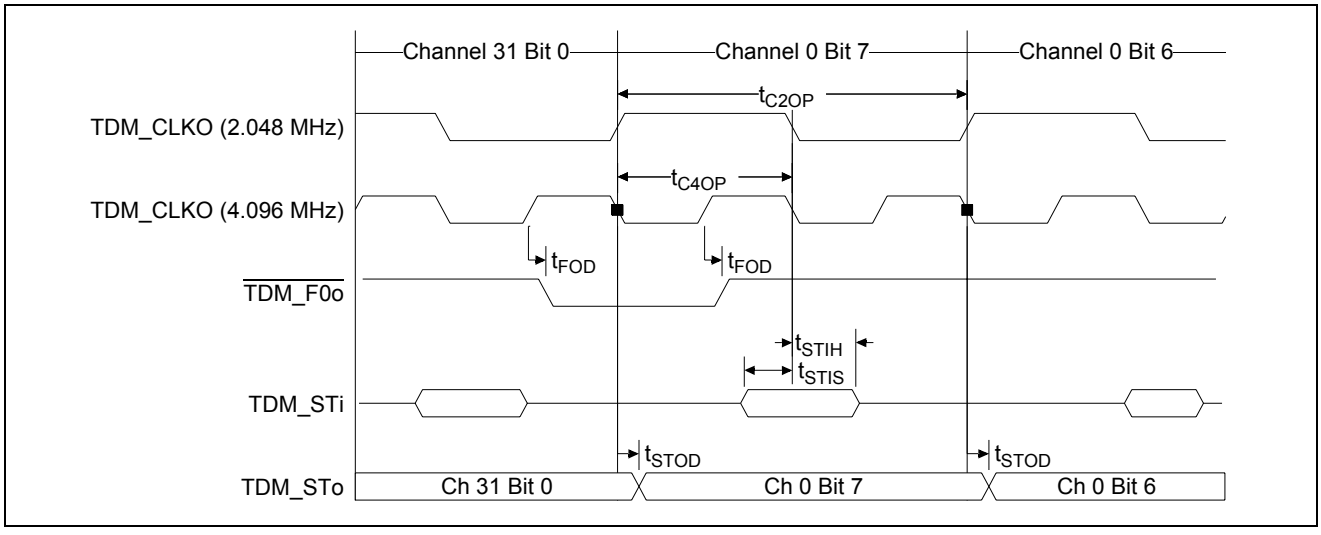


Figure 29 - TDM Bus Master Mode Timing at 2.048 Mbps

11.2 TDM Interface Timing - H.110 Mode

These parameters are based on the H.110 Specification from the Enterprise Computer Telephony Forum (ECTF) 1997.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
TDM_C8 Period	t_{C8P}	122.066-Φ	122	122.074+Φ	ns	Note 1 Note 2
TDM_C8 High	t_{C8H}	63-Φ	-	69+Φ	ns	
TDM_C8 Low	t_{C8L}	63-Φ	-	69+Φ	ns	
TDM_D Output Delay	t_{DOD}	0	-	11	ns	Load - 12 pF
TDM_D Output to HiZ	t_{DOZ}	-	-	33	ns	Load - 12 pF Note 3
TDM_D HiZ to Output	t_{ZDO}	0	-	11	ns	Load - 12 pF Note 3
TDM_D Input Delay to Valid	t_{DV}	0	-	83	ns	Note 4
TDM_D Input Delay to Invalid	t_{DIV}	102	-	112	ns	Note 4
$\overline{\text{TDM_FRAME}}$ width	t_{FP}	90	122	180	ns	Note 5
$\overline{\text{TDM_FRAME}}$ setup	t_{FS}	45	-	90	ns	
$\overline{\text{TDM_FRAME}}$ hold	t_{FH}	45	-	90	ns	
Phase Correction	F	0	-	10	ns	Note 6

Table 28 - TDM H.110 Timing Specification

Note 1: TDM_C8 and $\overline{\text{TDM_FRAME}}$ signals are required to meet the same timing standards and so are not defined independently.

Note 2: TDM_C8 corresponds to pin TDM_CLKi.

Note 3: t_{DOZ} and t_{ZDO} apply at every time-slot boundary.

Note 4: Refer to H.110 Standard from Enterprise Computer Telephony Forum (ECTF) for the source of these numbers.

Note 5: The $\overline{\text{TDM_FRAME}}$ signal is centred on the rising edge of TDM_C8. All timing measurements are based on this rising edge point; $\overline{\text{TDM_FRAME}}$ corresponds to pin $\overline{\text{TDM_F0i}}$.

Note 6: Phase correction (Φ) results from DPLL timing corrections.

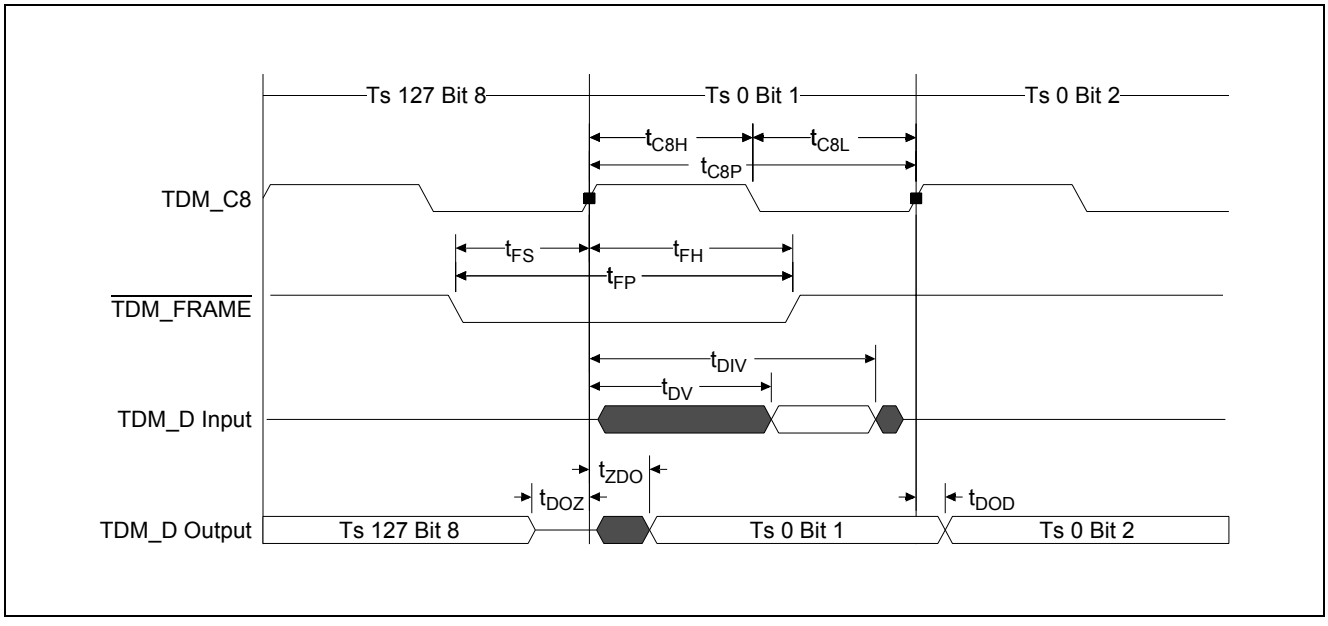


Figure 30 - H.110 Timing Diagram

11.3 TDM Interface Timing - H-MVIP

These parameters are based on the Multi-Vendor Integration Protocol (MVIP) specification for an H-MVIP Bus, Release 1.1a (1997).

Positive transitions of TDM_C2 are synchronous with the falling edges of $\overline{\text{TDM_C4}}$ and $\overline{\text{TDM_C16}}$. The signals TDM_C2, $\overline{\text{TDM_C4}}$ and $\overline{\text{TDM_C16}}$ correspond with pins TDM_CLKi. The signals $\overline{\text{TDM_F0}}$ correspond with pins $\overline{\text{TDM_F0i}}$. The signals TDM_HDS correspond with pins TDM_STi and TDM_STo.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
TDM_C2 Period	t_{C2P}	487.8	488.3	488.8	ns	
TDM_C2 High	t_{C2H}	220	-	268	ns	
TDM_C2 Low	t_{C2L}	220	-	268	ns	
$\overline{\text{TDM_C4}}$ Period	t_{C4P}	243.9	244.1	244.4	ns	
$\overline{\text{TDM_C4}}$ High	t_{C4H}	110	-	134	ns	
$\overline{\text{TDM_C4}}$ Low	t_{C4L}	110	-	134	ns	
$\overline{\text{TDM_C16}}$ Period	t_{C16P}	60.9	61.0	61.1	ns	
$\overline{\text{TDM_C16}}$ High	t_{C16H}	30	-	31	ns	
$\overline{\text{TDM_C16}}$ Low	t_{C16L}	30	-	31	ns	
TDM_HDS Output Delay	t_{PD}	-	-	30	ns	At 8.192 Mbps
TDM_HDS Output Delay	t_{PD}	-	-	100	ns	At 2.048 Mbps
TDM_HDS Output to HiZ	t_{HZD}	-	-	30	ns	
TDM_HDS Input Setup	t_S	30	-	0	ns	
TDM_HDS Input Hold	t_H	30	-	0	ns	

Table 29 - TDM H-MVIP Timing Specification

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
$\overline{\text{TDM_F0}}$ width	t_{FW}	200	244	300	ns	
$\overline{\text{TDM_F0}}$ setup	t_{FS}	50	-	150	ns	
$\overline{\text{TDM_F0}}$ hold	t_{FH}	50	-	150	ns	

Table 29 - TDM H-MVIP Timing Specification (continued)

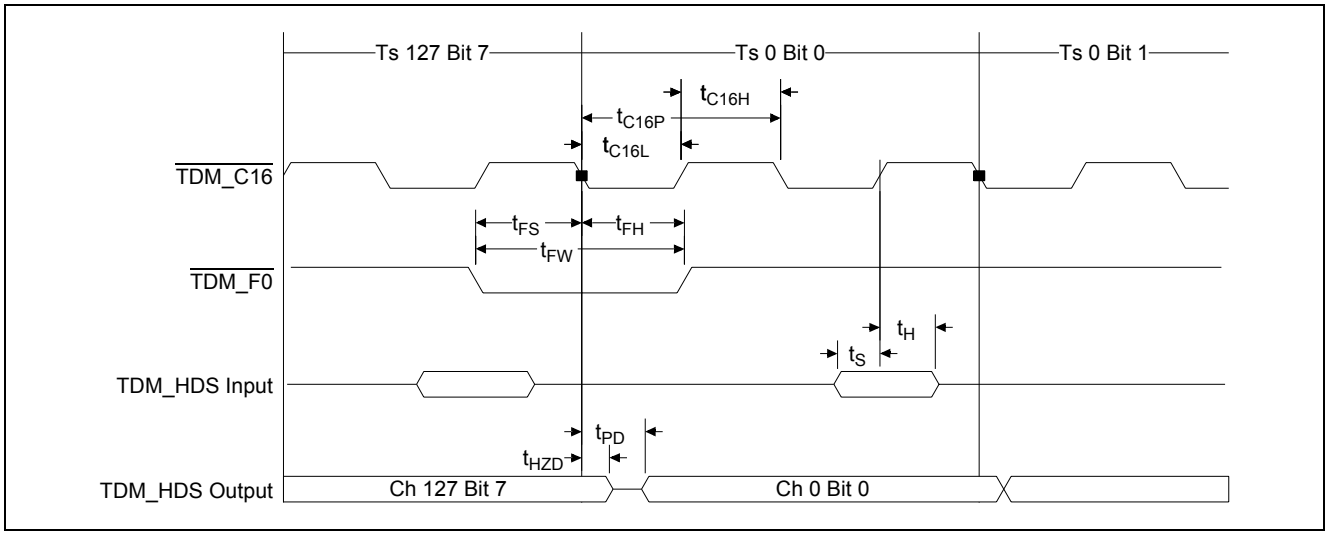


Figure 31 - TDM - H-MVIP Timing Diagram for 16 MHz Clock (8.192 Mbps)

11.4 TDM LIU Interface Timing

The TDM Interface can be used to directly drive into a Line Interface Unit (LIU). The interface can work in this mode with E1, DS1, J2, E3 and DS3. The frame pulse is not present, just data and clock is transmitted and received. Table 30 shows timing for DS3, which would be the most stringent requirement.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
TDM_TXCLK Period	t_{CTP}		22.353		ns	DS3 clock
TDM_TXCLK High	t_{CTH}	6.7			ns	
TDM_TXCLK Low	t_{CTL}	6.7			ns	
TDM_RXCLK Period	t_{CRP}		22.353		ns	DS3 clock
TDM_RXCLK High	t_{CRH}	9.0			ns	
TDM_RXCLK Low	t_{CRL}	9.0			ns	
TDM_TXDATA Output Delay	t_{PD}	3	-	10	ns	
TDM_RXDATA Input Setup	t_S	6			ns	
TDM_RXDATA Input Hold	t_H	3			ns	

Table 30 - TDM - LIU Structured Transmission/Reception

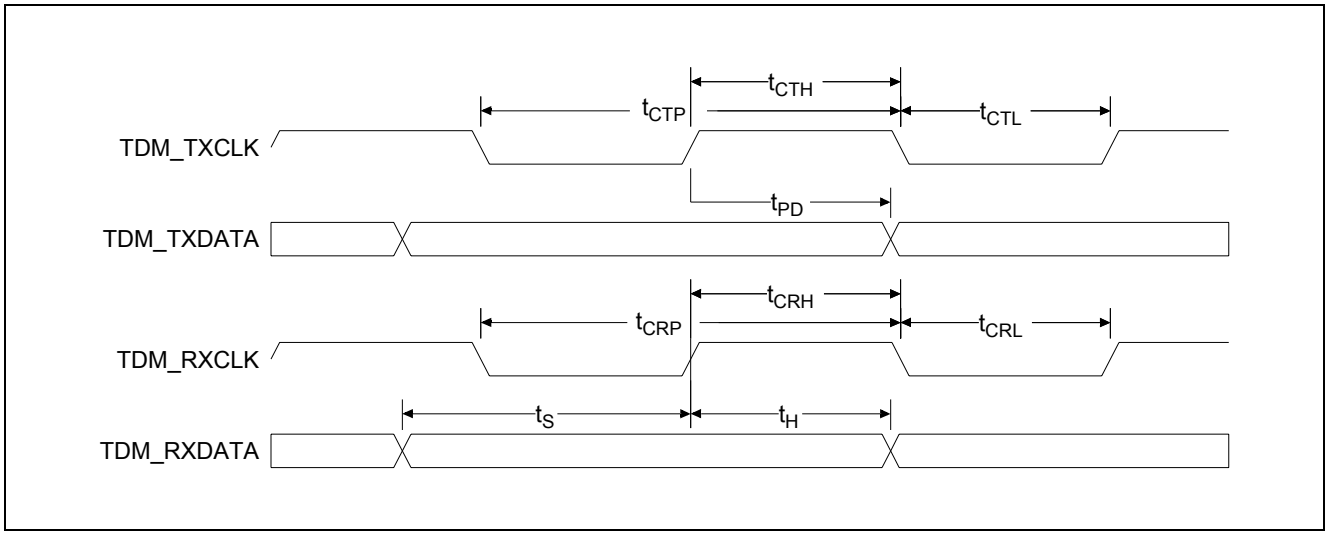


Figure 32 - TDM-LIU Structured Transmission/Reception

11.5 PAC Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
TDM_CLKiP High / Low Pulsewidth	t_{CPP}	10	-	-	ns	
TDM_CLKiS High / Low Pulsewidth	t_{CSP}	10	-	-	ns	

Table 31 - PAC Timing Specification

11.6 Packet Interface Timing

Data for the MII/GMII/TBI packet switching is based on Specification IEEE Std. 802.3 - 2000.

11.6.1 MII Transmit Timing

Parameter	Symbol	100 Mbps			Units	Notes
		Min.	Typ.	Max.		
TXCLK period	t_{CC}	-	40	-	ns	
TXCLK high time	t_{CHI}	14	-	26	ns	
TXCLK low time	t_{CLO}	14	-	26	ns	
TXCLK rise time	t_{CR}	-	-	5	ns	
TXCLK fall time	t_{CF}	-	-	5	ns	
TXCLK rise to TXD[3:0] active delay (TXCLK rising edge)	t_{DV}	1	-	25	ns	Load = 25 pF
TXCLK to TXEN active delay (TXCLK rising edge)	t_{EV}	1	-	25	ns	Load = 25 pF

Table 32 - MII Transmit Timing - 100 Mbps

Parameter	Symbol	100 Mbps			Units	Notes
		Min.	Typ.	Max.		
TXCLK to TXER active delay (TXCLK rising edge)	t_{ER}	1	-	25	ns	Load = 25 pF

Table 32 - MII Transmit Timing - 100 Mbps

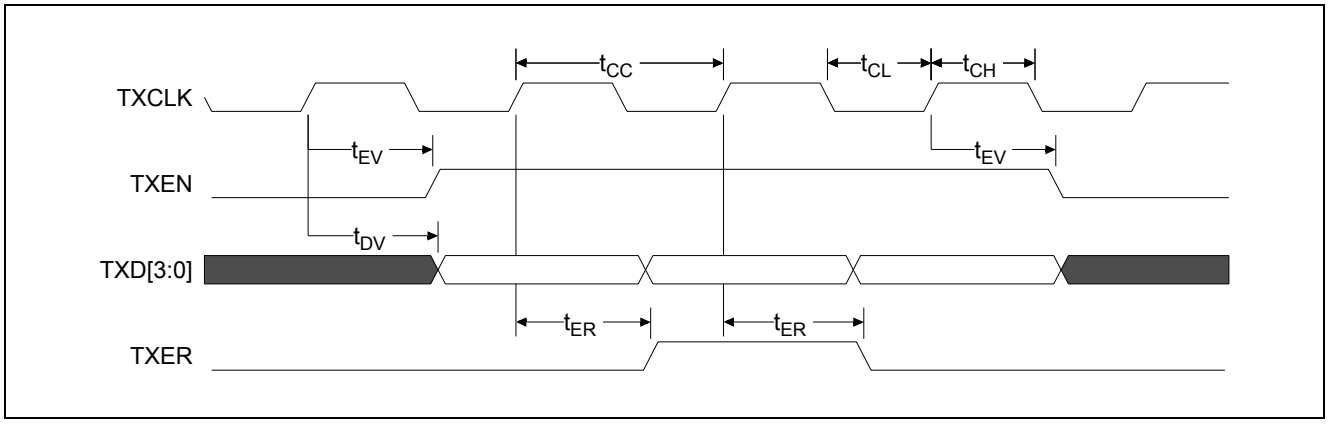


Figure 33 - MII Transmit Timing Diagram

11.6.2 MII Receive Timing

Parameter	Symbol	100 Mbps			Units	Notes
		Min.	Typ.	Max.		
RXCLK period	t_{CC}	-	40	-	ns	
RXCLK high wide time	t_{CH}	14	20	26	ns	
RXCLK low wide time	t_{CL}	14	20	26	ns	
RXCLK rise time	t_{CR}	-	-	5	ns	
RXCLK fall time	t_{CF}	-	-	5	ns	
RXD[3:0] setup time (RXCLK rising edge)	t_{DS}	10	-	-	ns	
RXD[3:0] hold time (RXCLK rising edge)	t_{DH}	5	-	-	ns	
RXDV input setup time (RXCLK rising edge)	t_{DVS}	10	-	-	ns	
RXDV input hold time (RXCLK rising edge)	t_{DVH}	5	-	-	ns	
RXER input setup time (RXCL edge)	t_{ERS}	10	-	-	ns	
RXER input hold time (RXCLK rising edge)	t_{ERH}	5	-	-	ns	

Table 33 - MII Receive Timing - 100 Mbps

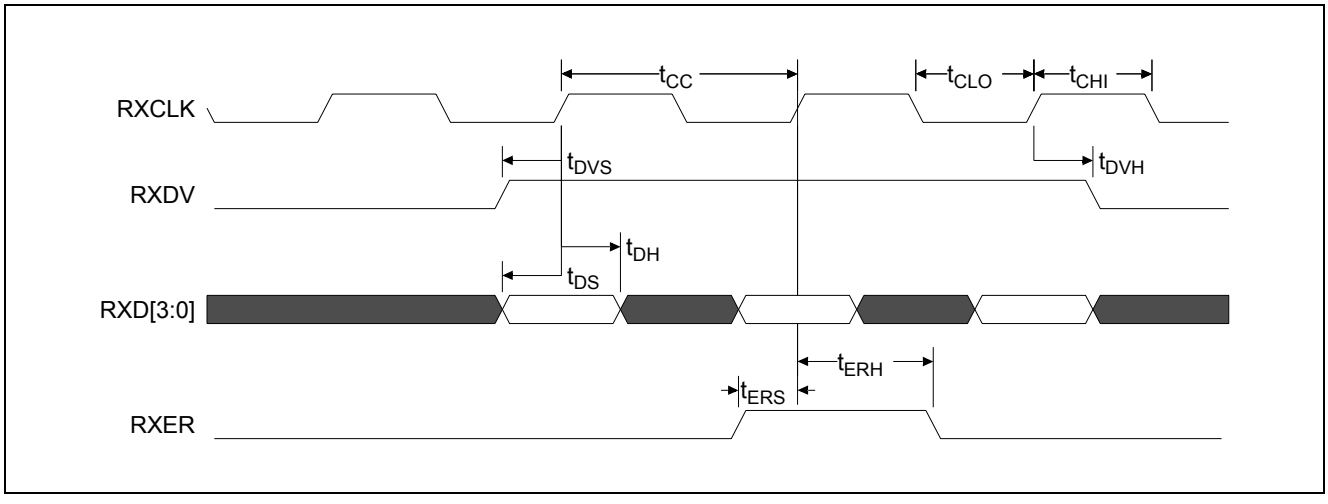


Figure 34 - MII Receive Timing Diagram

11.6.3 GMII Transmit Timing

Parameter	Symbol	1000 Mbps			Units	Notes
		Min.	Typ.	Max.		
GTXCLK period	t_{GC}	7.5	-	8.5	ns	
GTXCLK high time	t_{GCH}	2.5	-	-	ns	
GTXCLK low time	t_{GCL}	2.5	-	-	ns	
GTXCLK rise time	t_{GCR}	-	-	1	ns	
GTXCLK fall time	t_{GCF}	-	-	1	ns	
GTXCLK rise to TXD[7:0] active delay	t_{DV}	1.5	-	6	ns	Load = 25 pF
GTXCLK rise to TXEN active delay	t_{EV}	2	-	6	ns	Load = 25 pF
GTXCLK rise to TXER active delay	t_{ER}	1	-	6	ns	Load = 25 pF

Table 34 - GMII Transmit Timing - 1000 Mbps

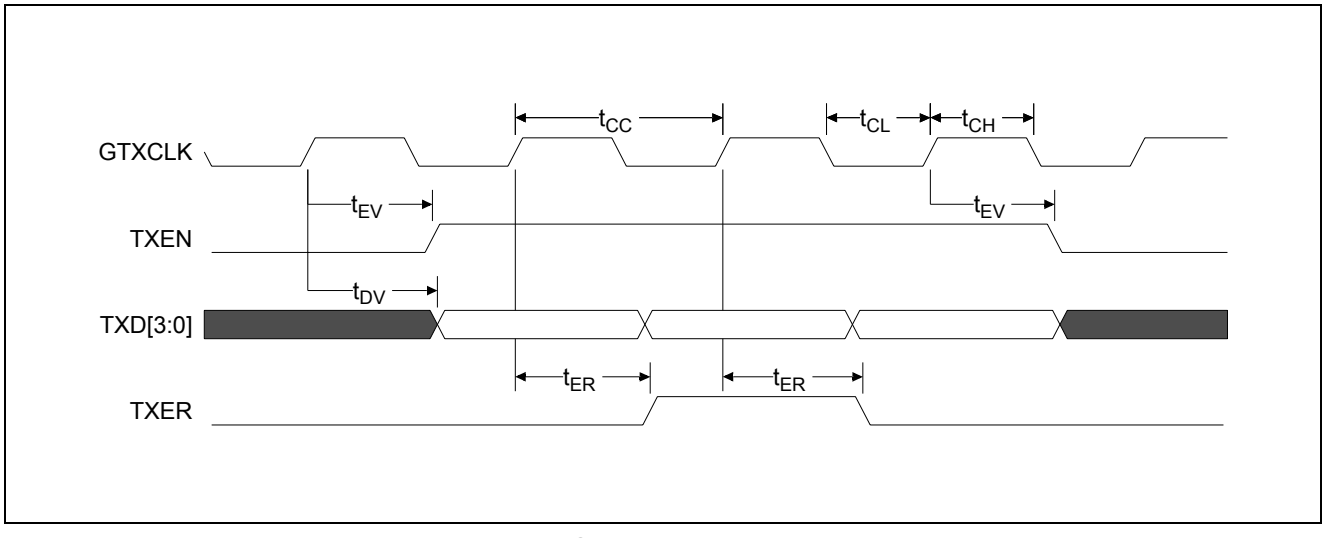


Figure 35 - GMII Transmit Timing Diagram

11.6.4 GMII Receive Timing

Parameter	Symbol	1000 Mbps			Units	Notes
		Min.	Typ.	Max.		
RXCLK period	t_{CC}	7.5	-	8.5	ns	
RXCLK high wide time	t_{CH}	2.5	-	-	ns	
RXCLK low wide time	t_{CL}	2.5	-	-	ns	
RXCLK rise time	t_{CR}	-	-	1	ns	
RXCLK fall time	t_{CF}	-	-	1	ns	
RXD[7:0] setup time (RXCLK rising edge)	t_{DS}	2	-	-	ns	
RXD[7:0] hold time (RXCLK rising edge)	t_{DH}	1	-	-	ns	
RXDV setup time (RXCLK rising edge)	t_{DVS}	2	-	-	ns	
RXDV hold time (RXCLK rising edge)	t_{DVH}	1	-	-	ns	
RXER setup time (RXCLK rising edge)	t_{ERS}	2	-	-	ns	
RXER hold time (RXCLK rising edge)	t_{ERH}	1	-	-	ns	

Table 35 - GMII Receive Timing - 1000 Mbps

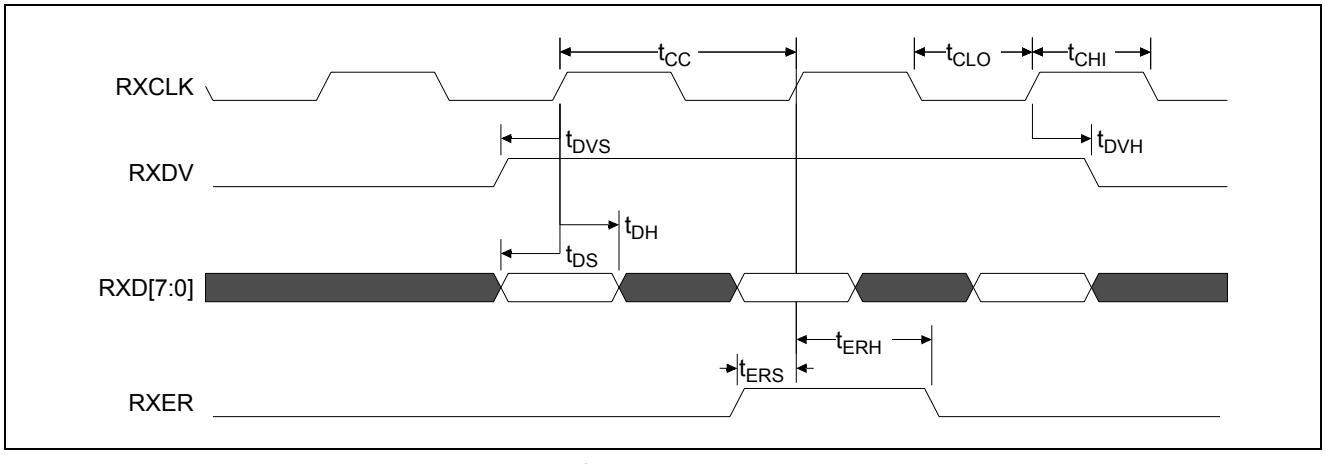


Figure 36 - GMII Receive Timing Diagram

11.6.5 TBI Interface Timing

Parameter	Symbol	1000 Mbps			Units	Notes
		Min.	Typ.	Max.		
GTXCLK period	t_{GC}	7.5	-	8.5	ns	
GTXCLK high wide time	t_{GH}	2.5	-	-	ns	
GTXCLK low wide time	t_{GL}	2.5	-	-	ns	
TXD[9:0] Output Delay (GTXCLK rising edge)	t_{DV}	1	-	6		Load = 25 pF
RCB0/RBC1 period	t_{RC}	15	16	17	ns	
RCB0/RBC1 high wide time	t_{RH}	5	-	-	ns	
RCB0/RBC1 low wide time	t_{RL}	5	-	-	ns	
RCB0/RBC1 rise time	t_{RR}	-	-	2	ns	
RCB0/RBC1 fall time	t_{RF}	-	-	2	ns	
RXD[9:0] setup time (RCB0 rising edge)	t_{DS}	2	-	-	ns	
RXD[9:0] hold time (RCB0 rising edge)	t_{DH}	1	-	-	ns	
REFCLK period	t_{FC}	7.5	-	8.5	ns	
REFCLK high wide time	t_{FH}	2.5	-	-	ns	
REFCLK low wide time	t_{FL}	2.5	-	-	ns	

Table 36 - TBI Timing - 1000 Mbps

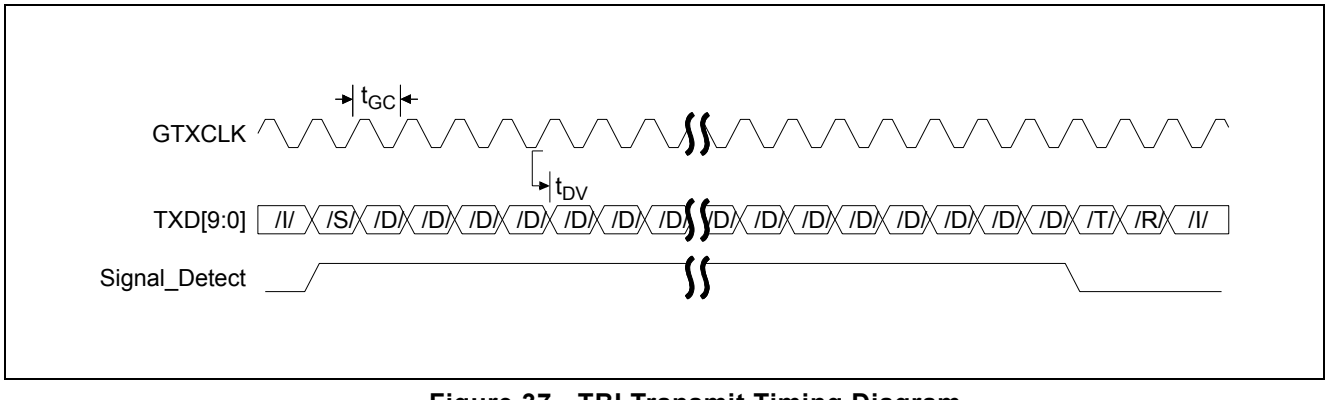


Figure 37 - TBI Transmit Timing Diagram

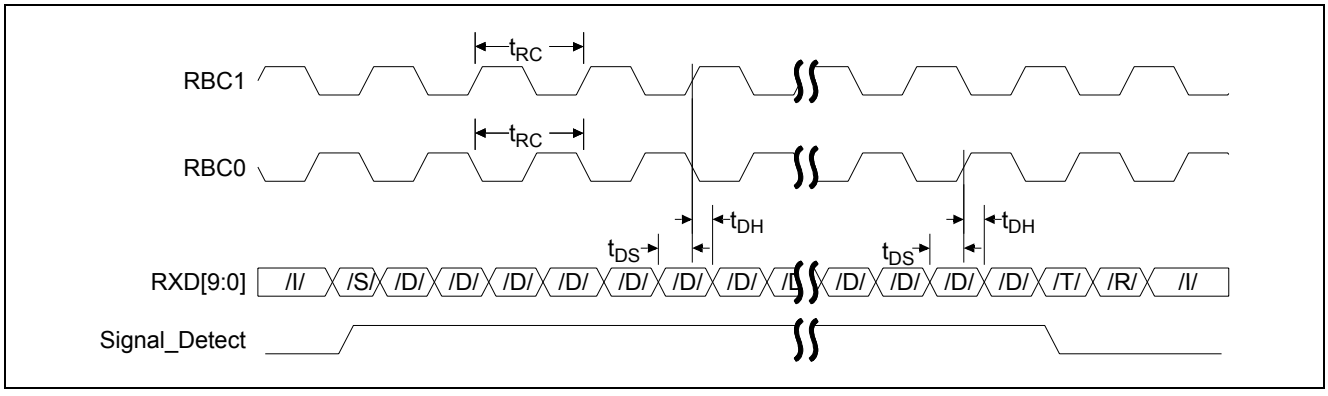


Figure 38 - TBI Receive Timing Diagram

11.6.6 Management Interface Timing

The management interface is common for all inputs and consists of a serial data I/O line and a clock line.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
M_MDC Clock Output period	t_{MP}	1990	2000	2010	ns	Note 1
M_MDC high	t_{MHI}	900	1000	1100	ns	
M_MDC low	t_{MLO}	900	1000	1100	ns	
M_MDC rise time	tMR	-	-	5	ns	
M_MDC fall time	t_{MF}	-	-	5	ns	
M_MDIO setup time (MDC rising edge)	t_{MS}	10	-	-	ns	Note 1
M_MDIO hold time (M_MDC rising edge)	t_{MH}	10	-	-	ns	Note 1
M_MDIO Output Delay (M_MDC rising edge)	t_{MD}	1	-	300	ns	Note 2

Table 37 - MAC Management Timing Specification

Note 1: Refer to Clause 22 in IEEE802.3 (2000) Standard for input/output signal timing characteristics.

Note 2: Refer to Clause 22C.4 in IEEE802.3 (2000) Standard for output load description of MDIO.

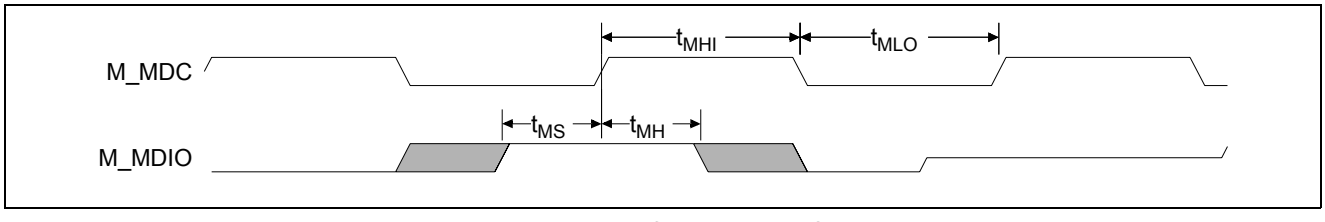


Figure 39 - Management Interface Timing for Ethernet Port - Read

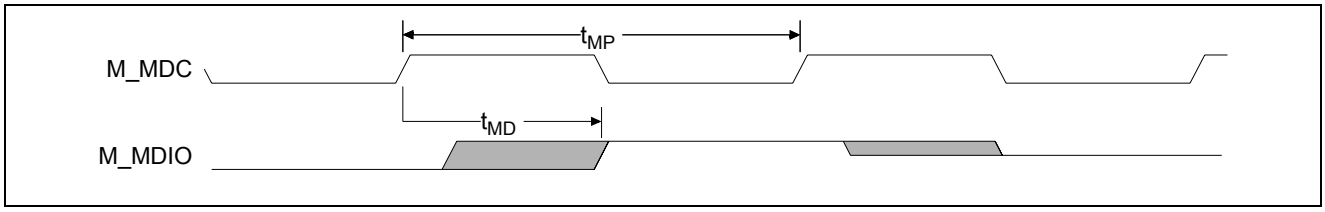


Figure 40 - Management Interface Timing for Ethernet Port - Write

11.7 External Memory Interface Timing

The timings for the External Memory Interface are based on the requirements of a ZBT-SRAM device, with the system clock speed at 100 MHz.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
RAM_DATA[63:0] Output Valid Delay	t_{RDV}	1	-	4	ns	Load C_L = 30 pF
RAM_RW/RAM_ADDR[19:0] Delay	t_{RAV}	1	-	4	ns	Load C_L = 30 pF Note 1
RAM_BW[7:0]# Delay	t_{RBW}	1	-	4	ns	Load C_L = 30 pF
RAM_DATA[63:0] Setup Time	t_{RDS}	2	-	-	ns	
RAM_DATA[63:0] Hold Time	t_{RDH}	0.5	-	-	ns	
RAM_PARITY[7:0] Output Valid Delay	t_{RPV}	1	-	4	ns	Load C_L = 30 pF
RAM_PARITY[7:0] Setup Time	t_{RPS}	2	-	-	ns	
RAM_PARITY[7:0] Hold Time	t_{RPS}	0.5	-	-	ns	

Table 38 - External Memory Timing

Note 1: Must be capable of driving TWO separate RAM loads simultaneously.

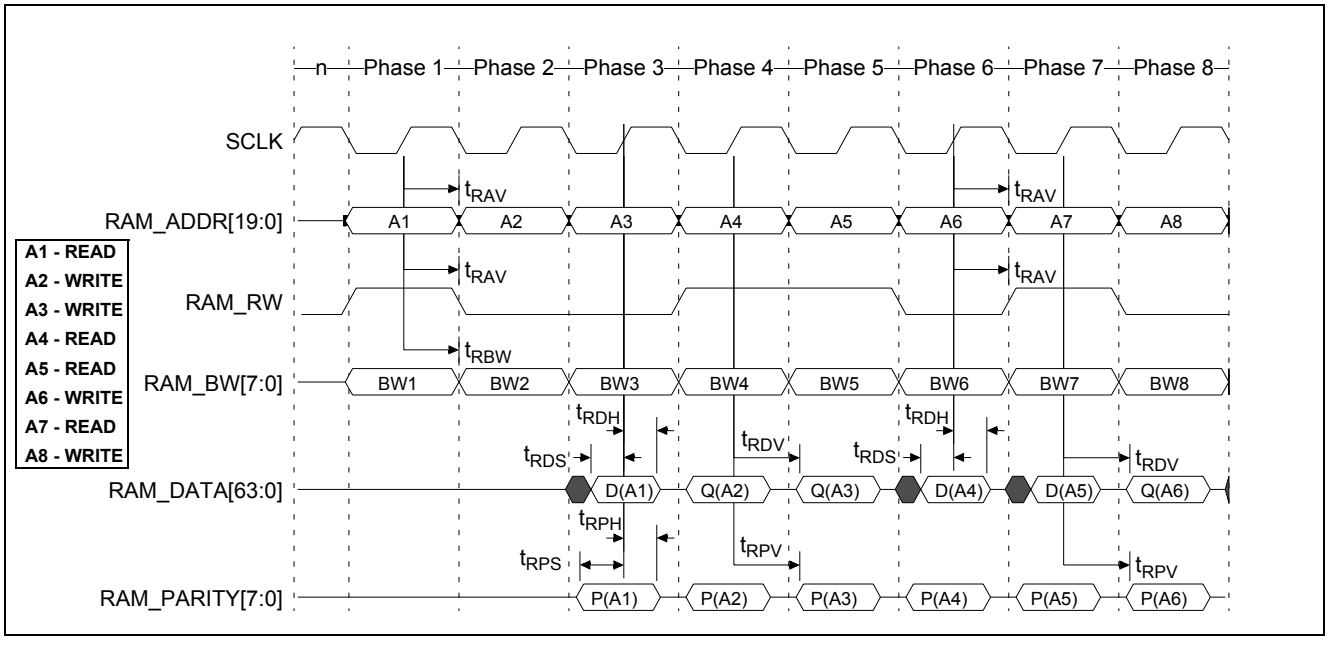


Figure 41 - External RAM Read and Write Timing

11.8 CPU Interface Timing

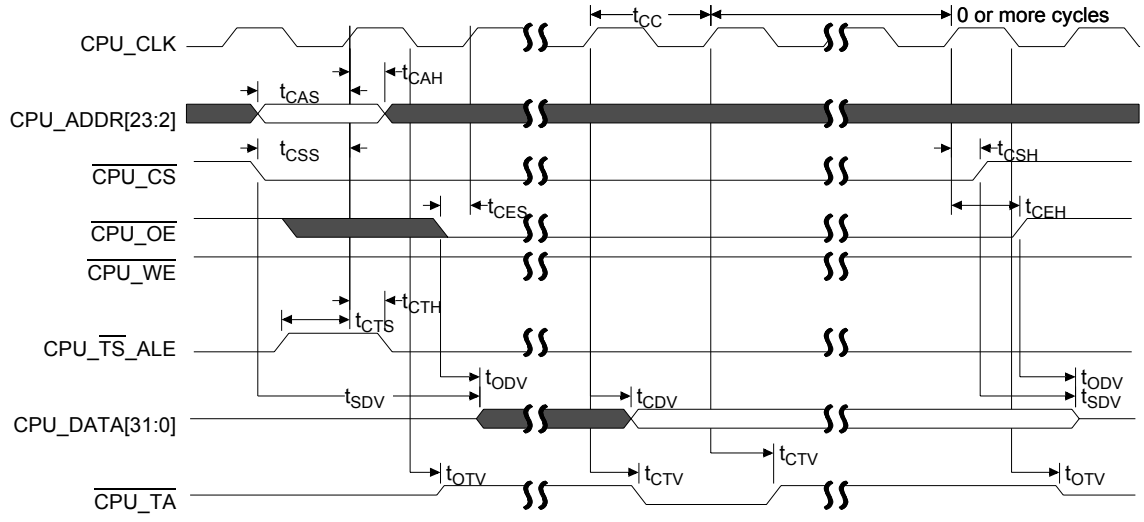
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
CPU_CLK Period	t_{CC}		15.152		ns	
CPU_CLK High Time	t_{CCH}	6			ns	
CPU_CLK Low Time	t_{CCL}	6			ns	
CPU_CLK Rise Time	t_{CCR}			4	ns	
CPU_CLK Fall Time	t_{CCF}			4	ns	
CPU_ADDR[23:2] Setup Time	t_{CAS}	4			ns	
CPU_ADDR[23:2] Hold Time	t_{CAH}	2			ns	
CPU_DATA[31:0] Setup Time	t_{CDS}	4			ns	
CPU_DATA[31:0] Hold Time	t_{CDH}	2			ns	
$\overline{\text{CPU_CS}}$ Setup Time	t_{CSS}	4			ns	
$\overline{\text{CPU_CS}}$ Hold Time	t_{CSH}	2			ns	
$\overline{\text{CPU_WE}}$/$\overline{\text{CPU_OE}}$ Setup Time	t_{CES}	5			ns	
$\overline{\text{CPU_WE}}$/$\overline{\text{CPU_OE}}$ Hold Time	t_{CEH}	2			ns	
CPU_$\overline{\text{TS}}$_ALE Setup Time	t_{CTS}	4			ns	
CPU_$\overline{\text{TS}}$_ALE Hold Time	t_{CTH}	2			ns	
$\overline{\text{CPU_SDACK1}}$/$\overline{\text{CPU_SDACK2}}$ Setup Time	t_{CKS}	2			ns	
$\overline{\text{CPU_SDACK1}}$/$\overline{\text{CPU_SDACK2}}$ Hold Time	t_{CKH}	2			ns	Note 1
$\overline{\text{CPU_TA}}$ Output Valid Delay	t_{CTV}	2		11.3	ns	Note 1, 2
$\overline{\text{CPU_DREQ0}}$/$\overline{\text{CPU_DREQ1}}$ Output Valid Delay	t_{CWV}	2		6	ns	Note 1
$\overline{\text{CPU_IREQ0}}$/$\overline{\text{CPU_IREQ1}}$ Output Valid Delay	t_{CRV}	2		6	ns	Note 1
CPU_DATA[31:0] Output Valid Delay	t_{CDV}	2		7	ns	Note 1
$\overline{\text{CPU_CS}}$ to Output Data Valid	t_{SDV}	3.2		10.4	ns	
$\overline{\text{CPU_OE}}$ to Output Data Valid	t_{ODV}	3.3		10.4	ns	
CPU_CLK(falling) to $\overline{\text{CPU_TA}}$ Valid	t_{OTV}	3.2		9.5	ns	

Table 39 - CPU Timing Specification

Note 1: Load = 50 pF maximum

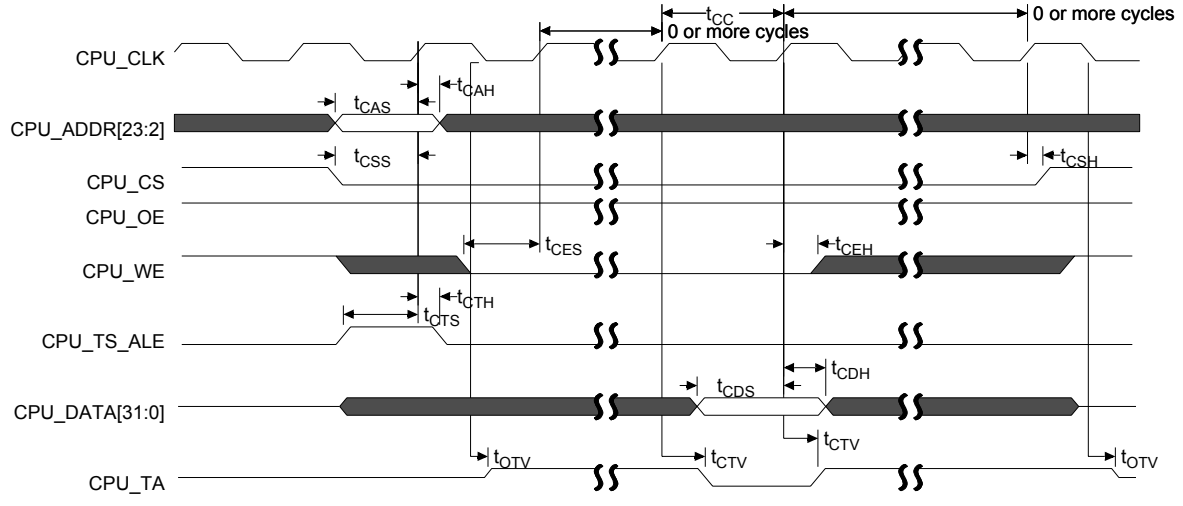
Note 2: The maximum value of t_{CTV} may cause setup violations if directly connected to the MPC8260. See Section 13.2 for details of how to accommodate this during board design.

The actual point where read/write data is transferred occurs at the positive clock edge following the assertion of $\overline{\text{CPU_TA}}$, not at the positive clock edge during the assertion of $\overline{\text{CPU_TA}}$.



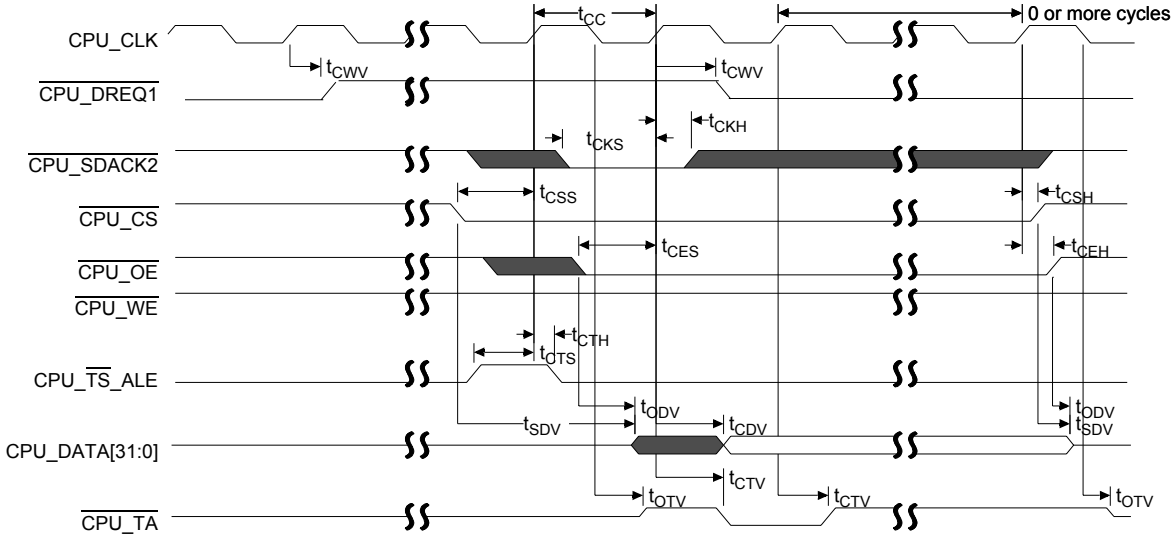
NOTE: CPU_DATA is valid when $\overline{\text{CPU_TA}}$ is asserted. CPU_DATA will remain valid while both $\overline{\text{CPU_CS}}$ and $\overline{\text{CPU_OE}}$ are asserted. $\overline{\text{CPU_TA}}$ will continue to be driven until $\overline{\text{CPU_CS}}$ is deasserted. $\overline{\text{CPU_CS}}$ and $\overline{\text{CPU_OE}}$ must BOTH be asserted to enable the CPU_DATA output.

Figure 42 - CPU Read - MPC8260



NOTE: Following assertion of CPU_TA, CPU_CS may be deasserted. The MPC8260 will continue to assert CPU_CS until CPU_TA has been synchronized internally. CPU_TA will continue to be driven until CPU_CS is finally deasserted. During continued assertion of CPU_CS, CPU_WE and CPU_DATA may be removed.

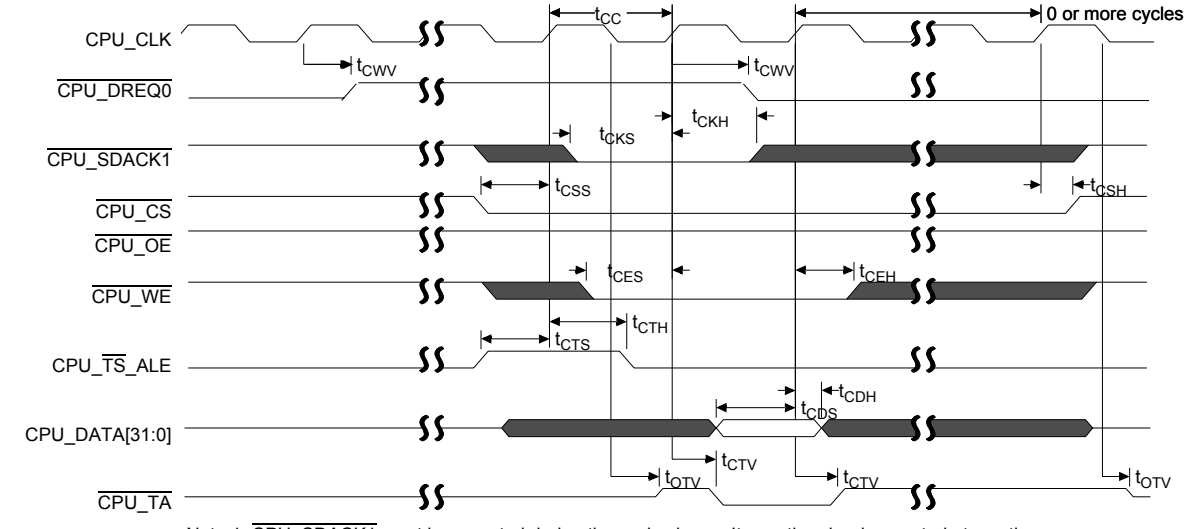
Figure 43 - CPU Write - MPC8260



Note 1: CPU_SDACK2 must be asserted during the cycle shown. It may then be deasserted at any time. CPU_DATA is valid when CPU_TA is asserted (always timed as shown). CPU_DATA will remain valid while CPU_CS and CPU_OE are asserted. CPU_TA will continue to be driven until CPU_CS is deasserted. CPU_CS and CPU_OE must BOTH be asserted to enable the CPU_DATA output.

Note 2: CPU_DREQ1 shown with positive polarity
CPU_SDACK1 shown with negative polarity

Figure 44 - CPU DMA Read - MPC8260



Note 1: CPU_SDACK1 must be asserted during the cycle shown. It may then be deasserted at any time. Following assertion of CPU_TA (always timed as shown), CPU_CS may be deasserted. The MPC8260 will continue to assert CPU_CS until CPU_TA has been synchronized internally. CPU_TA will continue to be driven until CPU_CS is finally deasserted. During continued assertion of CPU_CS, CPU_WE and CPU_DATA may be removed.

Note 2: CPU_DREQ0 shown with positive polarity
CPU_SDACK1 shown with negative polarity

Figure 45 - CPU DMA Write - MPC8260

11.9 System Function Port

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
SYSTEM_CLK Frequency	CLK_{FR}	-	100	-	MHz	Note 1, Note 2 and Note 5
SYSTEM_CLK accuracy (synchronous master mode)	CLK_{ACS}	-	-	±30	ppm	Note 3
SYSTEM_CLK accuracy (synchronous slave mode and asynchronous mode)	CLK_{ACA}	-	-	±200	ppm	Note 4

Table 40 - System Clock Timing

Note 1: The system clock frequency stability affects the holdover-operating mode of the DPLL. Holdover Mode is typically used for a short duration while network synchronisation is temporarily disrupted. Drift on the system clock directly affects the Holdover Mode accuracy. Note that the absolute system clock accuracy does not affect the Holdover accuracy, only the change in the system clock (SYSTEM_CLK) accuracy while in Holdover. For example, if the system clock oscillator has a temperature coefficient of 0.1 ppm/ºC, a 10ºC change in temperature while the DPLL is in will result in a frequency accuracy offset of 1ppm. The intrinsic frequency accuracy of the DPLL Holdover Mode is 0.06 ppm, excluding the system clock drift.

Note 2: The system clock frequency affects the operation of the DPLL in free-run mode. In this mode, the DPLL provides timing and synchronisation signals which are based on the frequency of the accuracy of the master clock (i.e. frequency of clock output equals 8.192 MHz ± SYSTEM_CLK accuracy ± 0.005 ppm).

Note 3: The absolute SYSTEM_CLK accuracy must be controlled to ± 30 ppm in synchronous master mode to enable the internal DPLL to function correctly.

Note 4: In asynchronous mode and in synchronous slave mode the DPLL is not used. Therefore the tolerance on SYSTEM_CLK may be relaxed slightly.

Note 5: The quality of SYSTEM_CLK, or the oscillator that drives SYSTEM_CLK directly impacts the adaptive clock recovery performance. See Section 6.3.

11.10 JTAG Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
JTAG_CLK period	t_{JCP}	40	100		ns	
JTAG_CLK clock pulse width	t_{LOW}, t_{HIGH}	20	-	-	ns	
JTAG_CLK rise and fall time	t_{JRF}	0	-	3	ns	
$\overline{\text{JTAG_TRST}}$ setup time	t_{RSTSU}	10	-	-	ns	With respect to JTAG_CLK falling edge. Note 1
$\overline{\text{JTAG_TRST}}$ assert time	t_{RST}	10	-	-	ns	
Input data setup time	t_{JSU}	5	-	-	ns	Note 2
Input Data hold time	t_{JH}	15	-	-	ns	Note 2
JTAG_CLK to Output data valid	t_{JDV}	0	-	20	ns	Note 3
JTAG_CLK to Output data high impedance	t_{JZ}	0	-	20	ns	Note 3
JTAG_TMS, JTAG_TDI setup time	t_{TPSU}	5	-	-	ns	
JTAG_TMS, JTAG_TDI hold time	t_{TPH}	15	-	-	ns	
JTAG_TDO delay	t_{TOPDV}	0	-	15	ns	
JTAG_TDO delay to high impedance	t_{TPZ}	0	-	15	ns	

Table 41 - JTAG Interface Timing

Note 1: $\overline{\text{JTAG_TRST}}$ is an asynchronous signal. The setup time is for test purposes only.

Note 2: Non Test (other than JTAG_TDI and JTAG_TMS) signal input timing with respect to JTAG_CLK.

Note 3: Non Test (other than JTAG_TDO) signal output with respect to JTAG_CLK.

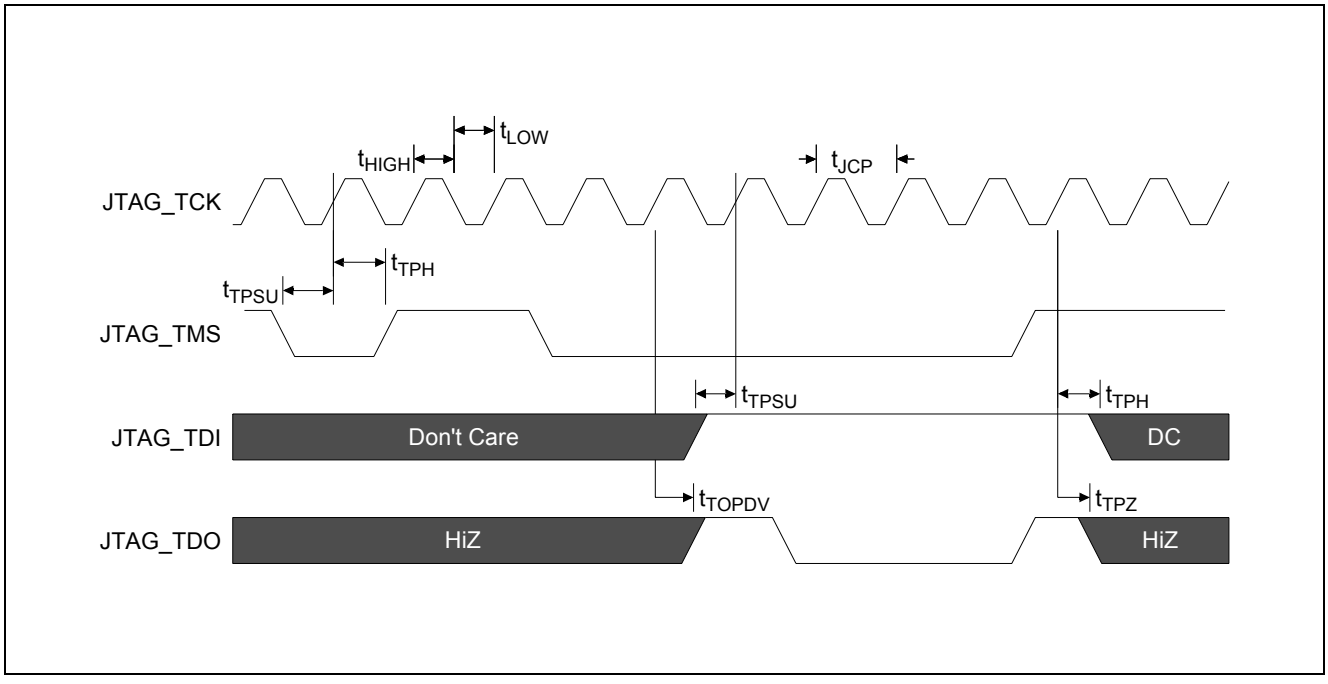


Figure 46 - JTAG Signal Timing

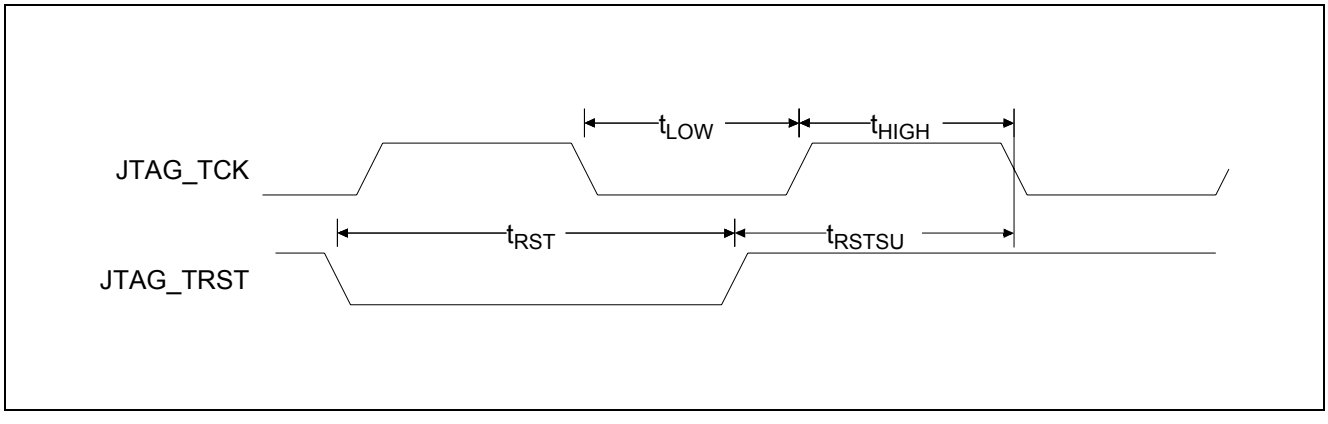


Figure 47 - JTAG Clock and Reset Timing

12.0 Power Characteristics

The following graph in Figure 48 illustrates typical power consumption figures for the ZL50110/11/14 family. Typical characteristics are at 1.8V core, 3.3V I/O, 25°C and typical processing. Power is plotted against the number of active contexts, which is the dominant factor for power consumption.

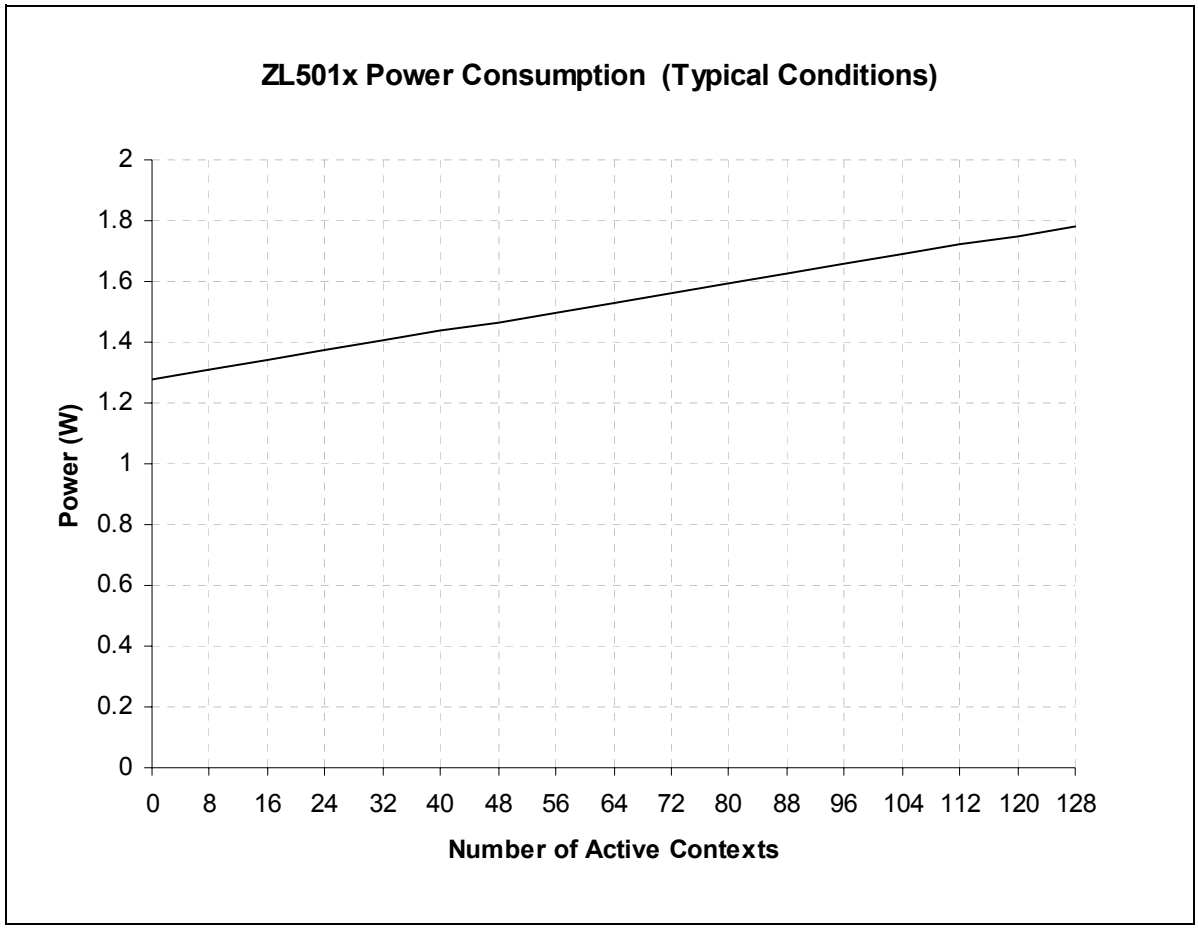


Figure 48 - ZL50110/11/14 Power Consumption Plot

13.0 Design and Layout Guidelines

This guide will provide information and guidance for PCB layouts when using the ZL50110/11/14. Specific areas of guidance are:

- High Speed Clock and Data, Outputs and Inputs
- CPU_TA Output

13.1 High Speed Clock & Data Interfaces

On the ZL50110/11/14 series of devices there are four high-speed data interfaces that need consideration when laying out a PCB to ensure correct termination of traces and the reduction of crosstalk noise. The interfaces being:

- External Memory Interface
- GMAC Interfaces
- TDM Interface
- CPU Interface

It is recommended that the outputs are suitably terminated using a series termination through a resistor as close to the output pin as possible. The purpose of the series termination resistor is to reduce reflections on the line. The value of the series termination and the length of trace the output can drive will depend on the driver output impedance, the characteristic impedance of the PCB trace (recommend 50 ohm), the distributed trace capacitance and the load capacitance. As a general rule of thumb, if the trace length is less than 1/6th of the equivalent length of the rise and fall times, then a series termination may not be required.

the equivalent length of rise time = rise time (ps) / delay (ps/mm)

For example:

Typical FR4 board delay = 6.8 ps/mm
Typical rise/fall time for a ZL50110/11/14 output = 2.5 ns

critical track length = (1/6) x (2500/6.8) = 61 mm

Therefore tracks longer than 61 mm will require termination.

As a signal travels along a trace it creates a magnetic field, which induces noise voltages in adjacent traces, this is crosstalk. If the crosstalk is of sufficiently strong amplitude, false data can be induced in the trace and therefore it should be minimised in the layout. The voltage that the external fields cause is proportional to the strength of the field and the length of the trace exposed to the field. Therefore to minimise the effect of crosstalk some basic guidelines should be followed.

First, increase separation of sensitive signals, a rough rule of thumb is that doubling the separation reduces the coupling by a factor of four. Alternatively, shield the victim traces from the aggressor by either routing on another layer separated by a power plane (in a correctly decoupled design the power planes have the same AC potential) or by placing guard traces between the signals usually held ground potential.

Particular effort should be made to minimise crosstalk from ZL50110/11/14 outputs and ensuring fast rise time to these inputs.

In Summary:

- Place series termination resistors as close to the pins as possible
- Minimise output capacitance
- Keep common interface traces close to the same length to avoid skew
- Protect input clocks and signals from crosstalk

13.1.1 External Memory Interface - special considerations during layout

The timing of address, data and control are all related to the system clock which is also used by the external SSRAM to clock these signals. Therefore the propagation delay of the clock to the ZL50110/11/14 and the SSRAM must be matched to within 250 ps, worst case conditions. Trace lengths of theses signals must also be minimized (<100 mm) and matched to ensure correct operation under all conditions.

13.1.2 GMAC Interface - special considerations during layout

The GMII interface passes data to and from the ZL50110/11/14 with their related transmit and receive clocks. It is therefore recommended that the trace lengths for transmit related signals and their clock and the receive related signals and their clock are kept to the same length. By doing this the skew between individual signals and their related clock will be minimized.

13.1.3 TDM Interface - special considerations during layout

Although the data rate of this interface is low the outputs edge speeds share the characteristics of the higher data rate outputs and therefore must be treated with the same care extended to the other interfaces with particular reference to the lower stream numbers which support the higher data rates. The TDM interface has numerous clocking schemes and as a result of this the input clock traces to the ZL50110/11/14 devices should be treated with care.

13.1.4 Summary

Particular effort should be made to minimise crosstalk from ZL50110/11/14 outputs and ensuring fast rise time to these inputs.

In Summary:

- Place series termination resistors as close to the pins as possible
- Minimise output capacitance
- Keep common interface traces close to the same length to avoid skew
- Protect input clocks and signals from crosstalk

13.2 CPU TA Output

The CPU_TA output signal from the ZL50110/11/14 is a critical handshake signal to the CPU that ensures the correct completion of a bus transaction between the two devices. As the signal is critical, it is recommend that the circuit shown in Figure 49 is implemented in systems operating above 40 MHz bus frequency to ensure robust operation under all conditions.

The following external logic is required to implement the circuit:

- 74LCX74 dual D-type flip-flop (one section of two)
- 74LCX08 quad AND gate (one section of four)
- 74LCX125 quad tri-state buffer (one section of four)
- 4K7 resistor x2

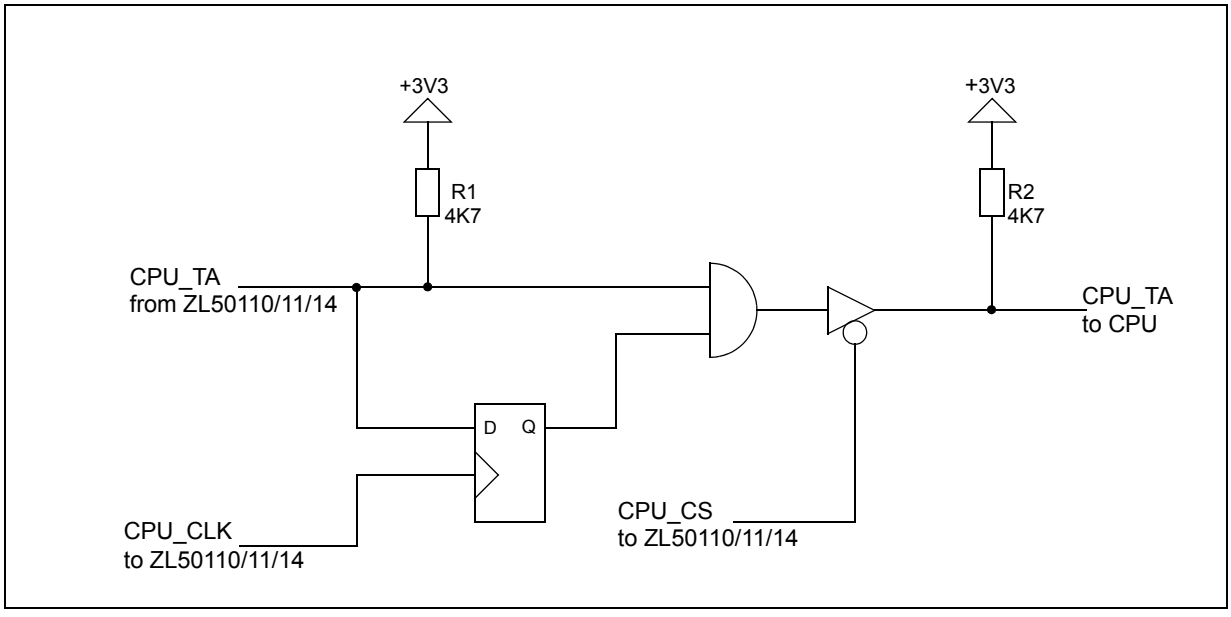


Figure 49 - CPU_TA Board Circuit

The function of the circuit is to extend the TA signal, to ensure the CPU correctly registers it. Resistor R2 must be fitted to ensure correct operation of the TA input to the processor. It is recommended that the logic is fitted close to the ZL50110/11/14 and that the clock to the 74LCX74 is derived from the same clock source as that input to the ZL50110/11/14.

13.3 Mx_LINKUP_LED Outputs

The ZL50111 and ZL50110/1/4 have different Mx_LINKUP_LED pin assignments as shown in Table 42.

Signal	ZL50111 Pin	ZL50110/4 Pin
M0_LINKUP_LED	AB23	G24
M1_LINKUP_LED	F26	G23
M2_LINKUP_LED	G23	NC
M3_LINKUP_LED	G24	NC

Table 42 - Mx_LINKUP_LED Pin Assignments

To generate a pin for pin compatible PCB for all three variants, the following stuffing options may be used as shown in Figure 50. For the ZL50111 variant, resistors R4 and R6 are not populated. For the ZL50110 and ZL50114 variants, resistors R1, R2, R3 and R5 as well as LEDs for M2 and M3 are not populated.

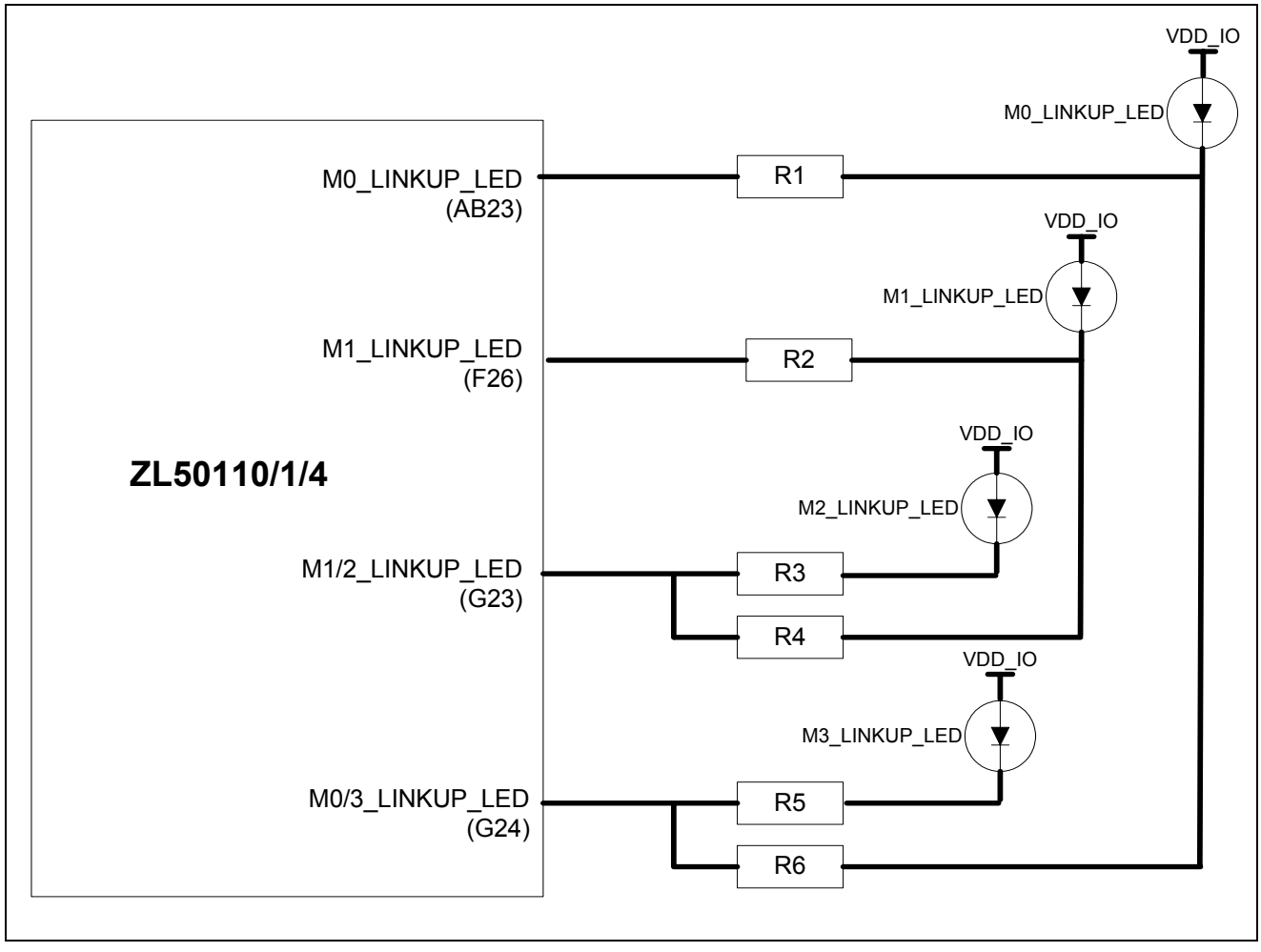


Figure 50 - Mx_LINKUP_LED Stuffing Option

Table 43 lists the various components that are used for each variant.

Component	ZL50111	ZL50110/4
R1	√	-
R2	√	-
R3	√	-
R4	-	√
R5	√	-
R6	-	√
M0 LED	√	√
M1 LED	√	√
M2 LED	√	-
M3 LED	√	-

Table 43 - Mx_LINKUP_LED Stuffing Option

14.0 Reference Documents

14.1 External Standards/Specifications

- IEEE Standard 1149.1-2001; Test Access Port and Boundary Scan Architecture
- IEEE Standard 802.3-2000; Local and Metropolitan Networks CSMA/CD Access Method and Physical Layer
- ECTF H.110 Revision 1.0; Hardware Compatibility Specification
- H-MVIP (GO-MVIP) Standard Release 1.1a; Multi-Vendor Integration Protocol
- MPC8260AEC/D Revision 0.7; Motorola MPC8260 Family Hardware Specification
- RFC 768; UDP
- RFC 791; IPv4
- RFC2460; IPv6
- RFC 1889; RTP
- RFC 2661; L2TP
- RFC 1213; MIB II
- RFC 1757; Remote Network Monitoring MIB (for SMIv1)
- RFC 2819; Remote Network Monitoring MIB (for SMIv2)
- RFC 2863; Interfaces Group MIB
- CCITT G.712; TDM Timing Specification (Method 2)
- G.823; Control of Jitter/Wander with digital networks based on the 2.048 Mbps hierarchy
- G.824; Control of Jitter/Wander with digital networks based on the 1.544 Mbps hierarchy
- ANSI T1.101 Stratum 3/4
- Telcordia GR-1244-CORE Stratum 3/4/4e
- IETF PWE3 draft-ietf-l2tpext-l2tp-base
- IETF PWE3 draft-ietf-pwe3-cesopsn
- IETF PWE3 draft-ietf-pwe3-satop
- ITU-T Y.1413 TDM-MPLS Network Interworking
- *Optional Packet Memory Device* - Micron MT55L128L32P1 8 Mb ZBT-SRAM

14.2 Zarlink Standards

- MSAN-126 Revision B, Issue 4; ST-BUS Generic Device Specification

15.0 Glossary

API Application Program Interface

ATM Asynchronous Transfer Mode

CDP Context Descriptor Protocol (the protocol used by Zarlink's MT9088x family of TDM-Packet devices)

CESoP Circuit Emulation Services over Packet

CESoPSN Circuit Emulation Services over Packet Switched Networks (draft-ietf-pwe3-cesopsn)

CONTEXT A programmed connection of a number of TDM timeslots assembled into a unique packet stream.

CPU Central Processing Unit

DMA Direct Memory Access

DPLL Digital Phase Locked Loop

DSP Digital Signal Processor

GMII Gigabit Media Independent Interface

H.100/H.110 High capacity TDM backplane standards

H-MVIP High-performance Multi-Vendor Integration Protocol (a TDM bus standard)

IA Implementation Agreement

IETF Internet Engineering Task Force

IP Internet Protocol (version 4, RFC 791, version 6, RFC 2460)

JTAG Joint Test Algorithms Group (generally used to refer to a standard way of providing a board-level test facility)

L2TP Layer 2 Tunneling Protocol (RFC 2661)

LAN Local Area Network

LIU Line Interface Unit

MAC Media Access Control

MEF Metro Ethernet Forum

MFA MPLS and Frame Relay Alliance

MII Media Independent Interface

MIB Management Information Base

MPLS Multi Protocol Label Switching

MTIE Maximum Time Interval Error

MVIP Multi-Vendor Integration Protocol (a TDM bus standard)

OC3 Optical Carrier 3 - 155.52 Mbps leased line

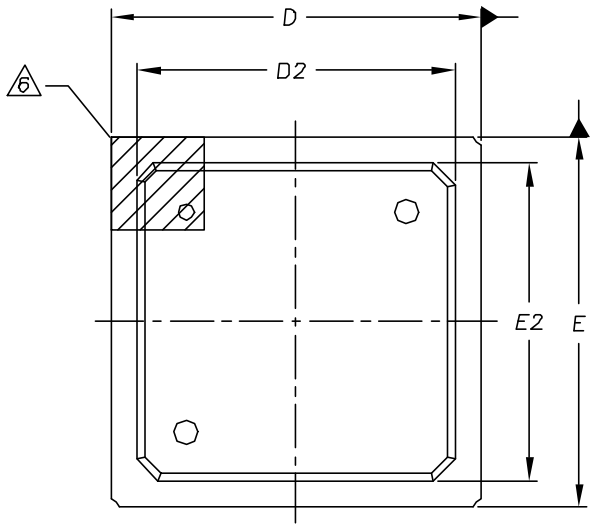
PDH Plesiochronous Digital Hierarchy

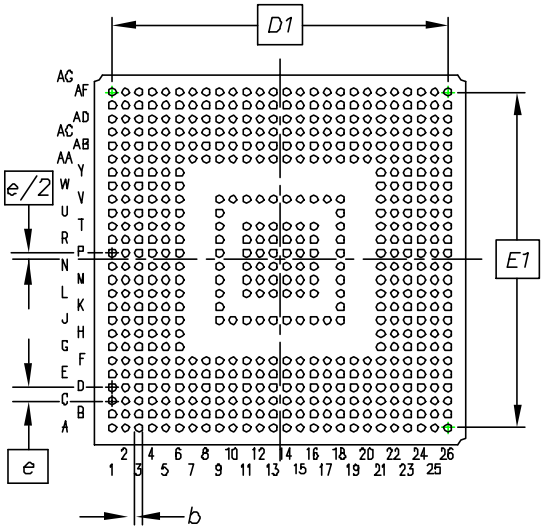
PLL Phase Locked Loop

PRS Primary Reference Source

PRX Packet Receive

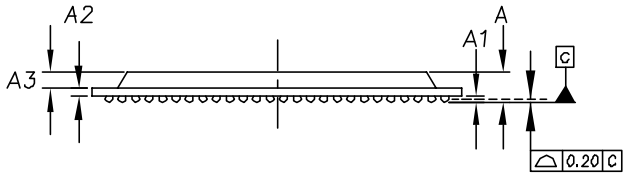
PSTN	Public Switched Telephone Circuit
PTX	Packet Transmit
PWE3	Pseudo-Wire Emulation Edge to Edge (a working group of the IETF)
QOS	Quality of Service
RTP	Real Time Protocol (RFC 1889)
PE	Protocol Engine
SAToP	Structure-Agnostic Transport over Packet
SSRAM	Synchronous Static Random Access Memory
ST BUS	Standard Telecom Bus, a standard interface for TDM data streams
TDL	Tapped Delay Line
TDM	Time Division Multiplexing
UDP	User Datagram Protocol (RFC 768)
UI	Unit Interval
VLAN	Virtual Local Area Network
WFQ	Weighted Fair Queuing
ZBT	Zero Bus Turnaround, a type of synchronous SRAM





SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.13	2.33	2.53	.084	.092	.100
A1	0.50	0.60	0.70	.020	.024	.028
A2	0.51	0.56	0.61	.020	.022	.024
A3	1.12	1.17	1.22	.044	.046	.048
b	0.60	0.75	0.90	.024	.030	.035
D	34.80	35.00	35.20	1.370	1.378	1.386
D1	31.75 BSC			1.250 BSC		
D2	29.90	30.00	30.10	1.177	1.181	1.185
E	34.80	35.00	35.20	1.370	1.378	1.386
E1	31.75 BSC			1.250 BSC		
E2	29.90	30.00	30.10	1.177	1.181	1.185
e	1.27 BSC			.050 BSC		

Confirms to JEDEC MS-034
BAR-2 iss. A



NOTE:
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSION 'b' IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER
3. PRIMARY DATUM -C- AND SEATING PLANE
   ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. NOT TO SCALE.
6. DETAILS OF A1 CORNER ARE OPTIONAL, AND MAY CONSIST OF INK DOT, LASER MARK OR METALISED MARKING, BUT MUST BE LOCATED WITHIN ZONE INDICATED.

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APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

BP

Package Code GA

Package Outline Drawing for 552 PBGA (35x35)mm, 1.27mm pitch

GPD00809



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