DG411/883, DG412/883 DG413/883

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August 2003

olithic Quad SPST CMOS Analog Switches

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **ON-Resistance <35Ω Max**
- **Low Power Consumption (P_D <35μW)**
- **Fast Switching Action**
  - **t_{ON} <175ns**
  - **t_{OFF} <145ns**
- **Low Charge Injection**
- **Upgrade from DG211/DG212**
- **TTL, CMOS Compatible**
- **Single or Split Supply Operation**

Applications

- **Audio Switching**
- **Battery Operated Systems**
- **Data Acquisition**
- **Hi-Rel Systems**
- **Sample and Hold Circuits**
- **Communication Systems**
- **Automatic Test Equipment**

Part Number Information

PART NUMBER	TEMP. RANGE	PACKAGE
DG411AK/883	-55°C to +125°C	16 Lead CerDIP
DG412AK/883	-55°C to +125°C	16 Lead CerDIP
DG413AK/883	-55°C to +125°C	16 Lead CerDIP

Description

The DG411/883 series monolithic CMOS analog switches are drop-in replacements for the popular DG211 and DG212 series devices. They include four independent single pole throw (SPST) analog switches, and TTL and CMOS compatible digital inputs.

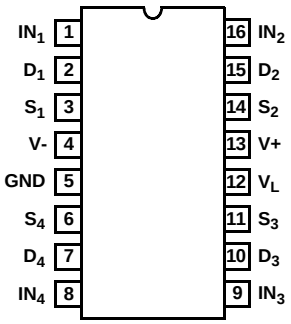
These switches feature lower analog ON resistance (<35Ω) and faster switch time (t_{ON} <175ns) compared to the DG211 or DG212. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG411/883 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling $40V_{P-P}$ signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±20V.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±15V analog input range. The switches in the DG411/883 and DG412/883 are identical, differing only in the polarity of the selection logic. Two of the switches in the DG413/883 (#1 and #4) use the logic of the DG211 and DG411/883 (i.e. a logic "0" turns the switch ON) and the other two switches use DG212 and DG412/883 positive logic. This permits independent control of turn-on and turn-off times for SPDT configurations, permitting "break-before-make" or "make-before-break" operation with a minimum of external logic.

Pinout

DG411/883, DG412/883, DG413/883 (CERDIP)
TOP VIEW

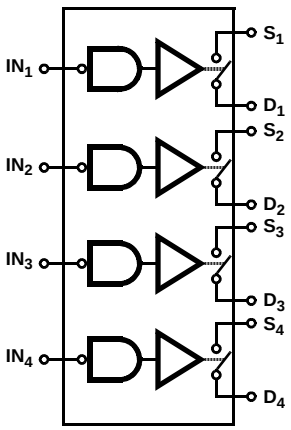


(NC) NO CONNECTION

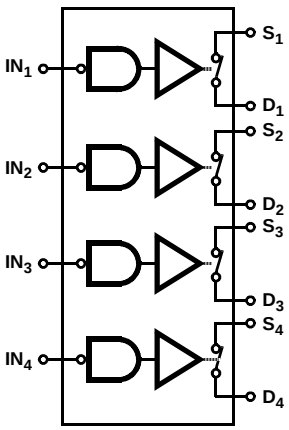
Functional Diagrams

Four SPST Switches per Package Switches Shown for Logic "1" Input

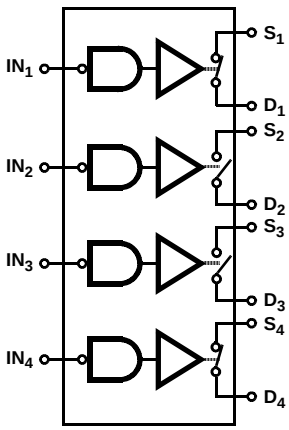
DG411/883



DG412/883



DG413/883



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Spec Number **512043**
File Number **3681.1**

Pin Description

PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic Control for Switch 1
2	D_1	Drain (Output) Terminal for Switch 1
3	S_1	Source (Input) Terminal for Switch 1
4	V-	Negative Power Supply Terminal
5	GND	Ground Terminal (Logic Common)
6	S_4	Source (Input) Terminal for Switch 4
7	D_4	Drain (Output) Terminal for Switch 4
8	IN_4	Logic Control for Switch 4
9	IN_3	Logic Control for Switch 3
10	D_3	Drain (Output) Terminal for Switch 3
11	S_3	Source (Input) Terminal for Switch 3
12	V_L	Logic Reference Voltage
13	V+	Positive Power Supply Terminal (Substrate)
14	S_2	Source (Input) Terminal for Switch 2
15	D_2	Drain (Output) Terminal for Switch 2
16	IN_2	Logic Control for Switch 2

TRUTH TABLE

	DG411/883	DG412/883	DG413/883	
LOGIC	SWITCH	SWITCH	SWITCH 1, 4	SWITCH 2, 3
0	ON	OFF	OFF	ON
1	OFF	ON	ON	OFF

NOTE: Logic “0” ≤0.8V. Logic “1” ≥2.4V.

Absolute Maximum Ratings

V+ to V- 44V
GND to V- 25V
V_L (Note 2) . . . . . (GND -0.3V) to (V+) +0.3V
Digital Inputs, V_S, V_D (Note 2) . . . . . (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Current, S or D (Pulsed 1ms, 10% Duty Cycle) 100mA
Storage Temperature Range (A Suffix) . . . . . -65^oC to $+125^oC$
Lead Temperature (Soldering 10s) . . . . . $+300^oC$

Thermal Information

Thermal Resistance (Note 3)	θ_{JA}	θ_{JC}
CerDIP Package	$75^oC/W$	$20^oC/W$

Junction Temperature . . . . . $+175^oC$
Operating Temperature (A Suffix) . . . . . -55^oC to $+125^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . ±20V Max
Operating Temperature Range . . . . . -55^oC to $+125^oC$
Input Low Voltage . . . . . 0.8V Max
Input High Voltage . . . . . 2.4V Min
Input Rise and Fall Time . . . . . ≤20ns

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V+ = +15V, V- = -15V, V_L = 5V, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS		GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Drain-to-Source ON Resistance	$R_{DS(ON)}$	V+ = +13.5V, V- = -13.5V, I_S = -10mA, V_D = ±8.5V	V_{IN} = 0.8V	1, 3	$+25^oC$, -55^oC	0	35	Ω
DG411/883				2	$+125^oC$	0	45	Ω
DG412/883			V_{IN} = 2.4V	1, 3	$+25^oC$, -55^oC	0	35	Ω
				2	$+125^oC$	0	45	Ω
DG413/883			V_{IN} = 0.8V or 2.4V (Note 1)	1, 3	$+25^oC$, -55^oC	0	35	Ω
				2	$+125^oC$	0	45	Ω
DG411/883		V+ = +10.8V, V- = -0V, I_S = -10mA, V_D = 3.0V and 8.0V	V_{IN} = 0.8V	1, 3	$+25^oC$, -55^oC	0	80	Ω
				2	$+125^oC$	0	100	Ω
DG412/883			V_{IN} = 2.4V	1, 3	$+25^oC$, -55^oC	0	80	Ω
				2	$+125^oC$	0	100	Ω
DG413/883			V_{IN} = 0.8V or 2.4V (Note 1)	1, 3	$+25^oC$, -55^oC	0	80	Ω
				2	$+125^oC$	0	100	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = -15.5V, V_S = 15.5V	V_{IN} = 2.4V	1	$+25^oC$	-0.25	+0.25	nA
DG411/883				2, 3	$+125^oC$, -55^oC	-20	+20	nA
DG412/883			V_{IN} = 0.8V	1	$+25^oC$	-0.25	+0.25	nA
				2, 3	$+125^oC$, -55^oC	-20	+20	nA
DG413/883			V_{IN} = 0.8V or 2.4V (Note 1)	1	$+25^oC$	-0.25	+0.25	nA
				2, 3	$+125^oC$, -55^oC	-20	+20	nA
DG411/883		V+ = 16.5V, V- = -16.5V, V_D = 15.5V, V_S = -15.5V	V_{IN} = 2.4V	1	$+25^oC$	-0.25	+0.25	nA
				2, 3	$+125^oC$, -55^oC	-20	+20	nA
DG412/883			V_{IN} = 0.8V	1	$+25^oC$	-0.25	+0.25	nA
				2, 3	$+125^oC$, -55^oC	-20	+20	nA
DG413/883			V_{IN} = 0.8V or 2.4V (Note 1)	1	$+25^oC$	-0.25	+0.25	nA
				2, 3	$+125^oC$, -55^oC	-20	+20	nA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V+ = +15V, V- = -15V, V_L = 5V, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS		GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Drain OFF Leakage Current	$I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = -15.5V, V_S = 15.5V	V_{IN} = 2.4V	1	+25°C	-0.25	+0.25	nA
DG411/883				2, 3	+125°C, -55°C	-20	+20	nA
DG412/883			V_{IN} = 0.8V	1	+25°C	-0.25	+0.25	nA
				2, 3	+125°C, -55°C	-20	+20	nA
DG413/883			V_{IN} = 0.8V or 2.4V (Note 1)	1	+25°C	-0.25	+0.25	nA
				2, 3	+125°C, -55°C	-20	+20	nA
DG411/883		V+ = 16.5V, V- = -16.5V, V_D = 15.5V, V_S = -15.5V	V_{IN} = 2.4V	1	+25°C	-0.25	+0.25	nA
				2, 3	+125°C, -55°C	-20	+20	nA
DG412/883			V_{IN} = 0.8V	1	+25°C	-0.25	+0.25	nA
				2, 3	+125°C, -55°C	-20	+20	nA
DG413/883			V_{IN} = 0.8V or 2.4V (Note 1)	1	+25°C	-0.25	+0.25	nA
				2, 3	+125°C, -55°C	-20	+20	nA
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, V_S = V_D = ±15.5V	V_{IN} = 0.8V	1	+25°C	-0.4	+0.4	nA
DG411/883				2, 3	+125°C, -55°C	-40	+40	nA
DG412/883			V_{IN} = 2.4V	1	+25°C	-0.4	+0.4	nA
				2, 3	+125°C, -55°C	-40	+40	nA
DG413/883			V_{IN} = 0.8V or 2.4V (Note 1)	1	+25°C	-0.4	+0.4	nA
				2, 3	+125°C, -55°C	-40	+40	nA
Input Current with V_{IN} Low	I_{IL}	Input Under Test = 0.8V, All Others = 2.4V		1, 2, 3	+25°C, +125°C, -55°C	-0.5	+0.5	µA
Input Current with V_{IN} High	I_{IH}	Input Under Test = 2.4V, All Others = 0.8V		1, 2, 3	+25°C, +125°C, -55°C	-0.5	+0.5	µA
Positive Supply Current	I+	V+ = 16.5V, V- = -16.5, V_{IN} = 0Vor 5.0V		1	+25°C	-	+1.0	µA
				2, 3	+125°C, -55°C	-	+5.0	µA
		V+ = 13.2V, V- = 0V, V_{IN} = 0Vor 5.0V V_L = 5.25V		1	+25°C	-	+1.0	µA
				2, 3	+125°C, -55°C	-	+5.0	µA
Negative Supply Current	I-	V+ = 16.5V, V- = -16.5, V_{IN} = 0V or 5.0V		1	+25°C	-1.0	-	µA
				2, 3	+125°C, -55°C	-5.0	-	µA
		V+ = 13.2V, V- = 0V, V_{IN} = 0V or 5.0V V_L = 5.25V		1	+25°C	-1.0	-	µA
				2, 3	+125°C, -55°C	-5.0	-	µA
Logic Supply Current	I_L	V+ = 16.5V, V- = -16.5, V_{IN} = 0V or 5.0V		1	+25°C	-	+1.0	µA
				2, 3	+125°C, -55°C	-	+5.0	µA
		V+ = 13.2V, V- = 0V, V_{IN} = 0V or 5.0V V_L = 5.25V		1	+25°C	-	+1.0	µA
				2, 3	+125°C, -55°C	-	+5.0	µA
Ground Current	I_{GND}	V+ = 16.5V, V- = -16.5, V_{IN} = 0V or 5.0V		1	+25°C	-1.0	-	µA
				2, 3	+125°C, -55°C	-5.0	-	µA
		V+ = 13.2V, V- = 0V, V_{IN} = 0V or 5.0V V_L = 5.25V		1	+25°C	-1.0	-	µA
				2, 3	+125°C, -55°C	-5.0	-	µA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V+ = +15V, V- = -15V, V_L = 5V, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn ON Time	t_{ON}	C_L = 35pF, V_S = ±10V, R_L = 300Ω	9, 11	+25°C, -55°C	0	175	ns
			10	+125°C	0	240	ns
		V+ = 12V, V- = 0V, C_L = 35pF, V_S = +8V, R_L = 300Ω	9, 11	+25°C, -55°C	0	250	ns
			10	+125°C	0	400	ns
Turn OFF Time	t_{OFF}	C_L = 35pF, V_S = ±10V, R_L = 300Ω	9, 11	+25°C, -55°C	0	145	ns
			10	+125°C	0	160	ns
		V+ = 12V, V- = 0V, C_L = 35pF, V_S = +8V, R_L = 300Ω	9, 11	+25°C, -55°C	0	125	ns
			10	+125°C	0	140	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Tested at: V+ = +15V, V- = -15V, V_L = 5V, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Charge Injection	Q	See Figure 2, V_G = 0V, R_G = 0Ω, T_A = +25°C, C_L = 10nF	9	+25°C	-100	+100	pC
				+25°C			pC
		See Figure 2, V_G = 6V, R_G = 0Ω, T_A = +25°C C_L = 10nF, V+ = 12V, V- = 0V	9	+25°C	-100	+100	pC
				+25°C			pC

NOTES:

1. V_{IN} = Input Voltage to Perform Proper Function.
2. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. All leads soldered or welded to PC board.
4. Parameters listed in Table 3 are controlled via design or process and are not directly tested at final production. These parameters are lab characterized upon initial design release or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:
2760µm x 1780µm x 485 ± 25µm

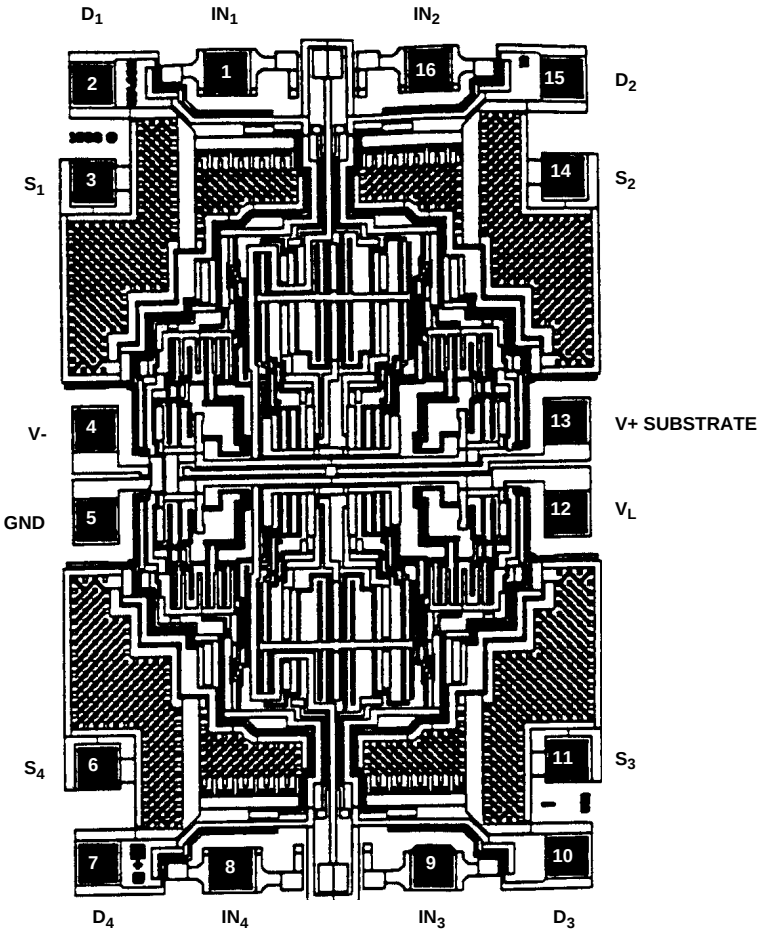
METALLIZATION:
Type: SiAl
Thickness: 12kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
$1.5 \times 10^5 A/cm^2$

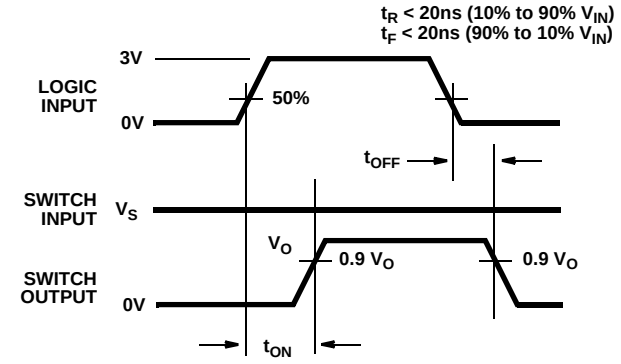
Metallization Mask Layout

DG411/883, DG412/883, DG413/883



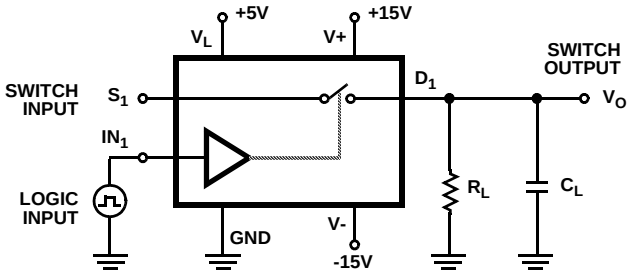
Test Circuits

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A.



Repeat test for all IN and S.
For load conditions, see Specifications C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + R_{DS(ON)}}$$

FIGURE 1B.

FIGURE 1. SWITCHING TIME

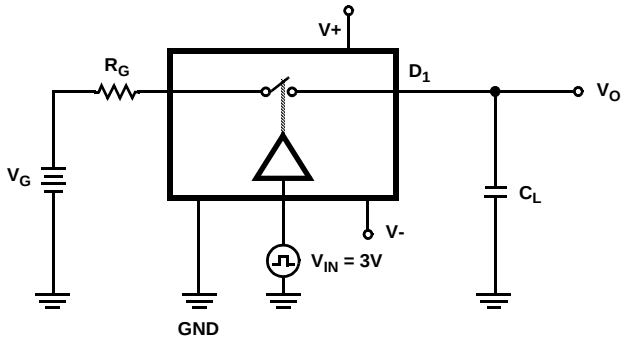
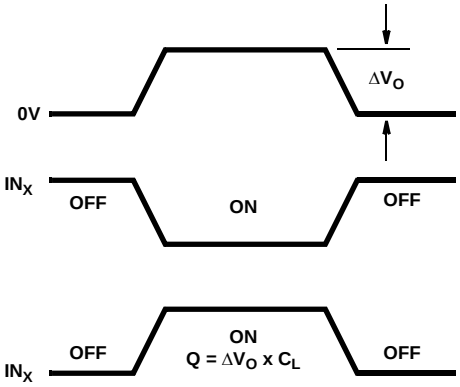


FIGURE 2A.



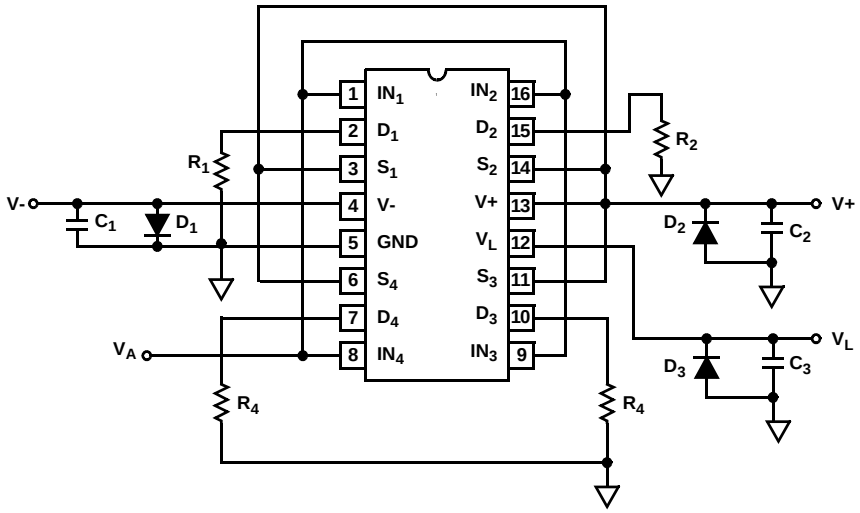
IN_X dependent on switch configuration input polarity determined by sense of switch.

FIGURE 2B.

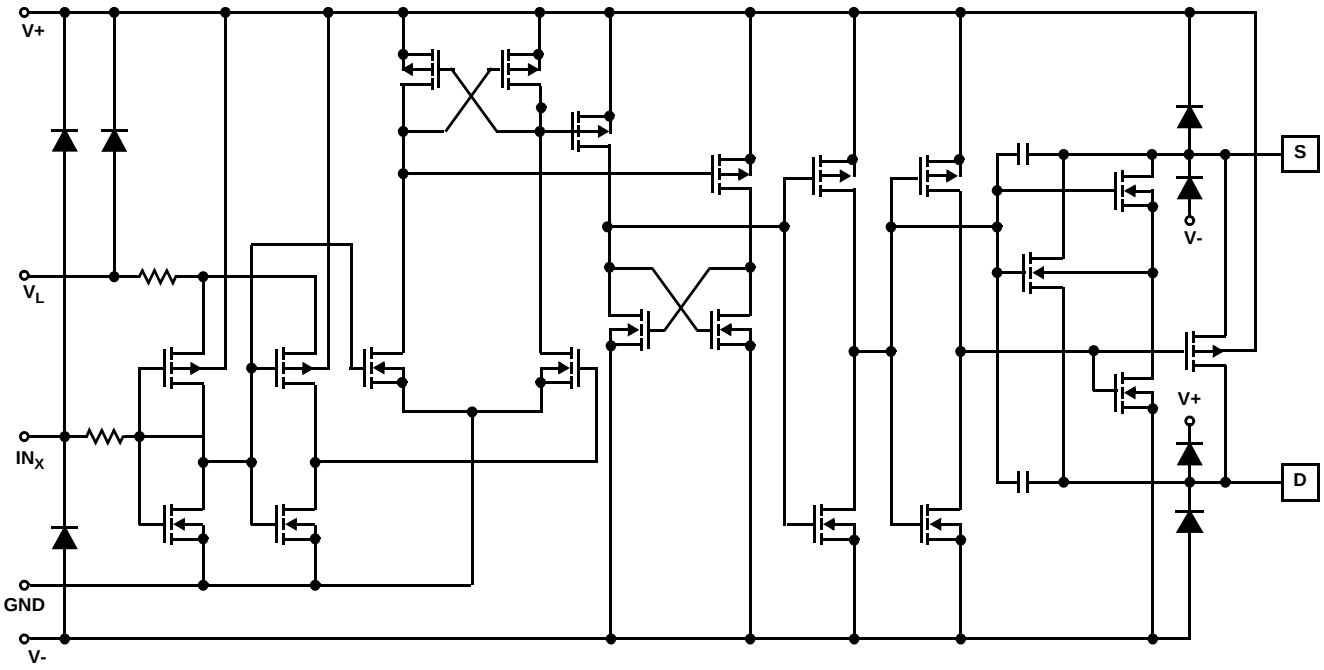
FIGURE 2. CHARGE INJECTION

Burn-In Circuit

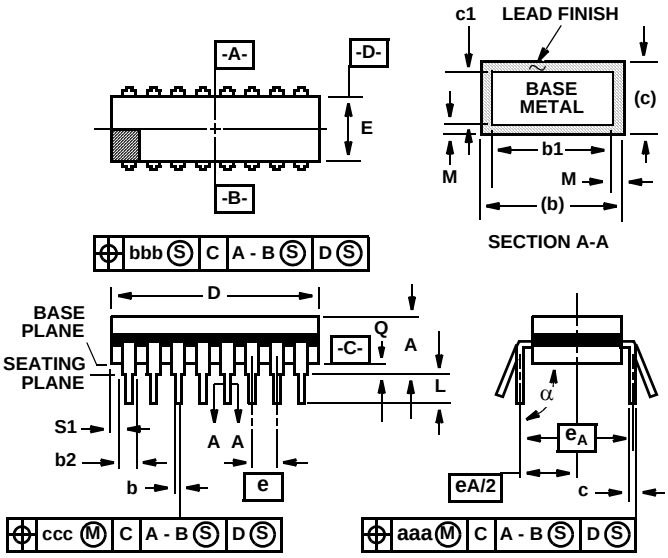
DG411/883, DG412/883, DG413/883 CERAMIC DIP



Typical Schematic Diagram (Typical Channel)



Ceramic Dual-In-Line Frit Seal Packages (CerDIP)



F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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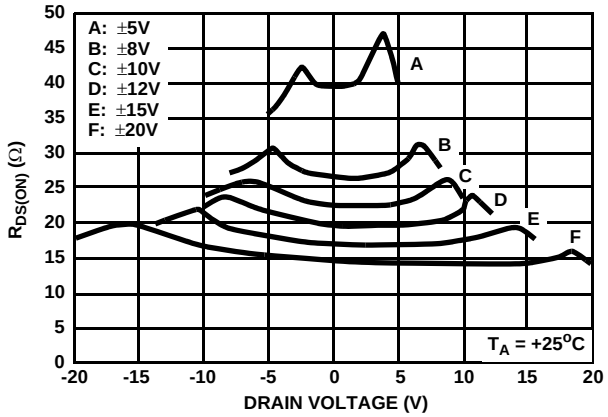
DESIGN INFORMATION

Monolithic Quad SPST CMOS Analog Switches

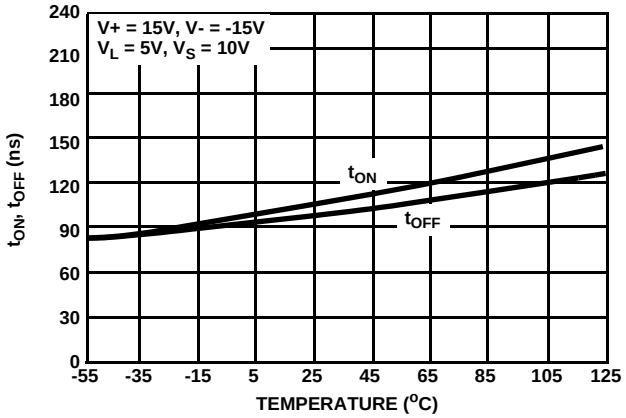
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Typical Performance Curves

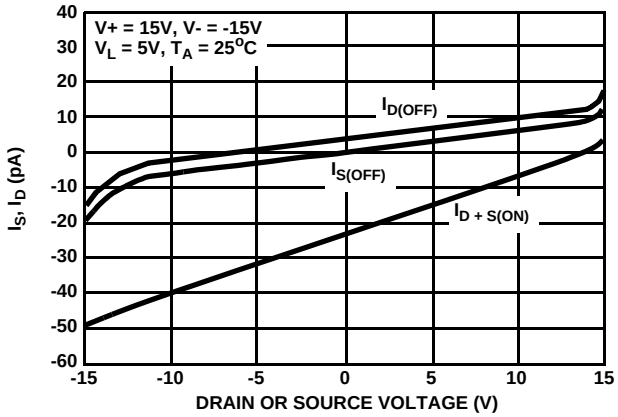
ON-RESISTANCE vs V_D AND POWER SUPPLY VOLTAGE



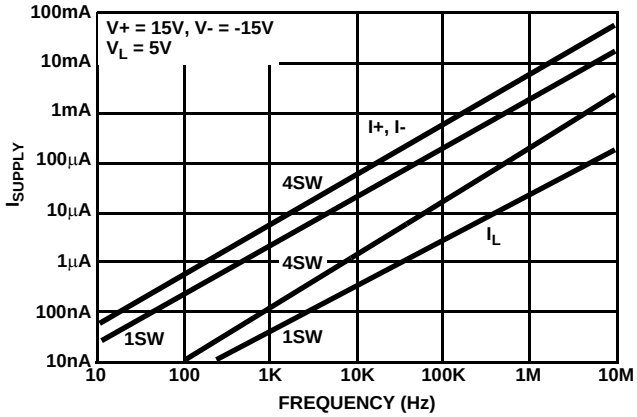
SWITCHING TIME vs TEMPERATURE



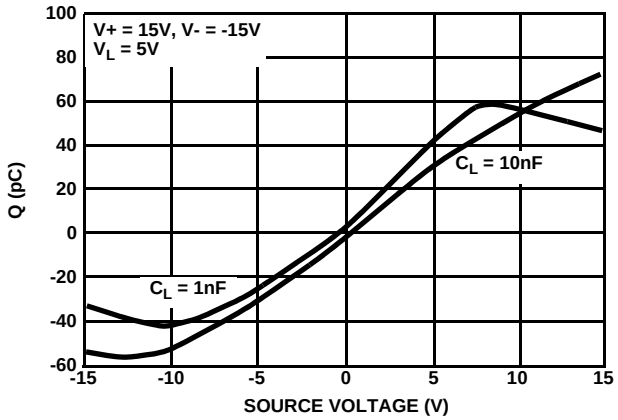
LEAKAGE CURRENT vs ANALOG VOLTAGE



SUPPLY CURRENT vs INPUT SWITCHING FREQUENCY



CHARGE INJECTION vs ANALOG VOLTAGE (V_D)



CHARGE INJECTION vs ANALOG VOLTAGE (V_S)

