TLC34076, TLC34076M
Data Manual

Video Interface Palette

SLAS054A
October 1997

TEXAS INSTRUMENTS

Printed on Recycled Paper

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Section	Title	Page
1	**Introduction**	**1–1**
1.1	Features	1–1
1.2	Functional Block Diagram	1–3
1.3	Terminal Assignments	1–4
1.4	Ordering Information	1–7
1.5	Terminal Functions (TLC34076C and TLC34076M)	1–8
2	**Detailed Description**	**2–1**
2.1	Microprocessor Unit (MPU) Interface	2–1
2.2	Color Palette RAM	2–1
2.2.1	Writing to the Color Palette RAM	2–2
2.2.2	Reading From the Color Palette RAM	2–2
2.2.3	Palette Page Register	2–2
2.3	Input/Output Clock Selection and Generation	2–2
2.3.1	SCLK	2–5
2.3.2	VCLK	2–6
2.4	Multiplexing Scheme	2–8
2.4.1	VGA Pass-Through Mode	2–11
2.4.2	Multiplexing Modes	2–12
2.4.3	Special Nibble Mode	2–12
2.4.4	True-Color Modes	2–12
2.4.5	Multiplex Control Register	2–15
2.4.6	Read Masking	2–16
2.5	Reset	2–16
2.5.1	Power-On Reset	2–16
2.5.2	Hardware Reset	2–16
2.5.3	Software Reset	2–16
2.5.4	VGA Pass-Through Mode Default Conditions	2–17
2.6	Analog Output Specifications	2–17
2.7	Frame-Buffer Interface with Little-Endian and Big-Endian Modes	2–19
2.8	HSYNC, VSYNC, and BLANK	2–19
2.9	Split Shift Register Transfer VRAMs and Special Nibble Mode	2–20
2.9.1	Split Shift Register Transfer VRAMs	2–20
2.9.2	Special Nibble Mode	2–21
2.10	MUXOUT Output	2–23
2.11	General Control Register	2–23
2.11.1	HSYNCOUT and VSYNCOUT (Bits 0 and 1)	2–23
2.11.2	Split Shift Register Transfer Enable (SSRT) and Special Nibble Mode Enable (SNM) (Bits 2 and 3)	2–23
2.11.3	Pedestal Enable Control (Bit 4)	2–23
2.11.4	Sync Enable Control (Bit 5)	2–24

2.11.5 Little-Endian and Big-Endian Mode Control (Bit 6) 2–24
2.11.6 MUXOUT (Bit 7) 2–24
2.12 Test Register 2–24
2.12.1 Frame-Buffer Data Flow Test 2–25
2.12. Identification (ID) Code 2–25
2.12.3 Ones-Accumulation Screen Integrity Test 2–25
2.12.4 Analog Test 2–26

3 Electrical Specifications 3–1
3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)† 3–1
3.2 Recommended Operating Conditions 3–1
3.3 Electrical Characteristics 3–2
3.3.1 Electrical Characteristics for TLC34076C Over Operating Free-Air Temperature Range 3–2
3.3.2 Electrical Characteristics for TLC34076M Over Operating Free-Air Temperature Range 3–3
3.4 Operating Characteristics 3–4
3.4.1 Operating Characteristics for TLC34076C Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature 3–4
3.4.2 Operating Characteristics for TLC34076M Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature 3–5
3.5 Timing Requirements 3–6
3.5.1 Timing Requirements for TLC34076C Over Recommended Ranges of Supply Voltages and Operating Temperature 3–6
3.5.2 Timing Requirements for TLC34076M Over Recommended Ranges of Supply Voltages and Operating Temperature 3–8
3.6 Switching Characteristics for TLC34076C and TLC34076M Over Recommended Ranges of Supply Voltages and Operating Temperature 3–9
3.7 Timing Diagrams 3–12

Appendix A SCLK/VCLK and the TMS340x0 . . . . . A–1

Appendix B Printed Circuit Board Layout Considerations B–1

Appendix C SCLK Frequency < VCLK Frequency C–1

Appendix D Mechanical Data D–1

List of Illustrations

Figure *Title* *Page*

2–1 DOTCLK/VCLK/SCLK Relationship 2–4
2–2 SCLK/VCLK Control Timing (SSRT Disabled, SCLK Frequency = VCLK Frequency) 2–6
2–3 SCLK/VCLK Control Timing (SSRT Enabled, SCLK Frequency = VCLK Frequency) 2–7
2–4 SCLK/VCLK Control Timing (SSRT Disabled, SCLK Frequency = 4 y VCLK Frequency) 2–7
2–5 SCLK/VCLK Control Timing (SSRT Enabled, SCLK Frequency = 4 y VCLK Frequency) 2–8
2–6 Equivalent Circuit of the IOG Current Output 2–17
2–7 7.5-IRE, 8-Bit Composite Video Output 2–18
2–8 0-IRE, 8-Bit Composite Video Output 2–18
2–9 Relationship Between SFLAG/NFLAG, BLANK, and SCLK 2–20
2–10 SFLAG/NFLAG Timing in Special Nibble Mode 2–22
2–11 Test-Register Control-Word State Diagrams 2–25
2–12 Internal Comparator Circuitry for Analog Test 2–27
3–1 MPU Interface Timing 3–12
3–2 Video Input/Output Timing 3–13
3–3 SFLAG/NFLAG Timing (When SSRT Function is Enabled) 3–13

List of Tables

Table	*Title*	*Page*
2–1	Internal Register Map	2–1
2–2	Allocation of Palette Page Register Bits	2–2
2–3	Input Clock Selection Register Format	2–3
2–4	Output Clock Selection Register Format	2–3
2–5	VCLK/SCLK Divide Ratio Selection (Output Clock Selection Register Value in Hex)	2–4
2–6	Mode and Bus Width Selection	2–9
2–7	True-Color Modes	2–13
2–8	True-Color Bit Definitions	2–14
2–9	VGA Pass-Through Mode Default Conditions	2–17
2–10	Pixel Data Distribution in Special Nibble Mode	2–21
2–11	General Control Register Bit Functions	2–23
2–12	Test Mode Selection	2–24
2–13	Test Register Bit Definitions for Analog Test	2–26
2–14	Bit Coding for Analog Comparisons of Bits D7 – D4	2–26

1 Introduction

The TLC34076C and TLC34076M are commercial and military versions, respectively, of a Texas Instruments video interface palette (VIP) designed for lower system cost with a higher level of integration. Lower system cost and higher integration are achieved by incorporating all the high-speed timing, synchronizing, and multiplexing logic usually associated with graphics systems into one device, thus greatly reducing chip count. Since all high-speed signals (excluding the clock source) are contained on-chip, RF noise considerations are simplified. Maximum flexibility is provided through the pixel multiplexing scheme, which allows for 32-, 16-, 8-, and 4-bit pixel buses to be accommodated without any circuit modification. This enables the system to be easily reconfigured for varying amounts of available video RAM (VRAM). Data can be split into 1, 2, 4, or 8 bit-planes. The TLC34076 is software-compatible with the IMSG176/8 and Brooktree™ BT476/8 color palettes.

The TLC34076 VIP is pin-for-pin compatible with the TLC34075 VIP, but contains additional 24- and 16-bit true-color modes, as well as the ability to select little-endian or big-endian data formats for the pixel bus frame buffer interface.

The TLC34076 features a separate VGA bus that allows data from the feature connector of most VGA-supported personal computers to be fed directly into the palette without the need for external data multiplexing. This allows a replacement graphics board to remain downward compatible by utilizing the existing graphics circuitry often located on the motherboard.

The 24- and 16-bit true-color modes that are provided allow bits of color information to be transferred directly from the pixel port to the digital-to-analog converters (DACs). Depending on which true-color mode is selected, an overlay function is provided using the remaining bits of the pixel bus. The 24-bit modes allow overlay with the eight remaining bits of the pixel bus, while the TARGA™ (5-5-5) 16-bit mode allows overlay with the one remaining bit of the divided pixel bus.

The TLC34076 has a 256-by-24 color lookup table with triple 8-bit video D/A converters capable of directly driving a doubly terminated 75-Ω line. Sync generation is incorporated on the green output channel. HSYNC and VSYNC are fed through the device and optionally inverted to indicate screen resolution to the monitor. A palette page register provides the additional bits of palette address when 1, 2, or 4 bit-planes are used. This allows the screen colors to be changed with only one MPU write cycle.

Clocking is provided through one of four or five inputs (three TTL compatible and either one ECL compatible or two TTL compatible) and is software selectable. The video and shift clock outputs provide a software-selected divide ratio of the chosen clock input.

The TLC34076 can be connected directly to the serial port of VRAM devices, eliminating the need for any discrete logic. Support for split shift register transfers is also provided.

1.1 Features

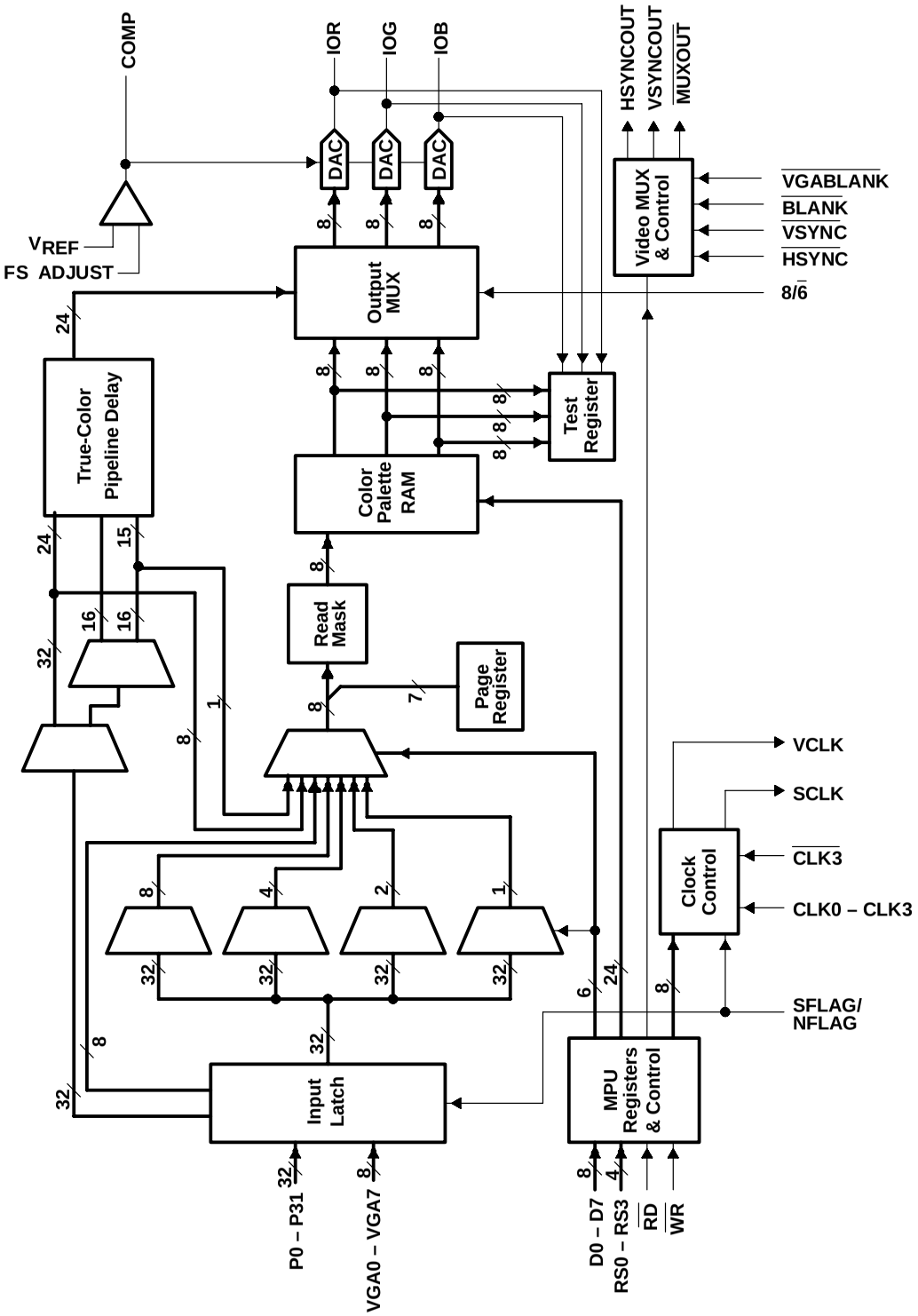
- Versatile Multiplexing Interface to Allow Lower Pixel Bus Rate
- High Level of Integration to Provide Lower System Cost and Complexity
- Direct VGA Pass-Through Capability
- Versatile Pixel Bus Interface to Support Little-Endian and Big-Endian Data Formats
- True-Color (direct-addressing) Mode to Support Various 24-Bit and 16-Bit Formats
- Compatible with 5-6-5 XGA Format
- Compatible with 5-5-5 TARGA Format
- Interfaces Directly to TMS34010/TMS34020 and Other Graphics Processors
- Triple 8-bit D/A Converters

Brooktree is a trademark of the Brooktree Corporation.
TARGA is a registered trademark of Truevision Incorporated.

- Available in 85-, 110-,135-, and 170-MHz Versions
- 256-Word Color Palette RAM
- Palette Page Register
- On-Chip Voltage Reference
- RS-343A-Compatible Outputs
- TTL-Compatible Inputs
- Standard MPU Interface
- Pixel Word Mask
- On-Chip Clock Selection
- Interfaces Directly to Video RAM
- Supports Split Shift Register Transfers
- Software Downward-Compatible with INMOS™ IMSG176/8 and Brooktree BT476/8 Color Palettes
- TIGA™-Software-Standard Compatible
- LinEPIC™ 1-µm CMOS Process

LinEPIC and TIGA are trademarks of Texas Instruments Incorporated.
INMOS is a trademark of INMOS International Limited.

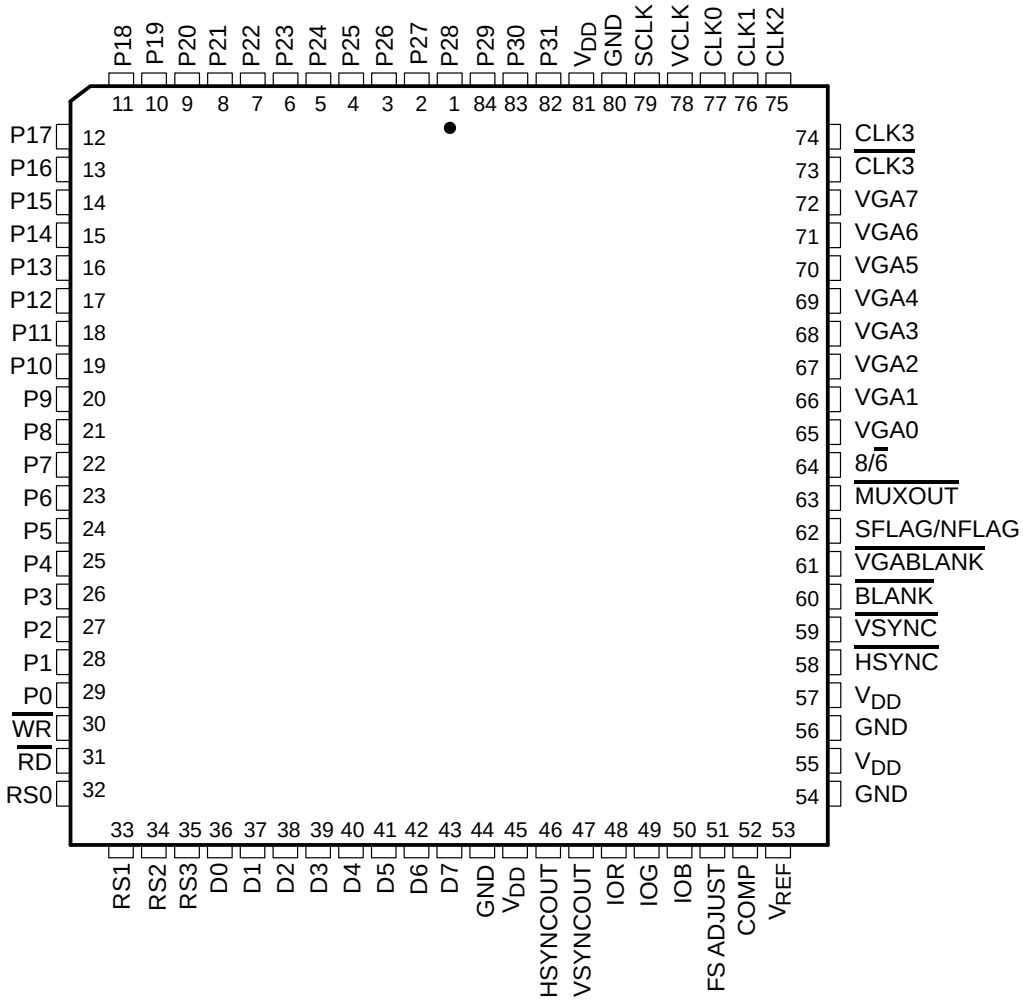
1.2 Functional Block Diagram



1.3 Terminal Assignments

The terminal assignments for TLC34076C are shown in the 84-pin FN package; terminal assignments for TLC34076M are shown in the 84-pin GA package.

84-PIN FN PACKAGE (TOP VIEW)



1.3 Terminal Assignments (Continued)

84-PIN GA PACKAGE (TOP VIEW)

	A	B	C	D	E	F	G	H	J	K	L	M
12	RS0	D0	D1	D3	D5	D7	V_{DD}	HSYNC-OUT	IOR	IOB	FS ADJUST	V_{REF}
11	$\overline{WR}$	RS2	RS3	D2	D4	D6	GND	VSYNC-OUT	IOG	COMP	V_{DD}	DV_{DD}
10	P0	$\overline{RD}$	RS1							GND	GND	$\overline{HSYNC}$
9	P2	P1									$\overline{VSYNC}$	$\overline{BLANK}$
8	P4	P3									$\overline{VGA\text{-}BLANK}$	SFLAG/ NFLAG
7	P6	P5									8/$\overline{6}$	$\overline{MUXOUT}$
6	P8	P7									VGA1	VGA0
5	P9	P10									VGA3	VGA2
4	P11	P12		● (ESD symbol or alignment dot on top)							VGA5	VGA4
3	P13	P15	P17							CLK2	$\overline{CLK3}$	VGA6
2	P14	P16	P19	P22	P24	P27	P29	P31	GND	CLK0	CLK1	VGA7
1	P18	P20	P21	P23	P25	P26	P28	P30	V_{DD}	SCLK	VCLK	CLK3

1.3 Terminal Assignments (Continued)

84-PIN GA PACKAGE (BOTTOM VIEW)

	M	L	K	J	H	G	F	E	D	C	B	A
12	V_{ref}	FS ADJUST	IOB	IOR	HSYNC-OUT	V_{DD}	D7	D5	D3	D1	D0	RS0
11	DV_{DD}	V_{DD}	COMP	IOG	VSYNC-OUT	GND	D6	D4	D2	RS3	RS2	$\overline{WR}$
10	$\overline{HSYNC}$	GND	GND							RS1	$\overline{RD}$	P0
9	$\overline{BLANK}$	$\overline{VSYNC}$									P1	P2
8	SFLAG/ NFLAG	$\overline{VGA\text{-}BLANK}$									P3	P4
7	$\overline{MUXOUT}$	$8/\overline{6}$									P5	P6
6	VGA0	VGA1									P7	P8
5	VGA2	VGA3									P10	P9
4	VGA4	VGA5				(ESD symbol or alignment dot on top) ●					P12	P11
3	VGA6	$\overline{CLK3}$	CLK2							P17	P15	P13
2	VGA7	CLK1	CLK0	GND	P31	P29	P27	P24	P22	P19	P16	P14
1	CLK3	VCLK	SCLK	V_{DD}	P30	P28	P26	P25	P23	P21	P20	P18

1.4 Ordering Information

TLC34076 – (X)XX M PP

Pixel clock frequency indicator
Must contain two or three characters:

–85:	85-MHz pixel clock
–110:	110-MHz pixel clock
–135:	135-MHz pixel clock
–170:	170-MHz pixel clock

Military extension

Package
Must contain two letters:

FN:	plastic, square, leaded chip carrier (formed leads)
GA:	84-pin (12 x 12) ceramic pin-grid array

1.5 Terminal Functions (TLC34076C and TLC34076M)

TERMINAL			I/O	DESCRIPTION
NAME	NO.†	NO.‡	I/O	DESCRIPTION
$\overline{\text{BLANK}}$, VGA$\overline{\text{BLANK}}$	60, 61	M9, L8	I	Blanking inputs. Two blanking inputs are provided in order to remove any external multiplexing of the signals that may cause data and Blank to skew. When the VGA pass-through mode is set in the multiplex control register, the VGA$\overline{\text{BLANK}}$ input is used for blanking; otherwise, $\overline{\text{BLANK}}$ is used.
CLK0 – CLK2	77, 76, 75	K2, L2, K3	I	Dot clock inputs. Any of the three clocks can drive the dot clock at frequencies up to 135 MHz. When VGA pass-through mode is active, CLK0 is used by default.
CLK3, $\overline{\text{CLK3}}$	74, 73	M1, L3	I	Dual-mode dot clock input. The clock input is an ECL-compatible input, but a TTL clock may be used on either CLK3 or $\overline{\text{CLK3}}$ when so selected in the input clock selection register. This input may be selected as the dot clock for any frequency of operation up to the device limit. It can also be used with a single-ended ECL clock source when the unused input is externally terminated to provide the proper common mode level.
COMP	52	K11	I	Compensation input. COMP provides compensation for the internal reference amplifier. A resistor (optional) and ceramic capacitor are required between COMP and V_{DD}. The resistor and capacitor must be as close to the device as possible to avoid noise pickup (see Appendix B for more details).
D0 – D7	36 – 43	B12, C12, D11, D12, E11, E12, F11, F12	I/O	MPU interface data bus. D0 – D7 transfers data in and out of the register map and palette/overlay RAM.
FS ADJUST	51	L12	I	Full-scale adjustment. A resistor connected between FS ADJUST and ground controls the full-scale range of the DACs.
GND	44, 54, 56, 80	J2, L10, K10, G11		Ground. All GND terminals must be connected together. The analog and digital GND terminals are connected internally.
HSYNCOUT, VSYNCOUT	46, 47	H12, H11	O	Horizontal and vertical sync outputs. The HSYNCOUT and VSYNCOUT are the true/complement gate mentioned in the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ description below (see Section 2.8).
$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$	58, 59	M10, L9	I	Horizontal and vertical sync inputs. $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ generate the sync level on the green current output. They are active-low inputs for the normal modes and are passed through a true/complement gate. For the VGA pass-through mode, they are passed through to HSYNCOUT and VSYNCOUT without polarity change as specified by the control register (see Section 2.8).
IOR, IOG, IOB	48, 49, 50	J12, J11, K12	O	Analog current outputs. The IOR, IOG, and IOB outputs can drive a 37.5-Ω load directly (doubly terminated 75-Ω line), thus eliminating the need for any external buffering.

† Terminal numbers shown are for the FN package.

‡ Terminal numbers shown are for the GA package.

NOTES: 1. Although leaving unused terminals floating does not adversely affect device operation, tying unused terminals to ground lowers power consumption, thus is recommended.

2. All digital inputs and outputs are TTL compatible, unless otherwise noted.

1.5 Terminal Functions (TLC34076C and TLC34076M) (Continued)

TERMINAL NAME	TERMINAL NO.†	TERMINAL NO.‡	I/O	DESCRIPTION
$\overline{\text{MUXOUT}}$	63	M7	O	MUX output control. $\overline{\text{MUXOUT}}$ is software programmable. It is set low to indicate to external devices that VGA pass-through mode is being used when the multiplex control register value is set to 2Dh. When bit 7 of the general-control register is set high after the mode is set, this output goes high. This terminal is only used for external control; it affects no internal circuitry.
P0 – P31	29–1, 84–82	A10, B9, A9, B8, A8, B7, A7, B6, A6, A5, B5, A4, B4, A3, A2, B3, B2, C3, A1, C2, B1, C1, D2, D1, E2, E1, F1, F2, G1, G2, H1, H2	I	Pixel input port. This port can be used in various modes as shown in the MUX control register. It is recommended that unused terminals be tied to ground. It also supports little-endian and big-endian data formats. All the unused terminals must be tied to GND.
$\overline{\text{RD}}$	31	B10	I	Read strobe input. A low on $\overline{\text{RD}}$ initiates a read from the TLC34076 register map. Reads are performed asynchronously and are initiated on the falling edge of $\overline{\text{RD}}$ (see Figure 3–1).
RS0 – RS3	32–35	A12, C10, B11, C11	I	Register select inputs. RSx specifies the location in the register map that is to be accessed (see Table 2–1).
SCLK	79	K1	O	Shift clock output. SCLK is selected as a submultiple of the dot clock input. SCLK is gated off during blanking.
SFLAG/ NFLAG	62	M8	I	Split shift register transfer flag or nibble flag input. SFLAG/NFLAG has two functions. When the general control register bit 3 = 0 and bit 2 = 1, the split shift register transfer function is enabled and a low-to-high transition on SFLAG/NFLAG during a blank sequence initiates an extra SCLK cycle to allow a split shift register transfer in the VRAMs. When the general control register bit 3 = 1 and bit 2 = 0, special nibble mode is enabled and this input is sampled at the falling edge of VCLK. A high value sampled indicates that the next SCLK rising edge should latch the high nibble of each byte of the pixel data bus; a low value sampled indicates that the low nibble of each byte of the pixel data bus should be latched (see Section 2.9). When the general control register bit 3 = 0 and bit 2 = 0, the condition of SFLAG/NFLAG is ignored. The condition of bit 3 = 1, bit 2 = 1 is not allowed, and device operation is unpredictable when they are so set.
VCLK	78	L1	O	Video clock output. VCLK is user-programmable output for synchronization of the TLC34076 to a graphics processor.
V_{DD}	45, 55, 57, 81	J1, L11, G12		Power. All V_{DD} terminals must be connected. The analog and digital V_{DD} terminals are connected internally.

† Terminal numbers shown are for the FN package.

‡ Terminal numbers shown are for the GA package.

NOTES: 1. Although leaving unused terminals floating does not adversely affect device operation, tying unused terminals to ground lowers power consumption, thus is recommended.

2. All digital inputs and outputs are TTL compatible, unless otherwise noted.

1.5 Terminal Functions (TLC34076C and TLC34076M) (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.†	NO.‡		
VGA0 – VGA7	65 – 72	M6, L6, M5, L5, M4, L4, M3, M2	I	VGA pass-through bus. The VGAn bus can be selected as the pixel bus for the VGA pass-through mode. It does not allow for any multiplexing.
V_{REF}	53	M12		Voltage reference for DACs. An internal voltage reference of nominally 1.235 V is supplied. A 0.1-µF ceramic capacitor between V_{REF} and GND is recommended for noise filtering using either the internal or an external reference voltage. The internal reference voltage can be overridden by an externally supplied voltage. The typical connection is shown in Appendix B.
$\overline{WR}$	30	A11	I	Write strobe input. A low on $\overline{WR}$ initiates a write to the TLC34076 register map. Write transfers are asynchronous. The data written to the register map is latched on the rising edge of $\overline{WR}$ (see Figure 3–1).
8/$\overline{6}$	64	L7	I	DAC resolution selection. The 8/$\overline{6}$ terminal selects the data bus width (8 or 6 bits) for the DACs and is provided to maintain compatibility with the INMOS IMSG176/8 color palette. When this terminal is high, 8-bit bus transfers are used, with D7 being the MSB and D0 the LSB. For 6-bit bus operation, while the color palette still has the 8-bit information, D5 shifts to the bit 7 position, D0 shifts to the bit 2 position, and the two LSBs are filled with zeros at the output MUX to the DAC. When read in the 6-bit mode, the palette holding register zeros the two MSBs.

† Terminal numbers shown are for the FN package.
‡ Terminal numbers shown are for the GA package.
NOTES: 1. Although leaving unused terminals floating does not adversely affect device operation, tying unused terminals to ground lowers power consumption, thus is recommended.
2. All digital inputs and outputs are TTL compatible, unless otherwise noted.

2 Detailed Description

2.1 Microprocessor Unit (MPU) Interface

The processor interface is controlled using read and write strobes ($\overline{RD}$, $\overline{WR}$), four register select terminals (RS0 – RS3), and the 8/$\overline{6}$ select terminal. The select 8/$\overline{6}$ terminal selects between 8-bit and 6-bit operation and is provided in order to maintain compatibility with the IMSG176/8 color palette. This operation is carried out to utilize the maximum range of the DACs.

The internal register map is shown in Table 2–1. The MPU interface operates asynchronously, with data transfers being synchronized by internal logic. All the register locations support read and write operations.

Table 2–1. Internal Register Map

RS3	RS2	RS1	RS0	REGISTER ADDRESSED BY MPU
L	L	L	L	Palette address register – write mode
L	L	L	H	Color palette holding register
L	L	H	L	Pixel read mask
L	L	H	H	Palette address register – read mode
L	H	L	L	Reserved
L	H	L	H	Reserved
L	H	H	L	Reserved
L	H	H	H	Reserved
H	L	L	L	General control register
H	L	L	H	Input clock selection register
H	L	H	L	Output clock selection register
H	L	H	H	Multiplex control register
H	H	L	L	Palette page register
H	H	L	H	Reserved
H	H	H	L	Test register
H	H	H	H	Reset state

2.2 Color Palette RAM

The color palette RAM is addressed by two internal 8-bit registers, one for reading from the RAM and one for writing to the RAM. These registers are automatically incremented following a RAM transfer, allowing the entire palette to be read/written with only one access of the address register. When the address register increments beyond the last location in RAM, it is reset to the first location (address 0). Although all read and write accesses to the RAM are asynchronous to SCLK, VCLK, and the dot clock, they are performed within one dot clock and so do not cause any noticeable disturbance on the display.

The color palette RAM is 24 bits wide for each location (8 bits each for red, green, and blue). When 6-bit mode is chosen (8/$\overline{6}$ = low), the two MSBs are still written to the color palette RAM. However, when they are read back in the 6-bit mode, the two MSBs are set to 0 to maintain compatibility with the IMSG176/8 and BT476/8 color palettes. The output MUX shifts the six LSBs to the six MSB positions, fills the two LSBs with 0s, then feeds the 8 bits to the DAC. With the 8/$\overline{6}$ terminal held low, data on the lowest 6 bits of the data bus are internally shifted up by two bits to occupy the upper six bits at the output MUX, and the bottom two bits are then cleared to 0. The test register and the ones-accumulation register both take data before the output MUX to give the user the maximum flexibility.

The color-palette RAM-access methodology is described in the following two sections and is fully compatible with the INMOS IMSG176/8 and Brooktree Bt476/8 color palettes.

2.2.1 Writing to the Color Palette RAM

To load the color palette RAM, the MPU must first write to the address register (write mode) with the address where the modification is to start. This action is followed by three successive writes to the palette-holding register with eight bits each of red, green, and blue data. After the blue data write cycle, the three bytes of color are concatenated into a 24-bit word and written to the color palette RAM location specified by the address register. The address register then increments to point to the next color palette RAM location, which the MPU may modify by simply writing another sequence of red, green, and blue data bytes. A block of color values in consecutive locations may be written to by writing the start address and performing continuous red, green, and blue write cycles until the entire block has been written.

2.2.2 Reading From the Color Palette RAM

Reading from the color palette RAM is performed by writing the location to be read to the address register. This action initiates a transfer from the color palette RAM into the holding register followed by an increment of the address register. Three successive MPU reads from the holding register produce red, green, and blue color data (6 or 8 bits, depending on the 8/$\overline{6}$ mode) for the specified location. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the holding register and the address register is again incremented. As with writing to the color palette RAM, a block of color values in consecutive locations may be read by writing the start address and performing continuous red, green, and blue read cycles until the entire block has been read.

2.2.3 Palette Page Register

The 8-bit palette page register provides high-speed color changing by removing the need for color palette RAM reloading. When using 1, 2, or 4 bit-planes, the additional planes are provided by the palette page register; e.g., when using four bit-planes, the pixel inputs specify the lower four bits of the color palette RAM address with the upper four bits being specified by the palette register. This provides the capability of selecting from 16 palette pages with only one chip access, thus allowing all the screen colors to be changed at the line frequency. A bit-to-bit correspondence is used; therefore, in the above configuration, palette page register bits 7 – 4 map onto color palette RAM address bits 7 – 4 respectively. This is listed in Table 2–2.

Since there is only one bit of overlay data in the 5-5-5 true color modes, the page register fills the seven remaining MSBs (same as one bit-plane in Table 2–2). All 8 bits need to be cleared to 0 in order to enable true color.

The additional bits from the palette page register are inserted before the read mask and hence, are subject to masking.

Table 2–2. Allocation of Palette Page Register Bits

NUMBER OF BIT PLANES	COLOR PALETTE RAM ADDRESS BITS							
	MSB							LSB
8	M	M	M	M	M	M	M	M
4	P7	P6	P5	P4	M	M	M	M
2	P7	P6	P5	P4	P3	P2	M	M
1	P7	P6	P5	P4	P3	P2	P1	M

Pn = nth bit from palette page register
M = bit from pixel port

2.3 Input/Output Clock Selection and Generation

The TLC34076 provides a maximum of five clock inputs. Three are dedicated to TTL inputs; the other two can be selected as either one ECL input or two extra TTL inputs. The TTL and ECL inputs can be used for video rates up to 135 MHz. The dual-mode clock input (ECL/TTL) is primarily an ECL input but can be used

as a TTL-compatible input when the input clock selection register is so programmed. The clock source used at power-up is CLK0; an alternative source can be selected by software during normal operation. This chosen clock input is used unmodified as the dot clock (representing the pixel rate to the monitor). The device does, however, allow for user programming of the SCLK and VCLK outputs (shift and video clocks) using the output clock selection register. The input/output clock selection registers are shown in Tables 2–3, 2–4, and 2–5.

Table 2–3. Input Clock Selection Register Format

BITS†				FUNCTION‡
3	2	1	0	
0	0	0	0	Select CLK0 as clock source§
0	0	0	1	Select CLK1 as clock source
0	0	1	0	Select CLK2 as clock source
0	0	1	1	Select CLK3 as TTL clock source
0	1	0	0	Select $\overline{\text{CLK3}}$ as TTL clock source
1	0	0	0	Select CLK3 and $\overline{\text{CLK3}}$ as ECL clock sources

† Register bits 4, 5, 6, and 7 are don't care bits.
‡ When the clock selection is altered, a minimum 30-ns delay is incurred before the new clocks are stabilized and running.
§ CLK0 is chosen at power-up to support the VGA pass-through mode.

Table 2–4. Output Clock Selection Register Format

BITS†						FUNCTION‡
5	4	3	2	1	0	
0	0	0	X	X	X	VCLK frequency = DOTCLK frequency
0	0	1	X	X	X	VCLK frequency = DOTCLK frequency/2
0	1	0	X	X	X	VCLK frequency = DOTCLK frequency/4
0	1	1	X	X	X	VCLK frequency = DOTCLK frequency/8
1	0	0	X	X	X	VCLK frequency = DOTCLK frequency/16
1	0	1	X	X	X	VCLK frequency = DOTCLK frequency/32
1	1	X	X	X	X	VCLK output held at logic high level (default condition)§
X	X	X	0	0	0	SCLK frequency = DOTCLK frequency
X	X	X	0	0	1	SCLK frequency = DOTCLK frequency/2
X	X	X	0	1	0	SCLK frequency = DOTCLK frequency/4
X	X	X	0	1	1	SCLK frequency = DOTCLK frequency/8
X	X	X	1	0	0	SCLK frequency = DOTCLK frequency/16
X	X	X	1	0	1	SCLK frequency = DOTCLK frequency/32
X	X	X	1	1	X	SCLK output held at logic level low (default condition)§

† Register bits 6 and 7 are don't care bits.
‡ When the clock selection is altered, a minimum 30-ns delay is incurred before the new clocks are stabilized and running.
§ These lines indicate the power-up conditions required to support the VGA pass-through mode.

Table 2–5. VCLK/SCLK Divide Ratio Selectio (Output Clock Selection Register Value in Hex)

SCLK / VCLK	BITS 2. . .0†	000	001	010	011	100	101
BITS 5. . .3†	divide DOTCLK by	1	2	4	8	16	32
000	1	00	01	02	03	04	05
001	2	08	09	0A	0B	0C	0D
010	4	10	11	12	13	14	15
011	8	18	19	1A	1B	1C	1D
100	16	20	21	22	23	24	25
101	32	28	29	2A	2B	2C	2D

† Output clock selection register bits

The ECL input can be used as a differential or single-ended input. When the CLK3 input is used as a single-ended ECL input, CLK3 must be externally terminated to set the input common-mode signal level. This can be done with a simple resistor divider, as is the case with fully differential ECL.

SCLK is designed to drive the VRAMs directly, and VCLK is designed to work with video control signals like BLANK and SYNC. While SCLK and VCLK are designed as a general-purpose shift clock and video clock, respectively, they also interface directly with the TMS340x0 graphics signal processor (GSP) family directly. Even though SCLK and VCLK can be selected independently, there is still a relationship between the two as discussed in subsequent paragraphs. Many system considerations have been carefully covered in the design, leaving maximum freedom to the user.

Internally, both SCLK and VCLK are generated from a common clock counter that increments on the rising edge of the DOTCLK. Therefore, when VCLK is enabled, it is in phase with SCLK (see Figure 2–1).

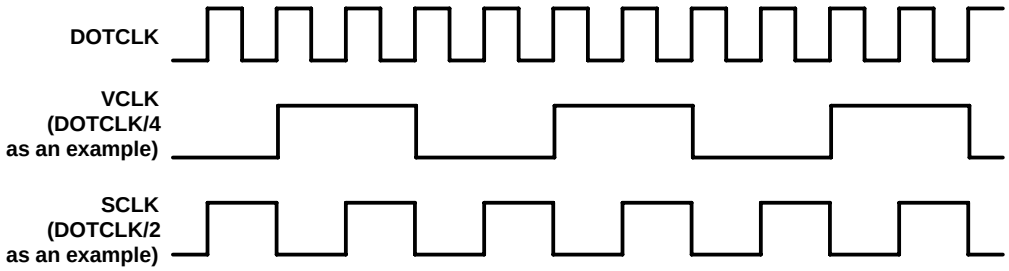


Figure 2–1. DOTCLK/VCLK/SCLK Relationship

The internal clock counter is reset to 0 any time the output clock-selection register (bits 5, 4, 2, 1) are all set to 1. This provides a simple mechanism to synchronize multiple VIPs, by providing a known phase relationship for the various system clocks. One can write directly to the Output Clock Selection register to cause this to occur, or any of the various resets (for POR, hardware, and software, see Section 1.5) also causes the appropriate bits to be written and the counters to reset. It is up to the user to provide some means of disabling the dot-clock input to the part while this reset is occurring, when multiple parts are to be synchronized.

Appendix A discusses the SCLK/VCLK relationship specific to the TMS340x0 GSP.

2.3.1 SCLK

Data is latched inside the device on the rising edge of LOAD, which is basically the same as SCLK but not disabled during Blank active period. Therefore, SCLK must be set as a function of the pixel bus width and the number of bit planes. SCLK can be selected as 1, 2, 4, 8, 16, or 32 divisions of the dot clock. When SCLK is not used, the output is switched off and held low to protect against VRAM lock-up due to invalid SCLK frequencies. SCLK is also held low during the Blank active period. The SCLK control timing has been designed to interface directly with the external system VRAM. The shift register in the system VRAM should be updated during the Blank active period. This allows the first SCLK out of Blank to clock the VRAM and enable the first group of pixel data to appear on the pixel bus, as well as at the TLC34076 pixel input port. The second SCLK after Blank latches the first group of pixel port data into the TLC34076.

The trailing edge of VCLK is used internally by the TLC34076 to sample and latch the $\overline{\text{BLANK}}$ input. When $\overline{\text{BLANK}}$ becomes active, SCLK is disabled as soon as possible. For example, when SCLK is high and the sampled $\overline{\text{BLANK}}$ goes low, SCLK is allowed to complete the clock cycle and return to the low state. SCLK is then held low until the sampled $\overline{\text{BLANK}}$ signal goes high. At this time, SCLK is enabled to clock the VRAM again. The TLC34076 video blanking circuitry is designed with sufficient pipeline delay to allow the internally sampled $\overline{\text{BLANK}}$ signal to align with the pipelined RGB data to the video DACs. The logic described herein works in situations where the SCLK period is shorter than, equal to, or longer than the VCLK period.

When the VRAM split shift-register operation is performed, the SCLK timing is adjusted to work with the SFLAG input. Basically, the split shift register operation inserts a SCLK during the Blank period. This causes the first group of pixel data to appear at the pixel port during the Blank signal. The first SCLK after Blank then latches this data into the TLC34076. Figure 2–3 shows the case when the split shift register transfer (SSRT) function is enabled. When a rising edge occurs on the SFLAG input, one SCLK with a minimum of 15-ns pulse duration is generated after the specified delay. Since this is designed to meet VRAM timing requirements, the SSRT-generated SCLK replaces the first SCLK in the regular shift register transfer case as previously described (see to Section 2.9 for a detailed explanation of the SSRT function).

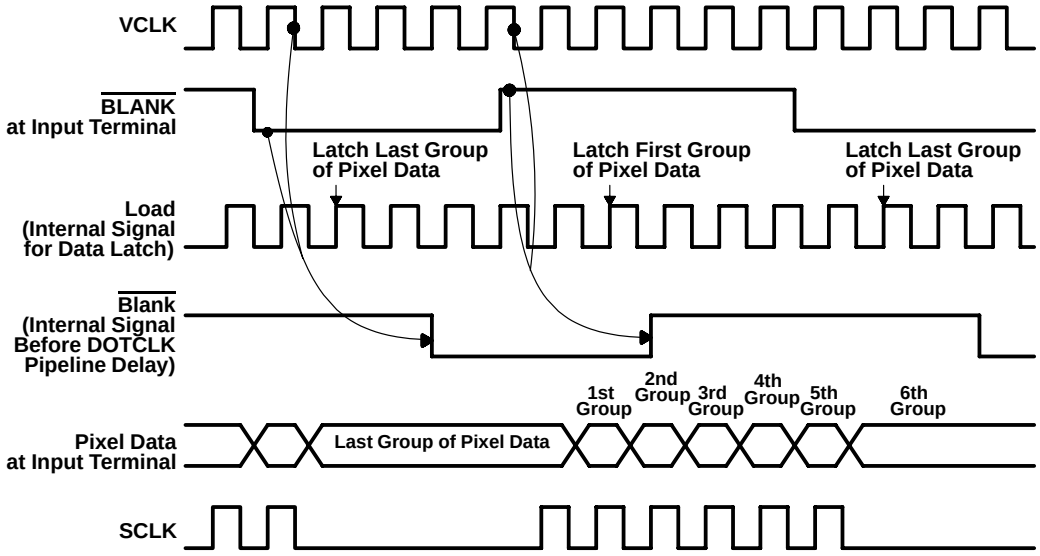
The default divide ratio for SCLK is 1:1 as used in mode 0.

Depending on the frequency relationship between SCLK and VCLK, their phase relationship could be critical (see Appendix C for a more detailed discussion).

2.3.2 VCLK

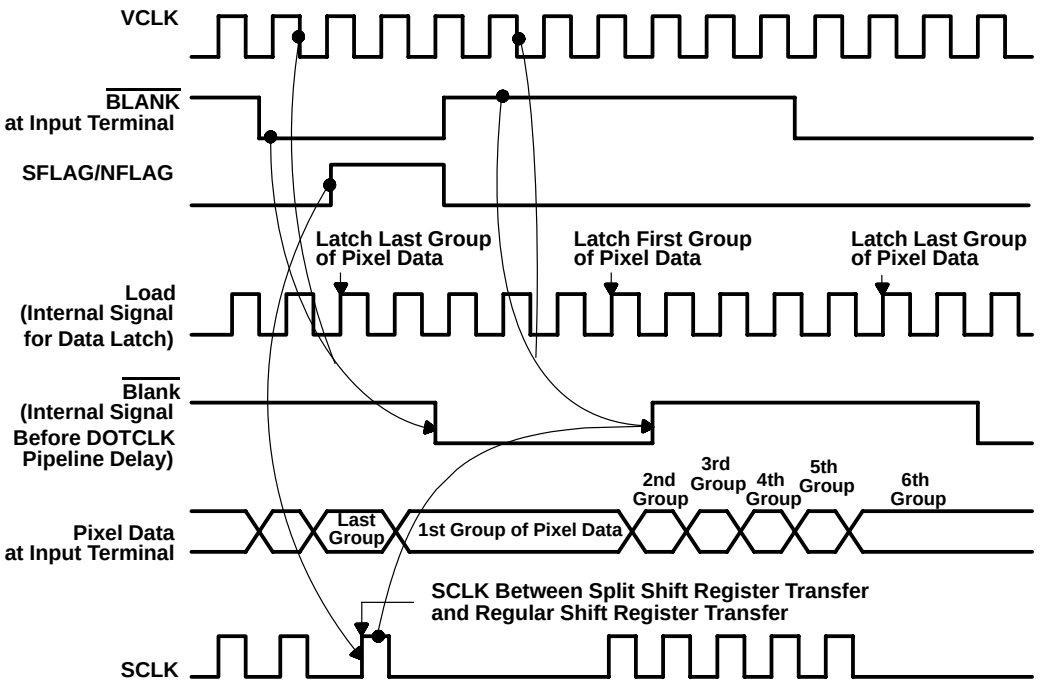
The VCLK frequency can be selected to be 1:1, 1:2, 1:4, 1:8, 1:16, or 1:32 of that of the dot clock, or it can be held at a high logic level, which is the VCLK default condition. VCLK is not used in VGA pass-through mode.

VCLK is used by a GSP or custom-designed control logic to generate control signals ($\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, and $\overline{\text{VSYNC}}$). As can be seen from Figures 2–2, 2–3, 2–4, and 2–5, since the control signals are sampled by VCLK, it is obvious that VCLK has to be enabled.



NOTE A: Either the SSRT function is disabled (general control register bit 2 = 0), or the SFLAG/NFLAG input is held low when the SSRT function is enabled (general-control register bit 2 = 1).

Figure 2–2. SCLK/VCLK Control Timing (SSRT Disabled, SCLK Frequency = VCLK Frequency)



NOTE A: The SSRT function is enabled (general control register bit 2 = 1).

Figure 2–3. SCLK/VCLK Control Timing (SSRT Enabled, SCLK Frequency = VCLK Frequency)

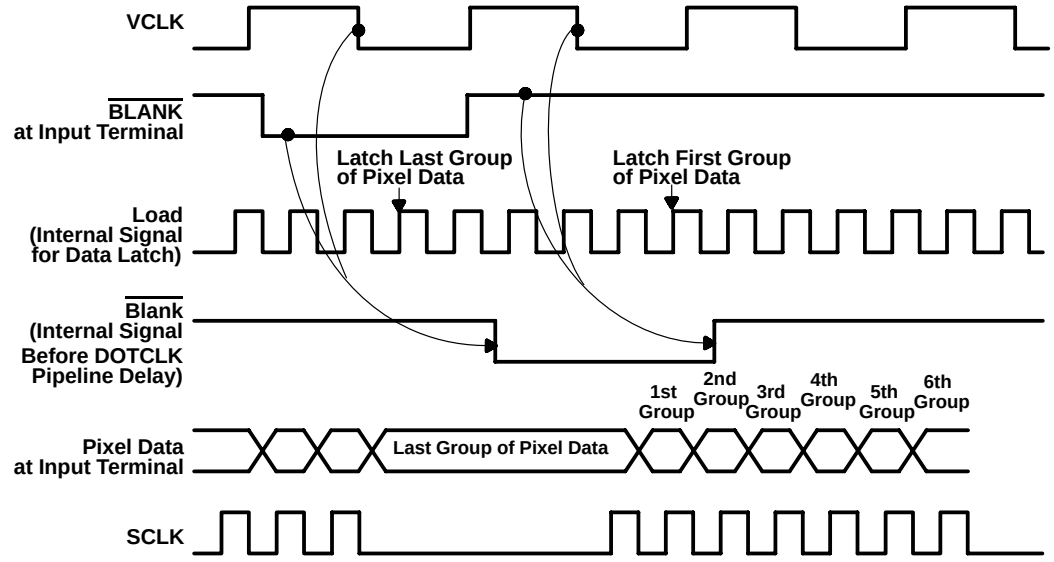
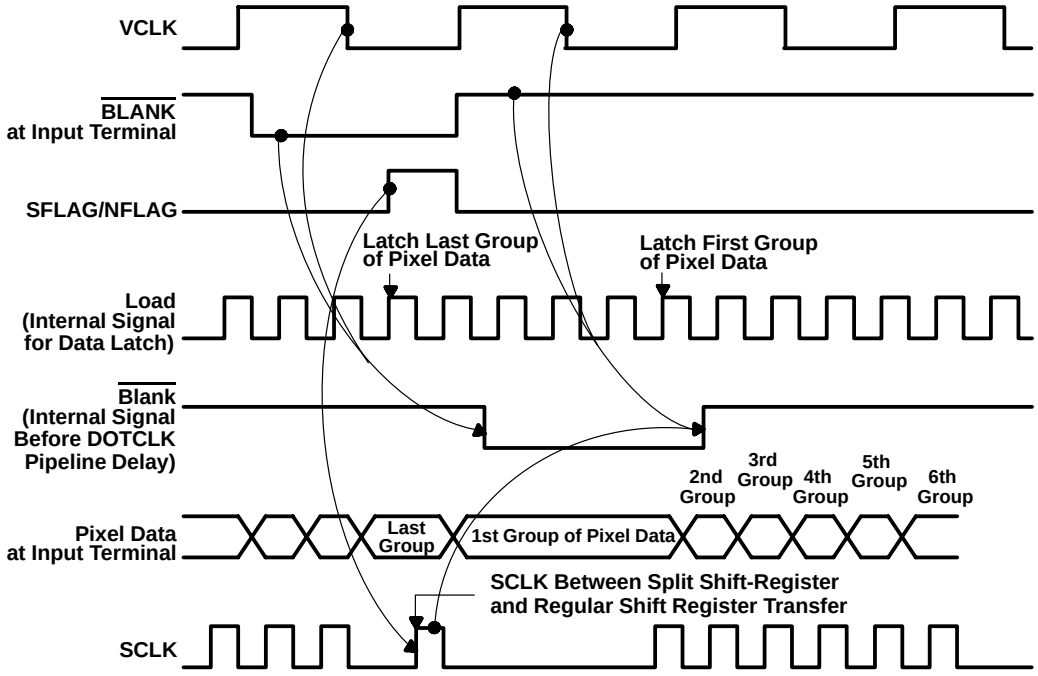


Figure 2–4. SCLK/VCLK Control Timing (SSRT Disabled, SCLK Frequency = 4 × VCLK Frequency)



NOTE A: Either the SSRT function is disabled (general-control register bit 2 = 0), or the SFLAG/NFLAG input is held low when the SSRT function is enabled (general-control register bit 2 = 1).

Figure 2–5. SCLK/VCLK Control Timing (SSRT Enabled, SCLK Frequency = 4 × VCLK Frequency)

2.4 Multiplexing Scheme

The TLC34076 offers a highly versatile multiplexing scheme as illustrated in Table 2–6. The on-chip multiplexing allows the system to be reconfigured to the amount of RAM available. For example, when only 256K bytes of memory are available, an 800-by-600 resolution mode with four bit-planes (4 bits per pixel) can be implemented using an 8-bit wide pixel bus. If, at a later date, another 256K bytes are added to another 8 bits of the pixel bus, the user has the option of using eight bit-planes at the same resolution or four bit-planes at a 1024 × 768 resolution. When an additional 512K bytes are added to the remaining 16 bits of the pixel bus, the user has the option of eight bit-planes at 1024 × 768 resolution or four bit-planes at 1280 × 1024 resolution. All the above can be achieved without any hardware modification and without any increase in the speed of the pixel bus.

Table 2–6. Mode and Bus Width Selection

MODE	MUX CONTROL REGISTER BITS†						DATA BITS PER PIXEL‡	PIXEL BUS WIDTH	SCLK DIVIDE RATIO§	PIXEL LATCHING SEQUENCE¶
	5	4	3	2	1	0				
0#	1	0	1	1	0	1	8	8	1	1) VGA7 – VGA0
1	0	1	0	0	0	0	1	4	4	1) P0 2) P1 3) P2 4) P3
	0	1	0	0	0	1	1	8	8	1) P0 2) P1 ⋮ 8) P7
	0	1	0	0	1	0	1	16	16	1) P0 2) P1 ⋮ 16) P15
	0	1	0	0	1	1	1	32	32	1) P0 2) P1 ⋮ 32) P31
2	0	1	0	1	0	0	2	4	2	1) P1 – P0 2) P3 – P2
	0	1	0	1	0	1	2	8	4	1) P1 – P0 2) P3 – P2 3) P5 – P4 4) P7 – P6
	0	1	0	1	1	0	2	16	8	1) P1 – P0 2) P3 – P2 ⋮ 8) P15 – P14
	0	1	0	1	1	1	2	32	16	1) P1 – P0 2) P3 – P2 ⋮ 16) P31 – P30

† Bits 6 and 7 are don't care bits.

‡ This is the number of bits of pixel port (or VGA port in mode 1) information used as color data for each displayed pixel, often referred to as the number of bit planes. This may be color palette address data (modes 0–5) or DAC data (mode 6).

§ The SCLK divide ratio is the number used for the output clock selection register. It indicates the number of pixels per bus load, or the number of pixels associated with each SCLK pulse. For example, with a 32-bit pixel bus width and 8 bit-planes, 4 pixels comprise each bus load. The SCLK divide ratio is not automatically set by mode selection, but must be written to the output clock selection register.

¶ For each operating mode, the pixel latching sequence indicates the sequence in which pixel port or VGA port data are latched into the device. The latching sequence is initiated by a rising edge on SCLK. For modes in which multiple groups of data are latched, the SCLK rising edge latches all the groups, and the pixel clock shifts them out starting with the low-numbered group. For example, in mode 3 with a 16-bit pixel bus width, the rising edge of SCLK latches all the data groups, and the pixel clock shifts them out in the order P3 – P0, P7 – P4, P11 – P8, and P15 – 12 terminals.

Mode 0 is the VGA pass-through mode.

NOTE 1: Although leaving unused pins floating does not adversely affect device operation, tying unused pins to ground lowers power consumption and, thus, is recommended.

Table 2–6. Mode and Bus Width Selection (Continued)

MODE	MUX CONTROL REGISTER BITS†						DATA BITS PER PIXEL‡	PIXEL BUS WIDTH	SCLK DIVIDE RATIO§	PIXEL LATCHING SEQUENCE¶
	5	4	3	2	1	0				
3	0	1	1	0	0	0	4	4	1	1) P3 – P0
	0	1	1	0	0	1	4	8	2	1) P3 – P0 2) P7 – P4
	0	1	1	0	1	0	4	16	4	1) P3 – P0 2) P7 – P4 3) P11 – P8 4) P15 – P12
	0	1	1	0	1	1	4	32	8	1) P3 – P0 2) P7 – P4 8) P31 – P28
4	0	1	1	1	0	0	8	8	1	1) P7 – P0
	0	1	1	1	0	1	8	16	2	1) P7 – P0 2) P15 – P8
	0	1	1	1	1	0	8	32	4	1) P7 – P0 2) P15 – P8 3) P23 – P16 4) P31 – P24

† Bits 6 and 7 are don't care bits.

‡ This is the number of bits of pixel port (or VGA port in mode 1) information used as color data for each displayed pixel, often referred to as the number of bit-planes. This may be color palette address data (modes 0–5) or DAC data (mode 6).

§ The SCLK divide ratio is the number used for the output clock selection register. It indicates the number of pixels per bus load, or the number of pixels associated with each SCLK pulse. For example, with a 32-bit pixel bus width and 8 bit-planes, four pixels comprise each bus load. The SCLK divide ratio is not automatically set by mode selection, but must be written to the output clock selection register.

¶ For each operating mode, the pixel latching sequence indicates the sequence in which pixel port or VGA port data are latched into the device. The latching sequence is initiated by a rising edge on SCLK. For modes in which multiple groups of data are latched, the SCLK rising edge latches all the groups, and the pixel clock shifts them out starting with the low-numbered group. For example, in mode 3 with a 16-bit pixel bus width, the rising edge of SCLK latches all the data groups, and the pixel clock shifts them out in the order P3 – P0, P7 – P4, P11 – P8, P15 – P12.

NOTE 1: Although leaving unused pins floating does not adversely affect device operation, tying unused pins to ground lowers power consumption and, thus, is recommended.

Table 2–6. Mode and Bus Width Selection (Continued)

MODE	MUX CONTROL REGISTER BITS†						DATA BITS PER PIXEL‡	PIXEL BUS WIDTH	SCLK DIVIDE RATIO§	PIXEL LATCHING SEQUENCE¶
	5	4	3	2	1	0				
5#	0	1	1	1	1	1	4	16	4	NFLAG = 0: 1) P3 – P0 2) P11 – P8 3) P19 – P16 4) P27 – P24 NFLAG = 1: 1) P7 – P4 2) P15 – P12 3) P23 – P20 4) P31 – P28
6‖	See Table 2–7 and Table 2–8									

† Bits 6 and 7 are don't care bits.

‡ This is the number of bits of pixel port (or VGA port in mode 1) information used as color data for each displayed pixel, often referred to as the number of bit-planes. This may be color palette address data (modes 0–5) or DAC data (mode 6).

§ The SCLK divide ratio is the number used for the output clock selection register. It indicates the number of pixels per bus load, or the number of pixels associated with each SCLK pulse. For example, with a 32-bit pixel bus width and 8 bit-planes, 4 pixels comprise each bus load. The SCLK divide ratio is not automatically set by mode selection, but must be written to the output clock selection register.

¶ For each operating mode, the pixel latching sequence indicates the sequence in which pixel port or VGA port data are latched into the device. The latching sequence is initiated by a rising edge on SCLK. For modes in which multiple groups of data are latched, the SCLK rising edge latches all the groups, and the pixel clock shifts them out starting with the low-numbered group. For example, in mode 3 with a 16-bit pixel bus width, the rising edge of SCLK latches all the data groups, and the pixel clock shifts them out in the order P3 – P0, P7 – P4, P11 – P8, P15 – P12.

Mode 5 is special nibble mode, the only mode in which the pixel bus width is not equal to the actual physical width, in bits, of the pixel bus. In this mode, the pixel bus is physically 32 bits wide; depending on the value of SFLAG/NFLAG, either the upper or lower nibble of each of the four physical bytes is selected to comprise the 16 bits of pixel data (equal to four 4-bit pixels).

‖ Mode 6 is true color mode, in which 24 bits of color information are transferred directly from the pixel port to the DACs; overlay is implemented with the remaining eight bits of the pixel bus. The distribution of pixel port data to the DACs is as follows: P31 – P24 are passed to the blue DAC, P23 – P16 are passed to the green DAC, and P15 – P8 are passed to the red DAC. P7 – P0 generate overlay data; this operation can be disabled by either grounding P7 – P0 or by clearing the read mask (see subsection 2.4.6).

NOTE 1: Although leaving unused pins floating will not adversely affect device operation, tying unused pins to ground lowers power consumption and, thus, is recommended.

2.4.1 VGA Pass-Through Mode

Mode 0, the VGA pass-through mode, emulates the VGA modes of most personal computers. The advantage of this mode is that the TLC34076 can take data presented on the feature connectors of most VGA-compatible PC systems into the device on a separate bus, thus requiring no external multiplexing. This feature is particularly useful for systems in which the existing graphics circuitry is on the motherboard. In this instance, it enables implementation of a drop-in graphics card that maintains compatibility with all existing software by using the on-board VGA circuitry but routing the emerging bit-plane data through the TLC34076. This is the default mode at power-up. When the VGA pass-through mode is selected after the device is powered up, the clock selection register, the general control register, and the pixel read mask register are set to their default states automatically.

Since this mode is designed with the feature connector philosophy, all the timing is referenced to CLK0, which is used by default for the VGA pass-through mode. For all the other normal modes, CLK0 – CLK3 are the oscillator sources for DOTCLK, VCLK, and SCLK; all the data and control timing is referenced to SCLK.

2.4.2 Multiplexing Modes

In addition to the VGA pass-through mode, there are four multiplexing modes available, all of which are referred to as normal modes. In each normal mode, a pixel bus width of 8, 16, or 32 bits may be used. Modes 1, 2, and 3 also support a pixel bus width of 4 bits. Data should always be presented on the least significant bits of the pixel bus. For example, when a 16-bit-wide pixel bus is used and there are 8 bits per pixel, each 8-bit pixel should be presented on P0 – P7. All the unused pixel bus terminals should be connected to GND.

Mode 1 uses a single bit-plane to address the color palette. The pixel port bit is fed into bit 0 of the palette address, with the seven high-order address bits being defined by the palette page register (see subsection 2.2.3). This mode has uses in high-resolution monochrome applications such as desktop publishing. This mode allows the maximum amount of multiplexing (a 32:1 ratio), thus giving a pixel bus rate of only 4 MHz at a screen resolution of 1280×1024 pixels. Although only a single-bit plane is used, alteration of the palette page register at the line frequency allows 256 different colors to be displayed simultaneously with two colors per line.

Mode 2 uses two bit-planes to address the color palette. The 2 bits are fed into the low-order address bits of the palette with the six high-order address bits being defined by the palette page register. This mode allows a maximum divide ratio of 16:1 on the pixel bus and is a 4-color alternative to mode 1.

Mode 3 uses four bit-planes to address the color palette. The 4 bits are fed into the low-order address bits of the palette with the four high-order address bits being defined by the palette page register. This mode provides 16 pages of 16 colors and can be used at SCLK divide ratios of 1:8.

Mode 4 uses eight bit-planes to address the color palette. Since all 8 bits of palette address are specified from the pixel port, the page register is not used. This mode allows dot-clock-to-SCLK ratios of 1:1 (8-bit bus), 2:1 (16-bit bus) or 4:1 (32-bit bus). Therefore, in a 32-bit configuration, a 1024×768 pixel screen can be implemented with an external data rate of only 16 MHz.

All normal multiplexing modes can support little-endian (default) and big-endian data formats at the pixel bus inputs (see subsection 2.6.1).

2.4.3 Special Nibble Mode

Mode 5 is the special nibble mode, which is enabled when the general-control register SNM bit 3 is set to 1 and the general-control register SSRT bit 2 is cleared to 0 (see Section 2.11). When the special nibble mode is enabled, it takes precedence over the other modes, and the mux control register setup is ignored. The SFLAG/NFLAG input is then used as a nibble flag to indicate which nibble of each byte holds the pixel data. Special-nibble mode is a variation of the 4-bit pixel mode with a 16-bit pixel width. All 32 inputs (P0 – P31) are connected as four bytes, but the 16-bit data bus is composed of either the lower or upper nibble of each of the four bytes (for more detailed information, see subsection 2.9.2). Since this mode uses four bit-planes for each pixel, they are fed into the low-order address bits of the palette, with the 4 high-order address bits being defined by the palette page register (see subsection 2.2.3).

2.4.4 True-Color Modes

Mode 6 is the true-color mode in which 24, 16, or 15 bits of data are transferred from the pixel port directly to the DACs, but with the same amount of pipeline delay as the overlay data and the control signals ($\overline{\text{BLANK}}$ and Sync). Depending on which true-color mode is selected, overlay is provided by utilizing the remaining bits of the pixel bus to address the palette RAM (see Tables 2–6 and 2–7). This results in a 24-bit RAM output that is then used as overlay information to the DACs. When all of the overlay inputs are cleared to 0, no overlay information is displayed. When a nonzero value is input, the color palette RAM is addressed and the resulting data is then fed through to the DACs and receives priority over the true-color data.

Table 2–7. True-Color Modes

MODE	MUX CONTROL REGISTER BITS†						DATA BITS PER PIXEL‡	PIXEL BUS WIDTH	SCLK DIVIDE RATIO§	OVERLAY BITS PER PIXEL (4)	PIXEL LATCHING SEQUENCE¶
	5	4	3	2	1	0					
6#											
6a	0	0	1	0	0	0	15	16	1	1	1) P15 – P0
6b	0	0	1	0	0	1	16	16	1	N/A	1) P15 – P0
6c	0	0	1	0	1	0	15	32	2	1	1) P15 – P0 2) P31 – P16
6d	0	0	1	0	1	1	16	32	2	N/A	1) P15 – P0 2) P31 – P16
6e	0	0	1	1	1	0	24	32	1	8	1) P31 – P0
6f	0	0	1	1	0	1	24	32	1	8	1) P31 – P0

† Bits 6 and 7 are don't care bits.

‡ This is the number of bits of pixel port (or VGA port in mode 1) information used as color data for each displayed pixel, often referred to as the number of bit-planes. This may be color palette address data (modes 0–5) or DAC data (mode 6).

§ The SCLK divide ratio is the number used for the output clock selection register. It indicates the number of pixels per bus load, or the number of pixels associated with each SCLK pulse. For example, with a 32-bit pixel bus width and eight bit-planes, four pixels comprise each bus load. The SCLK divide ratio is not automatically set by mode selection, but must be written to the output clock selection register.

¶ For each operating mode, the pixel latching sequence indicates the sequence in which pixel port or VGA port data are latched into the device. The latching sequence is initiated by a rising edge on SCLK. For modes in which multiple groups of data are latched, the SCLK rising edge latches all the groups, and the pixel clock shifts them out starting with the low-numbered group. For example, in mode 6d with a 32-bit pixel bus width, the rising edge of SCLK latches all the data groups, and the pixel clock shifts them out in the order P15 – P0 and P31 – P16.

Mode 6 is true-color mode in which 24 bits of color information are transferred directly from the pixel port to the DACs; overlay is implemented with the remaining 8 bits of the pixel bus. The distribution of pixel port data to the DACs is as follows: P31 – P24 are passed to the blue DAC, P23 – P16 are passed to the green DAC, and P15 – P8 are passed to the red DAC. P7 – P0 generate overlay data; this operation can be disabled by either grounding P7 – P0 or by clearing the read mask (see subsection 2.4.6).

NOTE 1: Although leaving unused terminals floating does not adversely affect device operation, tying unused terminals to ground lowers power consumption and is recommended.

Mode 6a is the TARGA compatible (5-5-5) true-color mode. In this 16-bit mode, there are 5 bits of red, 5 bits of green, 5 bits of blue, and an additional overlay bit (see Table 2–8 for the bit definitions).

Table 2–8. True-Color Bit Definitions

Little Endian

PIXEL BUS	P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
DATA BUS	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
a																
b																
c	O	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
d	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
e	O7	O6	O5	O4	O3	O2	O1	O0	R7	R6	R5	R4	R3	R2	R1	R0
f	B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0

PIXEL BUS	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
DATA BUS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
a	O	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
b	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
c	O	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
d	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
e	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
f	R7	R6	R5	R4	R3	R2	R1	R0	O7	O6	O5	O4	O3	O2	O1	O0

Big Endian

PIXEL BUS	P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
DATA BUS	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
a																
b																
c	B0	B1	B2	B3	B4	G0	G1	G2	G3	G4	R0	R1	R2	R3	R4	O
d	B0	B1	B2	B3	B4	G0	G1	G2	G3	G4	G5	R0	R1	R2	R3	R4
e	B0	B1	B2	B3	B4	B5	B6	B7	G0	G1	G2	G3	G4	G5	G6	G7
f	O0	O1	O2	O3	O4	O5	O6	O7	R0	R1	R2	R3	R4	R5	R6	R7

PIXEL BUS	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
DATA BUS	D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
a	B0	B1	B2	B3	B4	G0	G1	G2	G3	G4	R0	R1	R2	R3	R4	O
b	B0	B1	B2	B3	B4	G0	G1	G2	G3	G4	G5	R0	R1	R2	R3	R4
c	B0	B1	B2	B3	B4	G0	G1	G2	G3	G4	R0	R1	R2	R3	R4	O
d	B0	B1	B2	B3	B4	G0	G1	G2	G3	G4	G5	R0	R1	R2	R3	R4
e	R0	R1	R2	R3	R4	R5	R6	R7	O0	O1	O2	O3	O4	O5	O6	O7
f	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7

Mode 6b is the XGA compatible (5-6-5) true-color mode. This 16-bit mode has 5 bits of red, 6 bits of green, and 5 bits of blue data. The overlay function is not enabled in this mode (see Table 2–8 for the exact bit definitions).

Mode 6c is a multiplexed version of mode 6a that allows two 16-bit TARGA-compatible words to be latched into the TLC34076 pixel port with one SCLK. In this mode, the 16-bit word latched on pixel port inputs

P0 – P15 is executed first, while the word latched on P16 – P31 is executed last. The user should program the SCLK divide ratio in the output-clock selection register to divide by two (see Table 2–8 for the exact bit definitions).

Mode 6d is a multiplexed version of mode 6b that allows two 16-bit XGA-compatible words to be latched into the TLC34076 pixel port with one SCLK. In this mode, the 16-bit word latched on pixel port inputs P0 – P15 is executed first, while the word latched on P16 – P31 is executed last. The user should program the SCLK divide ratio in the output-clock selection register to divide by 2 (see Table 2–8 for the bit definitions).

Mode 6e is a 24-bit true-color mode that features 8 bits of data for each color, as well as 8 bits of overlay information. The order in which the color and overlay fields appear in the 32-bit word are the reverse of mode 6f (see Table 2–8 for the bit definitions).

Mode 6f is the 24-bit true-color mode used on the TLC34076. It also features 8 bits of data for each color, as well as 8 bits of overlay information (see Table 2–8 for the bit definitions).

Since only 5 bits (6 bits for green in mode 6b and 6d) are provided for each color in the 16-bit true-color modes (6a–6d), the color data is internally shifted by the TLC34076 to the five MSB positions (six MSB positions for green in modes 6b and 6d) before being presented to the 3-color DACs. The remaining lower 3 bits (lower 2 bits for green in modes 6b and 6d) then clear to 0.

When in true-color modes 6a or 6c, the internal palette page register fills the remaining seven MSBs of overlay data (see subsection 2.2.3). This occurs in these modes because there is only 1 bit of overlay information presented in the true-color word. In order to enable the true-color data to the DACs, all 8 overlay bits must be reset to 0. This can be accomplished by either writing zeros to the internal palette page register and the overlay bit, or by writing zeros to the internal read mask (see subsection 2.4.6).

When in true-color modes 6e or 6f, the data input only works in the 8-bit mode. In other words, when only 6 bits are to be used, the two LSB inputs for each color must be tied to GND. However, the palette, which is used by the overlay input, is still governed by 8/$\overline{6}$-input terminal and the output multiplexer (MUX) selects 8-bit data or 6-bit data accordingly. The 8/$\overline{6}$-input terminal is also valid in the other 16-bit modes as well.

Both little-endian (default) and big-endian data formats are supported by the true-color modes (see subsection 2.6.1 and Table 2–8 for more information).

2.4.5 Multiplex Control Register

The MUX is controlled using the 8-bit mux control register. The bit fields of the register are in Table 2–6 and Table 2–7.

As an example of how to use Table 2–6, suppose that the design goals specify a system with 8 data bits per pixel and the lowest possible SCLK rate. Table 2–6 shows that, for non-VGA pass-through operation, only mode 4 supports an 8-bit pixel depth. The lowest possible SCLK rate within mode 4 is 1:4. This set of conditions are selected by writing the value 1Eh to the mux control register. The pixel latching sequence column shows that, in this mode, pixel-input ports P7 – P0 should be connected to the earliest displayed pixel plane, followed by P15 – P8, P23 – P16, and then P31 – P24 as the last displayed pixel plane. Assuming that VCLK is programmed as DOTCLK/4, Table 2–5 shows that the 1:4 SCLK ratio is selected by writing the value 12h to the output clock selection register. The special nibble mode should also be disabled (see subsections 2.9.2 and 2.11.2).

When the mux control register is loaded with 2Dh, the TLC34076 enters the VGA pass-through mode which is the same condition as the default power-up mode. More details are given in subsection 2.5.4.

2.4.6 Read Masking

The read mask register enables or disables a pixel address bit from addressing the color palette RAM. Each palette address bit is logically ANDed with the corresponding bit from the read mask register before addressing the palette. This function is performed after the addition of the page register bits and, therefore, a zeroing of the read mask results in one unique palette location (location 0) and is not affected by the palette page register contents.

Note also that the read mask can zero the overlay data in the true-color modes. This is a handy way to disable the overlay (enable true-color data to the DACs) for a whole screen.

2.5 Reset

There are three ways to reset the TLC34076:

- Power-on reset
- Hardware reset
- Software reset

2.5.1 Power-On Reset

There is a power-on reset (POR) circuit built into the TLC34076. This POR works at power-on only. Even though this circuitry is provided, it is still recommended for the user to design a hardware reset circuit to ensure the reset condition after power-up as described in subsection 2.5.2.

Once the voltage is stabilized, the default condition for all registers is the VGA mode. When the TLC34076 is reset, the SCLK and VCLK counters are reset as well (see Section 2.3 and subsection 2.5.4).

2.5.2 Hardware Reset

The TLC34076 resets whenever RS3 – RS0 = HHHH and a rising edge occurs on $\overline{WR}$ input. Resetting of the TLC34076 is most reliable when many rising $\overline{WR}$ edges occur during the time RS=HHHH. This scheme (bursting $\overline{WR}$ strobes until the power supply voltage stabilizes) is suggested at power up when a hardware reset approach is used.

The default reset condition is VGA mode, and the values for each register are shown in subsection 2.5.4. Also when the TLC34076 is reset, the SCLK and VCLK counters are reset (see Section 2.3).

2.5.3 Software Reset

Whenever the mux control register is set for VGA pass-through mode after power up, all registers are initialized accordingly. Since VGA pass-through mode is the default condition at power up and hardware reset, the act of selecting the VGA pass-through mode through programming the mux control register is viewed as a software reset. Therefore, whenever mux control register bits 5 – 0 are set to 2Dh, the TLC34076 initiates a software reset. This also resets the SCLK and VCLK counters (see Section 2.3). This is referred to as a software reset, since it is typically initiated by software, unlike POR or hardware resets.

2.5.4 VGA Pass-Through Mode Default Conditions

The value contained in each register after hardware or software reset is shown in Table 2–9.

Table 2–9. VGA Pass-Through Mode Default Conditions

REGISTER NAME	DEFAULT VALUE
Mux control register	2Dh
Input clock selection register	00h
Output clock selection register	3Fh
Palette page register	00h
General control register	03h
Pixel read mask register	FFh
Palette address register	xxh
Palette holding register	xxh
Test register	(Pointing to color palette red value)

2.6 Analog Output Specifications

The DAC outputs are controlled by current sources (three for IOG and two each for IOR and IOB) as shown in Figure 2–6. In the normal case, there is a 7.5-IRE (Institute of Radio Engineers: predecessor to the IEEE) difference between Blank and Black levels, which is shown in Figure 2–7. When a 0-IRE pedestal is desired, it can be selected by resetting bit 4 of the general control register (see subsection 2.11.3). The video output for a 0-IRE pedestal is shown in Figure 2–8.

NOTE:
For a 75-Ω doubly terminated load, the V_{REF} = 1.235 V, R_{SET} = 523 Ω, RS-343A levels and tolerances in recommended operating conditions are assumed.

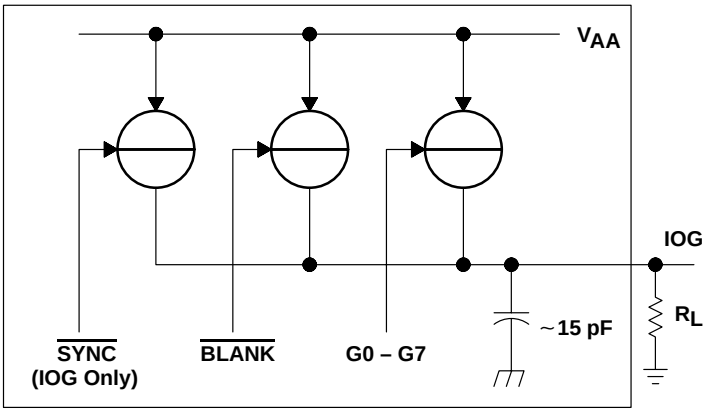


Figure 2–6. Equivalent Circuit of the IOG Current Output

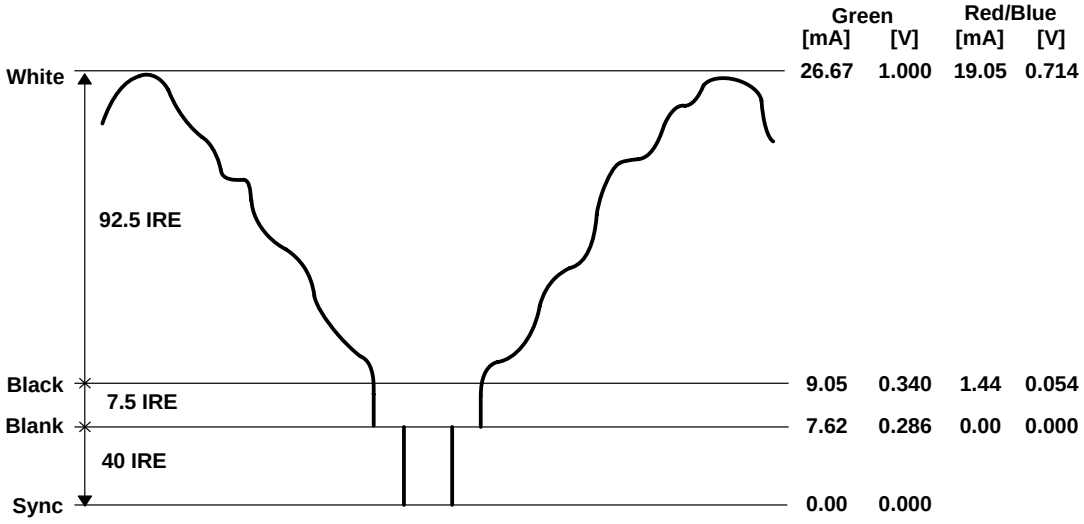


Figure 2–7. 7.5-IRE, 8-Bit Composite Video Output

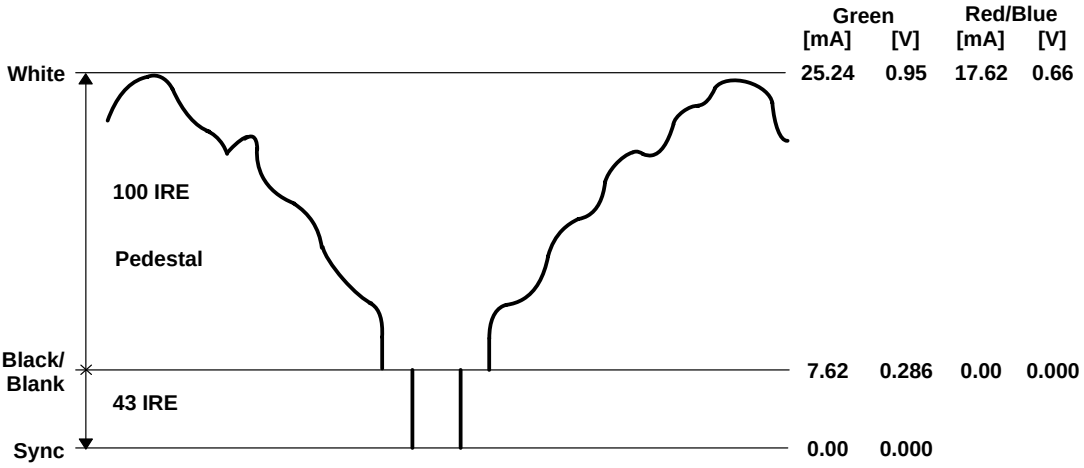


Figure 2–8. 0-IRE, 8-Bit Composite Video Output

A resistor (R_{SET}) is needed to connect FS ADJUST to GND to control the magnitude of the full-scale video signal. The IRE relationships in Figures 2–7 and 2–8 are maintained regardless of the full-scale output current.

The relationship between R_{SET} and the full-scale output current IOG is:

$$R_{SET}\ (\Omega) = K1 \times V_{REF}\ (V) / IOG\ (mA)$$

The full-scale output current on IOR and IOB for a given R_{SET} is:

$$IOR, IOB\ (mA) = K2 \times V_{REF}\ (V) / R_{SET}\ (\Omega)$$

where K1 and K2 are defined as:

IRE LEVEL	IOG		IOR, IOB	
	8-BIT OUTPUT	6-BIT OUTPUT	8-BIT OUTPUT	6-BIT OUTPUT
7.5-IRE	K1 = 11,294	K1 = 11,206	K2 = 8,067	K2 = 7,979
0-IRE	K1 = 10,684	K1 = 10,600	K2 = 7,462	K2 = 7,374

2.7 Frame-Buffer Interface with Little-Endian and Big-Endian Modes

The TLC34076 provides two clock signals for controlling the frame-buffer interface. They are SCLK and VCLK. SCLK can clock out data directly from the VRAM shift registers. Split shift-register transfer functionality is also supported. VCLK clocks and synchronizes control inputs like $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$.

The pixel data presented at the inputs is latched at the rising edge of SCLK in normal mode or the rising edge of CLK0 in VGA pass-through mode. Control inputs $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$ are sampled and latched at the falling edge of VCLK in normal mode, while $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and VGABLANK are latched at the rising edge of CLK0 in VGA pass-through mode. Both data and control signals are lined up at the DAC outputs to the monitor through the internal pipeline delay, so external glue logic is not required. The outputs of the DACs are capable of directly driving a 37.5-Ω load, as in the case of a doubly terminated 75-Ω cable (see Figures 2–7 and 2–8 for nominal output levels).

The frame-buffer interface (pixel bus) supports both little-endian and big-endian data formats for all normal multiplexing and true-color modes of operation. The data-format mode select is controlled by General Control register bit 6 (see Section 2.11). When GCR bit 6 is cleared to 0 (default), the format is set to the little-endian mode. When GCR bit 6 is set to 1, the format is set to the big-endian mode.

In a big-endian mode design the external VRAM data bus bits must be connected in reverse order to the TLC34076 pixel bus (i.e. D31 connected to P0, and D0 connected to P31, etc.). This ensures that the least significant channel always provides the first pixel to be displayed in the normal multiplexing modes.

2.8 $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$

For the normal modes, $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are active-low pulses, and they are passed through true/complement gates to the HSYNCOUT and VSYNCOUT outputs. The output polarities of HSYNCOUT and VSYNCOUT can be programmed through the general control register. However, for the VGA pass-through mode, the polarities needed for monitors are already provided at the feature connector from which $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are sourced, so the TLC34076 passes $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ through to HSYNCOUT and VSYNCOUT without polarity change. As described in Section 2.3 and Figures 2–2 through 2–5, the $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, and $\overline{\text{VSYNC}}$ inputs are sampled and latched on the falling edge of VCLK in the normal modes, and they are latched on the rising edge of the CLK0 input in the VGA pass-through mode (see Figure 3–2 for the detailed timing).

The $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs are used for both the VGA pass-through and normal modes. When the application uses both VGA pass-through and normal modes, an external multiplexer is needed to select $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ between the VGA pass-through mode and the normal mode. The $\overline{\text{MUXOUT}}$ signal is designed for this purpose (see Sections 2.10 and 2.11).

The $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$ signals have internal pipeline delays to align with the data at the DAC outputs. Due to the sample and latch timing delay, it is possible to have active SCLK pulses after the $\overline{\text{BLANK}}$ input becomes active. The relationship between VCLK and SCLK and the internal VCLK sample and latch delay need to be carefully reviewed and programmed (see Section 2.3 and Figures 2–2 and 2–3 for more details).

As shown in Figure 2–6 for the IOG DAC output, active $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ signals turn off the sync current source (after the pipeline delay) independent of the $\overline{\text{BLANK}}$ signal level. In real applications, $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ should only be active (low) when $\overline{\text{BLANK}}$ is active (low).

To alter the polarity of the HSYNCOUT and VSYNCOUT outputs in the normal modes, the MPU must set or clear the corresponding bits in the General Control register (see subsection 2.11.1). Again, these two bits affect only the normal modes, not the VGA pass-through mode. These bits default to 1.

2.9 Split Shift Register Transfer VRAMs and Special Nibble Mode

The following paragraphs describe the operation of the split shift register when effecting a transfer from the VRAMs, and the use of the special nibble mode. The special nibble mode provides a variation of the 4-bit pixel mode with a 16-bit bus width.

2.9.1 Split Shift Register Transfer VRAMs

The TLC34076 directly supports split shift register transfer (SSRT) VRAMs. In order to allow the VRAMs to perform a split shift-register transfer, an extra SCLK cycle must be inserted during the Blank sequence. This is initiated when the SSRT enable bit is set to 1, the SNM bit is reset to 0 , and a rising edge on the SFLAG/NFLAG input terminal is detected. An SCLK pulse is generated within 20 ns of the rising edge of the SFLAG/NFLAG signal. A minimum 15-ns high logic level duration is provided to satisfy all of the 15-ns VRAM requirements. By controlling the SFLAG/NFLAG rise time, the delay time from the rising edge of the VRAM TRG signal to SCLK can be satisfied. The relationship between the SCLK, SFLAG/NFLAG, and $\overline{\text{BLANK}}$ signals is shown in Figure 2-9.

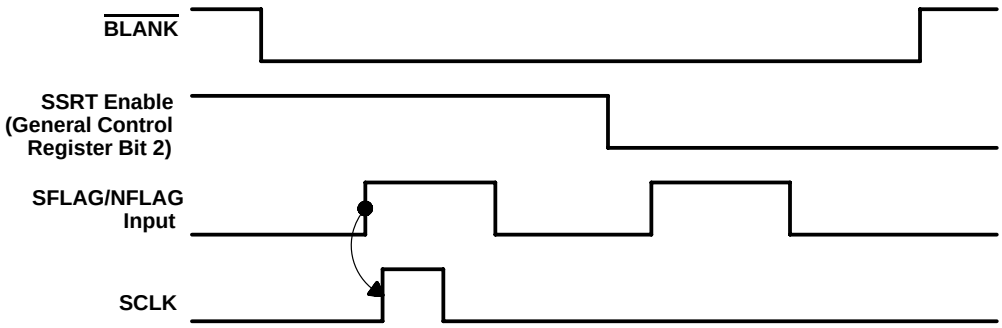


Figure 2–9. Relationship Between SFLAG/NFLAG, $\overline{\text{BLANK}}$, and SCLK

When SFLAG/NFLAG is designed as an R-S latch set by split shift register transfer timing and reset by $\overline{\text{BLANK}}$ going high, the delay from $\overline{\text{BLANK}}$ high to SFLAG/NFLAG low cannot exceed one-half of a SCLK cycle; otherwise, the SCLK generation logic may fail.

When the SSRT function is enabled but SFLAG/NFLAG is held low, SCLK runs as if the SSRT function is disabled. The SFLAG/NFLAG input is not qualified by the BLANK signal and needs to be held low whenever an SSRT SCLK pulse is not desired (see subsection 2.3.1 and Figures 2–2 through 2–8 for more system details).

2.9.2 Special Nibble Mode

Special nibble mode is enabled when the SNM bit (bit 3 in the General Control register) is set to 1 and the SSRT bit (bit 2 in the general control register) is reset to 0 (see Section 2.11). The special nibble mode provides a variation of the 4-bit pixel mode with a 16-bit bus width. While all 32 inputs (P0 – P31) are connected as four bytes, the 16-bit data bus is composed of the lower or upper nibble of each of the four bytes, depending on the level of the SFLAG/NFLAG input. The pixel data is distributed to the 16-bit data bus as shown in Table 2–10.

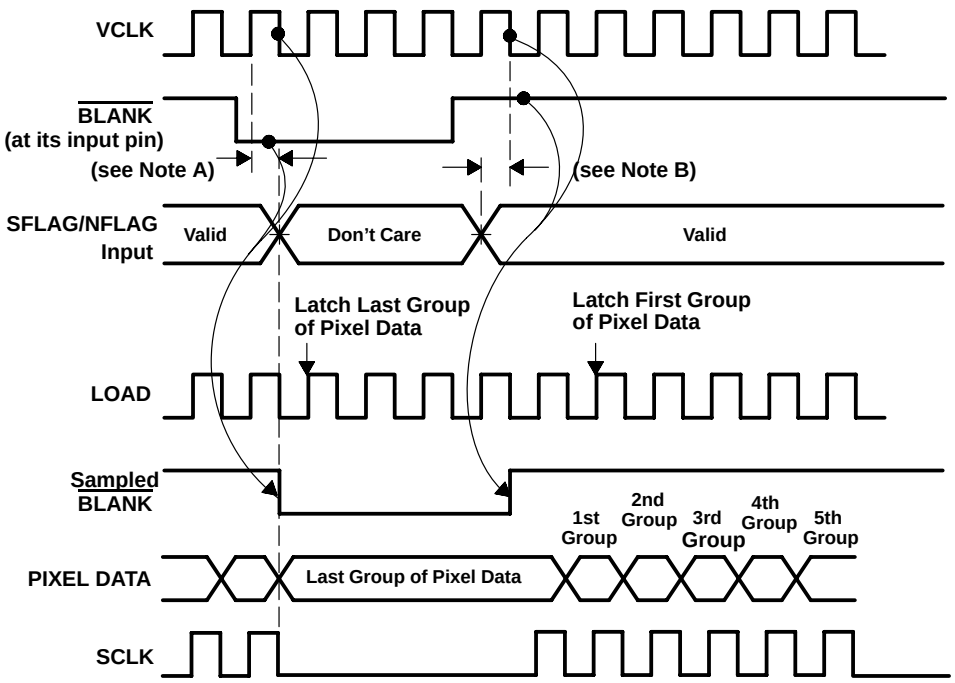
Table 2–10. Pixel Data Distribution in Special Nibble Mode

SNM BIT = 1, SSRT BIT = 0	
SFLAG/NFLAG = 1	**SFLAG/NFLAG = 0**
P7 – P4	P3 – P0
P15 – P12	P11 – P8
P23 – P20	P19 – P16
P31 – P28	P27 – P24

The SFLAG/NFLAG value is not latched by the TLC34076; therefore, it should stay at the same level during the whole active display period, changing levels only during the BLANK signal active time. (see to Figure 2–10, which is similar to Figure 2–2 except that the BLANK signal timing reference to SFLAG/NFLAG is explained). The SFLAG/NFLAG input has to meet the setup time and hold the data long enough to ensure that no pixel data is missed.

CAUTION:

If pixel data are not held valid until both SCLK and BLANK go low, the last few pixels can be missed.



NOTES: A. If the data is not held valid until SCLK and $\overline{\text{BLANK}}$ both go low, the last few pixels could be missed.
B. Setup time to the next VCLK falling edge after $\overline{\text{BLANK}}$ goes high must be met; otherwise, the first pixel data could be missed.

Figure 2–10. SFLAG/NFLAG Timing in Special Nibble Mode

Special nibble mode operates at the line frequency when $\overline{\text{BLANK}}$ is active. However, the typical application of this mode is double frame buffers with pixel data width of 4 bits. While one frame buffer is being displayed on the monitor, the other frame buffer can accept new picture information. SFLAG/NFLAG indicates which frame buffer is being displayed.

SNM and SSRT must be mutually exclusive. Unpredictable operation occurs when both the SNM and SSRT bits are set to 1. The mux control register should be set up as shown in Table 2–6. However, the SNM bit takes precedence over the other mux control register selections. In other words, when the mux control register is set up for another mode but special nibble mode is still enabled in the general control register, the input multiplex circuit takes whatever SCLK divide ratio the mux control register specifies and performs the nibble operation causing operational failure.

During special nibble mode, the input mux circuit latches all 8-bit inputs but only passes on the specified nibble. The specified nibble is stored in the four LSBs of the next register pipe after the input latch, and the four MSBs are cleared to 0 in that register. The register pipe contents are then passed to the read mask block. With this structure, the palette page register still functions normally, providing good flexibility to users.

When the general control register bit 3 = 0 and bit 2 = 0, both split shift-register transfers and the special nibble mode are disabled and the SFLAG/NFLAG input is ignored.

2.10 $\overline{\text{MUXOUT}}$ Output

$\overline{\text{MUXOUT}}$ is a TTL-compatible output. It is software programmable and controls external devices. Its typical application is to select the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs between the VGA pass-through mode and the normal modes. This output is driven low at power up or when the VGA pass-through mode is selected; at any other time it can be programmed to the desired polarity through the general control register bit 7.

2.11 General Control Register

The general control register controls HSYNC and VSYNC polarity, split shift register transfer enabling, special nibble mode, little-endian and big-endian modes, sync control, the ones-accumulation clock source, and the VGA pass-through indicator. The bit field definitions are given in Table 2–11:

Table 2–11. General Control Register Bit Functions

GENERAL CONTROL REGISTER BIT								FUNCTION
7	6	5	4	3	2	1	0	
X	X	X	X	X	X	X	0	HSYNCOUT is active-low
X	X	X	X	X	X	X	1	HSYNCOUT is active-high (default)
X	X	X	X	X	X	0	X	VSYNCOUT is active-low
X	X	X	X	X	X	1	X	VSYNCOUT is active-high (default)
X	X	X	X	X	0	X	X	Disable split shift register transfer (default)
X	X	X	X	0	1	X	X	Enable split shift register transfer
X	X	X	X	0	X	X	X	Disable special nibble mode (default)
X	X	X	X	1	0	X	X	Enable special nibble mode
X	X	X	0	X	X	X	X	0-IRE pedestal (default)
X	X	X	1	X	X	X	X	7.5-IRE pedestal
X	X	0	X	X	X	X	X	Disable sync (default)
X	X	1	X	X	X	X	X	Enable sync
X	0	X	X	X	X	X	X	Little-endian mode (default)
X	1	X	X	X	X	X	X	Big-endian mode
0	X	X	X	X	X	X	X	$\overline{\text{MUXOUT}}$ is low (default)
1	X	X	X	X	X	X	X	$\overline{\text{MUXOUT}}$ is high

2.11.1 HSYNCOUT and VSYNCOUT (Bits 0 and 1)

HSYNCOUT and VSYNCOUT polarity inversion is provided to allow indication to monitors of the current screen resolution. Since the polarities for the VGA pass-through mode are provided at the feature connector, the inputs to the TLC34076 already have right polarities for monitors, so the TLC34076 passes them through with pipeline delay (see Section 2.8). These 2 bits work only in the normal modes, and the input horizontal and vertical syncs are active-low incoming pulses. These 2 bits default to 1 but can be changed by software.

2.11.2 Split Shift Register Transfer Enable (SSRT) and Special Nibble Mode Enable (SNM) (Bits 2 and 3)

Section 2.9 provides a detailed description for SSRT and SNM.

2.11.3 Pedestal Enable Control (Bit 4)

Bit 4 specifies whether a 0- or 7.5-IRE blanking pedestal is to be generated on the video outputs. Having a 0-IRE blanking pedestal means that the Black and Blank levels are the same.

- 0 = 0-IRE pedestal (default)
- 1 = 7.5-IRE pedestal

2.11.4 Sync Enable Control (Bit 5)

Bit 5 specifies whether or not sync information is to be output onto IOG (see Table 2–11). Bit settings are:

- 0 = Disable sync (default)
- 1 = Enable sync

2.11.5 Little-Endian and Big-Endian Mode Control (Bit 6)

Bit 6 specifies either little-endain or big-endian data format for the pixel bus frame-buffer interface (see subsection 2.7.1). Settings are :

- 0 = little endian (default)
- 1 = big endian

2.11.6 $\overline{\text{MUXOUT}}$ (Bit 7)

Bit 7 indicates to external circuitry that the device is running in VGA pass-through mode. The $\overline{\text{MUXOUT}}$ bit does not affect the operation of the device (see Section 2.10). Bit settings are:

- 0 = $\overline{\text{MUXOUT}}$ is low (default in VGA pass-through mode)
- 1 = $\overline{\text{MUXOUT}}$ is high

2.12 Test Register

There are three test functions provided in the TLC34076, and they are all controlled and monitored through the test register. The three test functions are:

- Data flow check
- DAC analog test
- Screen integrity test

The test register has two ports: one for a control word that is accessed by writing to the register location, and one for the data word that is accessed by reading from the register location. Depending on the channel written in the control word, the data read presents the information for that channel.

The control word is 3 bits long and occupies D2 – D0 bit positions. It specifies which of the eight channels to inspect. Table 2–12 and state machine diagrams (see Figure 2–11) show how each channel is addressed.

Table 2–12. Test Mode Selection

D2	D1	D0	CHANNEL
0	0	0	Color palette red value
0	0	1	Color palette green value
0	1	0	Color palette blue value
0	1	1	Identification code
1	0	0	Ones-accumulation red value
1	0	1	Ones-accumulation green value
1	1	0	Ones-accumulation blue value
1	1	1	Analog test

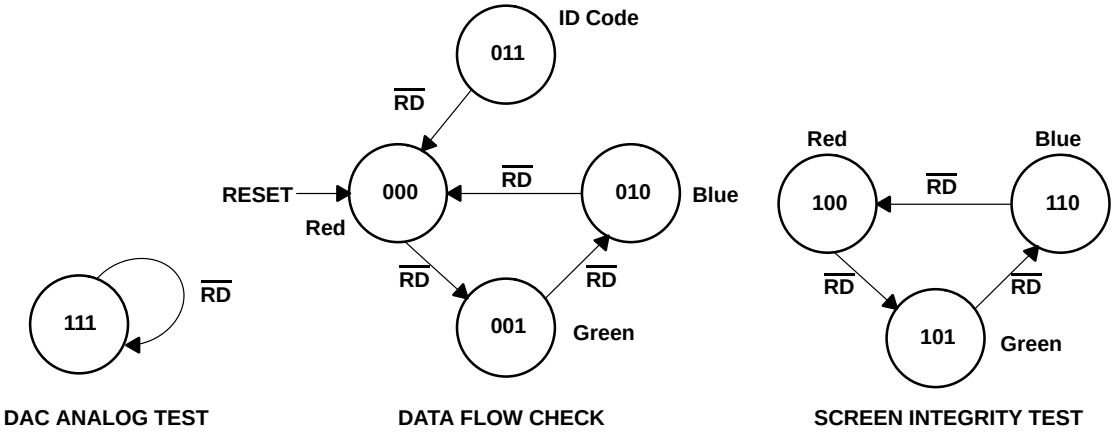


Figure 2–11. Test-Register Control-Word State Diagrams

2.12.1 Frame-Buffer Data Flow Test

The TLC34076 provides a means to check all the data entering each DAC but before the output MUX 8/$\overline{6}$ shift. When accessing these color channels, the data entering the DACs should be kept constant for the entire MPU read cycle. This can be done either by slowing down the dot clock or ensuring that the data is constant for a sufficiently long series of pixels. The value read is the data stored in the color palette location addressed by the data in the input MUX. The read operation causes a post-increment to point to the next color channel, and the post-increment of blue wraps back to red as shown in the state diagram of Figure 2–11. For example, when bits D2 – D0 are written as 001, then three successive reads are performed, and the values read out are green, blue, and red in this sequence.

2.12.2 Identification (ID) Code

The ID code can be used as a software identification for different versions. The ID code in the TLC34076 is static and can be read without consideration of the dot clock or video signals. To be user-friendly, the read post-increment applies to the ID register as well. However, when the state machine goes into the color channel, it does not return to the ID code unless the user writes 011 (binary) to bits D2, D1, and D0 again. If the test register was first written as 011 (binary) in bits D2, D1, and D0, then, when six successive reads are performed, the first value read is the ID, and the last value read is the green.

The ID value defined for the TLC34076 is 76 (hex).

2.12.3 Ones-Accumulation Screen Integrity Test

A technique called ones accumulation can detect errors in fixed screen displays. This type of error detection is useful for system checkout and field diagnostics.

Each of the 256 24-bit words in the TLC34076 internal color palette RAM is composed of three bytes, one each for the red, green, and blue components of the word. When bits D2 – D0 are programmed with the appropriate binary value (see subsection 2.12.4), the TLC34076 monitors the corresponding color byte that is output by the color palette RAM. For example, when bits D2 – D0 are programmed with the value 100, the TLC34076 monitors the red byte. As the current frame is scanned, for each color palette RAM word accessed, the designated color byte is checked to see how many 1 bits it contains, and this number is added to a temporary accumulator, the entire byte is checked, even when 6-bit mode is selected. For example, when the designated color byte contains the value 41h (0100 0001), then the value 2 is added to the temporary accumulator, as 41h contains two bits set at 1. This process is continued until an entire frame has been scanned; the same color byte is monitored for the entire frame. The temporary accumulator truncates any overflow above the value 255. Due to circuit speed limitations, the ones accumulation is

calculated at a speed of (DOTCLK frequency)/2. During the vertical retrace activated by a falling edge on the TLC34076 $\overline{\text{VSYNC}}$ input, the value in the temporary accumulator is transferred into the ones accumulation register, and then the temporary accumulator is reset to 0. The ones-accumulation register is updated only on the falling edge of $\overline{\text{VSYNC}}$, not by any vertical sync pulses coded into the composite video signal. Before the next frame scan begins, the TLC34076 automatically changes the value in bits D2 – D0 so that the ones accumulation performed during the next frame scan is for a different color byte (see the screen integrity test state diagram of Figure 2–11). As long as the screen display remains fixed, the ones-accumulation value for a particular color byte should not change; when it does, an error has occurred.

Since ones accumulation is calculated at DOTCLK/2 rate, there is uncertainty as to whether it starts its accumulation on an odd or even pixel. Regardless of whether the accumulation is performed on odd or even pixels, subsequent screens are accumulated starting at the same point every time, unless the part is reset or the DOTCLK source changes.

2.12.4 Analog Test

An analog test compares the voltage amplitudes of the analog red-green-blue (RGB) outputs to each other and to a 145-mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs or not and whether the DACs are functional. To perform an analog test, bits D2 – D0 must be set to 111; D7 – D4 bits are set as shown in Table 2–13. Bit D3 contains the result of the analog test. The bit coding for the analog comparison of bits D2 – D7 is shown in Table 2–14.

Table 2–13. Test Register Bit Definitions for Analog Test

BIT DEFINITION	READ/WRITE
D7: Red select	Read/Write
D6: Green select	Read/Write
D5: Blue select	Read/Write
D4: 145-mV reference select	Read/Write
D3: Result	Read

Table 2–14. Bit Coding for Analog Comparisons of Bits D7 – D4

D7 – D4	OPERATION	IF D3 = 1	IF D3 = 0
0000	Normal operation	Don't care	Don't care
1010	Red DAC compared to blue DAC	Red > blue	Red < blue
1001	Red DAC compared to 145-mV reference	Red > 145 mV	Red < 145 mV
0110	Green DAC compared to blue DAC	Green > blue	Green < blue
0101	Green DAC compared to 145-mV reference	Green > 145 mV	Green < 145 mV

NOTE 2: All the outputs have to be terminated to compare the voltage.

Figure 2–12 is a schematic of the internal comparator circuitry for the analog comparison test.

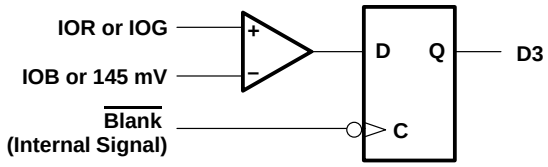


Figure 2–12. Internal Comparator Circuitry for Analog Test

The result of the analog comparison is strobed into bit D3 at the falling edge of an internal signal derived from the input BLANK signal. In order to have stable inputs to the comparator, the DAC should be set to a constant level between syncs. For normal operation, the data flow check, and the screen integrity test, bits D7 – D4 must be set to 0.

3 Electrical Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 7 V
Input voltage range, V_I . . . . . –0.5 V to V_{DD} + 0.5 V
Analog output short-circuit duration to any power supply or common . . . . . unlimited
Operating free-air temperature range, T_A: TLC34076C . . . . . 0°C to 70°C
TLC34076M . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Junction temperature, T_J . . . . . 175°C
Case temperature for 10 seconds T_C: FN and GA package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminal.

3.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75	5	5.25	V
V_{REF}	Reference voltage		1.15	1.235	1.26	V
V_{IH}	High-level input voltage	TTL inputs	2.4		V_{DD}+0.5	V
V_{IL}	Low-level input voltage	TTL inputs			0.8	V
V_{ID}	Differential input voltage	ECL inputs	0.6		6	V
V_{IC}	Common-mode input voltage	ECL inputs	2.85	3.15	V_{DD} – 0.5	V
R_L	Output load resistance			37.5		Ω
R_{SET}	FS ADJUST resistor			523		Ω
T_A	Operating free-air temperature	TLC34076C	0		70	°C
		TLC34076M	–55		125	

3.3 Electrical Characteristics

3.3.1 Electrical Characteristics for TLC34076C Over Operating Free-Air Temperature Range

PARAMETER				TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage			I_{OH} = –800 μA	2.4			V
V_{OL}	Low-level output voltage		$\overline{D0}$ – $\overline{D7}$, $\overline{MUXOUT}$, VCLK	I_{OL} = 3.2 mA			0.4	V
			HSYNCOUT, VSYNCOUT	I_{OL} = 15 mA			0.4	
			SCLK	I_{OL} = 18 mA			0.4	
I_{IH}	High-level input current		TTL inputs	V_I = 2.4 V			1	μA
			ECL inputs	V_I = 4 V			1	
I_{IL}	Low-level input current		TTL inputs	V_I = 0.8 V			–1	μA
			ECL inputs	V_I = 0.4 V			–1	
I_{DD}	Supply current	Pseudo-color mode	TLC34076-85	V_{DD} = 5 V, See Note 2			450	mA
			TLC34076-110				475	
			TLC34076-135				535	
			TLC34076-170				525	
		True-color mode	TLC34076-85	V_{DD} = 5 V, See Note 2			475	
			TLC34076-110				475	
			TLC34076-135				475	
			TLC34076-170				475	
I_{OZ}	High-impedance-state output current						10	μA
C_i	Input capacitance		TTL inputs	f = 1 MHz, V_I = 2.4 V		4		pF
			ECL inputs	f = 1 MHz, V_I = 4 V		4		

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

NOTE 2: I_{DD} is measured with the dot clock running at the maximum specified frequency, SCLK frequency = DOTCLK frequency/4, and the palette RAM loaded with full-range toggling patterns (00h/00h/FFh/FFh/00h/00h/FFh/FFh/ . . .). Pseudo-color mode is also known as color indexing mode.

3.3.2 Electrical Characteristics for TLC34076M Over Operating Free-Air Temperature Range

PARAMETERS				TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage			I_{OH} = –800 µA, V_{DD} = 4.75 V	2.4			V
V_{OL}	Low-level output voltage		$\overline{D0 – D7}$, $\overline{MUXOUT}$, VCLK	I_{OL} = 3.2 mA, V_{DD} = 4.75 V			0.4	V
			HSYNCOUT, VSYNCOUT	I_{OL} = 15 mA, V_{DD} = 4.75 V			0.4	
			SCLK	I_{OL} = 18 mA, V_{DD} = 4.75 V			0.4	
I_{IH}	High-level input current		TTL inputs	V_I = 2.4 V, V_{DD} = 5.25 V			10	µA
			ECL inputs	V_I = 4 V, V_{DD} = 5.25 V			10	
I_{IL}	Low-level input current		TTL inputs	V_I = 0.8 V, V_{DD} = 5.25 V			–10	µA
			ECL inputs	V_I = 0.8 V, V_{DD} = 5.25 V			–10	
I_{DD}	Supply current	Pseudo-color mode	TLC34076M-135	V_{DD} = 5 V, See Note 2			535	mA
		True-color mode	TLC34076M-135				475	
I_{OZ}	High-impedance-state output current			V_{DD} = 5.25 V		10	25	µA
C_i	Input capacitance		TTL inputs	f = 1 MHz, V_I = 2.4 V		4		pF
			ECL inputs	f = 1 MHz, V_I = 4 V		4		

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

NOTE 2: I_{DD} is measured with the dot clock running at the maximum specified frequency, SCLK frequency = DOTCLK frequency/4, and the palette RAM loaded with full-range toggling patterns (00h/00h/FFh/FFh/00h/00h/FFh/FFh/ . . .). Pseudo-color mode is also known as color-indexing mode.

3.4 Operating Characteristics

The following tables outline the operating characteristics for the TLC34076C and TLC34076M.

3.4.1 Operating Characteristics for TLC34076C Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution (each DAC)	8/$\overline{6}$ high		8		bits
		8/$\overline{6}$ low		6		
E_L	End-point linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
E_D	Differential linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
	Gray-scale error				5%	
	Output current (see Note 4)	White level relative to Blank	17.69	19.05	20.4	mA
		White level relative to Black (7.5 IRE only)	16.74	17.62	18.5	
		Black level relative to Blank (7.5 IRE only)	0.95	1.44	1.9	
		Blank level on IOR, IOB	0	5	50	µA
		Blank level on IOG (with Sync enabled)	6.29	7.6	8.96	mA
		Sync level on IOG (with Sync enabled)	0	5	50	µA
		One LSB (8/$\overline{6}$ high)		69.1		µA
		One LSB (8/$\overline{6}$ low)		276.4		
	DAC-to-DAC matching outputs			2%	5%	
	DAC-to-DAC crosstalk			–20		dB
V_{oc}	Output compliance voltage		–1		1.2	V
V_{REF}	Voltage reference output voltage		1.15	1.235	1.26	V
Z_O	Output impedance			50		kΩ
C_O	Output capacitance	f = 1 MHz, I_{OUT} = 0		13		pF
	Clock and data feedthrough			–20		dB
	Glitch impulse (see Note 3)			50		pV-s
		Normal mode	1 SCLK + 9 DOTCLK			
		VGA pass-through mode	7.5 DOTCLK			

NOTES: 3. Glitch impulse does not include clock and data feedthrough. The –3-dB test bandwidth is twice the clock rate.

4. Unless otherwise specified, test conditions for RS343-A video signals are those listed in the Recommended Operating Conditions, using external voltage reference V_{REF} = 1.235 V and R_{SET} = 523 Ω. When using the internal voltage reference, R_{SET} may need to be adjusted to meet these limits.

3.4.2 Operating Characteristics for TLC34076M Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Resolution (each DAC)	8/$\overline{6}$ high		8		bits
		8/$\overline{6}$ low		6		
E_L	End-point linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
E_D	Differential linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
	Gray-scale error				5%	
I_O	Output current (see Note 4)	White level relative to Blank	17.69	19.05	20.4	mA
		White level relative to Black (7.5 IRE only)	16.74	17.62	18.5	
		Black level relative to Blank (7.5 IRE only)	0.95	1.44	1.9	
		Blank level on IOR, IOB	−50	5	50	μA
		Blank level on IOG (with Sync enabled)	6.29	7.6	8.96	mA
		Sync level on IOG (with Sync enabled)	−50	5	50	μA
		One LSB (8/$\overline{6}$ high)		69.1		μA
		One LSB (8/$\overline{6}$ low)		276.4		
	DAC-to-DAC matching outputs			2%	5%	
	DAC-to-DAC crosstalk			−20		dB
V_{oc}	Output compliance voltage		−0.4		1.2	V
V_{REF}	Voltage reference output voltage		1.1	1.235	1.3	V
Z_O	Output impedance			50		kΩ
C_O	Output capacitance	f = 1 MHz, I_O = 0		13		pF
	Clock and data feedthrough			–20		dB
	Glitch impulse (see Note 3)			50		pV-s
	Pipeline delay	Normal mode	1 SCLK + 9 dot clock			periods
		VGA pass-through mode	7.5 dot clock			

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

NOTES: 3. Glitch impulse does not include clock and data feedthrough. The −3-dB test bandwidth is twice the clock rate.

4. Unless otherwise specified, test conditions for RS343-A video signals are those listed in the Recommended Operating Conditions, using external voltage reference V_{REF} = 1.235 V and R_{SET} = 523Ω. When using the internal voltage reference, R_{SET} may need to be adjusted to meet these limits.

3.5 Timing Requirements

The following tables outline the timing requirements for the TLC34076C and TLC34076M.

3.5.1 Timing Requirements for TLC34076C Over Recommended Ranges of Supply Voltages and Operating Temperature (see Note 5)

			-85		-110		UNIT
			MIN	MAX	MIN	MAX	
	DOTCLK frequency			85		110	MHz
	CLK0 frequency for VGA pass-through mode			85		85	MHz
t_{cyc}	Cycle time, CLK0 – CLK3 (see Figure 3–2)	TTL	11.8		9.1		ns
		ECL	11.8		9.1		
t_{su1}	Setup time, RS0 – RS3 valid before $\overline{RD}$ or $\overline{WR}\downarrow$ (see Figure 3–1)		10		10		ns
t_{h1}	Hold time, RS0 – RS3 valid after $\overline{RD}$ or $\overline{WR}$ low (see Figure 3–1)		10		10		ns
t_{su2}	Setup time, D0 – D7 valid before $\overline{WR}\uparrow$ (see Figure 3–1)		35		35		ns
t_{h2}	Hold time, D0 – D7 valid after $\overline{WR}$ high (see Figure 3–1)		0		0		ns
t_{su3}	Setup time, VGA0 – VGA7 and $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{VGABLANK}$ valid before CLK0-CLK3$\uparrow$ (see Figure 3–2)		2		2		ns
t_{h3}	Hold time, VGA0 – VGA7 and $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{VGABLANK}$ valid after CLK0 high (see Figure 3–2)		2		2		ns
t_{su4}	Setup time, P0 – P31 valid before SCLK$\uparrow$ (see Figure 3–2)		2		2		ns
t_{h4}	Hold time, P0 – P31 valid after SCLK high (see Figure 3–2)		5		5		ns
t_{su5}	Setup time, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ valid before VCLK low (see Figure 3–2)		5		5		ns
t_{h5}	Hold time, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ valid after VCLK$\downarrow$ (see Figure 3–2)		2		2		ns
t_{w1}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ low (see Figure 3–1)		50		50		ns
t_{w2}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ high (see Figure 3–1)		30		30		ns
t_{w3}	Pulse duration, CLK0–CLK3 high (see Figure 3–2)	TTL	4		3.5		ns
		ECL	4		3.5		
t_{w4}	Pulse duration, CLK0–CLK3 low (see Figure 3–2)	TTL	4		3.5		ns
		ECL	4		3.5		
t_{w5}	Pulse duration, SFLAG/NFLAG high (see Note 6 and Figure 3–3)		30		30		ns

NOTES: 5. TTL input signals are 0 to 3 V with less than 3 ns rise/fall time between the 10% and 90% levels, unless otherwise specified. ECL input signals are $V_{DD}-1.8$ V to $V_{DD}-0.8$ V with less than 2 ns rise/fall time between the 20% and 80% levels. For input and output signals, timing reference points are at the 10% and 90% signal levels. Analog output loads are less than 10 pF. D0 – D7 output loads are less than 50 pF. All other output loads are less than 50 pF, unless otherwise specified.

6. This parameter applies when the split shift–register transfer (SSRT) function is enabled (see subsection 2.9.1 for details).

3.5.1 Timing Requirements for TLC34076C Over Recommended Ranges of Supply Voltages and Operating Temperature (see Note 5) (Continued)

			-135		-170		UNIT
			MIN	MAX	MIN	MAX	
	DOTCLK frequency			135		170	MHz
	CLK0 frequency for VGA pass-through mode			85		85	MHz
t_{cyc}	Clock cycle time, CLK0-CLK3 (see Figure 3–2)	TTL	7.4		7.4		ns
		ECL	7.4		5.8		
t_{su1}	Setup time, RS0 – RS3 valid before $\overline{RD}$ or $\overline{WR}\downarrow$ (see Figure 3–1)		10		10		ns
t_{h1}	Hold time, RS0 – RS3 valid after $\overline{RD}$ or $\overline{WR}$ low (see Figure 3–1)		10		10		ns
t_{su2}	Setup time, D0 – D7 valid before $\overline{WR}\uparrow$ (see Figure 3–1)		35		35		ns
t_{h2}	Hold time, D0 – D7 valid after $\overline{WR}$ high (see Figure 3–1)		0		0		ns
t_{su3}	Setup time, VGA0 – VGA7, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{VGABLANK}$ valid before CLK0$\uparrow$ (see Figure 3–2)		2		2		ns
t_{h3}	Hold time, VGA0 – VGA7, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{VGABLANK}$ valid after CLK0 high (see Figure 3–2)		2		2		ns
t_{su4}	Setup time, P0 – P31 valid before SCLK$\uparrow$ (see Figure 3–2)		0		0		ns
t_{h4}	Hold time, P0 – P31 valid after SCLK high (see Figure 3–2)		5		5		ns
t_{su5}	Setup time, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ valid before VCLK low (see Figure 3–2)		5		5		ns
t_{h5}	Hold time, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ valid after VCLK low (see Figure 3–2)		2		2		ns
t_{w1}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ low (see Figure 3–1)		50		50		ns
t_{w2}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ high (see Figure 3–1)		30		30		ns
t_{w3}	Pulse duration, CLK0 –CLK3 high (see Figure 3–2)	TTL	3		3		ns
		ECL	3		2.5		
t_{w4}	Pulse duration, CLK0 –CLK3 low (see Figure 3–2)	TTL	3		3		ns
		ECL	3		2.5		
t_{w5}	Pulse duration, SFLAG/NFLAG high (see Note 6 and Figure 3–3)		30		30		ns

NOTES: 5. TTL input signals are 0 to 3 V with less than 3 ns rise/fall time between the 10% and 90% levels, unless otherwise specified. ECL input signals are $V_{DD}-1.8$ V to $V_{DD}-0.8$ V with less than 2 ns rise/fall time between the 20% and 80% levels. For input and output signals, timing reference points are at the 10% and 90% signal levels. Analog output loads are less than 10 pF. D0 – D7 output loads are less than 50 pF. All other output loads are less than 50 pF, unless otherwise specified.

6. This parameter applies when the split shift-register transfer (SSRT) function is enabled (see subsection 2.9.1 for details).

3.5.2 Timing Requirements for TLC34076M Over Recommended Ranges of Supply Voltages and Operating Temperature (see Note 5)

			MIN	NOM	MAX	UNIT
	Dot-clock frequency				135	MHz
	CLK0 frequency for VGA pass-through mode				85	MHz
t_c	Cycle time, CLK0 – CLK3 (see Figure 3–2)	TTL	7.4			ns
		ECL	7.4			
t_{su1}	Setup time, RS0 – RS3 valid before $\overline{RD}$ or $\overline{WR}\downarrow$ (see Figure 3–1)		10			ns
t_{h1}	Hold time, RS0 – RS3 valid after $\overline{RD}$ or $\overline{WR}$ low (see Figure 3–1)		10			ns
t_{su2}	Setup time, D0 – D7 valid before $\overline{WR}\uparrow$ (see Figure 3–1)		35			ns
t_{h2}	Hold time, D0 – D7 valid after $\overline{WR}$ high (see Figure 3–1)		0			ns
t_{su3}	Setup time, VGA0 – VGA7 and $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{VGABLANK}$ valid before CLK0-CLK3$\uparrow$ (see Figure 3–2)		2			ns
t_{h3}	Hold time, VGA0 – VGA7 and $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{VGABLANK}$ valid after CLK0 high (see Figure 3–2)		2			ns
t_{su4}	Setup time, P0 – P31 valid before SCLK$\uparrow$ (see Figure 3–2)		0			ns
t_{h4}	Hold time, P0 – P31 valid after SCLK high (see Figure 3–2)		8			ns
t_{su5}	Setup time, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ valid before VCLK$\downarrow$ (see Figure 3–2)		5			ns
t_{h5}	Hold time, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ valid after VCLK low (see Figure 3–2)		2			ns
t_{w1}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ low (see Figure 3–1)		50			ns
t_{w2}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ high (see Figure 3–1)		30			ns
t_{w3}	Pulse duration, CLK0 – CLK3 high (see Figure 3–2)	TTL		3		ns
		ECL		3		
t_{w4}	Pulse duration, CLK0 – CLK3 low (see Figure 3–2)	TTL		3		ns
		ECL		3		
t_{w5}	Pulse duration, SFLAG/NFLAG high (see Note 6 and Figure 3–3)			30		ns

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

NOTES: 5. TTL input signals are 0 to 3 V with less than 3 ns rise/fall time between the 10% and 90% levels, unless otherwise specified. ECL input signals are $V_{DD}-1.8$ V to $V_{DD}-0.8$ V with less than 2 ns rise/fall time between the 20% and 80% levels. For input and output signals, timing reference points are at the 10% and 90% signal levels. Analog output loads are less than 10 pF. D0 – D7 output loads are less than 50 pF. All other output loads are less than 50 pF, unless otherwise specified.

6. This parameter applies when the split shift register transfer (SSRT) function is enabled (see subsection 2.9.1 for details).

3.6 Switching Characteristics for TLC34076C and TLC34076M Over Recommended Ranges of Supply Voltages and Operating Temperature

PARAMETER		-85			-110			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
	SCLK frequency (see Note 7)			85			85	MHz
	VCLK frequency			85			85	MHz
t_{en}	Enable time, $\overline{RD}$ low to D0 – D7 valid (see Figure 3–1)			40			40	ns
t_{dis}	Disable time, $\overline{RD}$ high to D0 – D7 disabled (see Figure 3–1)			17			17	ns
t_v	Valid time, D0 – D7 valid after $\overline{RD}$ high (see Figure 3–1)	5			5			ns
t_{PLH}	Propagation delay, SFLAG/NFLAG high to SCLK↑ (see Note 8 and Figure 3–3)	0		20	0		20	ns
t_{d1}	Delay time, $\overline{RD}$ low to D0 – D7 starting to turn on (see Figure 3–1)	5			5			ns
t_{d2}	Delay time, selected input clock high/low to DOTCLK (internal signal) high/low (see Figure 3–2)		7			7		ns
t_{d3}	Delay time, DOTCLK high/low to VCLK high/low (see Figure 3–2)		6			6		ns
t_{d4}	Delay time, VCLK high/low to SCLK high/low (see Note 9 and Figure 3–2)	0		5	0		5	ns
t_{d5}	Delay time, DOTCLK high/low to SCLK high/low (see Figure 3–2)		8			8		ns
t_{d6}	Delay time, DOTCLK high to IOR/IOG/IOB active (analog output delay time) (see Note 10 and Figure 3–2)		20			20		ns
t_{d7}	Analog output settling time (see Note 11 and Figure 3–2)			8			6	ns
t_{d8}	Delay time, DOTCLK high to HSYNCOUT and VSYNCOUT valid (see Figure 3–2)		5			3		ns
t_{w6}	Pulse duration, SCLK high (see Note 12 and Figure 3–3)	15		55	15		55	ns
t_r	Rise time at HSYNCOUT analog output (see Note 13 and Figure 3–2)		2			2		ns
	Analog output skew	0		2	0		2	ns

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

NOTES: 7. SCLK can drive an output capacitive load up to 60 pF with worst-case transition time between the 10% and 90% levels less than 4 ns (typical 3 ns). SCLK can drive output capacitive loads up to 120 pF, with typical transition time (10% to 90%) of 4 ns.

8. This parameter applies when the split shift-register transfer (SSRT) function is enabled (see subsection 2.9.1 for details).
9. VCLK frequency = SCLK frequency.
10. Measured from the 90% point of the rising edge of DOTCLK to 50% of the full-scale transition.
11. Measured from the 50% point of the full-scale transition to the point at which the output has settled, within ± 1 LSB (settling time does not include clock and data feedthrough).
12. SCLK can be programmed to latch pixel data at the input port up to this limit. However, the SCLK output buffer can only be used up to the SCLK frequency limit of 85 MHz.
13. Measured between 10% and 90% of the full-scale transition.

3.6 Switching Characteristics (TLC34076C and TLC34076M) Over Recommended Ranges of Supply Voltages and Operating Temperature (Continued)

PARAMETER		-135			-170			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
	SCLK frequency (see Note 7)			85			85	MHz
	VCLK frequency			85			85	MHz
t_{en}	Enable time, $\overline{RD}$ low to D0 – D7 valid (see Figure 3–1)			40			40	ns
t_{dis}	Disable time, $\overline{RD}$ high to D0 – D7 disabled (see Figure 3–1)			17			17	ns
t_v	Valid time, D0 – D7 valid after $\overline{RD}$ high (see Figure 3–1)	5			5			ns
t_{PLH}	Propagation delay, SFLAG/NFLAG high to SCLK ↑ (see Note 8 and Figure 3–3)	0		20	0		20	ns
t_{d1}	Delay time, $\overline{RD}$ low to D0 – D7 valid (see Figure 3–1)	5			5			ns
t_{d2}	Delay time, selected input clock high/low to DOTCLK (internal signal) high/low (see Figure 3–2)		7			7		ns
t_{d3}	Delay time, DOTCLK high/low to VCLK high/low (see Figure 3–2)		6			6		ns
t_{d4}	Delay time, VCLK high/low to SCLK high/low (see Note 9 and Figure 3–2)	0		5	0		5	ns
t_{d5}	Delay time, DOTCLK high/low to SCLK high/low (see Figure 3–2)		8			8	5	ns

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

NOTES: 7. SCLK can drive output capacitive loads up to 60 pF, with worst case transition time between 10% and 90% levels less than 4 ns (typical 3 ns). SCLK can drive output capacitive loads up to 120 pF, with typical transition time (10% to 90%) of 4 ns.

8. This parameter applies when the split shift-register transfer (SSRT) function is enabled (see subsection 2.9.1 for details).
9. VCLK frequency = SCLK frequency.
10. Measured from the 90% point of the rising edge of DOTCLK to 50% of the full-scale transition.
11. Measured from the 50% point of the full-scale transition to the point at which the output has settled, within ± 1 LSB (settling time does not include clock and data feedthrough).
12. SCLK can be programmed to latch pixel data at the input port up to this limit. However, the SCLK output buffer can only be used up to the SCLK frequency limit of 85 MHz.
13. Measured between 10% and 90% of the full-scale transition.

3.6 Switching Characteristics (TLC34076C and TLC34076M) Over Recommended Ranges of Supply Voltages and Operating Temperature (Continued)

PARAMETER		-135			-170			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{d6}	Delay time, DOTCLK high to IOR/IOG/IOB active (analog output delay time) (see Note 10 and Figure 3–2)		20			20		ns
t_{d7}	Analog output settling time (see Note 11 and Figure 3–2)			6		5		ns
t_{d8}	Delay time, DOTCLK high to HSYNCOUT and VSYNCOUT valid (see Figure 3–2)		3			3		ns
t_{w6}	Pulse duration, SCLK high (see Note 8 and Figure 3–3)	15		55				ns
	Pixel data latching frequency (see Note 12)						110	MHz
t_r	Rise time at HSYNCOUT Analog output (see Note 13 and Figure 3–2)		2			2		ns
	Analog output skew	0		2	0		2	ns

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

8. This parameter applies when the split shift-register transfer (SSRT) function is enabled (see subsection 2.9.1 for details).
10. Measured from the 90% point of the rising edge of DOTCLK to 50% of the full-scale transition.
11. Measured from the 50% point of the full-scale transition to the point at which the output has settled, within ± 1 LSB (settling time does not include clock and data feedthrough).
12. SCLK can be programmed to latch pixel data at the input port up to this limit. However, the SCLK output buffer can only be used up to the SCLK frequency limit of 85 MHz.
13. Measured between 10% and 90% of the full-scale transition.

3.7 Timing Diagrams

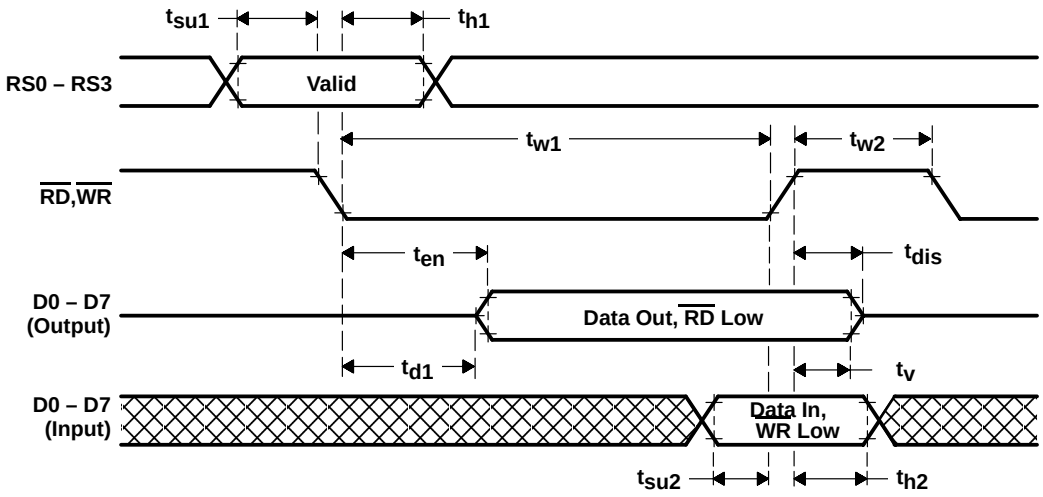


Figure 3–1. MPU Interface Timing

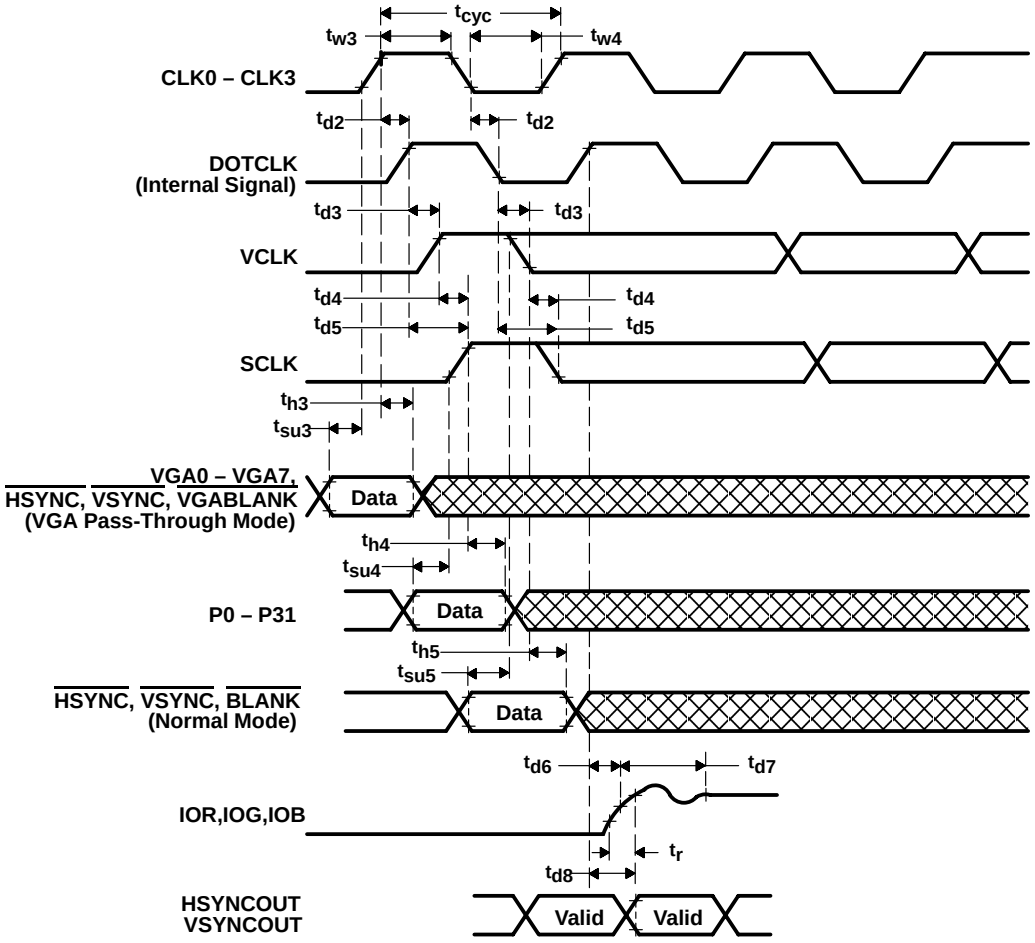


Figure 3–2. Video Input/Output Timing

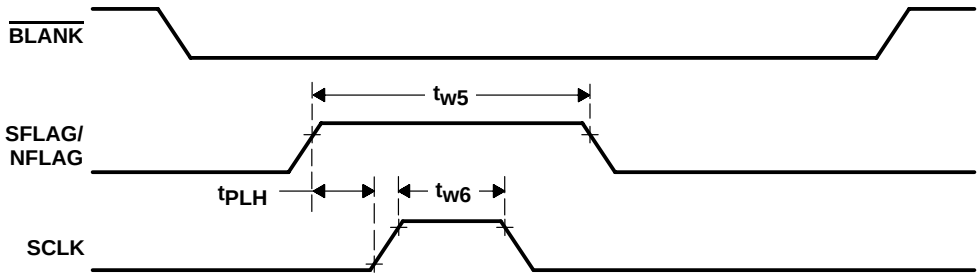


Figure 3–3. SFLAG/NFLAG Timing (When SSRT Function is Enabled)

Appendix A
SCLK/VCLK and the TMS340x0

While the TLC34076 SCLK and VCLK outputs are designed for compatibility with all graphics systems, they are also tightly coupled with the TMS340x0 graphics system processors. All the timing requirements of the TMS340x0 have been considered. However, there are a few points that need to be explained with regard to applications.

VCLK

All the video control signals in the TMS340x0 (i.e., $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, and $\overline{\text{VSYNC}}$) are triggered and generated from the falling edge of VCLK. The fact that the TLC34076 uses the falling edge to sample and latch the $\overline{\text{BLANK}}$ input gives users maximum freedom to choose the frequency of VCLK and interconnect the TLC34076 with the TMS340x0 GSP without glue logic. Needless to say, the VCLK frequency needs to be selected to be compatible with the minimum VCLK period required by the TMS340x0.

In the TMS340x0, the same VCLK falling edge that generates $\overline{\text{BLANK}}$ requests a screen refresh. When the VCLK period is longer than 16 TQs (TQ is the period of the TMS340x0 CLKIN), it is possible that the last SCLK pulse could be used falsely to transfer the VRAM data from memory to the shift register along with the last pixel transfer. The first SCLK pulse for the next scan line would then shift the first pixel data out of the pipe and the screen would then falsely start from the second pixel.

SCLK and SFLAG

The TLC34076 SCLK signal is compatible with current 10 ns and slower VRAMs. When split-shift register transfers are used, one SCLK pulse has to be generated between the regular shift register transfer and the split-shift register transfer to ensure correct operation. The SFLAG input is designed for this purpose. SFLAG can be generated from a programmable logic array and triggered by the rising edge of the $\overline{\text{TR}}/\overline{\text{QE}}$ signal or the rising edge of the $\overline{\text{RAS}}$ signal of the regular shift register transfer cycle. $\overline{\text{TR}}/\overline{\text{QE}}$ can be used if the minimum delay from when the VRAM $\overline{\text{TRG}}$ signal goes high to SCLK going high can be met by the programmable logic array delay; otherwise, $\overline{\text{RAS}}$ can be used.

Appendix B
Printed Circuit Board Layout Considerations

Printed Circuit Board (PCB) Considerations

A four-layer printed-circuit board (PCB) should be used with the TLC34076, one layer each for 5-V power and GND and two layers for signals. The layout should be optimized for the lowest possible noise on the TLC34076 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{DD} and GND terminals should be minimized so as to reduce inductive ringing. The terminal assignments for the TLC34076 P0 – P31 inputs were selected for minimum interconnect lengths between these inputs and the VRAM pixel data outputs. The TLC34076 should be located as close to the output connectors as possible to minimize noise pickup and reflections due to impedance mismatching.

Ground Plane

A single ground plane is recommended for both the TLC34076 and the rest of the logic. Separate digital and analog ground planes are not needed.

Power Plane

Split power planes are recommended for the TLC34076 and the rest of the logic. The TLC34076 and its associated analog circuitry should have their own power plane, referred to as AV_{CC} in Figure B–1. The two power planes should be connected at a single point through a ferrite bead as shown in Figures B–1, B–2, and B–3. This bead should be located within 3 inches of the TLC34076.

Supply Decoupling

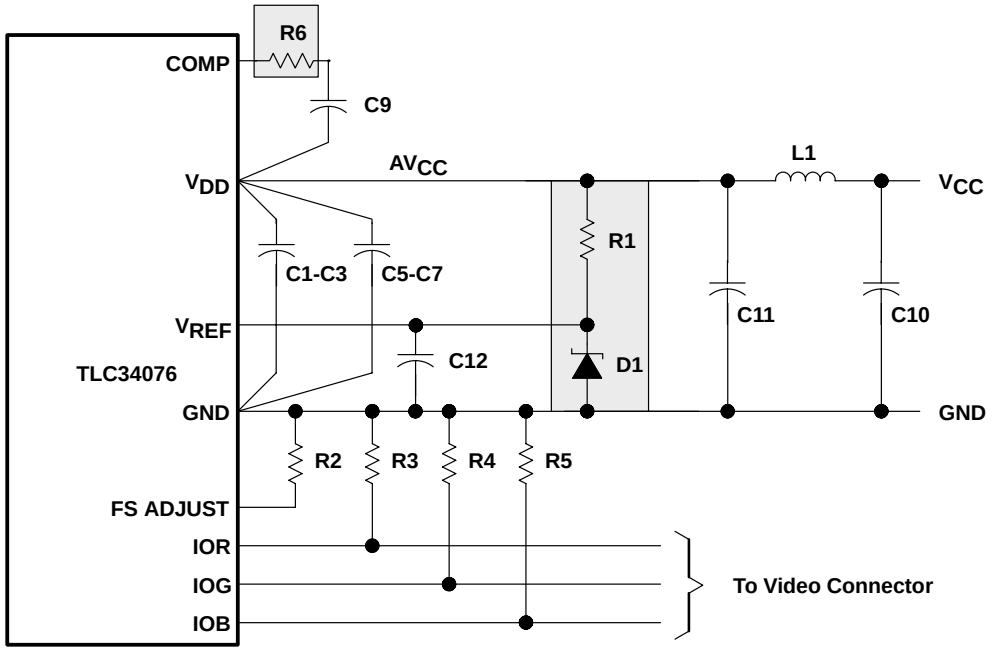
Bypass capacitors should be installed using the shortest leads possible, being consistent with reliable operation to reduce the lead inductance.

For the best performance, a 0.1-µF ceramic capacitor in parallel with a 0.01-µF chip capacitor should be used to decouple each of the three groups of power terminals to GND. These capacitors should be placed as close as possible to the device as shown in Figure B–2.

When a switching power supply is used, the designer should pay close attention to reducing power supply noise and should consider using a 3-terminal voltage regulator for supplying power to AV_{CC}.

COMP and V_{REF} Terminals

A 100-Ω resistor (optional) and 0.1-µF ceramic capacitor (approximate values) should be connected in series between the device COMP and V_{DD} terminals in order to avoid noise and color-smearing problems. Also, whether an internal or external voltage reference is used, a 0.1-µF capacitor should be connected between the device V_{REF} and GND terminals to further stabilize the video image. The resistor and capacitor values may vary depending on the board layout; experimentation may be required in order to determine optimum values.



LOCATION	DESCRIPTION
C1-C3, C9-C10, C12	0.1-μF ceramic capacitor
C5-C7	0.01-μF ceramic chip capacitor
C11	33-μF tantalum capacitor
L1	ferrite bead
R1	1000-Ω 1% metal-film resistor
R2	523-Ω 1% metal-film resistor
R3, R4, R5	75-Ω 1% metal-film resistor
R6	100-Ω 5% resistor
D1	1.2-V voltage reference

Figure B–1. Typical Connection Diagram and Components (Shaded Area is Optional)

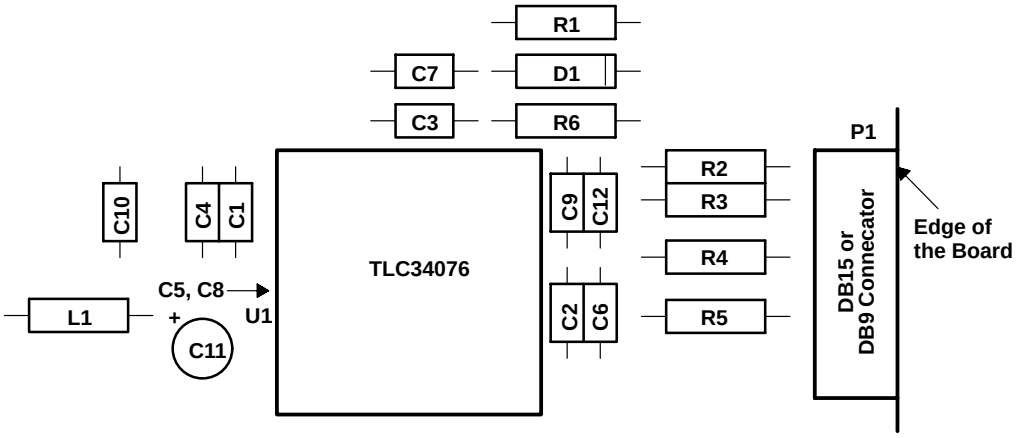


Figure B–2. Typical Component Placement (Component Side)

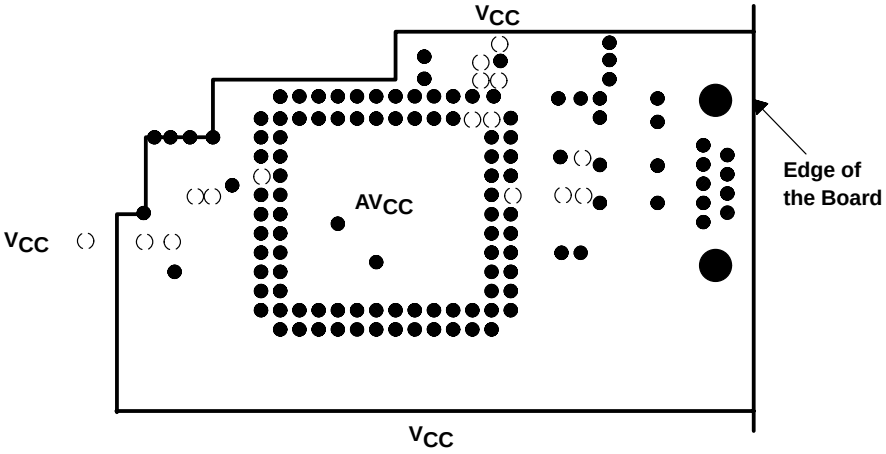


Figure B–3. Typical Split Power Plane (Solder Side)

Appendix C
SCLK Frequency < VCLK Frequency

The VCLK and SCLK outputs generated by the TLC34076 are both free-running clocks. The video control signals (i.e., $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$) are normally generated from VCLK, and a fixed relationship between the video control signals and VCLK can, therefore, be expected. The TLC34076 samples and latches the $\overline{\text{BLANK}}$ input on the falling edge of VCLK. It then looks at the Load signal to determine when to disable or enable SCLK at its output terminal. The decision is deterministic when the SCLK frequency is greater than or equal to the VCLK frequency. However, when the SCLK frequency is less than the VCLK frequency, the appearance of the SCLK waveform at its output terminal when $\overline{\text{BLANK}}$ is sampled low on the VCLK falling edge can vary (see Figures C–1 and C–2).

To avoid this variation in the SCLK output waveform, the SCLK and VCLK frequencies should be chosen so that HTOTAL is evenly divisible by the ratio of VCLK frequency:SCLK frequency; that is:

$$\text{remainder of} \left[\frac{\text{HTOTAL}}{\left(\frac{\text{VCLK frequency}}{\text{SCLK frequency}} \right)} \right] = 0$$

For example, if HTOTAL is even, VCLK frequency = DOTCLK frequency/8, and SCLK frequency = DOTCLK frequency/16, then the formula above is satisfied.

NOTE: When HTOTAL starts at zero (as in the TMS340x0 GSP), then the formula becomes:

$$\text{remainder of} \left[\frac{(\text{HTOTAL} + 1)}{\left(\frac{\text{VCLK frequency}}{\text{SCLK frequency}} \right)} \right] = 0$$

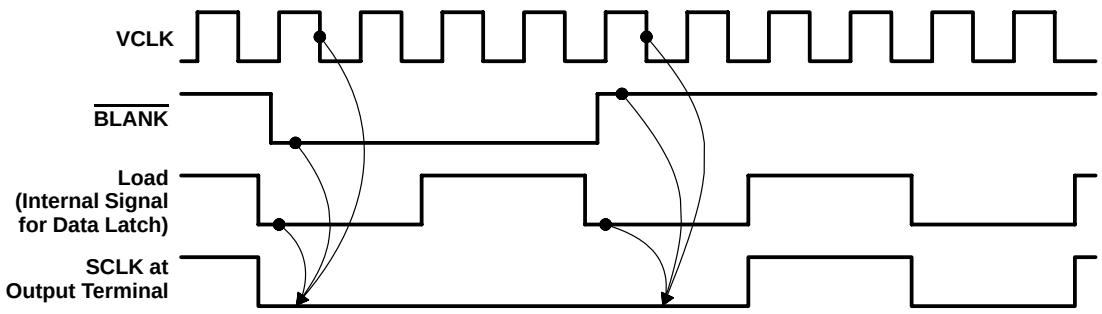


Figure C–1. VCLK and SCLK Phase Relationship (Case 1)

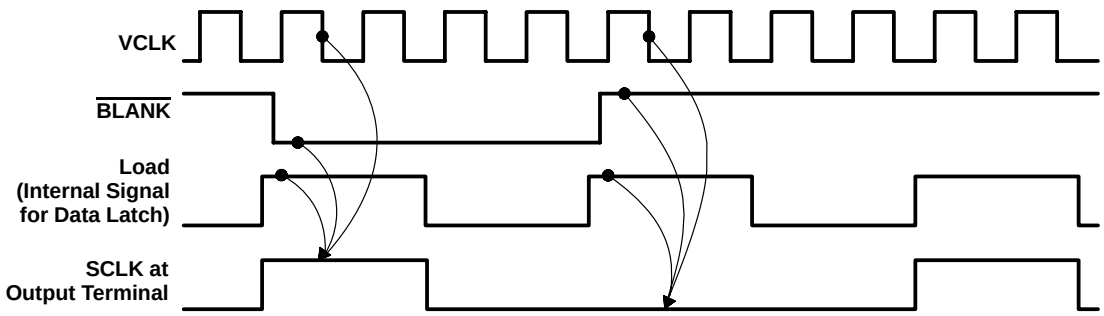
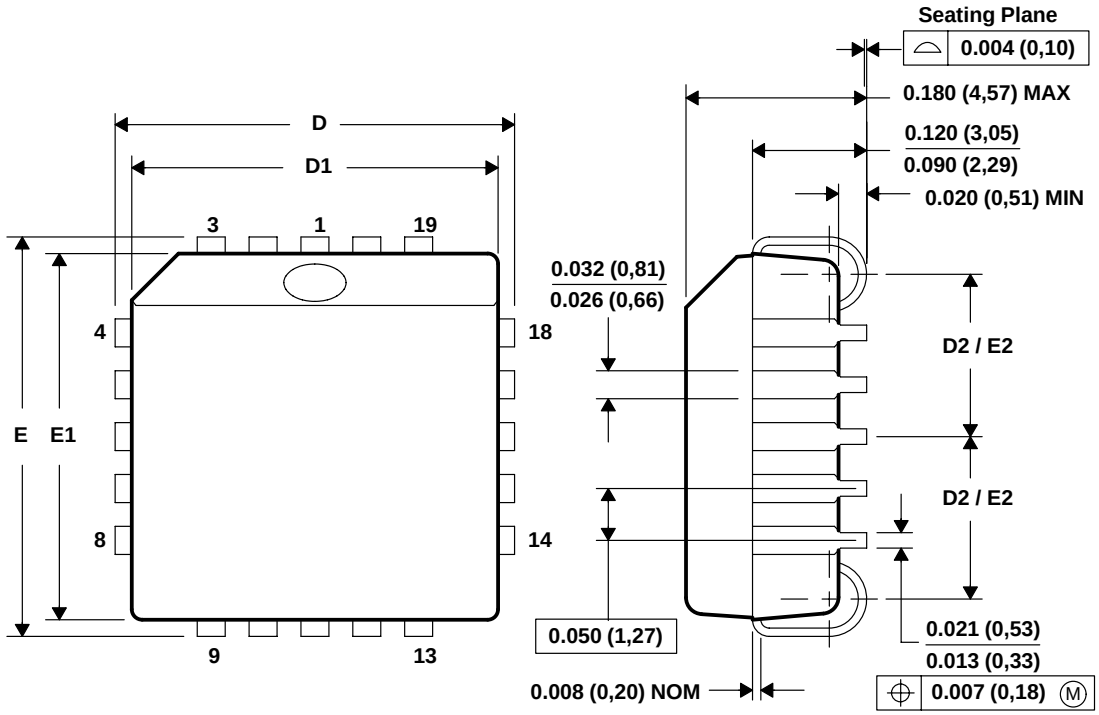


Figure C–2. VCLK and SCLK Phase Relationship (Case 2)

Appendix D
Mechanical Data

FN (S-PQCC-J)** **PLASTIC QUAD CHIP CARRIER**

20 PIN SHOWN



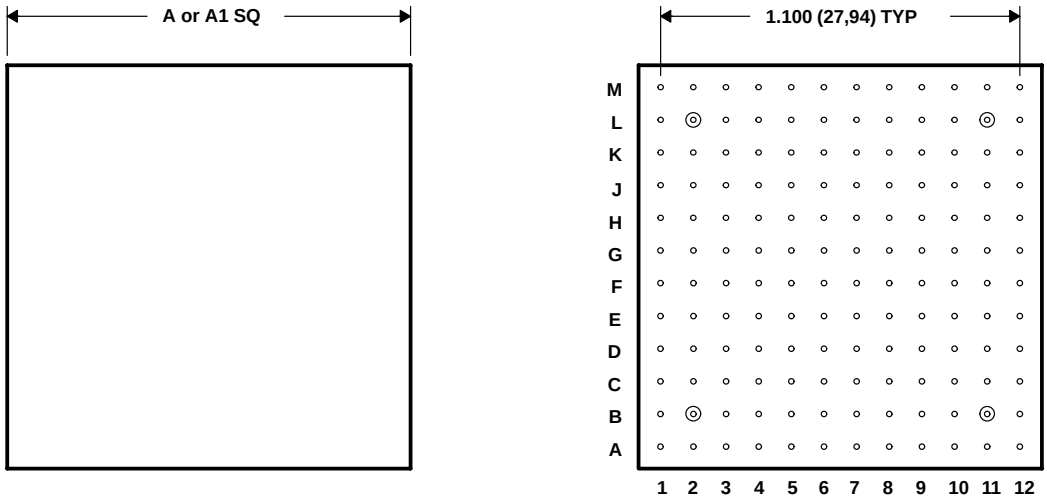
NO. OF PINS **	D / E		D1 / E1		D2 / E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

Mechanical Data (continued)

GA-GB (S-CPGA-P12 X 12) **CERAMIC PIN GRID ARRAY PACKAGE**



DIM	MIN	MAX	Notes
A	1.240 (31,50)	1.280 (32,51)	Large Outline
A1	1.180 (29,97)	1.235 (31,37)	Small Outline
B	0.110 (2,79)	0.205 (5,21)	Cavity Up
B1	0.095 (2,41)	0.205 (5,21)	Cavity Down
C	0.040 (1,02)	0.060 (1,52)	Cavity Up
C1	0.025 (0,63)	0.060 (1,52)	Cavity Down
MAXIMUM PINS WITHIN MATRIX – 144			

4040114-5/B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Index mark may appear on top or bottom depending on package vendor.
D. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
F. The pins can be gold-plated or solder-dipped.
G. Falls within MIL-STD-1835 CMGA4-PN and CMGA16-PN and JEDEC MO-067AD and MO-066AD, respectively