1Mx18, 512Kx36
18Mb DDR-IIP (Burst 2) CIO SYNCHRONOUS SRAM

(2.0 Cycle Read Latency)

ADVANCED INFORMATION
JULY 2012

FEATURES

- 512Kx36 and 1Mx18 configuration available.
- On-chip Delay-Locked Loop (DLL) for wide data valid window.
- Common I/O read and write ports.
- Synchronous pipeline read with self-timed late write operation.
- Double Data Rate (DDR) interface for read and write input ports.
- 2.0 cycle read latency.
- Fixed 2-bit burst for read and write operations.
- Clock stop support.
- Two input clocks (K and K#) for address and control registering at rising edges only.
- Two echo clocks (CQ and CQ#) that are delivered simultaneously with data.
- +1.8V core power supply and 1.5, 1.8V VDDQ, used with 0.75, 0.9V VREF.
- HSTL input and output interface.
- Registered addresses, write and read controls, byte writes, data in, and data outputs.
- Full data coherency.
- Boundary scan using limited set of JTAG 1149.1 functions.
- Byte write capability.
- Fine ball grid array (FBGA) package:
  13mmx15mm and 15mmx17mm body size
  165-ball (11 x 15) array
- Programmable impedance output drivers via 5x user-supplied precision resistor.
- Data Valid Pin (QVLD).
- ODT (On Die Termination) feature is supported optionally on data input, K/K#, and BW_x#.
- The end of top mark (A/A1/A2) is to define options.
  IS61DDP2B251236A : Don't care ODT function and pin connection
  IS61DDP2B251236A1 : Option1
  IS61DDP2B251236A2 : Option2
  Refer to more detail description at page 6 for each ODT option.

DESCRIPTION

The 18Mb IS61DDP2B251236A/A1/A2 and IS61DDP2B21M18A/A1/A2 are synchronous, high-performance CMOS static random access memory (SRAM) devices. These SRAMs have a common I/O bus. The rising edge of K clock initiates the read/write operation, and all internal operations are self-timed. Refer to the *Timing Reference Diagram for Truth Table* for a description of the basic operations of these DDR-IIP (Burst of 2) CIO SRAMs.

Read and write addresses are registered on alternating rising edges of the K clock. Reads and writes are performed in double data rate.

The following are registered internally on the rising edge of the K clock:

- Read/write address
- Read enable
- Write enable
- Byte writes
- Data-in for first burst address
- Data-Out for first burst address

The following are registered on the rising edge of the K# clock:

- Byte writes
- Data-in for second burst address
- Data-Out for second burst address

Byte writes can change with the corresponding data-in to enable or disable writes on a per-byte basis. An internal write buffer enables the data-ins to be registered one cycle after the write address. The first data-in burst is clocked one cycle later than the write command signal, and the second burst is timed to the following rising edge of the K# clock.

During the burst read operation, the data-outs from the first bursts are updated from output registers of the third rising edge of the K clock (starting two clock cycles later after read command). The data-outs from the second burst are updated with the third rising edge of the K# clock where read command receives at the first rising edge of K.

The device is operated with a single +1.8V power supply and is compatible with HSTL I/O interfaces.

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a.) the risk of injury or damage has been minimized;
b.) the user assume all such risks; and
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Package ballout and description

x36 FBGA Ball Configuration (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	NC/SA[1]	NC/SA[1]	R/W#	BW_2#	K#	BW_1#	LD#	SA	NC/SA[1]	CQ
B	NC	DQ27	DQ18	SA	BW_3#	K	BW_0#	SA	NC	NC	DQ8
C	NC	NC	DQ28	V_{SS}	SA	NC	SA	V_{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V_{SS}	V_{SS}	V_{SS}	VSS	V_{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V_{DDQ}	V_{SS}	V_{SS}	VSS	V_{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ14
H	D_{off}#	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ32	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	DQ10
P	NC	NC	DQ26	SA	SA	QVLD	SA	SA	NC	DQ9	DQ0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

Notes:
1. The following balls are reserved for higher densities: 3A for 36Mb, 10A for 72Mb, and 2A for 144Mb.

x18 FBGA Ball Configuration (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	NC/SA[1]	SA	R/W#	BW_1#	K#	NC/SA[1]	LD#	SA	NC/SA[1]	CQ
B	NC	DQ9	NC	SA	NC/SA[1]	K	BW_0#	SA	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	SA	NC	SA	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	VSS	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	VSS	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	D_{off}#	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	SA	SA	QVLD	SA	SA	NC	NC	DQ0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

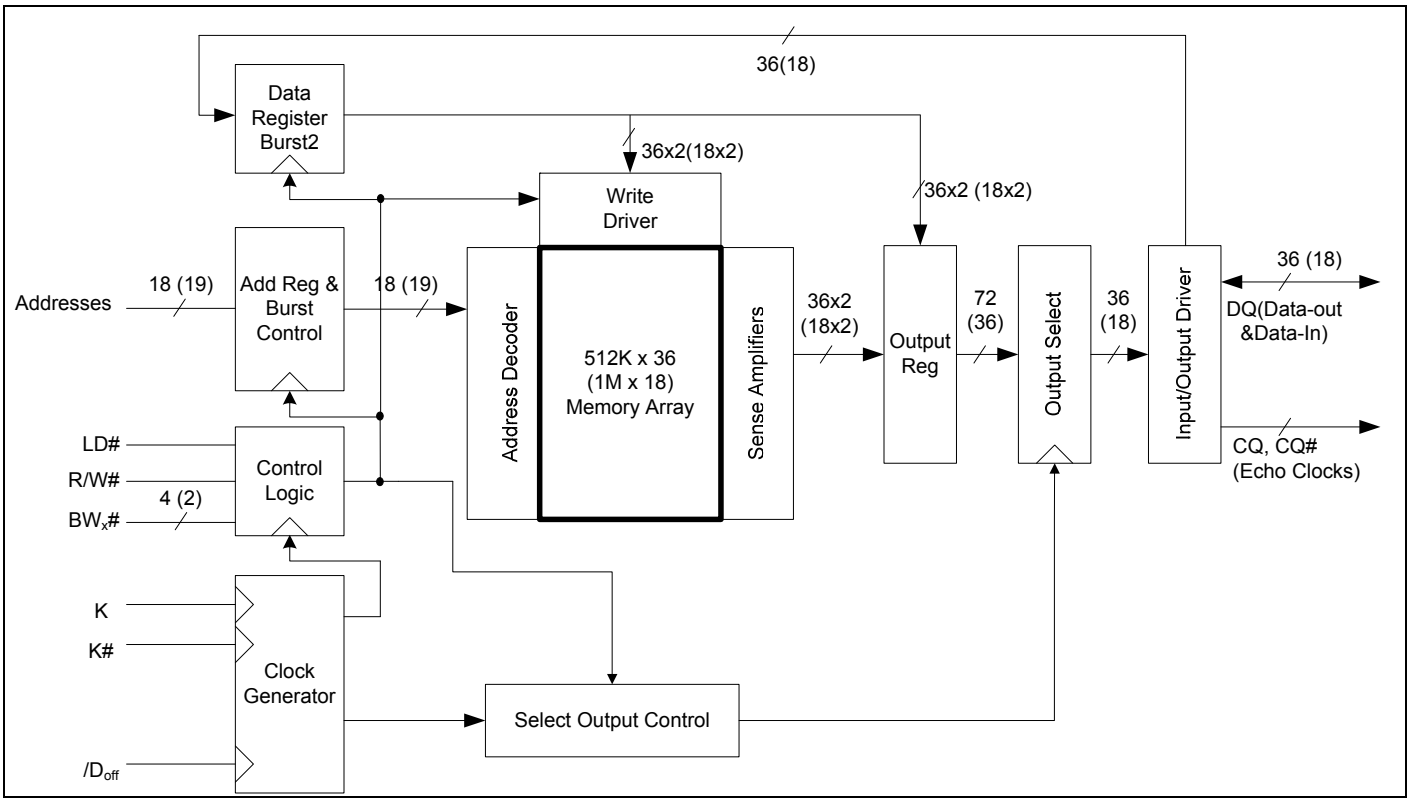
Notes:
1. The following balls are reserved for higher densities: 10A for 36Mb, 2A for 72Mb, 7A for 144Mb, and 5B for 288Mb.

Ball Descriptions

Symbol	Type	Description
K, K#	Input	Input clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of K#. K# is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges. These balls cannot remain VREF level.
CQ, CQ#	Output	Synchronous echo clock outputs: The edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when Q tri-states.
Doff#	Input	DLL disable and reset input : when low, this input causes the DLL to be bypassed and reset the previous DLL information. When high, DLL will start operating and lock the frequency after tCK lock time. The device behaves in one clock read latency mode when the DLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz.
QVLD	Output	Valid output indicator: The Q Valid indicates valid output data. QVLD is edge aligned with CQ and CQ#.
SA	Input	Synchronous address inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. These inputs are ignored when device is deselected.
DQ0 - DQn	Bidir	Data input and output signals. Input data must meet setup and hold times around the rising edges of K and K# during WRITE operations. These pins drive out the requested data when the read operation is active. Valid output data is synchronized to the respective CQ and CQ. See BALL CONFIGURATION figures for ball site location of individual signals. The x18 device uses DQ0~DQ17. DQ18~DQ35 should be treated as NC pin. The x36 device uses DQ0~DQ35.
R/W#	Input	Synchronous Read or Write input. When LD# is low, this input designates the access type (read when it is High, write when it is Low) for loaded address. R/W# must meet the setup and hold times around edge of K.
LD#	Input	Synchronous load. This input is brought Low when a bus cycle sequence is defined. This definition includes address and read/write direction.
BW_x#	Input	Synchronous byte writes: When low, these inputs cause their respective byte to be registered and written during WRITE cycles. These signals are sampled on the same edge as the corresponding data and must meet setup and hold times around the rising edges of K and #K for each of the two rising edges comprising the WRITE cycle. See Write Truth Table for signal to data relationship.
V_{REF}	Input reference	HSTL input reference voltage: Nominally VDDQ/2, but may be adjusted to improve system noise margin. Provides a reference voltage for the HSTL input buffers.
V_{DD}	Power	Power supply: 1.8 V nominal. See DC Characteristics and Operating Conditions for range.
V_{DDQ}	Power	Power supply: Isolated output buffer supply. Nominally 1.5 V. See DC Characteristics and Operating Conditions for range.
V_{SS}	Ground	Ground of the device
ZQ	Input	Output impedance matching input: This input is used to tune the device outputs to the system data bus impedance. Q and CQ output impedance are set to 0.2xRQ, where RQ is a resistor from this ball to ground. This ball can be connected directly to VDDQ, which enables the minimum impedance mode. This ball cannot be connected directly to VSS or left unconnected. In ODT (On Die Termination) enable devices, the ODT termination values tracks the value of RQ. The ODT range is selected by ODT control input.
TMS, TDI, TCK	Input	IEEE1149.1 input pins for JTAG.
TDO	Output	IEEE1149.1 output pins for JTAG.
NC	N/A	No connect: These signals should be left floating or connected to ground to improve package heat dissipation.
ODT	Input	ODT control; Refer to SRAM features for the details.

SRAM Features description

Block Diagram



Note: Numerical values in parentheses refer to the x18 device configuration.

Read Operations

The SRAM operates continuously in a burst-of-two mode. Read cycles are started by registering R/W# in active high state at the rising edge of the K clock. K and K#, are also used to control the timing to the outputs. The data corresponding to the first address is clocked two cycles later by the rising edge of the K clock. The data corresponding to the second burst is clocked two and half cycles later by the following rising edge of the K# clock. A set of free-running echo clocks, CQ and CQ#, are produced internally with timings identical to the data-outs. The echo clocks can be used as data capture clocks by the receiver device.

Whenever LD# is low, a new address is registered at the rising edge of the K clock. A NOP operation (LD# is high) does not terminate the previous read. The output drivers disable automatically to a high-Z state.

Write Operations

Write operations can also be initiated at every other rising edge of the K clock whenever R/W# is low. The write address is also registered at that time. When the address needs to change, LD# needs to be low simultaneously to be registered by the rising edge of K. Again, the write always occurs in bursts of two.

Because of its common I/O architecture, the data bus must be tri-stated at least one cycle before the new data-in is presented at the DQ bus.

The write data is provided in a ‘late write’ mode; that is, the data-in corresponding to the first address of the burst, is presented one clock cycle later or at the rising edge of the following K clock. The data-in corresponding to the second write burst address follows next, registered by the rising edge of K#.

The data-in provided for writing is initially kept in write buffers. The information on these buffers is written into

the array on the third write cycle. A read cycle to the last two write address produces data from the write buffers. Similarly, a read address followed by the same write address produces the latest write data. The SRAM maintains data coherency.

During a write, the byte writes independently control which byte of any of the two burst addresses is written. (See *X18/X36 Write Truth Tables* and *Timing Reference Diagram for Truth Table*)

Whenever a write is disabled (R/W# is high at the rising edge of K), data is not written into the memory.

RQ Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to enable the SRAM to adjust its output driver impedance. The value of RQ must be 5x the value of the intended line impedance driven by the SRAM. For example, an RQ of 250Ω results in a driver impedance of 50Ω. The allowable range of RQ to guarantee impedance matching is between 175Ω and 350Ω at V_{DDQ}=1.5V. The RQ resistor should be placed less than two inches away from the ZQ ball on the SRAM module. The capacitance of the loaded ZQ trace must be less than 7.5pF.

The ZQ pin can also be directly connected to V_{DDQ} to obtain a minimum impedance setting. ZQ should not be connected to V_{SS}.

Programmable Impedance and Power-Up Requirements

Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. During power-up, the driver impedance is in the middle of allowable impedances values. The final impedance value is achieved within 1024clock cycles.

Valid Data Indicator (QVLD)

A data valid pin (QVLD) is available to assist in high-speed data output capture. This output signal is edge-aligned with the echo clock and is asserted HIGH half a cycle before valid read data is available and asserted LOW half a cycle before the final valid read data arrives.

Delay Locked Loop (DLL)

Delay Locked Loop (DLL) is a new system to align the output data coincident with clock rising or falling edge to enhance the output valid timing characteristics. It is locked to the clock frequency and is constantly adjusted to match the clock frequency. Therefore device can have stable output over the temperature and voltage variation.

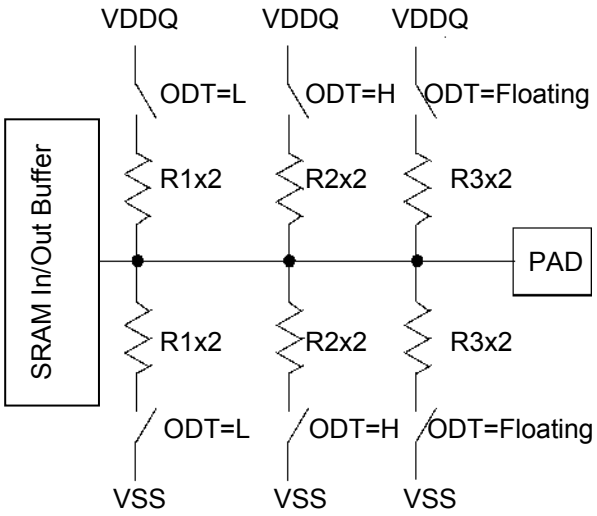
DLL has a limitation of locking range and jitter adjustment which are specified as tKHKH and tKCvar respectively in the AC timing characteristics. In order to turn this feature off, applying logic low to the Doff# pin will bypass this. In the DLL off mode, the device behaves with one clock cycle latency and a longer access time which is known in DDR-I or legacy QUAD mode.

The DLL can also be reset without power down by toggling Doff# pin low to high or stopping the input clocks K and K# for a minimum of 30ns.(K and K# must be stayed either at higher than VIH or lower than VIL level. Remaining Vref is not permitted.) DLL reset must be issued when power up or when clock frequency changes abruptly. After DLL being reset, it gets locked after 2048 cycles of stable clock.

ODT (On Die Termination)

On Die Termination (ODT) is a feature that allows a SRAM to turn on/off termination resistance for ODT pins. The ODT feature is designed to improve signal integrity of the memory channel by allowing the SRAM controller to turn on/off termination resistance independently for any or all SRAM devices.
ODT can have three status, High, Low, and Floating. Each status can have different ODT termination values which tracks the value of RQ (See the picture below) In DDR-IIP devices having common I/O bus, ODT is automatically enabled at the write operation of SRAM and disabled at the read operation of SRAM.

Fig1. Functional representation of ODT



	R1	R2	R3
Option1[3]	0.3x RQ[1]	0.6x RQ[2]	0.6x RQ[2]
Option2[4]	ODT disable	0.6x RQ[2]	ODT disable

Notes
1. Allowable range of RQ to guarantee impedance matching a tolerance of ±20% is 175Ω<RQ<350Ω.
2. Allowable range of RQ to guarantee impedance matching a tolerance of ±20% is 175Ω<RQ<250Ω.
3. ODT control pin is connected to VDDQ through 3.5kΩ. Therefore it is recommended to connect it to VSS through less than 100Ω to make it low.
4. ODT control pin is connected to VSS through 3.5kΩ. Therefore it is recommended to connect it to VDDQ through less than 100Ω to make it high.

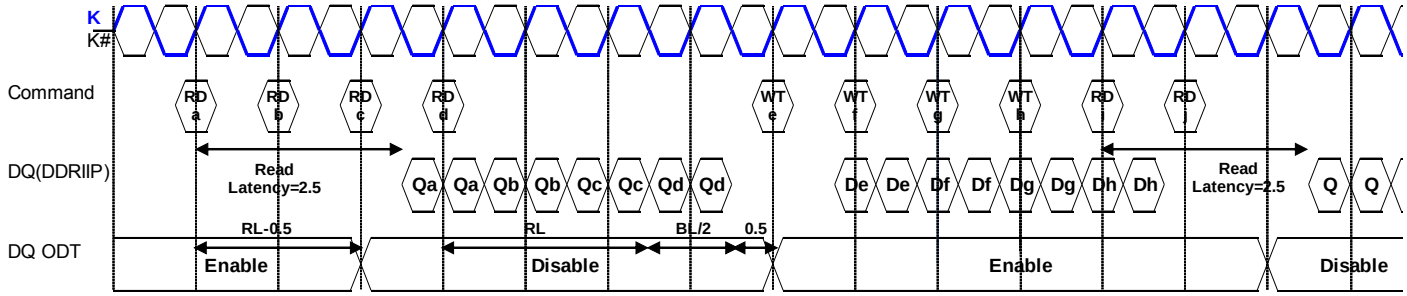
ODT PINS

1) ODT Pin in option1

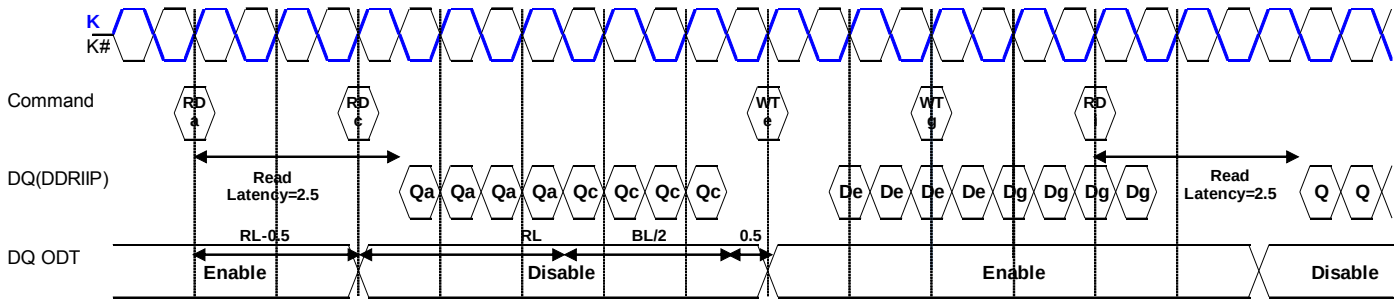
. ODT values of K, K#, DQs, and Wx# are controlled by ODT pin.
. ODT for DQs will be on and off depending on the status. Read command will turn ODT off as the following rule.

Off: First Read Command + Read Latency - 0.5 cycle
On: Last Read Command + Read Latency + BL/2 cycle + 0.5 cycle (See below timing chart)

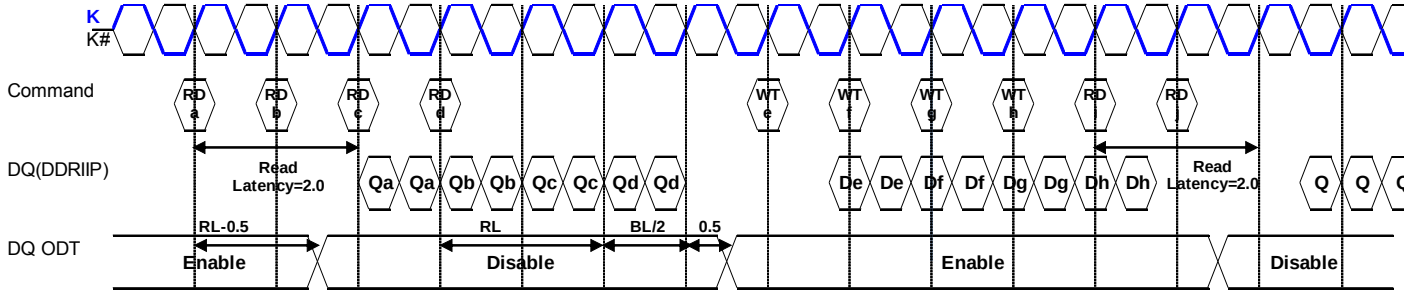
Example1) BL=2, RL(Read Latency=2.5)



Example2) BL=4, RL(Read Latency=2.5)



Example3) BL=2, RL(Read Latency=2.0)



2) ODT Pin in option2

-. Same ODT pin rule of option1 applies except K and K#.

Power-Up and Power-Down Sequences

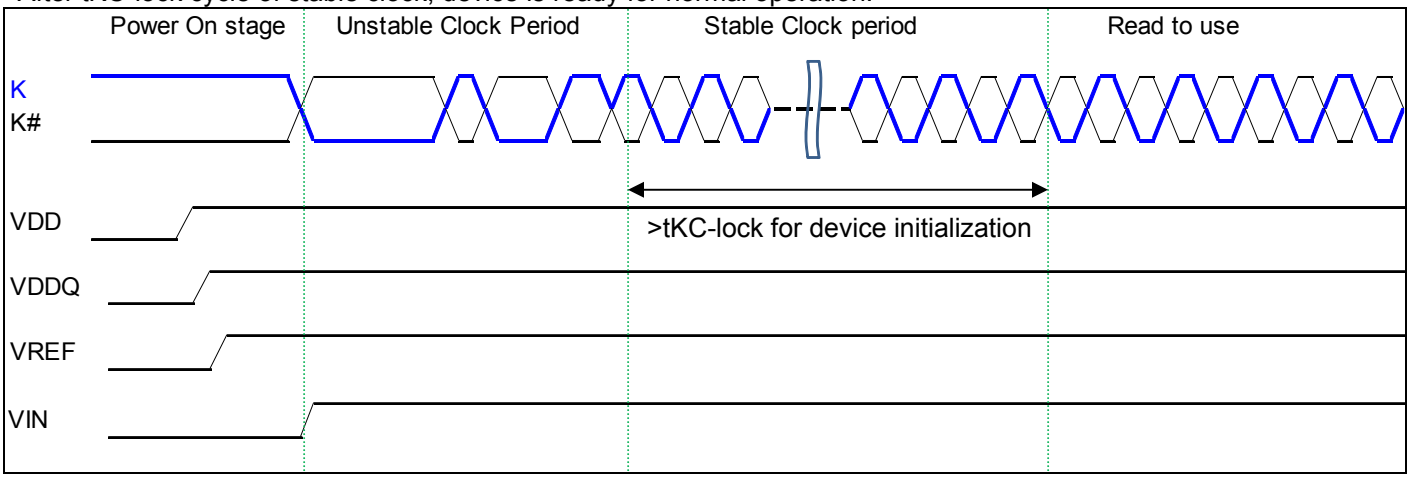
The recommendation of voltage apply sequence is : $V_{DD} \rightarrow V_{DDQ}$ [1)] $\rightarrow V_{REF}$ [2)] $\rightarrow V_{IN}$

Notes:
V_{DDQ} can be applied concurrently with V_{DD}.
V_{REF} can be applied concurrently with V_{DDQ}.

After power and clock signals are stabilized, device can be ready for normal operation after tKC-Lock cycles. In tKC-lock cycle period, device initializes internal logics and locks DLL. Depending on /Doff status, locking DLL will be skipped. The following timing pictures are possible examples of power up sequence.

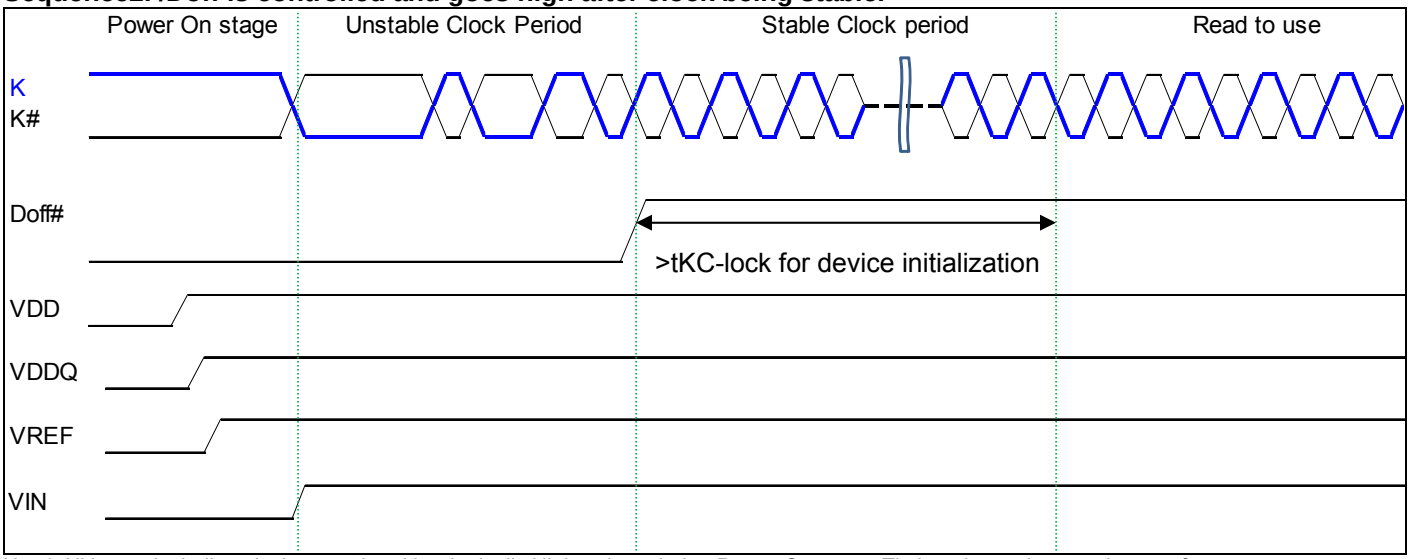
Sequence1. /Doff is fixed low

After tKC-lock cycle of stable clock, device is ready for normal operation.



Note) All inputs including clocks must be either logically High or Low during Power On stage. Timing above shows only one of cases.

Sequence2. /Doff is controlled and goes high after clock being stable.

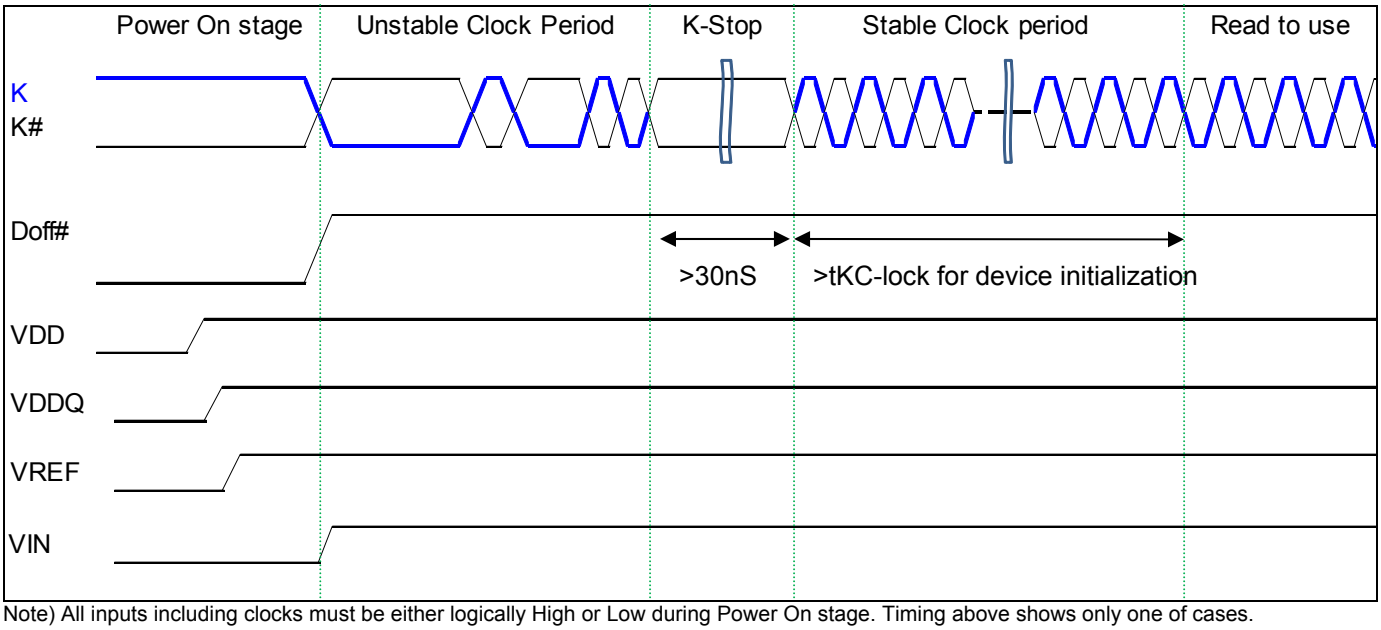


Note) All inputs including clocks must be either logically High or Low during Power On stage. Timing above shows only one of cases.

Sequence3. /Doff is controlled but goes high before clock being stable.

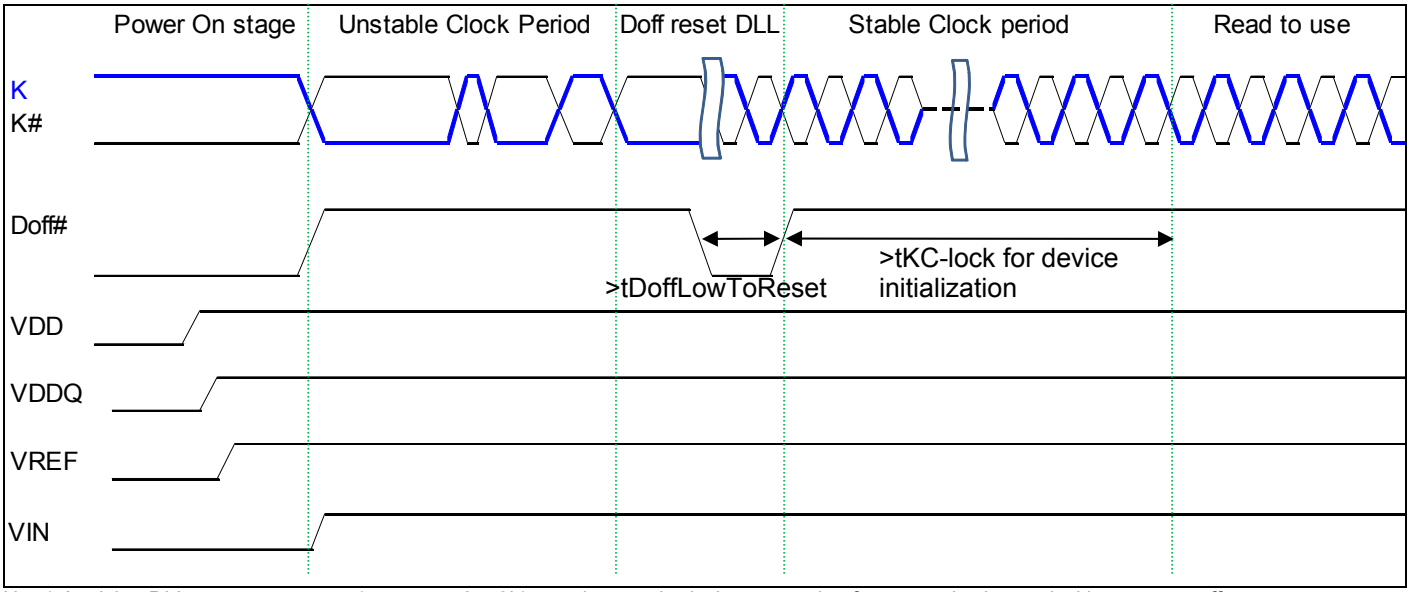
Because DLL has a risk to be locked with the unstable clock, DLL needs to be reset and locked with the stable input.

a) K-stop to reset. If K or K# stays at VIH or VIL for more than 30nS, DLL will be reset and ready to re-lock. In tKC-Lock period, DLL will be locked with a new stable value. Device can be ready for normal operation after that.



Note) All inputs including clocks must be either logically High or Low during Power On stage. Timing above shows only one of cases.

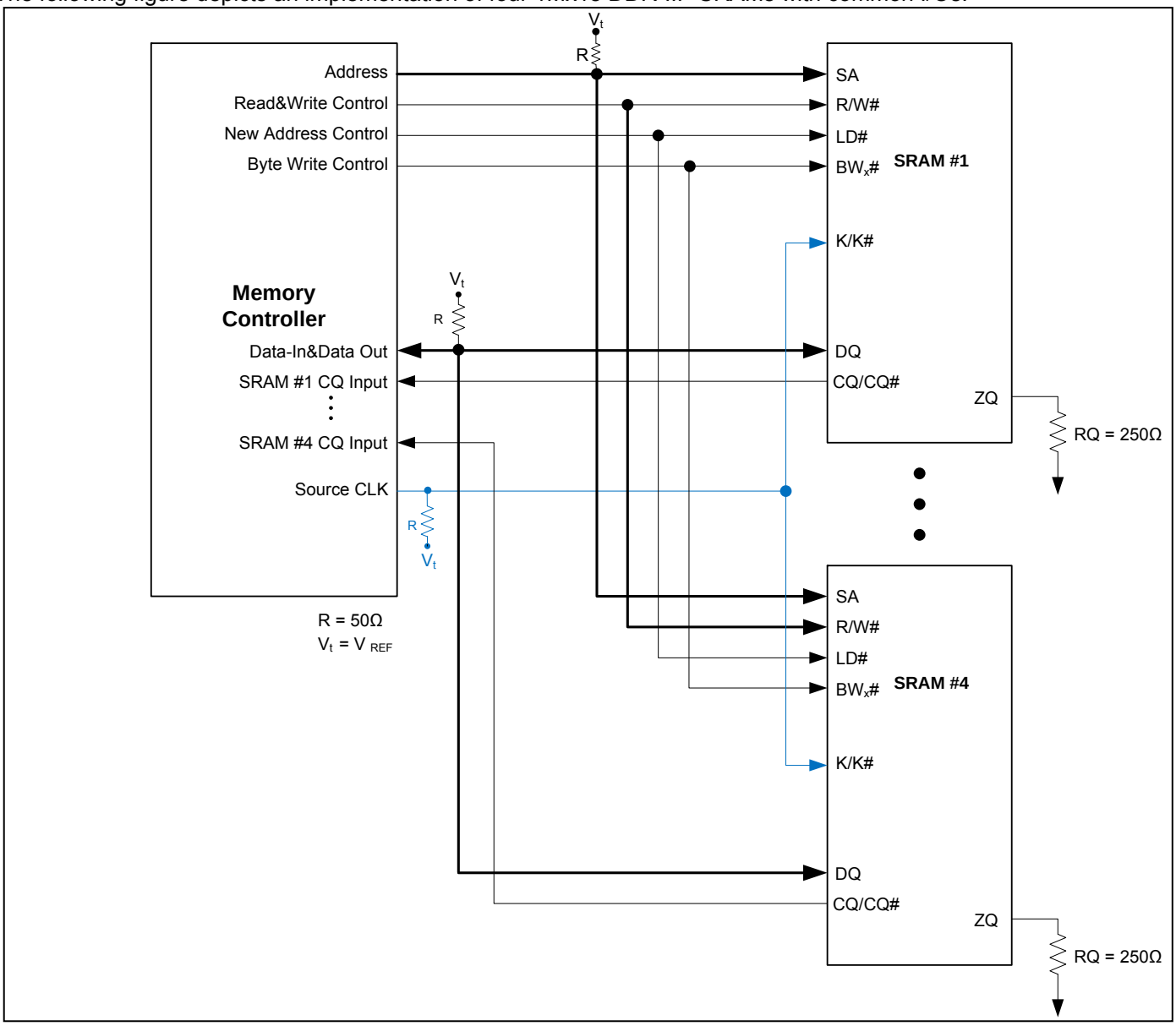
a) /Doff Low to reset. If /Doff toggled low to high, DLL will be reset and ready to re-lock. In tKC-Lock period, DLL will be locked with a new stable value. Device can be ready for normal operation after that.



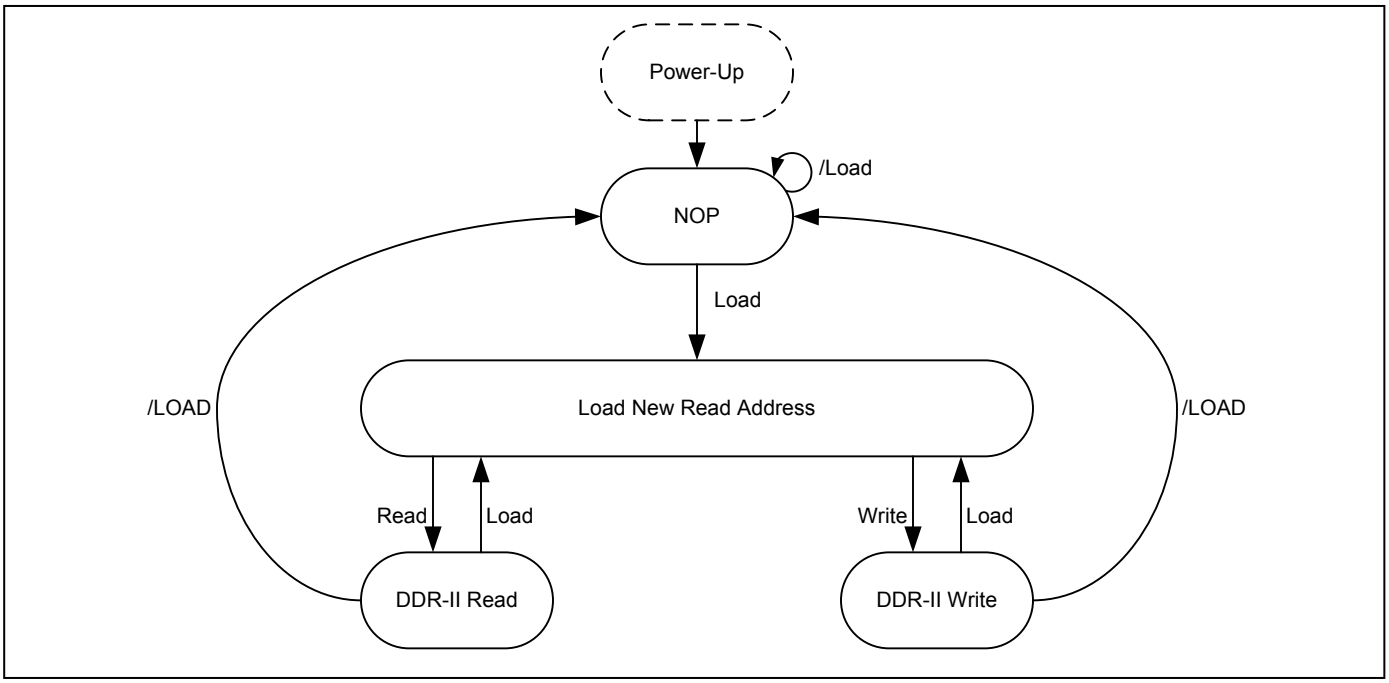
Note) Applying DLL reset sequences (sequence 3a, 3b) are also required when operating frequency is changed without power off.
Note) All inputs including clocks must be either logically High or Low during Power On stage. Timing above shows only one of cases.

Application Example

The following figure depicts an implementation of four 1Mx18 DDR-IIP SRAMs with common I/Os.



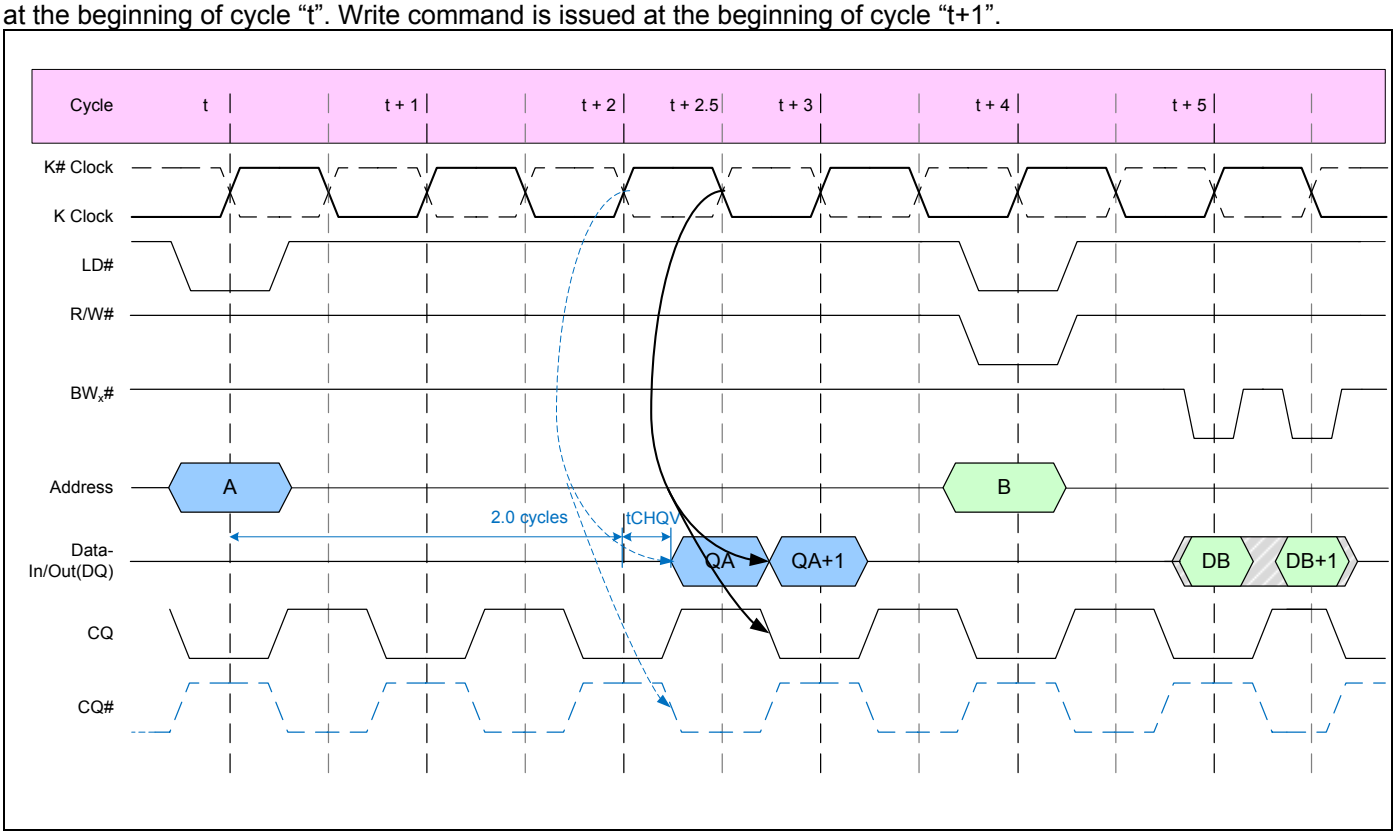
State Diagram



Notes:
1. Internal burst counter is fixed as two-bit linear; that is, when first address is A0+0, next internal burst address is A0+1.
2. Read refers to read active status with R/W# = High.
3. Write refers to write active status with R/W# = LOW.
4. Load refers to read new address active status with LD# = low.
5. Load is read new address inactive status with LD = high.

Timing Reference Diagram for Truth Table

The *Timing Reference Diagram for Truth Table* is helpful in understanding the *Clock and Write Truth Tables*, as it shows the cycle relationship between clocks, address, data in, data out, and control signals. Read command is issued at the beginning of cycle "t". Write command is issued at the beginning of cycle "t+1".



Clock Truth Table

(Use the following table with the *Timing Reference Diagram for Truth Table*.)

Mode	Clock	Controls		Data Out / Data In	
	K	LD#	R/W#	Q_A / D_B	Q_{A+1} / D_{B+1}
Stop Clock	Stop	X	X	Previous State	Previous State
No Operation (NOP)	L → H	H	X	High-Z	High-Z
Read A	L → H	L	H	D_{OUT} at K# (t+2.0) ↑	D_{OUT} at K (t+2.5) ↑
Write B	L → H	L	L	D_B at K (t+5.0) ↑	D_B at K# (t+5.5) ↑

Notes:
1. X = "don't care"; H = logic "1"; L = logic "0".
2. A read operation is started when control signal R/W# is active high.
3. A write operation is started when control signal R/W# is active low.
4. Before entering into stop clock, all pending read and write commands must be completed.
5. For timing definitions, refer to the *AC Timing Characteristics* table. Signals must meet AC specifications at timings indicated in parenthesis with respect to switching clocks K and K#

x18 Write Truth Table

(Use the following table with the *Timing Reference Diagram for Truth Table*.)

Operation	K (t+1.0)	K (t+1.5)	BW_0	BW_1	D_B	D_{B+1}
Write Byte 0	L → H		L	H	D0-8 (t+4.0)	
Write Byte 1	L → H		H	L	D9-17 (t+4.0)	
Write All Bytes	L → H		L	L	D0-17 (t+4.0)	
Abort Write	L → H		H	H	Don't Care	
Write Byte 0		L → H	L	H		D0-8 (t+4.5)
Write Byte 1		L → H	H	L		D9-17 (t+4.5)
Write All Bytes		L → H	L	L		D0-17 (t+4.5)
Abort Write		L → H	H	H		Don't Care

Notes:
1. For all cases, R/W# needs to be active low during the rising edge of K occurring at time t.
2. For timing definitions refer to the *AC Timing Characteristics* table. Signals must meet AC specifications with respect to switching clocks K and K#.

x36 Write Truth Table

(Use the following table with the *Timing Reference Diagram for Truth Table*.)

Operation	K (t+1.0)	K (t+1.5)	BW_0	BW_1	BW_2	BW_3	D_B	D_{B+1}
Write Byte 0	L → H		L	H	H	H	D0-8 (t+4.0)	
Write Byte 1	L → H		H	L	H	H	D9-17 (t+4.0)	
Write Byte 2	L → H		H	H	L	H	D18-26 (t+4.0)	
Write Byte 3	L → H		H	H	H	L	D27-35 (t+4.0)	
Write All Bytes	L → H		L	L	L	L	D0-35 (t+4.0)	
Abort Write	L → H		H	H	H	H	Don't Care	
Write Byte 0		L → H	L	H	H	H		D0-8 (t+4.5)
Write Byte 1		L → H	H	L	H	H		D9-17 (t+4.5)
Write Byte 2		L → H	H	H	L	H		D18-26 (t+4.5)
Write Byte 3		L → H	H	H	H	L		D27-35 (t+4.5)
Write All Bytes		L → H	L	L	L	L		D0-35 (t+4.5)
Abort Write		L → H	H	H	H	H		Don't Care

Notes:
1. For all cases, R/W# needs to be active low during the rising edge of K occurring at time t.
2. For timing definitions refer to the *AC Timing Characteristics* table. Signals must meet AC specifications with respect to switching clocks K and K#.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	V_{DD}	–0.5	2.9	V
I/O Power Supply Voltage	V_{DDQ}	–0.5	2.9	V
DC Input Voltage	V_{IN}	–0.5	V_{DD}+0.3	V
Data Out Voltage	V_{DOUT}	–0.5	2.6	V
Junction Temperature	T_J	-	110	°C
Storage Temperature	T_{STG}	–55	+125	°C

Note:
Stresses greater than those listed in this table can cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Temperature Range

Temperature Range	Symbol	Min	Max	Units
Commercial	T_A	0	+70	°C
Industrial	T_A	–40	+85	°C

DC Electrical Characteristics

(Over the Operating Temperature Range, V_{DD}=1.8V±5%)

Parameter	Symbol	Min	Max	Units	Notes
x36 Average Power Supply Operating Current (I_{OUT}=0, V_{IN}=V_{IH} or V_{IL})	I_{DD18} I_{DD20} I_{DD22} I_{DD25}	–	1300 1200 1100 1000	mA	1,2
x18 Average Power Supply Operating Current (I_{OUT}=0, V_{IN}=V_{IH} or V_{IL})	I_{DD18} I_{DD20} I_{DD22} I_{DD25}	–	1250 1150 1050 950	mA	1,2
Power Supply Standby Current (R#=V_{IH}, W#=V_{IH}. All other inputs=V_{IH} or V_{IL}, I_{IH}=0)	I_{SB18} I_{SB20} I_{SB22} I_{SB25}	–	380 360 340 320	mA	1,2
Input leakage current (0 ≤V_{IN}≤V_{DDQ} for all input balls except V_{REF}, ZQ, TCK, TMS, TDI ball)	I_{LI}	–2	+2	µA	3.4
Output leakage current (0 ≤V_{OUT} ≤V_{DDQ} for all output balls except TDO ball; Output must be disabled.)	I_{LO}	–2	+2	µA	
Output “high” level voltage(I_{OH}=–100uA, Nominal ZQ)	V_{OH}	V_{DDQ}–0.2	V_{DDQ}	V	
Output “low” level voltage (I_{OH}= 100uA, Nominal ZQ)	V_{OL}	V_{SS}	V_{SS}+0.2	V	

Notes:
1. I_{OUT} = chip output current.
2. The numeric suffix indicates the part operating at speed, as indicated in *AC Timing Characteristics* table (that is, I_{DD25} indicates 2.5ns cycle time).
3. ODT must be disabled.
4. Balls with ODT and DOFF# do not follow this spec, I_{LI} = ±100uA.

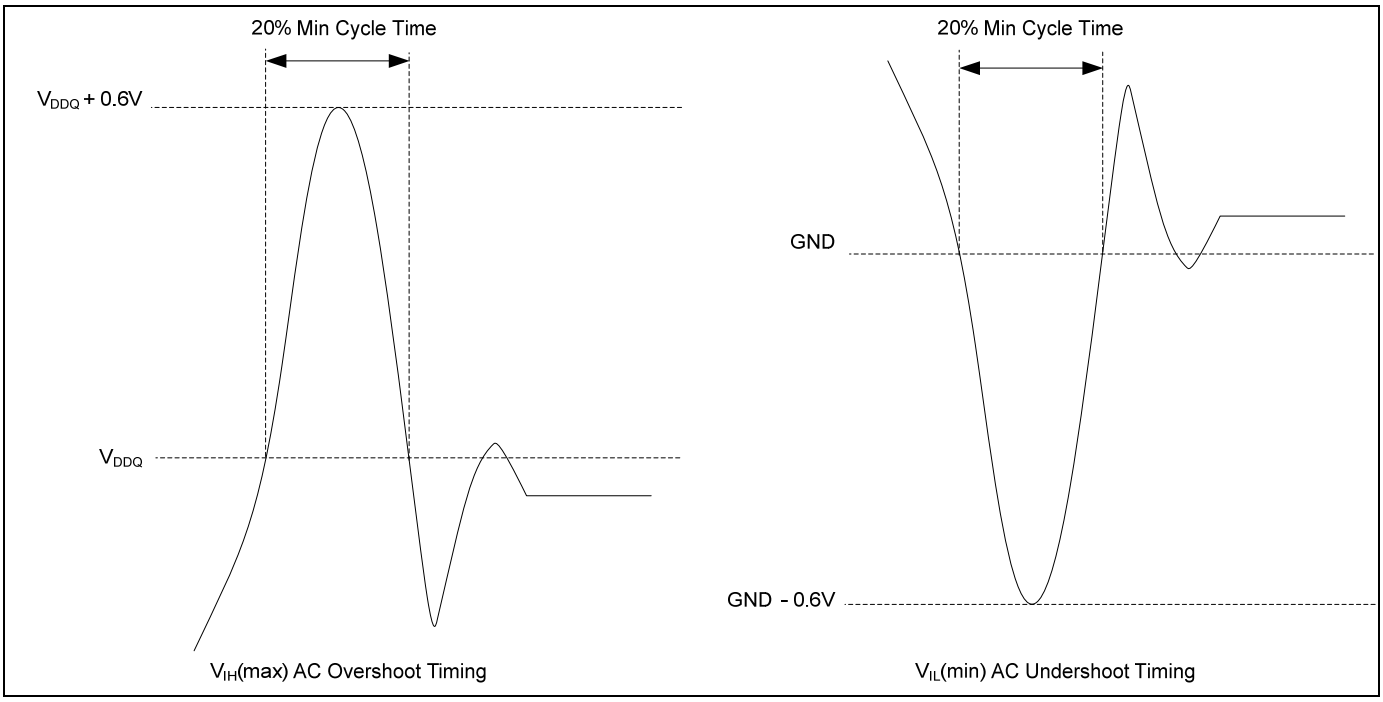
Recommended DC Operating Conditions

(Over the Operating Temperature Range)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Supply Voltage	V_{DD}	1.8–5%	1.8	1.8+5%	V	1
Output Driver Supply Voltage	V_{DDQ}	1.4	1.5	V_{DD}	V	1
Input High Voltage	V_{IH}	V_{REF}+0.1	-	V_{DDQ}+0.2	V	1, 2
Input Low Voltage	V_{IL}	–0.2	-	V_{REF} –0.1	V	1, 3
Input Reference Voltage	V_{REF}	0.68	0.75	0.95	V	1, 5
Clock Signal Voltage	V_{IN-CLK}	–0.2	-	V_{DDQ}+0.2	V	1, 4

Notes:
1. All voltages are referenced to V_{SS}. All V_{DD}, V_{DDQ}, and V_{SS} pins must be connected.
2. V_{IH}(max) AC = See *0vershoot and Undershoot Timings*.
3. V_{IL}(min) AC = See *0vershoot and Undershoot Timings*.
4. V_{IN-CLK} specifies the maximum allowable DC excursions of each clock (K and K#).
5. Peak-to-peak AC component superimposed on VREF may not exceed 5% of VREF.

Overshoot and Undershoot Timings

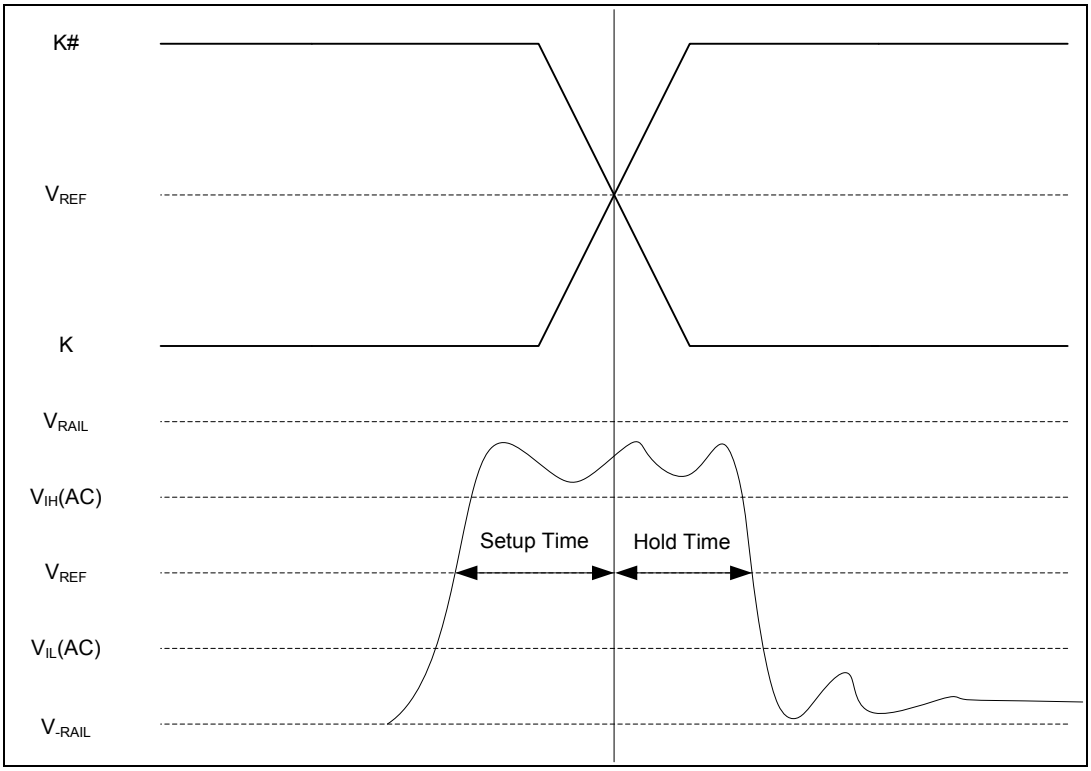


Typical AC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
AC Input Logic HIGH	V_{IH} (AC)	V_{REF}+0.2		V	1, 2, 3, 4
AC Input Logic LOW	V_{IL} (AC)		V_{REF}–0.2	V	1, 2, 3, 4
Clock Input Logic HIGH	V_{IH-CLK} (AC)	V_{REF}+0.2		V	1, 2, 3
Clock Input Logic LOW	V_{IL-CLK} (AC)		V_{REF}–0.2	V	1, 2, 3

Notes:
1. The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. Performance is a function of V_{IH} and V_{IL} levels to clock inputs.
3. See the *AC Input Definition* diagram.
4. See the *AC Input Definition* diagram. The signals should swing monotonically with no steps rail-to-rail with input signals never ringing back past V_{IH} (AC) and V_{IL} (AC) during the input setup and input hold window. V_{IH} (AC) and V_{IL} (AC) are used for timing purposes only.

AC Input Definition



PBGA Thermal Characteristics

Parameter	Symbol	13x15 BGA	15x17 BGA	Units
Thermal resistance (junction to ambient at airflow = 1m/s)	$R_{\theta JA}$	19.6	18.0	°C/W
Thermal resistance (junction to pins)	$R_{\theta JB}$	4.02	3.30	°C/W
Thermal resistance (junction to case)	$R_{\theta JC}$	4.53	4.20	°C/W

Note: these parameters are guaranteed by design and tested by a sample basis only.

Pin Capacitance

Parameter	Symbol	Test Condition	Max	Units
Input or output capacitance except DQ pins	C_{IN} ,C_O	T_A = 25°C, f = 1 MHz, V_{DD} = 1.8V, V_{DDQ} = 1.5V	5	pF
DQ capacitance (DQ0–DQx)	C_{DQ}		6	pF
Clocks Capacitance (K, K, C, C)	C_{CLK}		4	pF

Note: these parameters are guaranteed by design and tested by a sample basis only.

Programmable Impedance Output Driver DC Electrical Characteristics

(Over the Operating Temperature Range, V_{DD}=1.8V±5%, V_{DDQ}=1.5V/1.8V)

Parameter	Symbol	Min	Max	Units	Notes
Output Logic HIGH Voltage	V_{OH}	V_{DDQ}/2 -0.12	V_{DDQ}/2 + 0.12	V	1, 3
Output Logic LOW Voltage	V_{OL}	V_{DDQ}/2 -0.12	V_{DDQ}/2 + 0.12	V	2, 3

Notes:
1. For 175Ω□□≤ RQ ≤□350Ω:

$$|I_{OH}| = \frac{\left(\frac{V_{DDQ}}{2}\right)}{\left(\frac{RQ}{5}\right)}$$

2. For 175Ω□□≤□RQ ≤□350Ω:

$$|I_{OL}| = \frac{\left(\frac{V_{DDQ}}{2}\right)}{\left(\frac{RQ}{5}\right)}$$

3. Parameter Tested with RQ=250Ω and V_{DDQ}=1.5V

AC Test Conditions

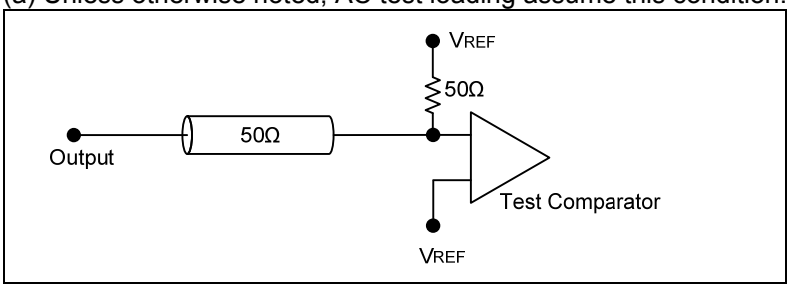
(Over the Operating Temperature Range, V_{DD}=1.8V±5%, V_{DDQ}=1.5V/1.8V)

Parameter	Symbol	Conditions	Units	Notes
Output Drive Power Supply Voltage	V_{DDQ}	1.5/1.8	V	
Input Logic HIGH Voltage	V_{IH}	V_{REF}+0.5	V	
Input Logic LOW Voltage	V_{IL}	V_{REF}–0.5	V	
Input Reference Voltage	V_{REF}	0.75/0.9	V	
Input Rise Time	T_R	2.0	V/ns	
Input Fall Time	T_F	2.0	V/ns	
Output Timing Reference Level		V_{REF}	V	
Clock Reference Level		V_{REF}	V	
Output Load Conditions				1, 2

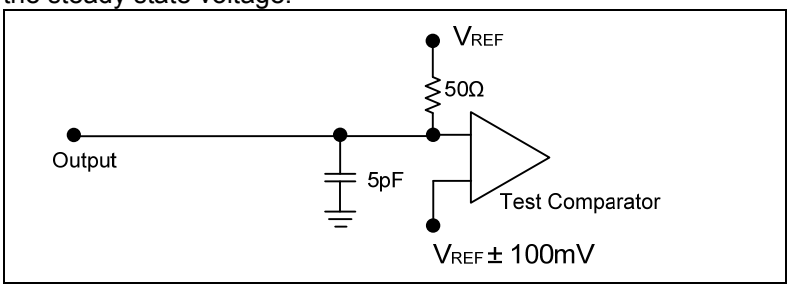
Notes:
1. See *AC Test Loading.*
2. Parameter Tested with RQ=250Ω and V_{DDQ}=1.5V

AC Test Loading

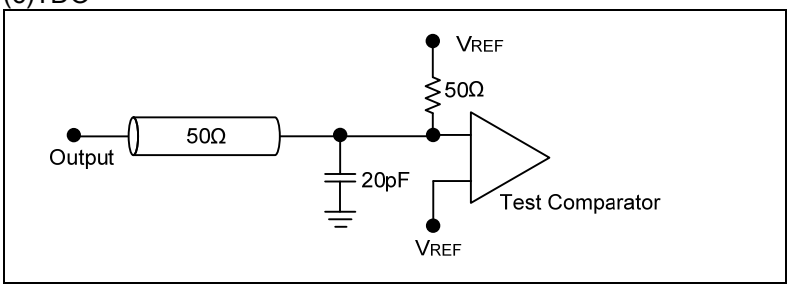
(a) Unless otherwise noted, AC test loading assume this condition.



(b) tCHQZ and tCHQX1 are specified with 5pF load capacitance and measured when transition occurs ±100mV from the steady state voltage.



(c)TDO



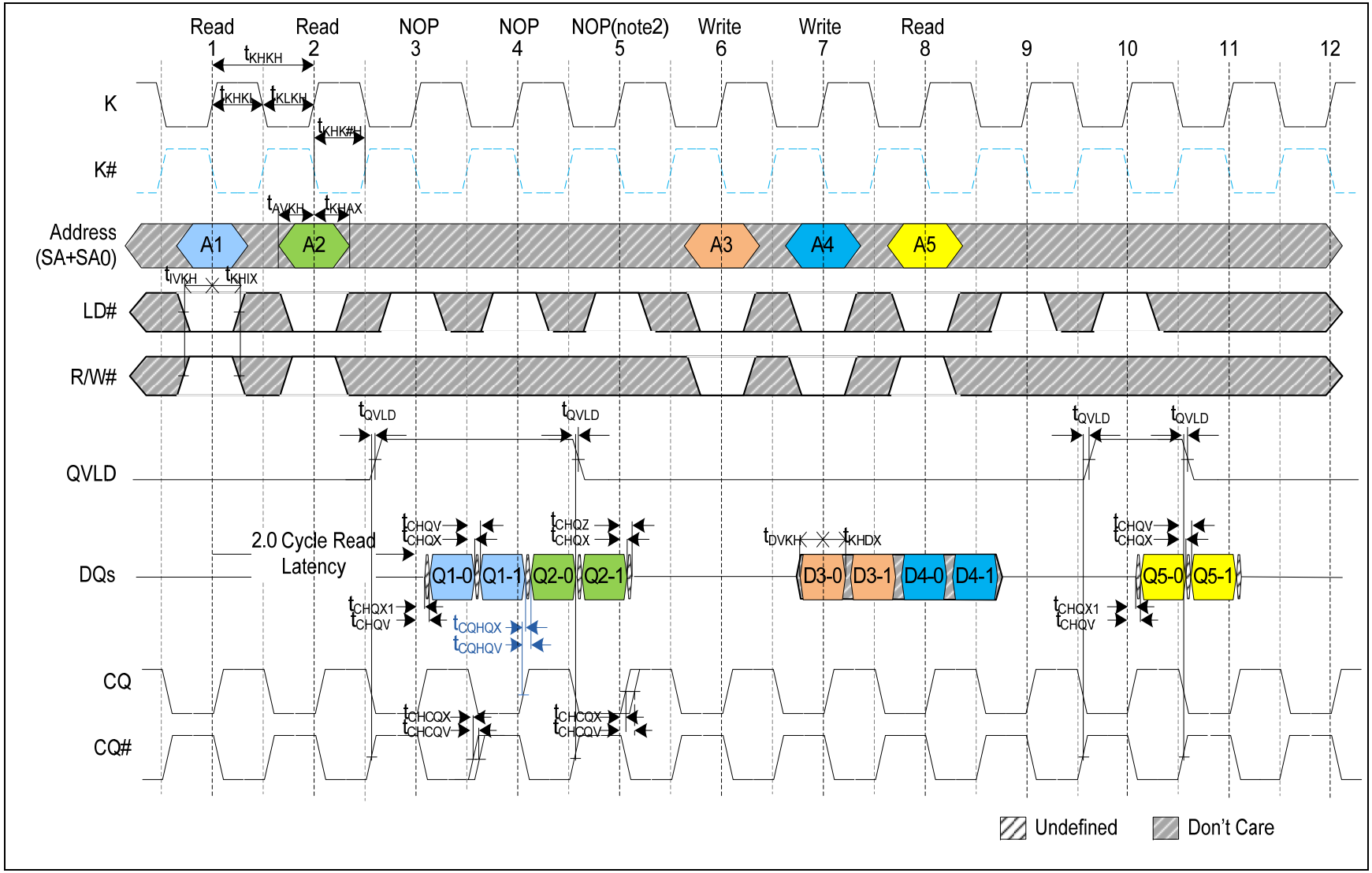
AC Timing Characteristics

(Over the Operating Temperature Range, V_{DD}=1.8V±5%, V_{DDQ}=1.5V/1.8V)

Parameter	Symbol	18 (550MHz)		20 (500MHz)		22 (450MHz)		25 (400MHz)		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock											
Clock Cycle Time (K, K#)	tKHKH	1.82	8.40	2.00	8.40	2.2	8.40	2.50	8.40	ns	
Clock Phase Jitter (K, K#)	tKC var		0.15		0.15		0.15		0.20	ns	4
Clock High Time (K, K#)	tKHKL	0.4		0.4		0.4		0.4		cycle	
Clock Low Time (K, K#)	tKLKH	0.4		0.4		0.4		0.4		cycle	
Clock to Clock# (K, K#)	tKHK#H	0.82		0.90		0.99		1.13		ns	
DLL Lock Time (K)	tKC lock	2048		2048		2048		2048		cycles	5
Doff Low period to DLL reset	tDoffLowToReset	5		5		5		5		ns	
K static to DLL reset	tKCreset	30		30		30		30		ns	
Output Times											
K, K# High to Output Valid	tCHQV		0.45		0.45		0.45		0.45	ns	
K, K# High to Output Hold	tCHQX	-0.45		-0.45		-0.45		-0.45		ns	
K, K# High to Echo Clock Valid	tCHCQV		0.45		0.45		0.45		0.45	ns	
K, K# High to Echo Clock Hold	tCHCQX	-0.45		-0.45		-0.45		-0.45		ns	
CQ, CQ# High to Output Valid	tCQHQV		0.15		0.15		0.2		0.2	ns	6
CQ, CQ# High to Output Hold	tCQHQX	-0.15		-0.15		-0.2		-0.2		ns	6
K, High to Output High-Z	tCHQZ		0.45		0.45		0.45		0.45	ns	
K, High to Output Low-Z	tCHQX1	-0.45		-0.45		-0.45		-0.45		ns	
CQ, CQ# High to QVLD Valid	tQVLD	-0.15	0.15	-0.15	0.15	-0.20	0.20	-0.20	0.20	ns	
Setup Times											
Address valid to K rising edge	tAVKH	0.23		0.25		0.30		0.40		ns	
R#,W# control inputs valid to K rising edge	tIVKH	0.23		0.25		0.30		0.40		ns	2
BW_x# control inputs valid to K rising edge	tIVKH2	0.18		0.20		0.25		0.28		ns	2
Data-in valid to K, K# rising edge	tDVKH	0.18		0.20		0.25		0.28		ns	
Hold Times											
K rising edge to address hold	tKHAX	0.23		0.25		0.30		0.40		ns	2
K rising edge to R#,W# control inputs hold	tKHIX	0.23		0.25		0.30		0.40		ns	2
K rising edge to BW_x# control inputs hold	tKHIX2	0.18		0.20		0.25		0.28		ns	
K, K# rising edge to data-in hold	tKHDX	0.18		0.20		0.25		0.28		ns	

Notes:
1. All address inputs must meet the specified setup and hold times for all latching clock edges.
2. During normal operation, VIH, VIL, TRISE, and TFALL of inputs must be within 20% of VIH, VIL, TRISE, and TFALL of clock.
3. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
4. V_{DD} slew rate must be less than 0.1V DC per 50ns for DLL lock retention. DLL lock time begins once V_{DD} and input clock are stable.
5. The data sheet parameters reflect tester guard bands and test setup variations.
6. To avoid bus contention, at a given voltage and temperature tCHQX1 is bigger than tCHQZ. The specs as shown do not imply bus contention because tCHQX1 is a MIN parameter that is worst case at totally different test conditions (0 C, 1.9V) than tCHQZ, which is a MAX parameter (worst case at 70 C, 1.7V) It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

Read, Write, and NOP Timing Diagram



Notes: 1. Q1-0 refers to the output from address A1. Q1-1 refers to the output from the next burst address following A1.
2. The NOP cycle is not necessary for correct device operation, however, at high clock frequencies, it might be required to prevent bus contention.

IEEE 1149.1 Serial Boundary Scan of JTAG

These SRAMs incorporate a serial boundary scan Test Access Port (TAP) controller in 165 FBGA package. That is fully compliant with IEEE Standard 1149.1-2001. The TAP controller operates using standard 1.8 V interface logic levels.

Disabling the JTAG feature

These SRAMs operate without using the JTAG feature. To disable the TAP controller, TCK must be tied Low (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to VDD through a pull up resistor. TDO must be left unconnected. Upon power up, the device comes up in a reset state, which does not interfere with the operation of the device.

Test Access Port Signal List:

Test Clock (TCK)

The test clock is to operate only TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is to set commands of the TAP controller and is sampled on the rising edge of TCK. This pin can be left unconnected at SRAM operation. The pin is pulled up internally to keep logic high level.

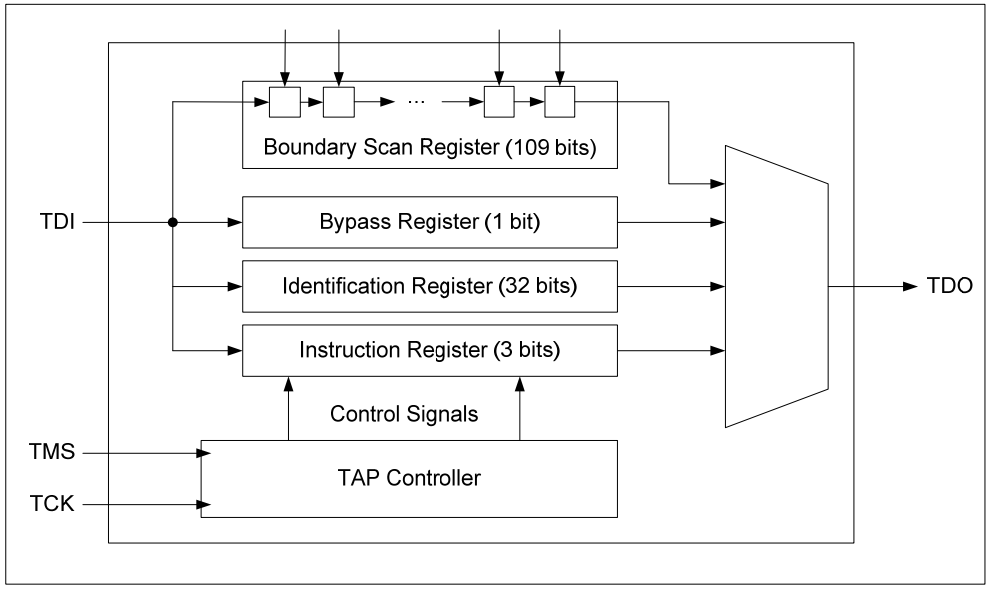
Test Data-In (TDI)

The TDI pin is to receive serially input information into the instruction and data registers. It can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register (Refer to the TAP Controller State Diagram). TDI is internally pulled up and can be unconnected at SRAM. TDI is connected to the most significant bit (MSB) on any register.

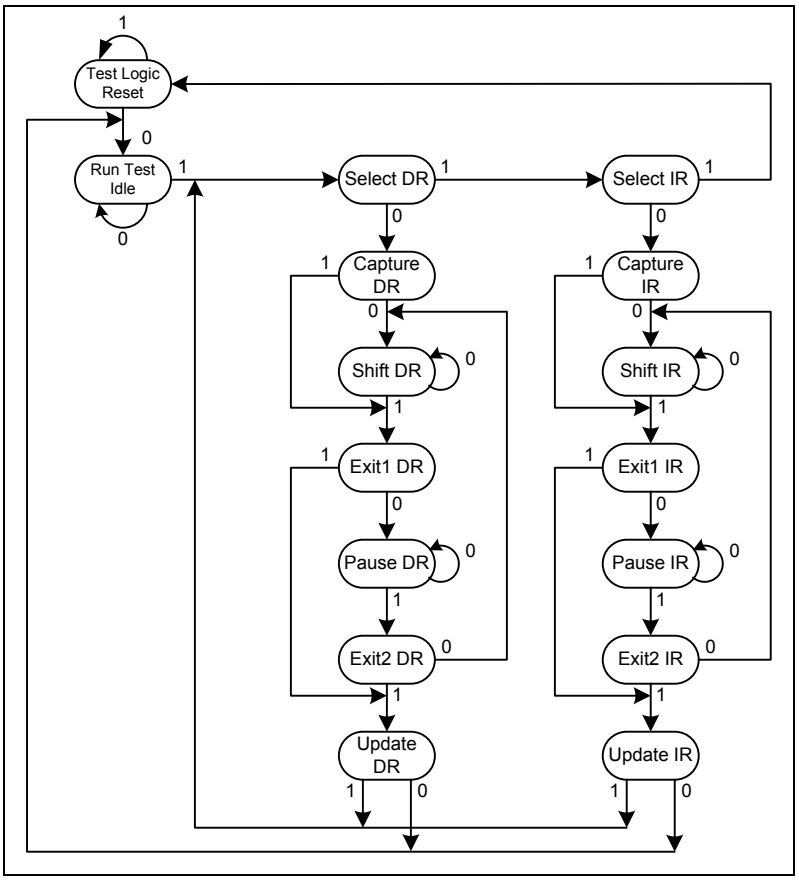
Test Data-Out (TDO)

The TDO pin is to drive serially clock data out from the JTAG registers. The output is active, depending upon the current state of the TAP state machine (Refer to instruction codes). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

TAP Controller State and Block Diagram



TAP Controller State Machine



Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This Reset does not affect the operation of the SRAM and can be performed while the SRAM is operating. At power up, the TAP is reset internally to ensure that TDO comes up in a High Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

Instruction Register

This register is loaded during the update-IR state of the TAP controller. Three-bit instructions can be serially loaded into the instruction register. At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section. When the TAP controller is in the capture-IR state, the two LSBs are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

The bypass register is a single-bit register that can be placed between the TDI and TDO balls. It is to skip certain chips without serial boundary scan. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and output balls on the SRAM. Several No Connected(NC) balls are also included in the scan register to reserve other product options. The boundary scan register is loaded with the contents of the SRAM input and output ring when the TAP controller is in the capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the input and output ring. Each bit corresponds to one of the balls on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the shift-DR state. The ID register has a vendor ID code and other information

TAP Instruction Set

TAP Instruction Set is available to set eight instructions with the three bit instruction register and all combinations are listed in the TAP Instruction Code Table. Three of listed instructions on this table are reserved and must not be used. Instructions are loaded serially into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High Z state until the next command is supplied during the Update IR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a IEEE 1149.1 basic instruction which connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state.. A snapshot of data on the inputs and output balls is captured in the boundary scan register when the TAP controller is in a Shift-DR state. The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates significantly faster. Because there is a large difference between the clock frequencies, it is possible that during the capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition. This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible. To ensure that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time. The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/ PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register. Once the data is captured, it is possible to shift out the data by putting the TAP into the shift-DR state. This places the boundary scan register between the TDI and TDO balls.
PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation. The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required, that is, while the data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

PRIVATE

Do not use these instructions. They are reserved for future use and engineering mode.

EXTEST

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the Shift-DR controller state. IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode. The boundary scan register has a special bit located at bit #109. When this scan cell, called the "EXTEST output bus tri-state," is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High Z condition. This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is pre-set LOW to enable the output when the device is powered up, and also when the TAP controller is in the Test-Logic-Reset state.

JTAG DC Operating Characteristics

(Over the Operating Temperature Range, V_{DD}=1.8V±5%)

Parameter	Symbol	Min	Max	Units	Notes
JTAG Input High Voltage	V_{IH1}	1.3	V_{DD}+0.3	V	
JTAG Input Low Voltage	V_{IL1}	–0.3	0.5	V	
JTAG Output High Voltage	V_{OH1}	1.4	-	V	$\|I_{OH1}\|$=2mA
JTAG Output Low Voltage	V_{OL1}	-	0.4	V	I_{OL1}=2mA
JTAG Output High Voltage	V_{OH2}	1.6	-	V	$\|I_{OH2}\|$=100uA
JTAG Output Low Voltage	V_{OL2}	-	0.2	V	I_{OL2}=100uA
JTAG Input Leakage Current	I_{LIJTAG}	-100	+100	uA	0 ≤ Vin ≤ VDD
JTAG Output Leakage Current	I_{LOJTAG}	-5	+5	uA	0 ≤ Vout ≤ VDD

Notes:
1. All voltages referenced to VSS (GND); All JTAG inputs and outputs are LVTTL-compatible.

JTAG AC Test Conditions

(Over the Operating Temperature Range, V_{DD}=1.8V±5%, V_{DDQ}=1.5V/1.8V)

Parameter	Symbol	Conditions	Units
Input Pulse High Level	V_{IH1}	1.3	V
Input Pulse Low Level	V_{IL1}	0.5	V
Input Rise Time	T_{R1}	1.0	ns
Input Fall Time	T_{F1}	1.0	ns
Input and Output Timing Reference Level		0.9	V

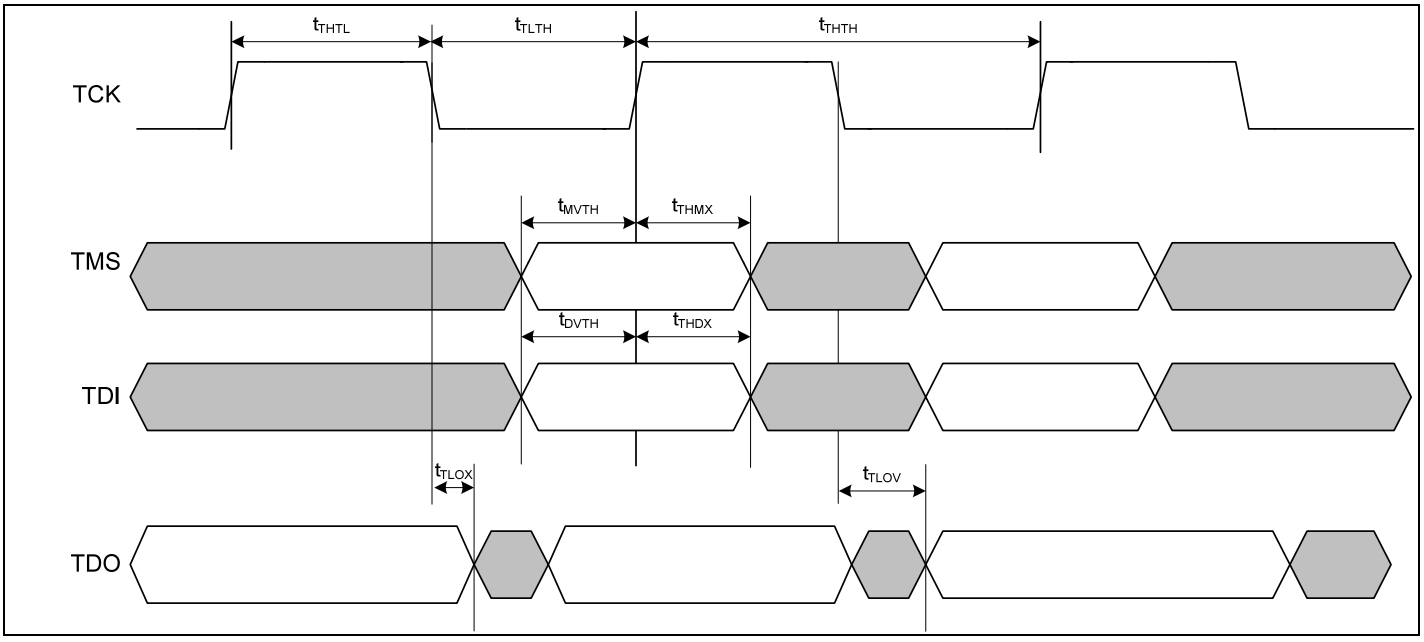
JTAG AC Characteristics

(Over the Operating Temperature Range, V_{DD}=1.8V±5%, V_{DDQ}=1.5V/1.8V)

Parameter	Symbol	Min	Max	Units
TCK cycle time	t_{THTH}	50	–	ns
TCK high pulse width	t_{THTL}	20	–	ns
TCK low pulse width	t_{TLTH}	20	–	ns
TMS Setup	t_{MVTH}	5	–	ns
TMS Hold	t_{THMX}	5	–	ns
TDI Setup	t_{DVTH}	5	–	ns
TDI Hold	t_{THDX}	5	–	ns
Capture Setup	t_{CVTH}	5	–	ns
Capture Hold	t_{THCX}	5	–	ns
TCK Low to Valid Data*	t_{TLOV}	–	10	ns
TCK Low to Invalid Data*	t_{TLQX}	0	–	ns

Note: See *AC Test Loading(c)*

JTAG Timing Diagram



Instruction Set

Code	Instruction	TDO Output
000	EXTEST	Boundary Scan Register
001	IDCODE	32-bit Identification Register
010	SAMPLE-Z	Boundary Scan Register
011	PRIVATE	Do Not Use
100	SAMPLE(/PRELOAD)	Boundary Scan Register
101	PRIVATE	Do Not Use
110	PRIVATE	Do Not Use
111	BYPASS	Bypass Register

ID Register Definition

Revision Number (31:29)	Part Configuration (28:12)	Vendor ID Code (11:1)	Start Bit (0)
000	0TDEF0WX01PQLBTS0	00011010101	1

Part Configuration Definition:

1. DEF = 001 for 18Mb, 010 for 36Mb, 011 for 72Mb
2. WX = 11 for x36, 10 for x18
3. P = 1 for II+(QUAD-P/DDR-IIP), 0 for II(QUAD/DDR-II)
4. Q = 1 for QUAD, 0 for DDR-II
5. L = 1 for RL=2.5, 0 for RL≠2.5
6. B = 1 for burst of 4, 0 for burst of 2
7. S = 1 for Separate I/O, 0 for Common I/O
8. T = 1 for ODT option, 0 for No ODT option

Boundary Scan Exit Order

ORDER	Pin ID
1	6R
2	6P
3	6N
4	7P
5	7N
6	7R
7	8R
8	8P
9	9R
10	11P
11	10P
12	10N
13	9P
14	10M
15	11N
16	9M
17	9N
18	11L
19	11M
20	9L
21	10L
22	11K
23	10K
24	9J
25	9K
26	10J
27	11J
28	11H
29	10G
30	9G
31	11F
32	11G
33	9F
34	10F
35	11E
36	10E

ORDER	Pin ID
37	10D
38	9E
39	10C
40	11D
41	9C
42	9D
43	11B
44	11C
45	9B
46	10B
47	11A
48	10A
49	9A
50	8B
51	7C
52	6C
53	8A
54	7A
55	7B
56	6B
57	6A
58	5B
59	5A
60	4A
61	5C
62	4B
63	3A
64	2A
65	1A
66	2B
67	3B
68	1C
69	1B
70	3D
71	3C
72	1D

ORDER	Pin ID
73	2C
74	3E
75	2D
76	2E
77	1E
78	2F
79	3F
80	1G
81	1F
82	3G
83	2G
84	1H
85	1J
86	2J
87	3K
88	3J
89	2K
90	1K
91	2L
92	3L
93	1M
94	1L
95	3N
96	3M
97	1N
98	2M
99	3P
100	2N
101	2P
102	1P
103	3R
104	4R
105	4P
106	5P
107	5N
108	5R
109	Internal

Notes:
1. NC pins as defined on the **FBGA Ball Assignments** are read as ”don’t cares”.
2. State of internal pin (#109) is loaded via JTAG

Ordering Information

Commercial Range: 0°C to +70°C

Speed	Order Part No.	Organization	Package
550 MHz	IS61DDP2B251236A-550M3	512Kx36	165 FBGA (15x17 mm)
	IS61DDP2B251236A-550M3L	512Kx36	165 FBGA (15x17 mm), lead free
	IS61DDP2B21M18A-550M3	1Mx18	165 FBGA (15x17 mm)
	IS61DDP2B21M18A-550M3L	1Mx18	166 FBGA (15x17 mm), lead free
500 MHz	IS61DDP2B251236A-500M3	512Kx36	165 FBGA (15x17 mm)
	IS61DDP2B251236A-500M3L	512Kx36	165 FBGA (15x17 mm), lead free
	IS61DDP2B21M18A-500M3	1Mx18	165 FBGA (15x17 mm)
	IS61DDP2B21M18A-500M3L	1Mx18	165 FBGA (15x17 mm), lead free
450 MHz	IS61DDP2B251236A-450M3	512Kx36	165 FBGA (15x17 mm)
	IS61DDP2B251236A-450M3L	512Kx36	165 FBGA (15x17 mm), lead free
	IS61DDP2B21M18A-450M3	1Mx18	165 FBGA (15x17 mm)
	IS61DDP2B21M18A-450M3L	1Mx18	165 FBGA (15x17 mm), lead free
400 MHz	IS61DDP2B251236A-400M3	512Kx36	165 FBGA (15x17 mm)
	IS61DDP2B251236A-400M3L	512Kx36	165 FBGA (15x17 mm), lead free
	IS61DDP2B21M18A-400M3	1Mx18	165 FBGA (15x17 mm)
	IS61DDP2B21M18A-400M3L	1Mx18	165 FBGA (15x17 mm), lead free

Commercial Range: °C to +70°C

Speed	Order Part No.	Organization	Package
550 MHz	IS61DDP2B251236A-550B4	512Kx36	165 FBGA (13x15 mm)
	IS61DDP2B251236A-550B4L	512Kx36	165 FBGA (13x15 mm), lead free
	IS61DDP2B21M18A-550B4	1Mx18	165 FBGA (13x15 mm)
	IS61DDP2B21M18A-550B4L	1Mx18	166 FBGA (13x15 mm), lead free
500 MHz	IS61DDP2B251236A-500B4	512Kx36	165 FBGA (13x15 mm)
	IS61DDP2B251236A-500B4L	512Kx36	165 FBGA (13x15 mm), lead free
	IS61DDP2B21M18A-500B4	1Mx18	165 FBGA (13x15 mm)
	IS61DDP2B21M18A-500B4L	1Mx18	165 FBGA (13x15 mm), lead free
450 MHz	IS61DDP2B251236A-450B4	512Kx36	165 FBGA (13x15 mm)
	IS61DDP2B251236A-450B4L	512Kx36	165 FBGA (13x15 mm), lead free
	IS61DDP2B21M18A-450B4	1Mx18	165 FBGA (13x15 mm)
	IS61DDP2B21M18A-450B4L	1Mx18	165 FBGA (13x15 mm), lead free
400 MHz	IS61DDP2B251236A-400B4	512Kx36	165 FBGA (13x15 mm)
	IS61DDP2B251236A-400B4L	512Kx36	165 FBGA (13x15 mm), lead free
	IS61DDP2B21M18A-400B4	1Mx18	165 FBGA (13x15 mm)
	IS61DDP2B21M18A-400B4L	1Mx18	165 FBGA (13x15 mm), lead free

Industrial Range: -40°C to +85°C

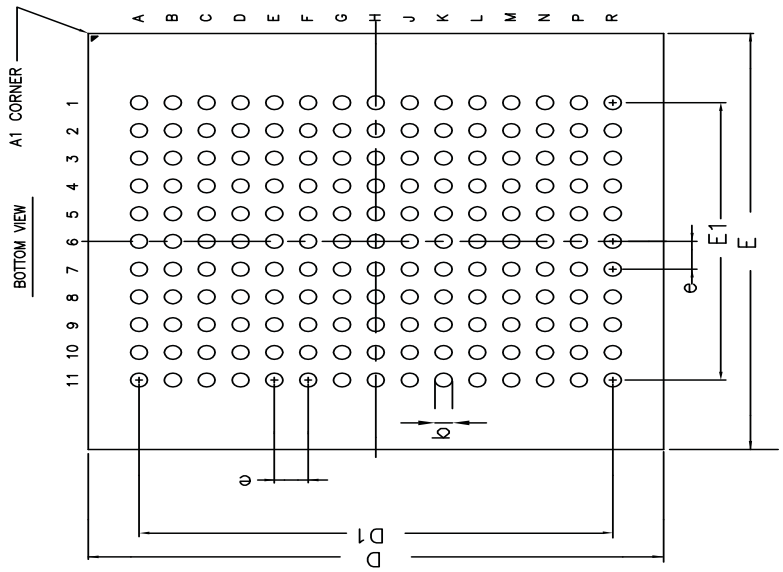
Speed	Order Part No.	Organization	Package
550 MHz	IS61DDP2B251236A-550M3I	512Kx36	165 FBGA (15x17 mm)
	IS61DDP2B251236A-550M3LI	512Kx36	165 FBGA (15x17 mm), lead free
	IS61DDP2B21M18A-550M3I	1Mx18	165 FBGA (15x17 mm)
	IS61DDP2B21M18A-550M3LI	1Mx18	166 FBGA (15x17 mm), lead free
500 MHz	IS61DDP2B251236A-500M3I	512Kx36	165 FBGA (15x17 mm)
	IS61DDP2B251236A-500M3LI	512Kx36	165 FBGA (15x17 mm), lead free
	IS61DDP2B21M18A-500M3I	1Mx18	165 FBGA (15x17 mm)
	IS61DDP2B21M18A-500M3LI	1Mx18	165 FBGA (15x17 mm), lead free
450 MHz	IS61DDP2B251236A-450M3I	512Kx36	165 FBGA (15x17 mm)
	IS61DDP2B251236A-450M3LI	512Kx36	165 FBGA (15x17 mm), lead free
	IS61DDP2B21M18A-450M3I	1Mx18	165 FBGA (15x17 mm)
	IS61DDP2B21M18A-450M3LI	1Mx18	165 FBGA (15x17 mm), lead free
400 MHz	IS61DDP2B251236A-400M3I	512Kx36	165 FBGA (15x17 mm)
	IS61DDP2B251236A-400M3LI	512Kx36	165 FBGA (15x17 mm), lead free
	IS61DDP2B21M18A-400M3I	1Mx18	165 FBGA (15x17 mm)
	IS61DDP2B21M18A-400M3LI	1Mx18	165 FBGA (15x17 mm), lead free

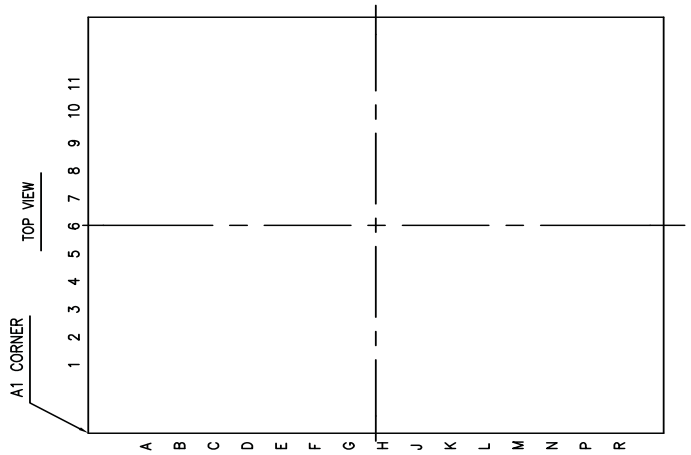
Industrial Range: -40°C to +85°C

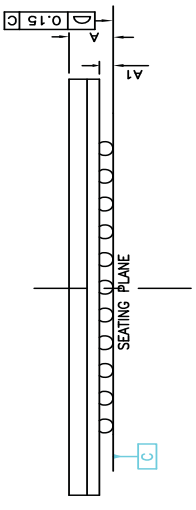
Speed	Order Part No.	Organization	Package
550 MHz	IS61DDP2B251236A-550B4I	512Kx36	165 FBGA (13x15 mm)
	IS61DDP2B251236A-550B4LI	512Kx36	165 FBGA (13x15 mm), lead free
	IS61DDP2B21M18A-550B4I	1Mx18	165 FBGA (13x15 mm)
	IS61DDP2B21M18A-550B4LI	1Mx18	166 FBGA (13x15 mm), lead free
500 MHz	IS61DDP2B251236A-500B4I	512Kx36	165 FBGA (13x15 mm)
	IS61DDP2B251236A-500B4LI	512Kx36	165 FBGA (13x15 mm), lead free
	IS61DDP2B21M18A-500B4I	1Mx18	165 FBGA (13x15 mm)
	IS61DDP2B21M18A-500B4LI	1Mx18	165 FBGA (13x15 mm), lead free
450 MHz	IS61DDP2B251236A-450B4I	512Kx36	165 FBGA (13x15 mm)
	IS61DDP2B251236A-450B4LI	512Kx36	165 FBGA (13x15 mm), lead free
	IS61DDP2B21M18A-450B4I	1Mx18	165 FBGA (13x15 mm)
	IS61DDP2B21M18A-450B4LI	1Mx18	165 FBGA (13x15 mm), lead free
400 MHz	IS61DDP2B251236A-400B4I	512Kx36	165 FBGA (13x15 mm)
	IS61DDP2B251236A-400B4LI	512Kx36	165 FBGA (13x15 mm), lead free
	IS61DDP2B21M18A-400B4I	1Mx18	165 FBGA (13x15 mm)
	IS61DDP2B21M18A-400B4LI	1Mx18	165 FBGA (13x15 mm), lead free

Package drawing – 15x17x1.4 BGA

SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.40	0.055	—	—
A1	0.27	—	0.46	0.018	—	0.011
b	0.40	0.45	0.50	0.020	0.018	0.016
D	16.90	17.00	17.10	0.673	0.669	0.665
D1	13.90	14.00	14.10	0.555	0.551	0.547
E	14.90	15.00	15.10	0.594	0.591	0.587
E1	9.90	10.00	10.10	0.398	0.394	0.390
e	1.00 BSC			0.039 BSC		







NOTE :

1. Controlling dimension : mm

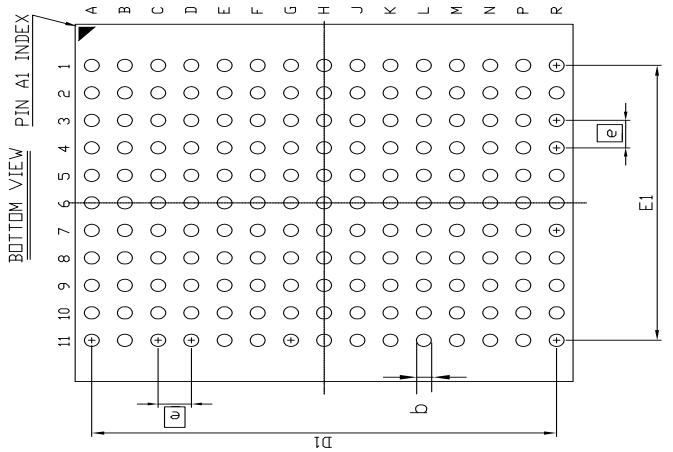
ISSI	TITLE	165L 15x17mm LF-BGA Package Outline	REV. B	DATE 12/10/2007

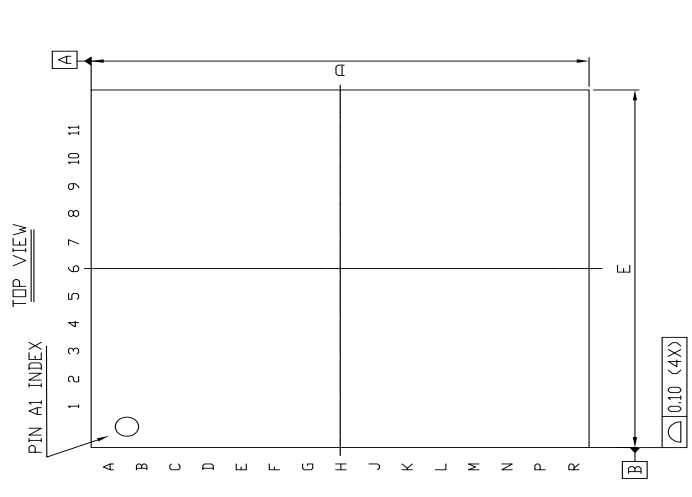
Package drawing – 13x15x1.4 BGA

SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.40	—	—	0.055
A1	0.25	—	0.40	0.010	—	0.016
b	0.40	0.45	0.50	0.016	0.018	0.020
D	14.90	15.00	15.10	0.587	0.591	0.594
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	12.90	13.00	13.10	0.508	0.512	0.516
E1	9.90	10.00	10.10	0.390	0.394	0.398
e	1.00 BSC			0.039 BSC		

NOTE :

1. CONTROLLING DIMENSION : MM .







ISSI	TITLE	165L 13x15x1.4mm LF-BGA Package Outline	REV. A
			DATE 11/29/2011