



## UPS1602

## LINEAR INTEGRATED CIRCUIT

### HIGH PERFORMANCE CURRENT MODE POWER SWITCH

#### DESCRIPTION

The UTC **UPS1602** is designed to provide several special enhancements to satisfy the needs, for example, power-saving mode for low standby power (<0.3w), frequency hopping , constant output power limiting , slope compensation ,over current protection (OCP), over voltage protection (OVP), over load protection (OLP), under voltage lock out (UVLO), short Circuit Protection (SCP) and Over Temperature Protection (OTP), etc. IC will be shut down or can auto-restart in those situations.

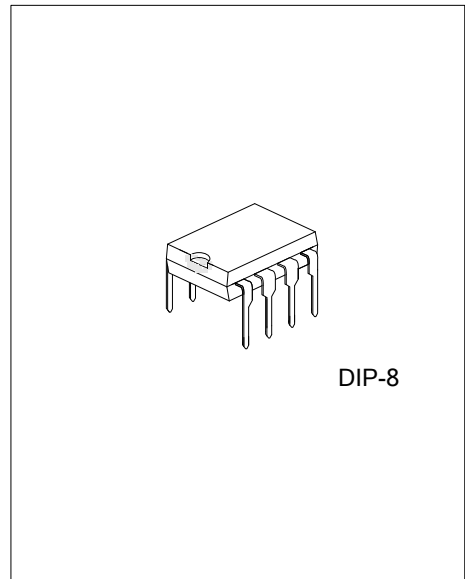
#### FEATURES

- \* Low startup current (about 22μA)
- \* Fixed switching frequency(Norm. is 68KHz)
- \* Frequency hopping for Improved EMI Performance.
- \* Lower than 0.3W Standby Power Design
- \* Linearly decreasing frequency to 26KHz during light load
- \* Soft start
- \* Internal Slope Compensation
- \* Constant Power Limiting for universal AC input Range
- \* Gate Output Maximum Voltage Clamp(15V)
- \* Max duty cycle 74%
- \* Over temperature protection
- \* Overload protection
- \* Over voltage protection
- \* Leading edge blanking
- \* Cycle-by-Cycle current limiting
- \* Under Voltage Lock Out
- \* Short Circuit Protection

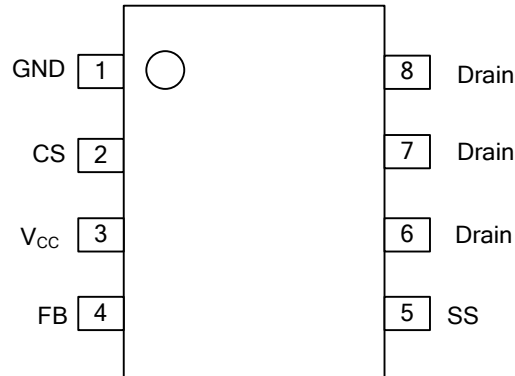
#### ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UPS1602L-D08-T	UPS1602G-D08-T	DIP-8	Tube

UPS1602L-D08-T 	(1) T: Tube (2) D08: DIP-8 (3) G: Halogen Free, L: Lead Free
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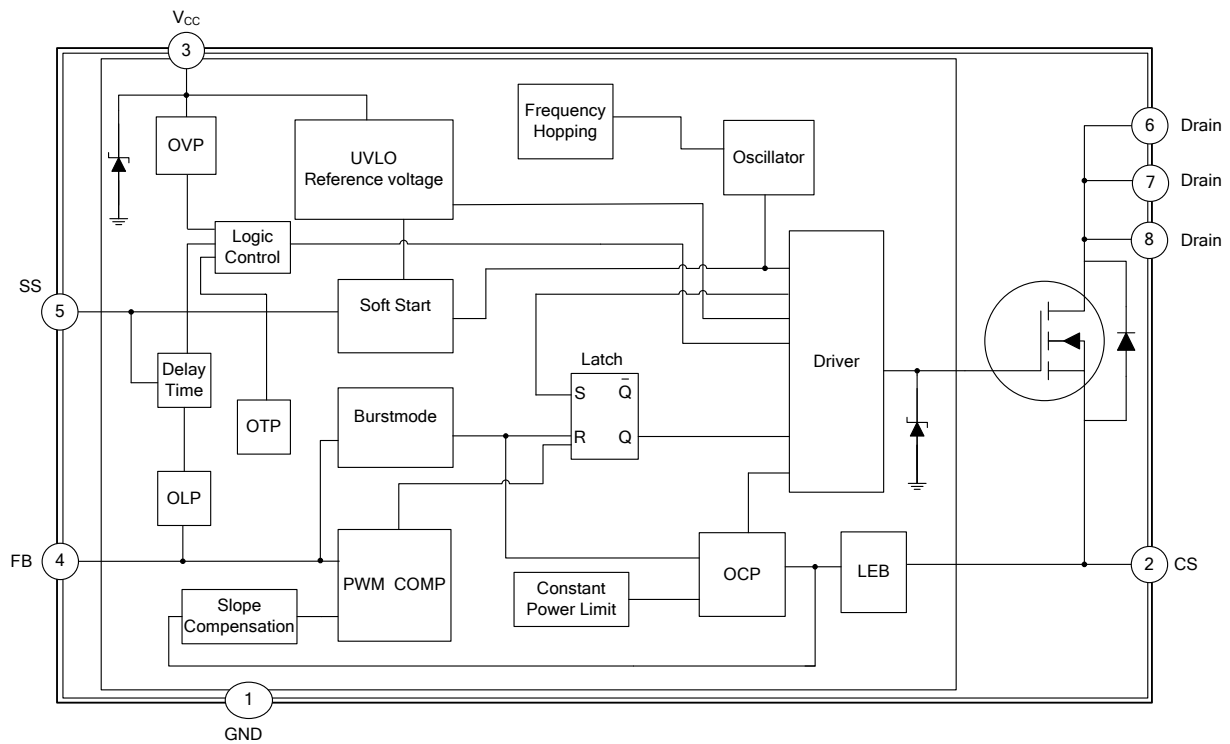
### ■ PIN CONFIGURATION



### ■ PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
1	GND	Ground
2	CS	Controller current sense input
3	V <sub>CC</sub>	Supply voltage
4	FB	Feedback
5	SS	Soft-start, connect Capacitor C <sub>SOFTS</sub> to GND
6, 7, 8	Drain	Power MOSFET drain

### ■ BLOCK DIAGRAM



- Notes:
- OLP (Over Load Protection)
  - OVP (Over Voltage Protection)
  - OTP (Over Temperature Protection)
  - OCP (Over Current Protection)
  - UVLO (Under Voltage Latch-Out)
  - LEB (Led Edge Blanking)
  - SS (Soft Start)

■ ABSOLUTE MAXIMUM RATINGS ( $T_A=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC}$	30	V
Input Voltage to FB Pin	$V_{FB}$	-0.3 ~ 6.2	V
Input Voltage to CS Pin	$V_{CS}$	-0.3 ~ 2.8	V
Junction Temperature	$T_J$	+150	$^{\circ}\text{C}$
Operating Temperature	$T_{OPR}$	-40 ~ +125	$^{\circ}\text{C}$
Storage Temperature	$T_{STG}$	-50 ~ +150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC}$	8.6 ~ 22	V

■ ELECTRICAL CHARACTERISTICS ( $T_A=25^{\circ}\text{C}$ ,  $V_{CC}=15\text{V}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>SUPPLY SECTION</b>							
Start Up Current	$I_{STR}$	$V_{CC} = V_{CC(ON)} - 0.1\text{V}$		22	45	$\mu\text{A}$	
Supply Current with switch	$I_{OFF}$	$V_{SS} = 0, I_{FB} = 0$		7	9	mA	
	$I_{ON}$	$V_{SS} = 4.8\text{V}, I_{FB} = 0$		7	9	mA	
<b>UNDER-VOLTAGE LOCKOUT SECTION</b>							
Start Threshold Voltage	$V_{THD(ON)}$		13.5	14.2	15	V	
Min. Operating Voltage	$V_{CC(MIN)}$		7.5	8.2	9	V	
Hysteresis	$V_{CC(HY)}$			6		V	
<b>INTERNAL VOLTAGE REFERENCE</b>							
Reference Voltage	$V_{REF}$	measured at pin $V_{FB}$	6.3	6.5	6.7	V	
<b>CONTROL SECTION</b>							
$V_{FB}$ Operating Level	$V_{MIN}$		0.5			V	
	$V_{MAX}$				4.4		
Burst-Mode Out FB Voltage	$V_{FB(OUT)}$	$V_{CS} = 0$		1.7		V	
Reduce-Frequency end FB Voltage	$V_{FB(END)}$	$V_{CS} = 0$		1.6		V	
Burst-Mode Enter FB Voltage	$V_{FB(IN)}$	$V_{CS} = 0$		1.5		V	
Switch Frequency	Normal Power-Saving	$F_{(SW)}$	$V_{FB} = 4\text{V}$	61	68	75	kHz
			Before enter burst mode	20		40	kHz
Duty Cycle		$D_{MAX}$	$V_{FB} = 4.4\text{V}, V_{CS} = 0$	68	74	80	%
		$D_{MIN}$	$V_{FB} < 0.5\text{V}$	0			%
Frequency Hopping	$F_{J(SW)}$		$\pm 1.5$	$\pm 3$	$\pm 4.5$	kHz	
Frequency Variation VS $V_{CC}$ Deviation	$F_{DV}$	$V_{CC} = 10$ to $20\text{V}$			5	%	
Frequency Variation VS Temperature Deviation	$F_{DT}$	$T = -40$ to $105^{\circ}\text{C}$			5	%	
Feedback Resistor	$R_{FB}$	$V_{FB} = 0\text{V}$	16	21	26	k $\Omega$	
Soft-Start Time	$T_{SS}$	$C_{SS} = 0.47\mu\text{F}$	9.9	11.2	12.6	ms	
<b>PROTECTION SECTION</b>							
OVP threshold	$V_{OVP1}$	$V_{SS} < 3.5\text{V}, V_{FB} > 5\text{V}$		19		V	
	$V_{OVP2}$	$V_{SS} = 4.8\text{V}, V_{FB} = 3\text{V}$		28		V	
OLP threshold	$V_{FB(OLP)}$	$V_{CS} = 0, SS\text{-PIN OPEN}$	4.7	4.9	5.1	V	
Delay Time Of OLP	$T_{D-OLP}$	$C_{SS} = 0.47\mu\text{F}$	55	62	70	ms	
OTP threshold	$T_{(THR)}$		120	135	150	$^{\circ}\text{C}$	
OVP Disable threshold	$V_{SS(DEACT)}$	$V_{FB} > 5\text{V}, V_{CC} = 22\text{V}$	3.9	4.1	4.3	V	
OLP Enable threshold	$V_{SS(ACT)}$	$V_{FB} > 5\text{V}$	5.1	5.4	5.7	V	

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CURRENT LIMITING SECTION</b>						
Peak Current Limitation	$V_{CS}$	$V_{FB}=4.4V$		0.86	1	V
Threshold Voltage For $I_{VIN}=60\mu A$	$V_{SENSE-L}$	$I_{VIN}=60\mu A$		0.77		V
<b>POWER MOS-TRANSISTOR SECTION</b>						
Drain-Source Breakdown Voltage	$V_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	650			V
Turn-on voltage between gate and source	$V_{TH}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2		4	V
Drain-Source Diode Continuous Source Current	$I_S$				2	A
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=1A$		3.8	5	$\Omega$
Rise Time	$t_R$	$V_{DD} = 300V, I_D = 2.4A$		25	60	ns
Fall Time	$t_F$	$R_G = 25\Omega$ (Note 1,2)		25	60	ns

- Note: 1. Pulse Test: Pulse Width $\leq 300\mu s$ , Duty cycle $\leq 2\%$   
 2. Essentially independent of operating temperature

■ FUNCTIONAL DESCRIPTION

The internal reference voltages and bias circuit work at  $V_{CC} > V_{THD(ON)}$ , and shutdown at  $V_{CC} < V_{CC(MIN)}$ .

(1) Soft-Start

When every IC power on, driver output duty cycle will be decided by voltage  $V_{SS}$  on soft-start capacitor and  $V_{CS}$  on current sense resistor at beginning. After  $V_{SS}$  reach 4.2V, the whole soft-start phase end, and driver duty cycle depend on  $V_{FB}$  and  $V_{CS}$ . The relation among  $V_{SS}$ ,  $V_{FB}$  and  $V_{OUT}$  as followed Fig.3.

Furthermore, soft-start phase should end before  $V_{CC}$  reach  $V_{CC(MIN)}$  during  $V_{CC}$  power on. Otherwise, if soft-start phase remain not end before  $V_{CC}$  reach  $V_{CC(MIN)}$  during  $V_{CC}$  power on, IC will enter auto-restart phase and not set up  $V_{OUT}$ . So the value of  $C_{SS}$  should be between 0.1 $\mu$ F and 4.7 $\mu$ F.

Finally soft-start also set OVP1 active phase. OVP1 active phase between 0 and  $V_{SS(DEACT)}$ , OVP1 will not be sensed after  $V_{SS}$  reach  $V_{SS(DEACT)}$ . The Soft-start phase  $T_{SS}$ :  $T_{SS} = 23.8 \times C_{SS}$  (ms) (Example:  $C_{SS} = 0.47\mu$ F, then  $T_{SS} = 23.8 \times 0.47 = 11.2$ ms).

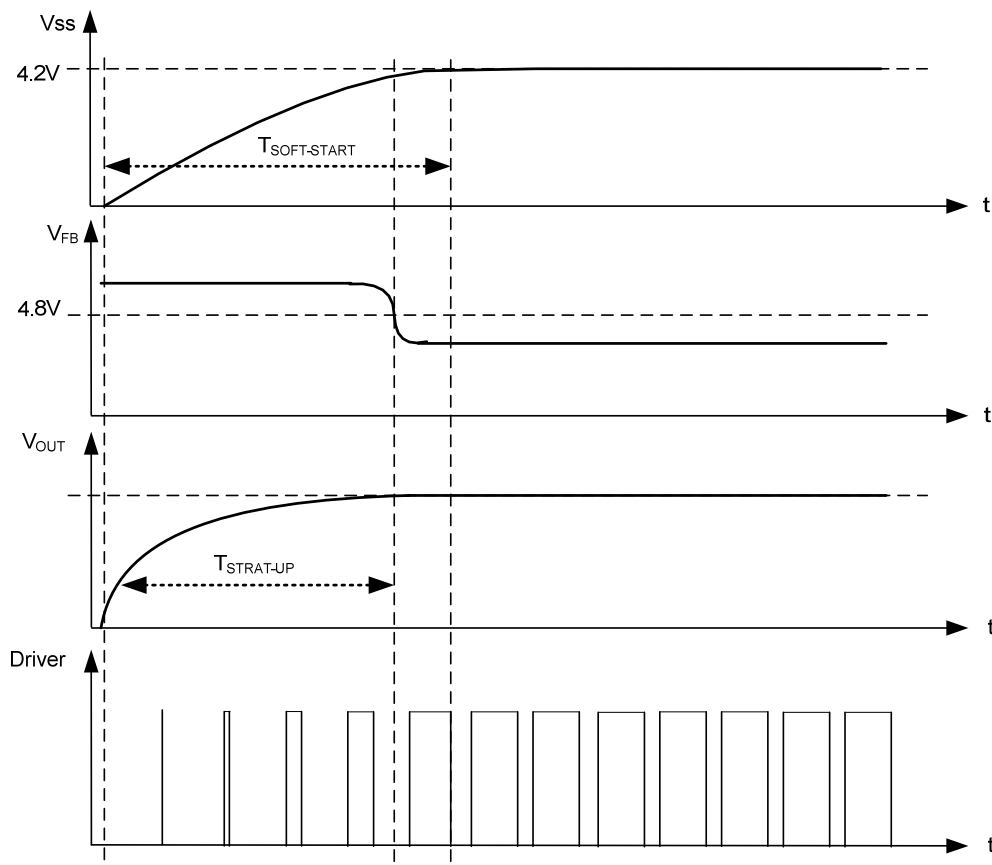


Fig.3 Soft-start phase

■ FUNCTIONAL DESCRIPTION(Cont.)

**(2) Switch Frequency Set**

The maximum switch frequency is set to 68kHz. Switch frequency is modulated by output power  $P_{OUT}$  during IC operating. At no load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the subber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. So lower switch frequency at lower load, which more and more improve IC's efficiency at light load. At from no load to light load condition, the IC will operate at from Burst mode to Reducing Frequency Mode. The relation curve between  $f_{sw}$  and  $P_{OUT}/P_{OUT(MAX)}$  as followed Fig.4.

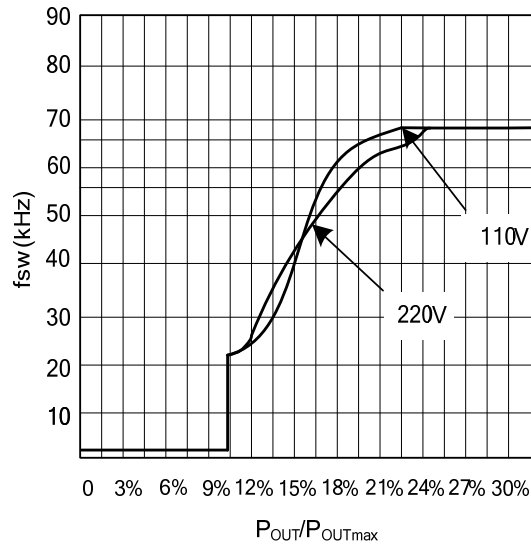


Fig.4 The relation curve between  $f_{sw}$  and relative output power  $P_{OUT}/ P_{OUT(MAX)}$

**(3) Internal Synchronized Slope Compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation, this greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

**(4) Frequency Hopping For EMI Improvement**

The Frequency hopping is implemented in the IC; there are two oscillators built-in the IC. The first oscillator is to set the normal switching frequency; the switching frequency is modulated with a period signal generated by the 2nd oscillator. The relation between the first oscillator and the 2nd oscillator as followed Fig.5. So the tone energy is evenly spread out, the spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

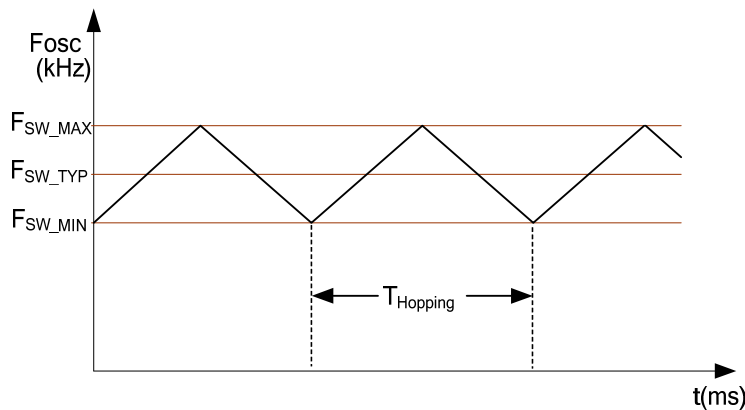


Fig.5 Frequency Hopping

■ FUNCTIONAL DESCRIPTION(Cont.)

(5) Constant Output Power Limit

When the SENSE voltage, across the sense resistor  $R_S$ , reaches the threshold voltage, around 1V, the output GATE drive will be turned off after a small propagation delay  $t_D$ . This propagation delay will introduce an additional current proportional to  $t_D \times V_{IN} / L_P$ . Since the propagation delay is nearly constant regardless of the input line voltage  $V_{IN}$ . Higher input line voltage will result in a larger additional current and hence the output power limit is also higher than that under low input line voltage. To guarantee the output power is a constant for universal input AC voltage, there is a dynamic peak limit circuit to compensate the system delay  $T_{D-OC}$  that the system delay brings on.  $I_{PEAK-MAX} = 0.8V / R_{SENSE} (V_{IN} = 264V_{AC})$ ,  $I_{PEAK-MAX} = 1V / R_{SENSE} (V_{IN} = 85V_{AC})$ . This proprietary compensation ensures a constant output power limit for wide AC input voltage from 90VAC to 264VAC.

(6) Protection section

The IC takes on more protection functions such as OLP, OVP and OTP etc. In case of those failure modes for continual blanking time, the driver is shut down. At the same time, IC enters auto-restart,  $V_{CC}$  power on and driver is reset after  $V_{CC}$  power on again.

OLP

After soft-start phase end, IC will shutdown driver if over load state occurs for continual  $T_{D-OLP}$ . OLP function will not inactive during soft-start phase. OLP case as followed Fig. 6. The test circuit as followed Fig.8.  $T_{D-OLP} = 5.53 \times T_{SS}$ .

OVP

There are two kinds of OVP circuits, the first OVP function are enabled only when  $V_{SS} < V_{SS(DEACT)}$  &  $V_{FB} > V_{FB(OLP)}$  during soft-start phase. During above condition, driver will be shutdown if over voltage state occurs ( $V_{CC} > V_{OV1}$ ) for continual a blanking time. The first OVP function will not inactive after soft-start phase. The second OVP will shutdown the switching of the power MOSFET whenever  $V_{CC} > V_{OV2}$ . The first OVP case as followed Fig.7. The test circuit as followed Fig. 9.

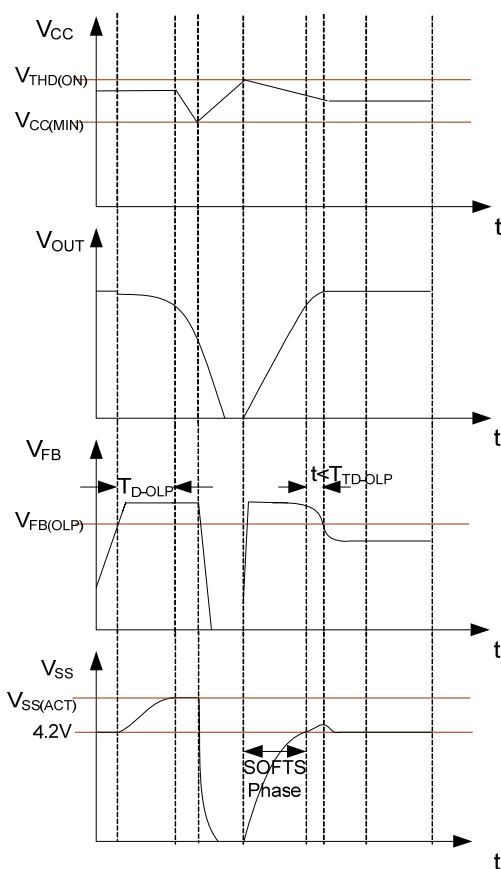


Fig.6 OLP case

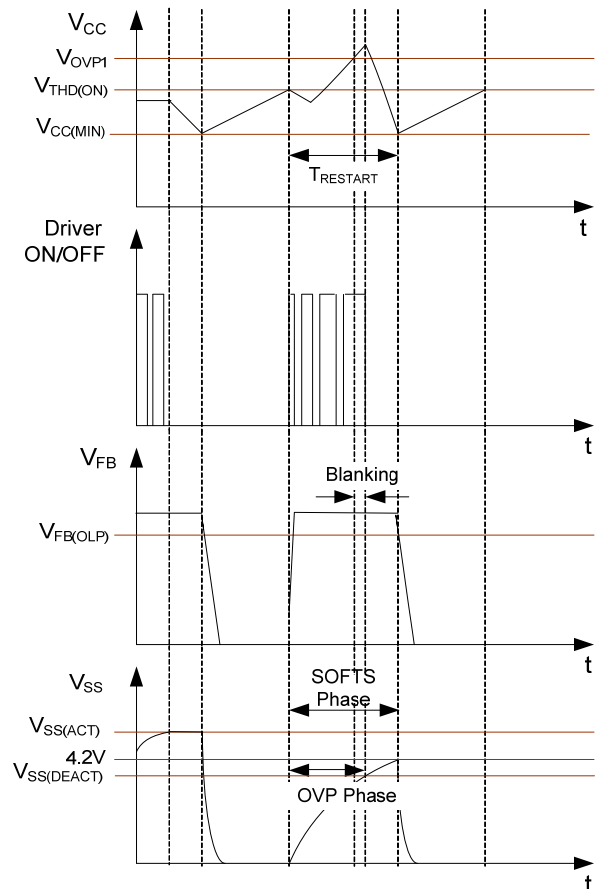


Fig.7 OVP case



■ FUNCTIONAL DESCRIPTION(Cont.)

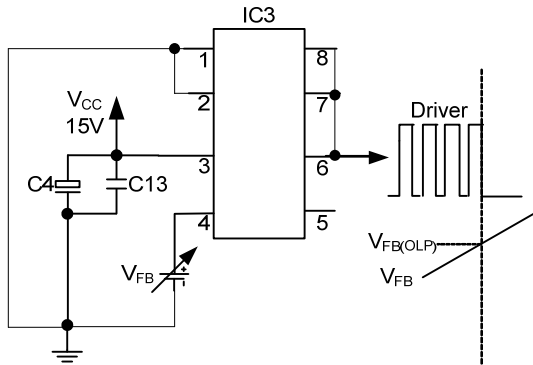


Fig.8 OLP test circuit

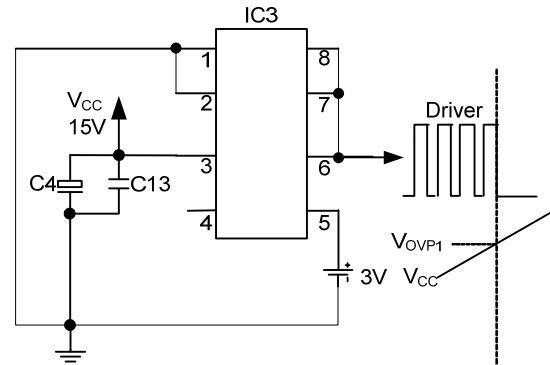


Fig.9 OVP test circuit

**OTP**

OTP will shut down driver when junction temperature  $T_J > T_{(THR)}$  for continual a blanking time.

**(7) Driver Output Section**

The driver-stage drives the gate of the MOSFET and is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when reaching the MOSFET threshold. This is achieved by a slope control of the rising edge at the driver's output. The output driver is clamped by an internal 15V Zener diode in order to protect power MOSFET transistors against undesirable gate over voltage.

**(8) Inside power switch MOS transistor**

Specific power MOS transistor parameter is as "POWER MOS TRANSISTOR SECTION" in electrical characteristics table.

## ■ TYPICAL APPLICATION CIRCUIT

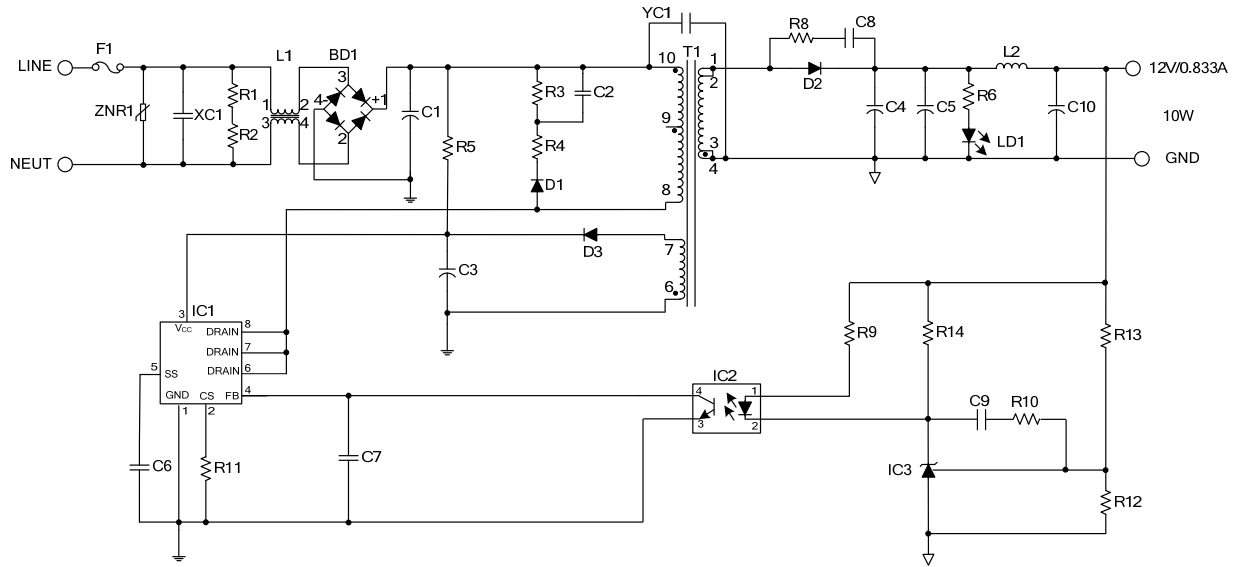
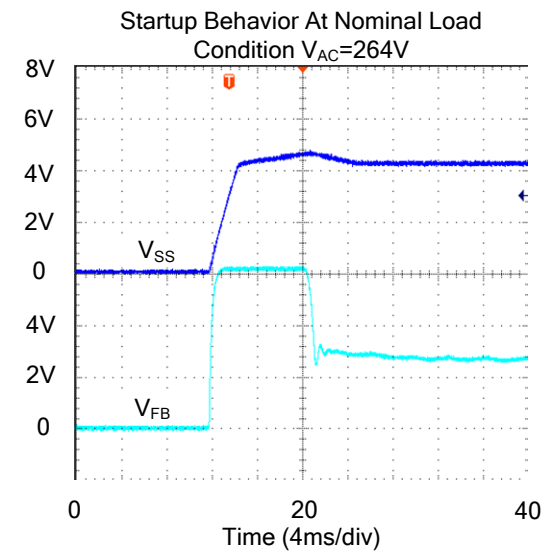
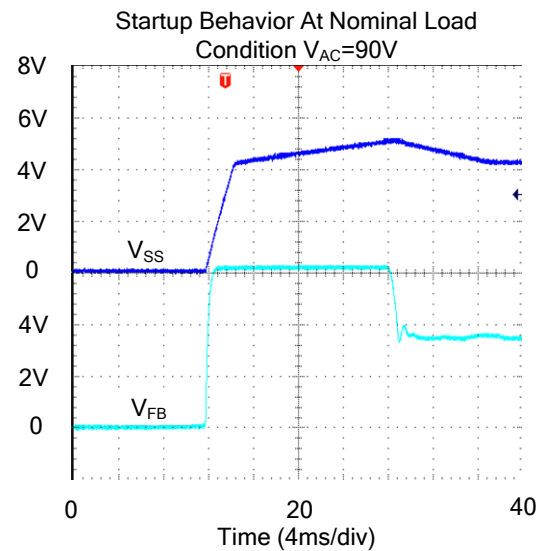
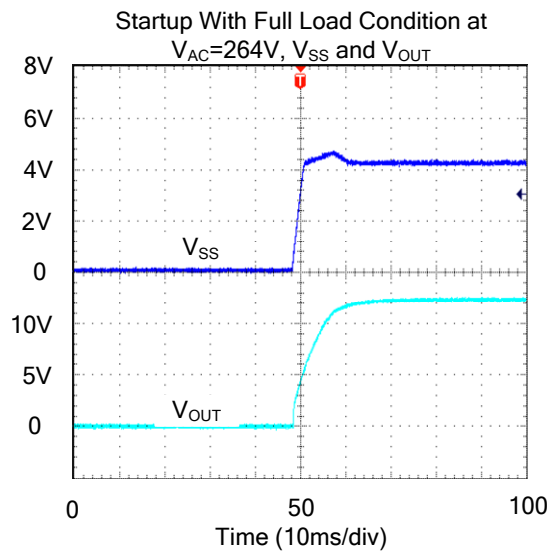
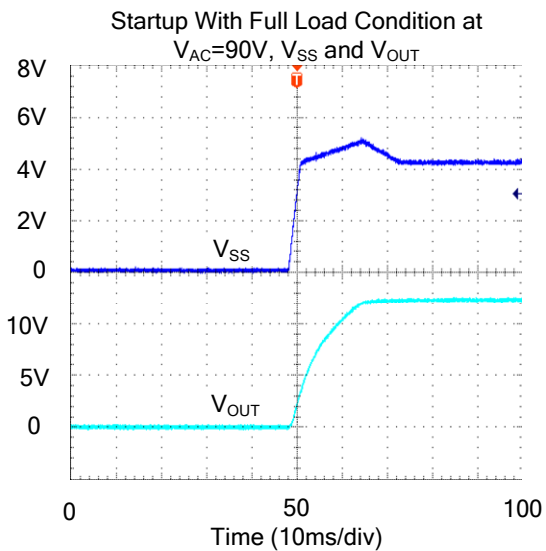
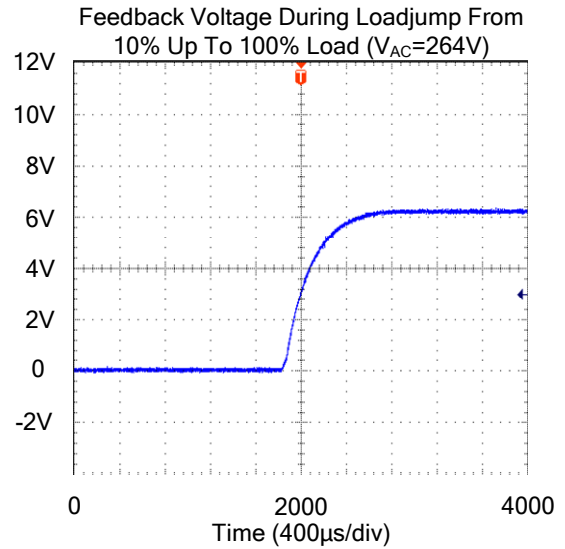
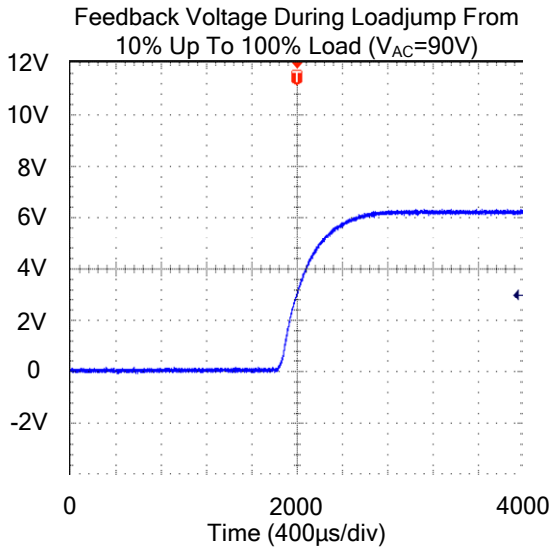


Fig.10 UTC **UPS1602** Typical Application Circuit

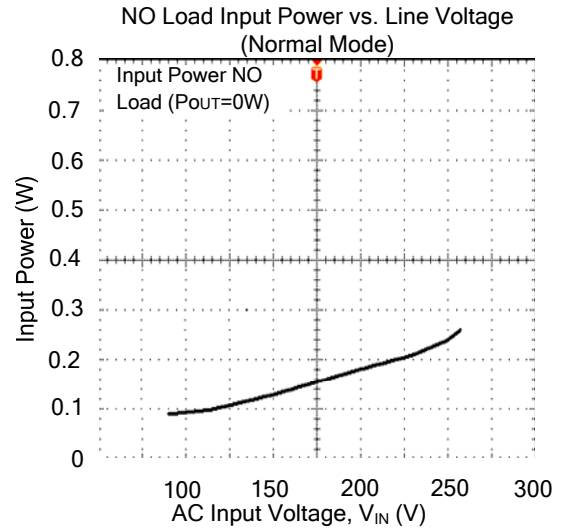
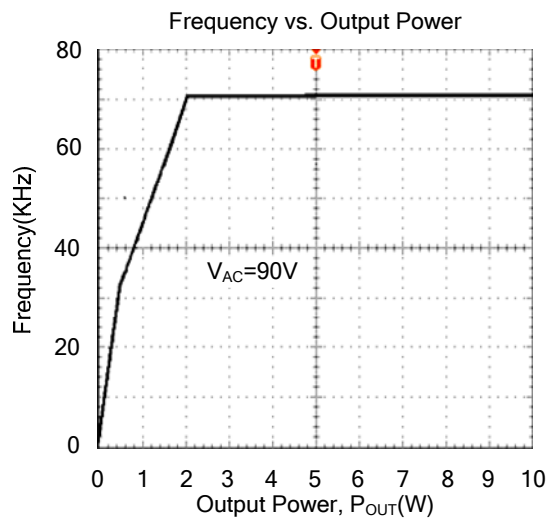
**Table1. Components reference description for UPS1602 application circuit**

DESIGNATOR	PART TYPE	DESIGNATOR	PART TYPE	DESIGNATOR	PART TYPE
C1	22 $\mu$ F	R4	100	D3	RS1D
C2	0.001 $\mu$ F	R5	1M $\Omega$	IC1	<b>UPS1602</b>
C3	22 $\mu$ F	R6	10K	IC2	PC-817
C4	330 $\mu$ F	R8	15 $\Omega$	IC3	TL431
C5	330 $\mu$ F	R9	560 $\Omega$	YC1	222
C6	0.1 $\mu$ F	R10	1K $\Omega$	T1	EE22
C7	0.01 $\mu$ F	R11	1.5 $\Omega$	L1	UU9.8
C8	0.001 $\mu$ F	R12	3.9K $\Omega$	L2	2uH
C9	0.1 $\mu$ F	R13	15K $\Omega$	LD1	LED
C10	220 $\mu$ F	R14	1.8K $\Omega$	F1	1A/250V
R1	2.2M $\Omega$	D1	FR107	ZNR1	7D471K
R2	2.2M $\Omega$	D2	SB3100	BD1	DI106
R3	68K $\Omega$			XC1	154

## ■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS(Cont.)



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