



# BUK9Y7R6-40E

N-channel 40 V, 7.6 mΩ logic level MOSFET in LFPAK56

20 February 2013

Product data sheet

## 1. General description

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with  $V_{GS(th)}$  rating of greater than 0.5 V at 175 °C

## 3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 5\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	79	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	-	95	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 20\text{ A}; T_j = 25\text{ °C}; \text{Fig. 11}$	-	6.4	7.6	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 5\text{ V}; I_D = 20\text{ A}; V_{DS} = 32\text{ V}; T_j = 25\text{ °C}; \text{Fig. 13}; \text{Fig. 14}$	-	5.5	-	nC

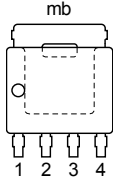
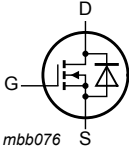


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## 5. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LPAK; Power-SO8 (SOT669)</b></p>	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BUK9Y7R6-40E	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

## 7. Marking

**Table 4. Marking codes**

Type number	Marking code
BUK9Y7R6-40E	97E640

## 8. Limiting values

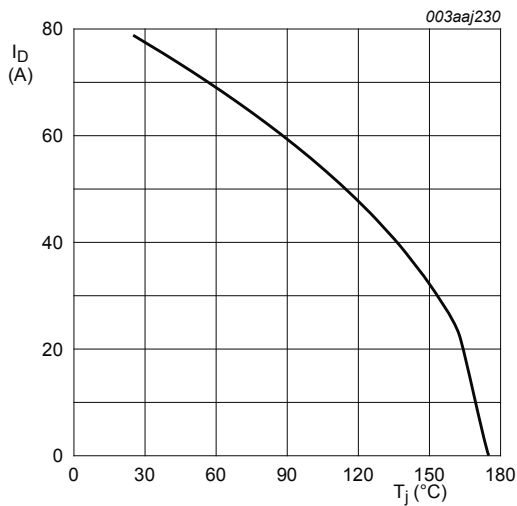
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	40	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	40	V
$V_{GS}$	gate-source voltage	$T_j \leq 175\text{ °C}$ ; DC	-10	10	V
		$T_j \leq 175\text{ °C}$ ; Pulsed	[1][2]	-15	15
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 1	-	79	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 1	-	56	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; Fig. 4	-	315	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 2	-	95	W

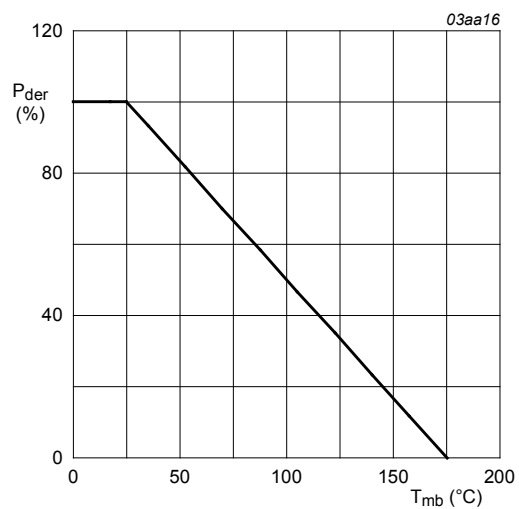
Symbol	Parameter	Conditions	Min	Max	Unit
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	79	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	315	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 79 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 5 V; T <sub>j(init)</sub> = 25 °C; unclamped; <a href="#">Fig. 3</a>	[3][4]	-	43 mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T<sub>j</sub> and or V<sub>GS</sub>
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.



**Fig. 1. Continuous drain current as a function of mounting base temperature**

$$V_{GS} \geq 5V$$



**Fig. 2. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

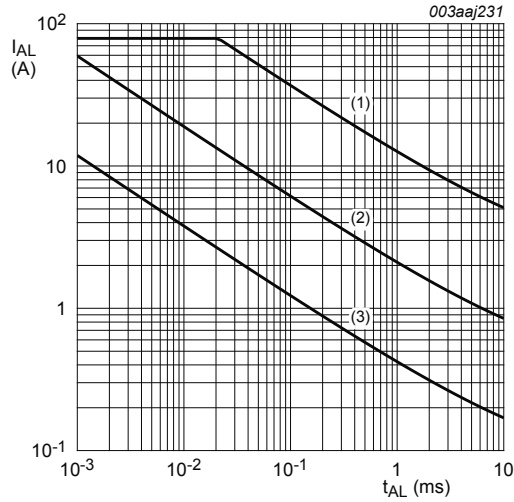


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j (int)} = 25^{\circ}C$ ; (2)  $T_{j (int)} = 150^{\circ}C$ ; (3) Repetitive Avalanche

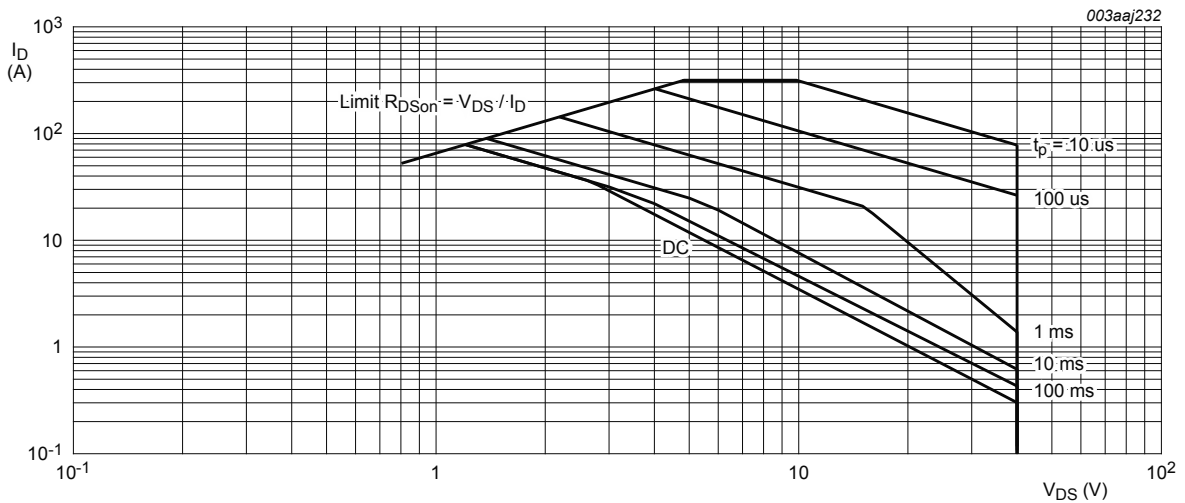


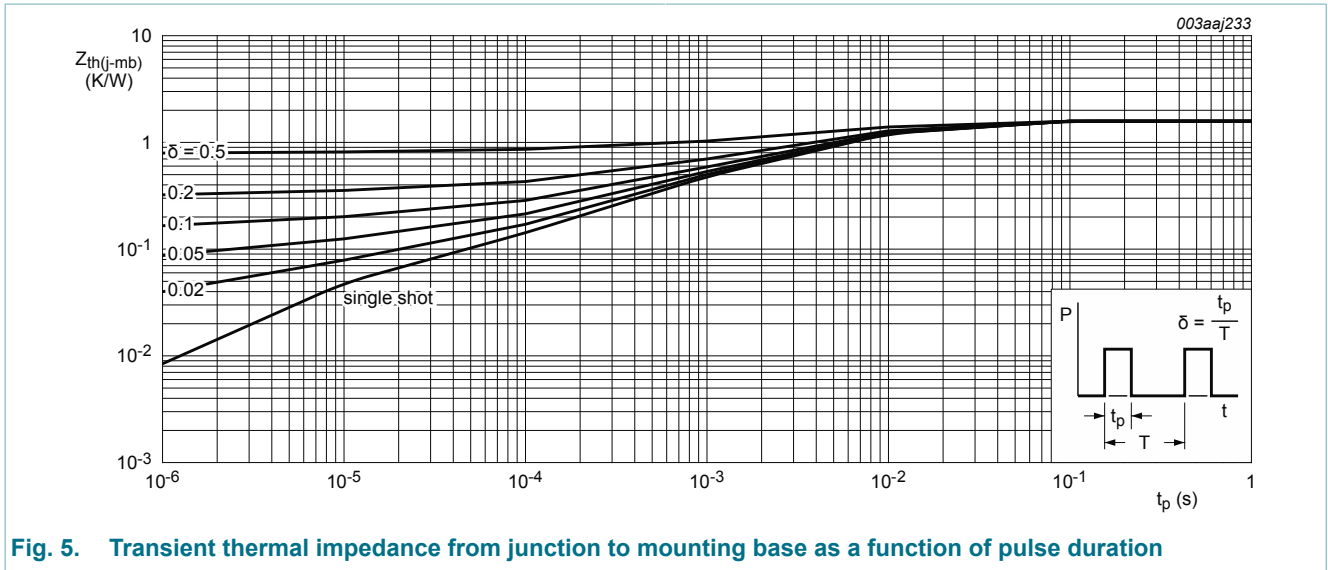
Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	1.58	K/W



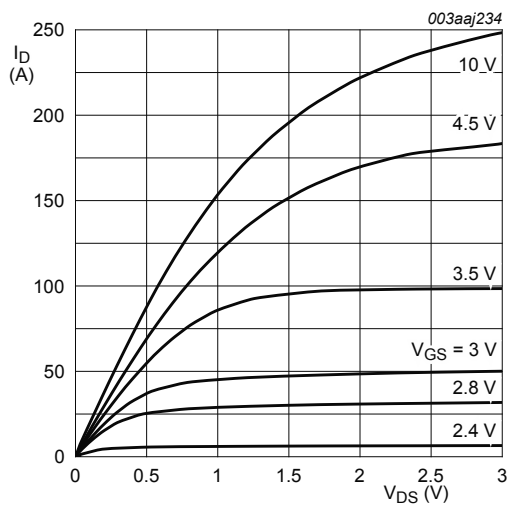
**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 10. Characteristics

**Table 7. Characteristics**

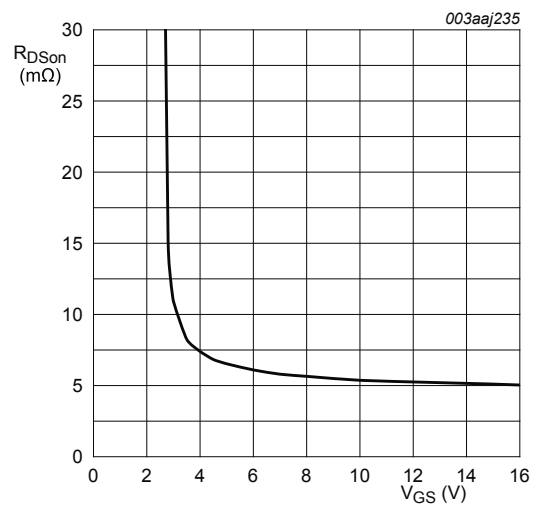
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 9; Fig. 10</a>	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 9</a>	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 9</a>	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.04	1	$\mu A$
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5 V; I_D = 20 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	6.4	7.6	mΩ
		$V_{GS} = 10 V; I_D = 20 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	5.3	6	mΩ
		$V_{GS} = 5 V; I_D = 20 A; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 11; Fig. 12</a>	-	-	15.28	mΩ
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 20 A; V_{DS} = 32 V; V_{GS} = 5 V;$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 13; Fig. 14</a>	-	16.4	-	nC
$Q_{GS}$	gate-source charge		-	5.1	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{GD}$	gate-drain charge		-	5.5	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$	-	1807	2403	pF
$C_{oss}$	output capacitance	$T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	-	260	312	pF
$C_{rss}$	reverse transfer capacitance		-	126	173	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.5\text{ } \Omega; V_{GS} = 5\text{ V};$	-	11.3	-	ns
$t_r$	rise time	$R_{G(ext)} = 5\text{ } \Omega; T_j = 25\text{ }^\circ\text{C}$	-	20.9	-	ns
$t_{d(off)}$	turn-off delay time		-	22.7	-	ns
$t_f$	fall time		-	16.6	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 20\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	-	0.84	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	17	-	ns
$Q_r$	recovered charge	$V_{DS} = 25\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	8.1	-	nC



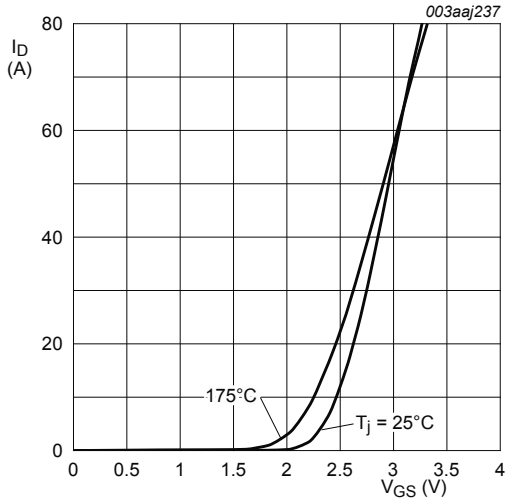
$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ } \mu\text{s}$

**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**



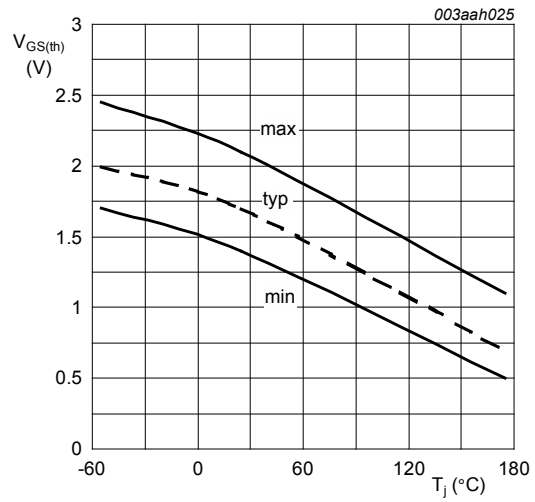
**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25\text{ }^\circ\text{C}; I_D = 20\text{ A}$



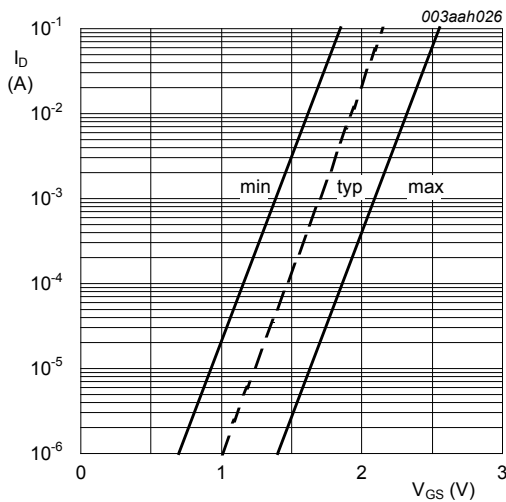
**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$V_{DS} = 10V$



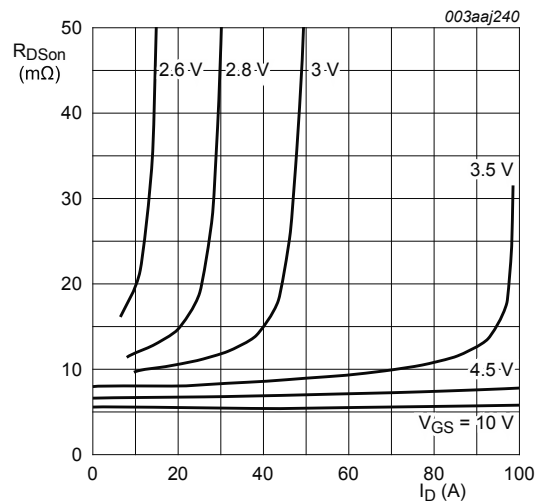
**Fig. 9. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$



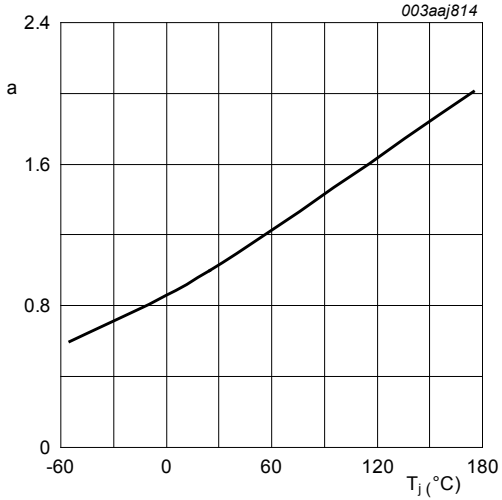
**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25^\circ\text{C}; V_{DS} = 5V$



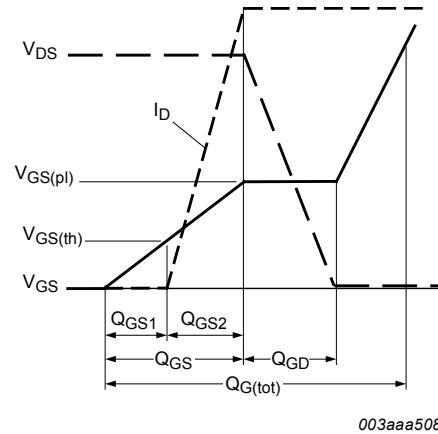
$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$

**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**

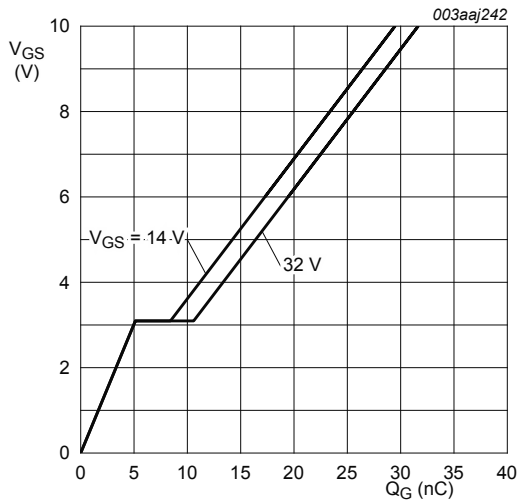


**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ C)}}$$

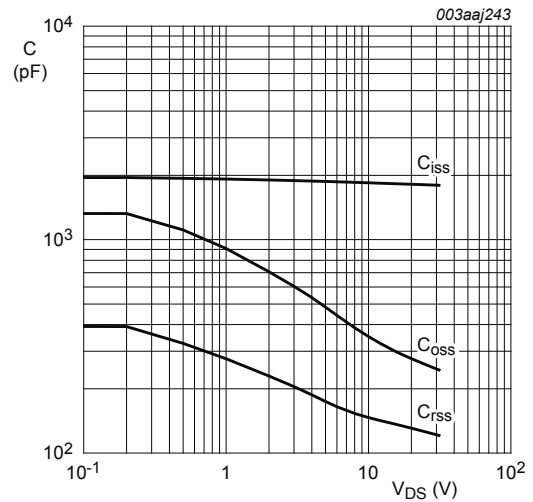


**Fig. 13. Gate charge waveform definitions**



**Fig. 14. Gate-source voltage as a function of gate charge; typical values**

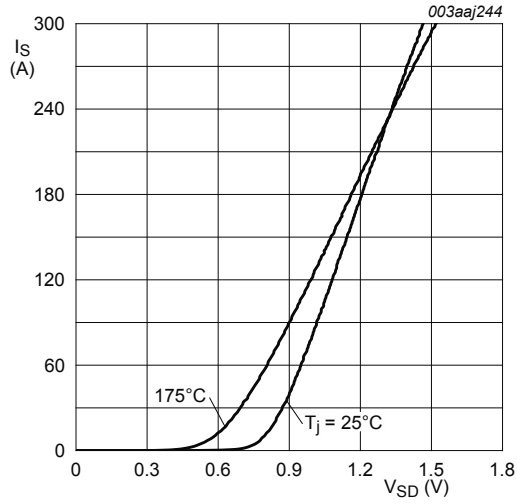
$$T_j = 25^\circ C; I_D = 20 A$$



**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$$V_{GS} = 0 V; f = 1 MHz$$





**Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

$$V_{GS} = 0V$$

11. Package outline

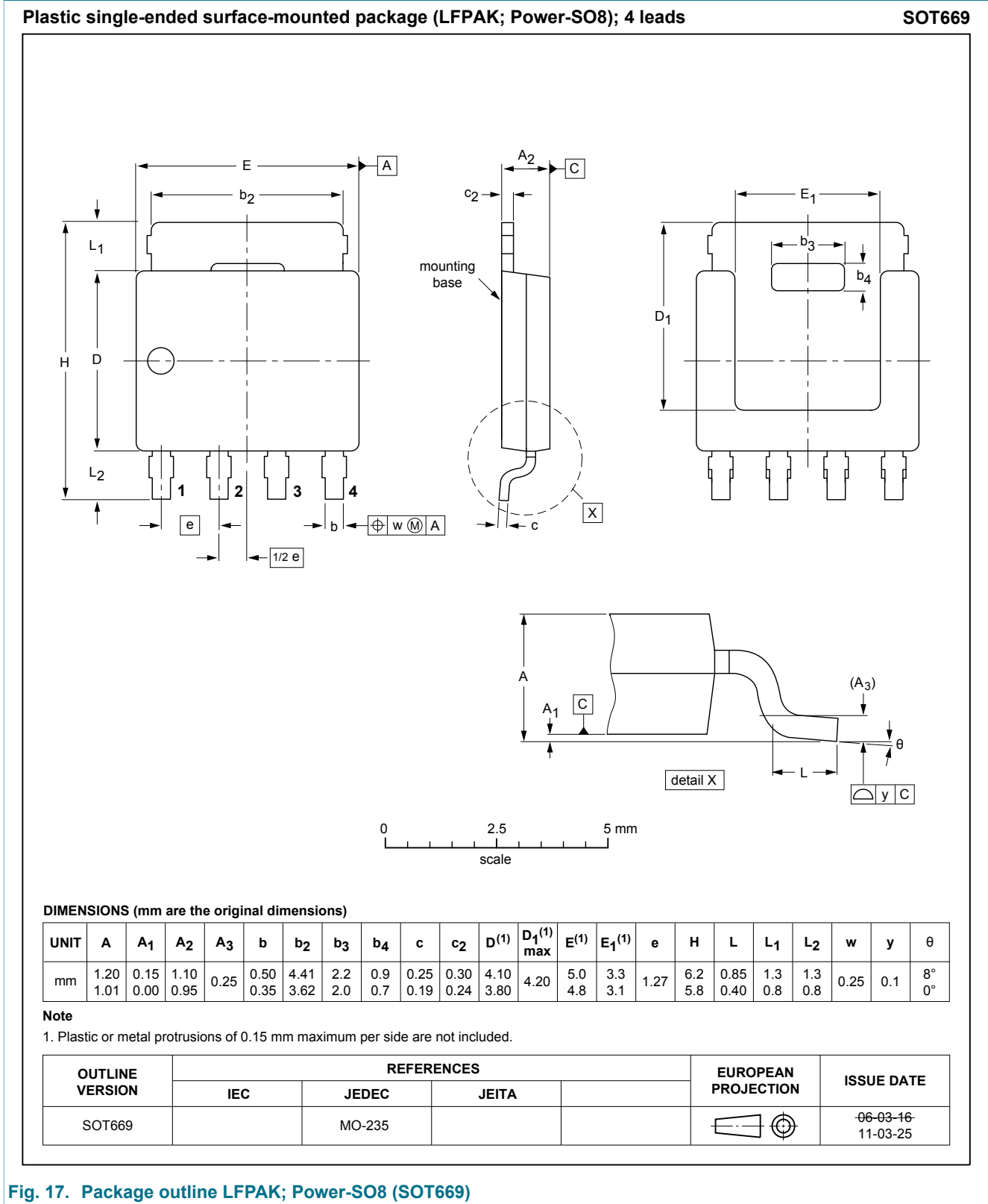


Fig. 17. Package outline LPAK; Power-SO8 (SOT669)

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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