HD74ALVCHR162269A

12-bit to 24-bit Registered Bus Exchanger with 3-state Outputs

HITACHI

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Description

The HD74ALVCHR162269A is a 12-bit to 24-bit registered bus exchanger, which is intended for applications where two separate ports must be multiplexed onto, or de-multiplexed from, a single port. It is particularly suitable as an interface between synchronous DRAMs and high speed microprocessors. The HD74ALVCHR162269A is designed specifically for low voltage (from 2.5 V to 3.3 V) V_{CC} operation.

Data is stored in the internal B-port registers on the low to high transition of the CLK input, provided that the appropriate $\overline{\text{CLKENA}}$ inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B-port. For data transfer in the B to A direction, a single storage register is provided. The $\overline{\text{SEL}}$ line selects 1B or 2B data for the A outputs.

The register on the A output permits the fastest possible data transfer, thus extending the period that the data will be valid on the bus. The control pins are registered so that all transactions are synchronous with the clock. Data flows is controlled by the active low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB1}}$, $\overline{\text{OEB2}}$).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

All outputs, which are designed to sink up to 12 mA, include 26 Ω resistors to reduce overshoot and undershoot.

Features

- All outputs have equivalent 26 Ω series resistors, so no external resistors are required.
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors.

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Function Table

Inputs			Outputs	
CLK	**$\overline{OEA}$**	**$\overline{OEB}$**	**A**	**1B, 2B**
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z

Output-enable table

Inputs				Outputs	
$\overline{CLKENA1}$	**$\overline{CLKENA2}$**	**CLK**	**A**	**1B**	**2B**
L	H	↑	L	L	$2B_0$ *1
L	H	↑	H	H	$2B_0$ *1
L	L	↑	L	L	L
L	L	↑	H	H	H
H	L	↑	L	$1B_0$ *1	L
H	L	↑	H	$1B_0$ *1	H
H	H	X	X	$1B_0$ *1	$2B_0$ *1

A-to-B storage table ($\overline{OEB}$ = L)

Inputs				
CLK	**$\overline{SEL}$**	**1B**	**2B**	**Output A**
X	H	X	X	A_0 *1
X	L	X	X	A_0 *1
↑	H	L	X	L
↑	H	H	X	H
↑	L	X	L	L

B-to-A storage ($\overline{OEA}$ = L)

H : High level

L : Low level

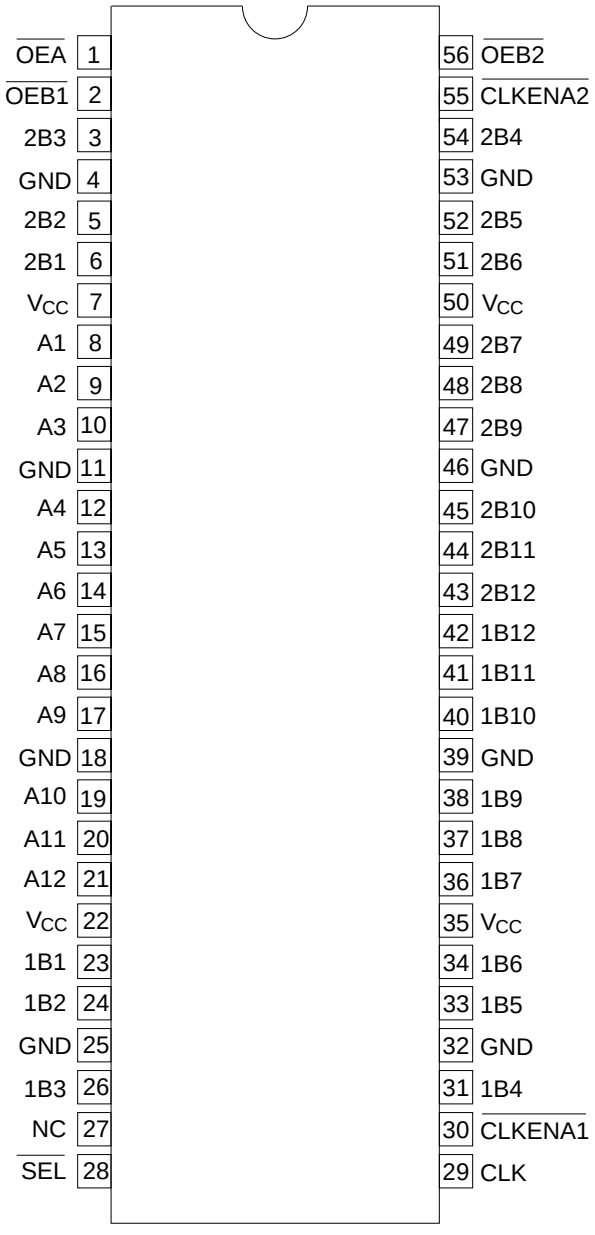
X : Immaterial

Z : High impedance

↑ : Low to high transition

Note: 1. Output level before the indicated steady state input conditions were established.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	–0.5 to 4.6	V	
Input voltage range [*1, 2]	V_I	–0.5 to 4.6	V	Except I/O ports
		–0.5 to V_{CC} +0.5		I/O ports
Output voltage range [*1, 2]	V_O	–0.5 to V_{CC} +0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±50	mA	V_O = 0 to V_{CC}
Continuous current through	I_{CC} / I_{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air) [*3]	P_T	1	W	TSSOP
Storage temperature range	Tstg	–65 to 150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

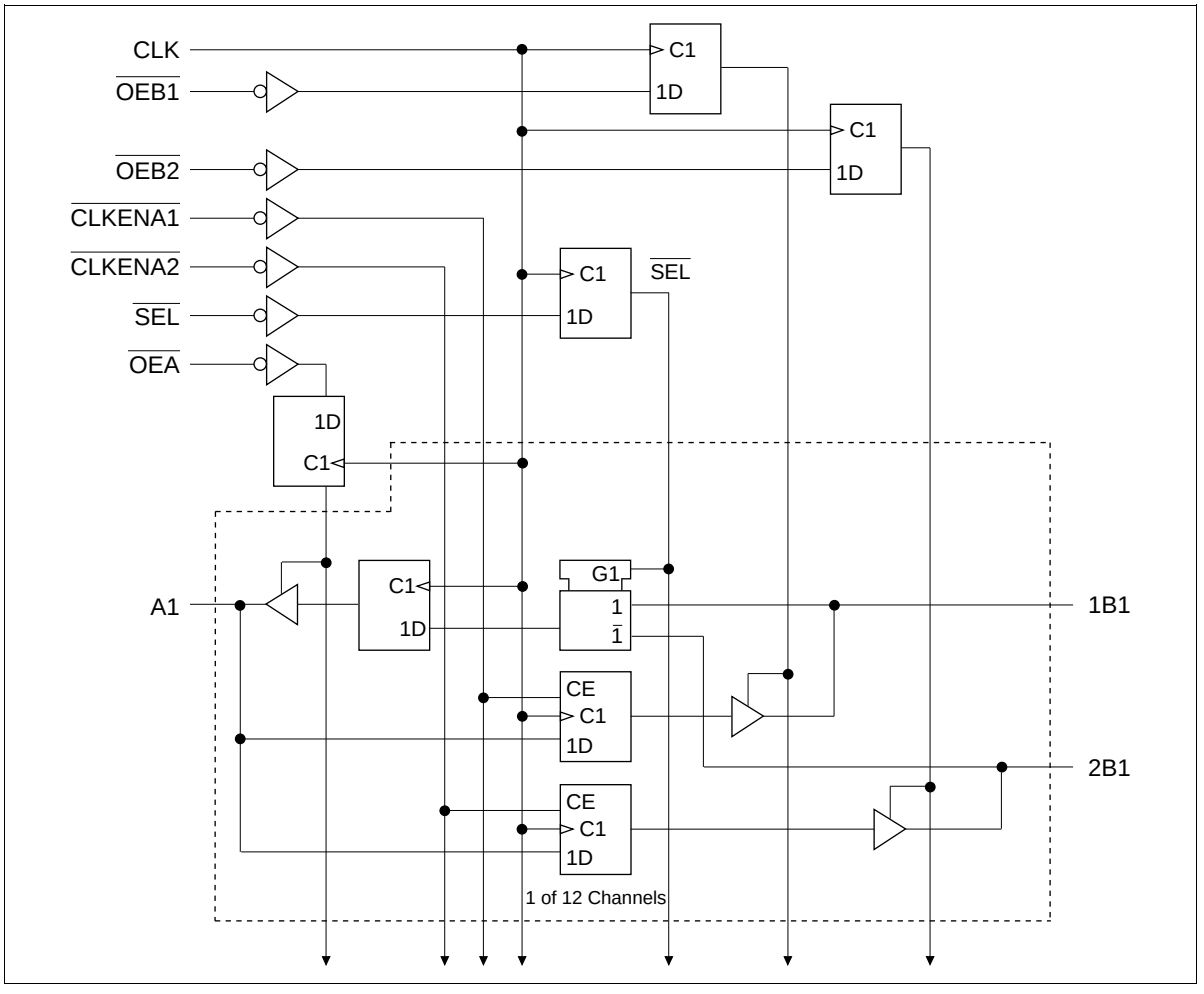
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum power dissipation is calculated using a junction temperature of 150°C and board trace length of 750 mils.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{CC}	2.3	3.6	V	
Input voltage	V_I	0	V_{CC}	V	
Output voltage	V_O	0	V_{CC}	V	
High-level output current	I_{OH}	—	–6	mA	V_{CC} = 2.3 V
		—	–8		V_{CC} = 2.7 V
		—	–12		V_{CC} = 3.0 V
Low-level output current	I_{OL}	—	6	mA	V_{CC} = 2.3 V
		—	8		V_{CC} = 2.7 V
		—	12		V_{CC} = 3.0 V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating free-air temperature	Ta	–40	85	°C	

Note: Unused or floating control pins must be held high or low.

Logic Diagram



Electrical Characteristics (Ta = –40 to 85°C)

Item	Symbol	V_{CC} (V)	Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.3 to 2.7	1.7	—	V	
		2.7 to 3.6	2.0	—		
	V_{IL}	2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
Output voltage	V_{OH}	Min to Max	V_{CC}–0.2	—	V	I_{OH} = –100 µA
		2.3	1.9	—		I_{OH} = –4 mA, V_{IH} = 1.7 V
		2.3	1.7	—		I_{OH} = –6 mA, V_{IH} = 1.7 V
		2.7	2.2	—		I_{OH} = –4 mA, V_{IH} = 2.0 V
		2.7	2.0	—		I_{OH} = –8 mA, V_{IH} = 2.0 V
		3.0	2.4	—		I_{OH} = –6 mA, V_{IH} = 2.0 V
		3.0	2.0	—		I_{OH} = –12 mA, V_{IH} = 2.0 V
	V_{OL}	Min to Max	—	0.2		I_{OL} = 100 µA
		2.3	—	0.4		I_{OL} = 4 mA, V_{IL} = 0.7 V
		2.3	—	0.55		I_{OL} = 6 mA, V_{IL} = 0.7 V
		2.7	—	0.4		I_{OL} = 4 mA, V_{IL} = 0.8 V
		2.7	—	0.6		I_{OL} = 8 mA, V_{IL} = 0.8 V
		3.0	—	0.55		I_{OL} = 6 mA, V_{IL} = 0.8 V
		3.0	—	0.8		I_{OL} = 12 mA, V_{IL} = 0.8 V
Input current	I_{IN}	3.6	—	±5.0	µA	V_{IN} = V_{CC} or GND
	$I_{IN (hold)}$	2.3	45	—		V_{IN} = 0.7 V
		2.3	–45	—		V_{IN} = 1.7 V
		3.0	75	—		V_{IN} = 0.8 V
		3.0	–75	—		V_{IN} = 2.0 V
		3.6	—	±500		V_{IN} = 0 to 3.6 V
Off state output current [*1]	I_{OZ}	3.6	—	±10	µA	V_{OUT} = V_{CC} or GND
Quiescent supply current	I_{CC}	3.6	—	40	µA	V_{IN} = V_{CC} or GND
	ΔI_{CC}	3.0 to 3.6	—	750		One input at (V_{CC}–0.6) V, other inputs at V_{CC} or GND

Notes: 1. For I/O ports, the parameter I_{OZ} includes the input leakage current.

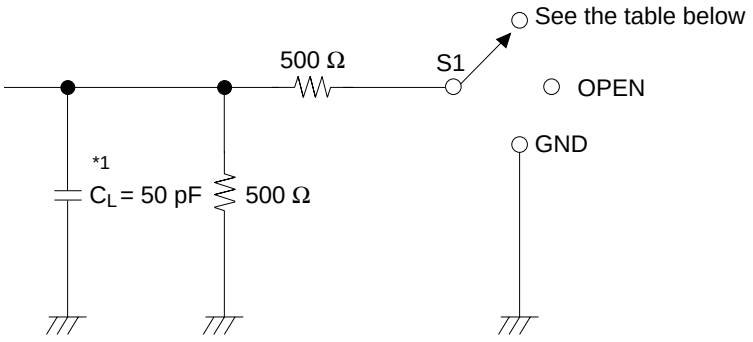
Switching Characteristics (Ta = –40 to 85°C)

Item	Symbol	V_{CC} (V)	Min	Typ	Max	Unit	From (Input)	To (Output)
Maximum clock frequency	f_{max}	2.5±0.2	—	—	—	MHz		
		2.7	—	—	—			
		3.3±0.3	135	—	—			
Propagation delay time	t_{PLH}	2.5±0.2	—	—	—	ns	CLK	B
	t_{PHL}	2.7	—	—	—			
		3.3±0.3	2.0	—	5.0			
		2.5±0.2	—	—	—		CLK	A
		2.7	—	—	—			
		3.3±0.3	1.0	—	4.0			
Output enable time	t_{ZH}	2.5±0.2	—	—	—	ns	CLK	B
	t_{ZL}	2.7	—	—	—			
		3.3±0.3	2.0	—	5.0			
		2.5±0.2	—	—	—		CLK	A
		2.7	—	—	—			
		3.3±0.3	1.0	—	4.5			
Output disable time	t_{HZ}	2.5±0.2	—	—	—	ns	CLK	B
	t_{LZ}	2.7	—	—	—			
		3.3±0.3	2.0	—	5.0			
		2.5±0.2	—	—	—		CLK	A
		2.7	—	—	—			
		3.3±0.3	1.0	—	4.5			
Input capacitance	C_{IN}	3.3	—	3.5	—	pF		
Output capacitance	C_O	3.3	—	9.0	—	pF		

Switching Characteristics (Ta = –40 to 85°C) (cont)

Item	Symbol	V_{cc} (V)	Min	Typ	Max	Unit	FROM (Input)
Setup time	t_{su}	2.5±0.2	—	—	—	ns	A data before CLK↑
		2.7	—	—	—		"H" or "L"
		3.3±0.3	1.0	—	—		
		2.5±0.2	—	—	—		B data before CLK↑
		2.7	—	—	—		"H" or "L"
		3.3±0.3	1.0	—	—		
		2.5±0.2	—	—	—		$\overline{SEL}$ before CLK↑
		2.7	—	—	—		"H" or "L"
		3.3±0.3	1.0	—	—		
		2.5±0.2	—	—	—		$\overline{CLKENA1}$ or
		2.7	—	—	—		$\overline{CLKENA2}$ before CLK↑
		3.3±0.3	1.0	—	—		"H" or "L"
		2.5±0.2	—	—	—		$\overline{OE}$ before CLK↑
		2.7	—	—	—		"H" or "L"
		3.3±0.3	1.0	—	—		
Hold time	t_h	2.5±0.2	—	—	—	ns	A data after CLK↑
		2.7	—	—	—		"H" or "L"
		3.3±0.3	0.5	—	—		
		2.5±0.2	—	—	—		B data after CLK↑
		2.7	—	—	—		"H" or "L"
		3.3±0.3	0.5	—	—		
		2.5±0.2	—	—	—		$\overline{SEL}$ aftrer CLK↑
		2.7	—	—	—		"H" or "L"
		3.3±0.3	0.5	—	—		
		2.5±0.2	—	—	—		$\overline{CLKENA1}$ or
		2.7	—	—	—		$\overline{CLKENA2}$ after CLK↑
		3.3±0.3	0.5	—	—		"H" or "L"
		2.5±0.2	—	—	—		$\overline{OE}$ after CLK↑
		2.7	—	—	—		"H" or "L"
		3.3±0.3	0.5	—	—		
Pulse width	t_w	2.5±0.2	—	—	—	ns	CLK "H" or "L"
		2.7	—	—	—		
		3.3±0.3	2.0	—	—		

Test Circuit

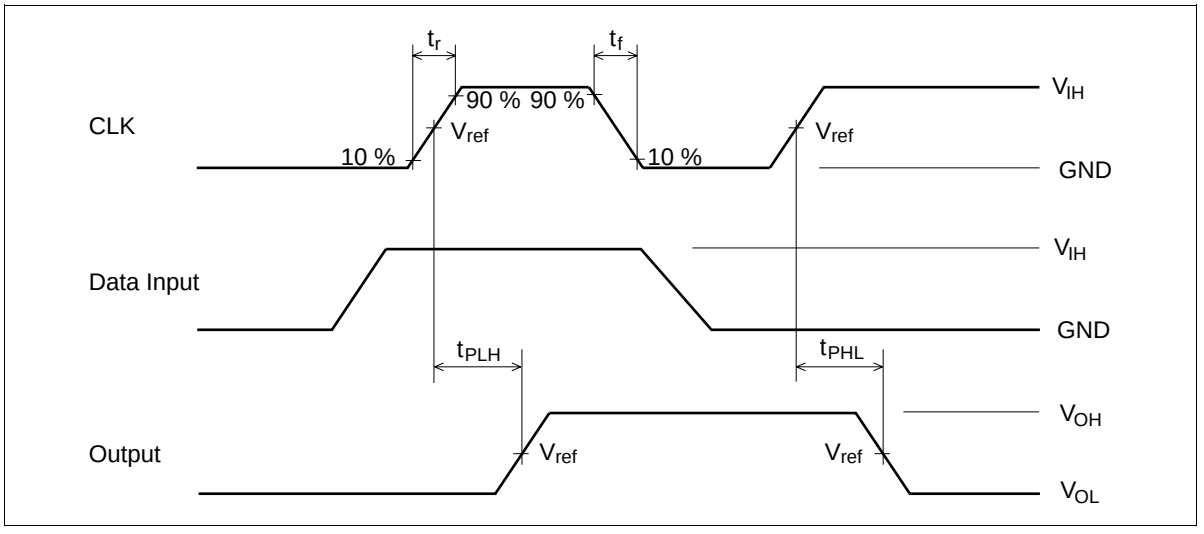


Load Circuit for Outputs

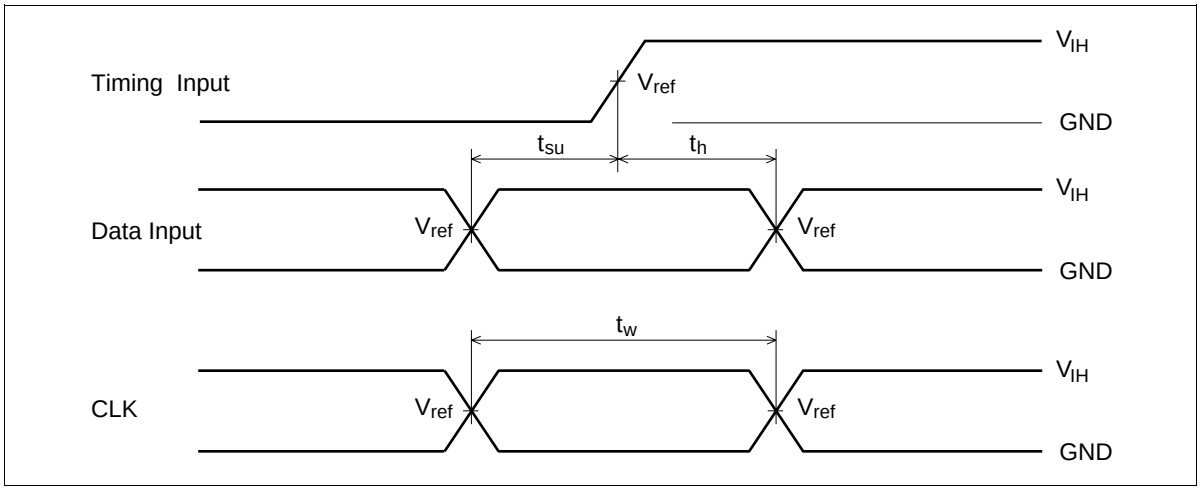
Symbol	Vcc=2.5±0.2V	Vcc=2.7V, 3.3±0.15V
t_{PLH} / t_{PHL}	OPEN	OPEN
t_{su} / t_h / t_w		
t_{ZH} / t_{HZ}	GND	GND
t_{ZL} / t_{LZ}	4.6 V	6.0 V

Note: 1. C_L includes probe and jig capacitance.

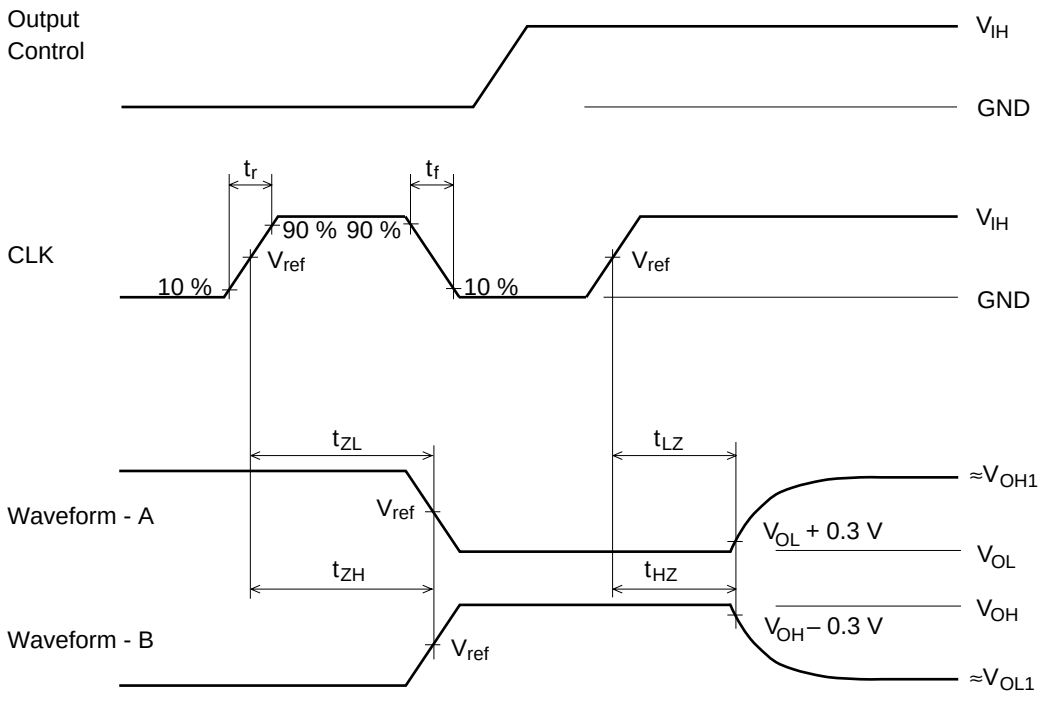
Waveforms – 1



Waveforms – 2



Waveforms – 3

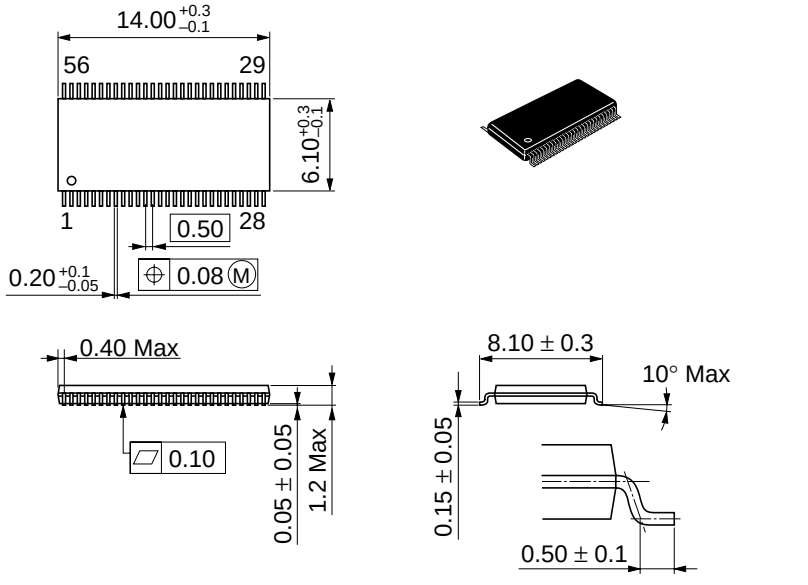


TEST	Vcc=2.5±0.2V	Vcc=2.7V, 3.3±0.15V
V_{IH}	2.3 V	2.7 V
V_{ref}	1.2 V	1.5 V
V_{OH1}	2.3 V	3.0 V
V_{OL1}	GND	GND

Note: 1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_o = 50Ω, $t_r \leq 2.5$ns, $t_f \leq 2.5$ns.
2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
4. The outputs are measured one at a time with one transition per measurement.

Package Dimensions

Unit : mm



Hitachi code	TTP-56D
EIAJ code	—
JEDEC code	—

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