4.5V to 28V Input, 3A Output, Synchronous Step Down SWIFT™ Converter

Check for Samples: TPS54335 , TPS54336

FEATURES

- **Two 128mΩ/84mΩ MOSFETs for 3A Continuous Output Current**
- **TPS54335: Internal 2ms Slow Start, 50kHz–1.5MHz Adjustable**
- **TPS54336: Adjustable Slow Start, Fixed 340kHz**
- **Low 2uA Shutdown Quiescent Current**
- **0.8V Internal Voltage Reference with ±1.5% Accuracy Over Temperature**
- **Fixed-Frequency Current Mode Control**
- **Pulse Skipping Boosts Efficiency at Light Loads**
- **Overcurrent Protection for Both MOSFETs with Hiccup Mode for Severe Fault Conditions**
- **Thermal and Overvoltage Transient Protection**
- **Available in Easy-to-Use 8-Pin SOIC PowerPAD™**
- **Monotonic Start-Up into Pre-biased Outputs**

APPLICATIONS

- **Consumer Applications such as DTV, Set Top Boxes, LCD displays, CPE Equipment**
- **Battery Chargers**
- **Industrial and Car Audio Power Supplies**
- **5V,12V and 24V Distributed Power Systems**

DESCRIPTION

The TPS54335/6 is a 28V, 3A, low Iq, current mode, synchronous monolithic buck converter with integrated MOSFETs.

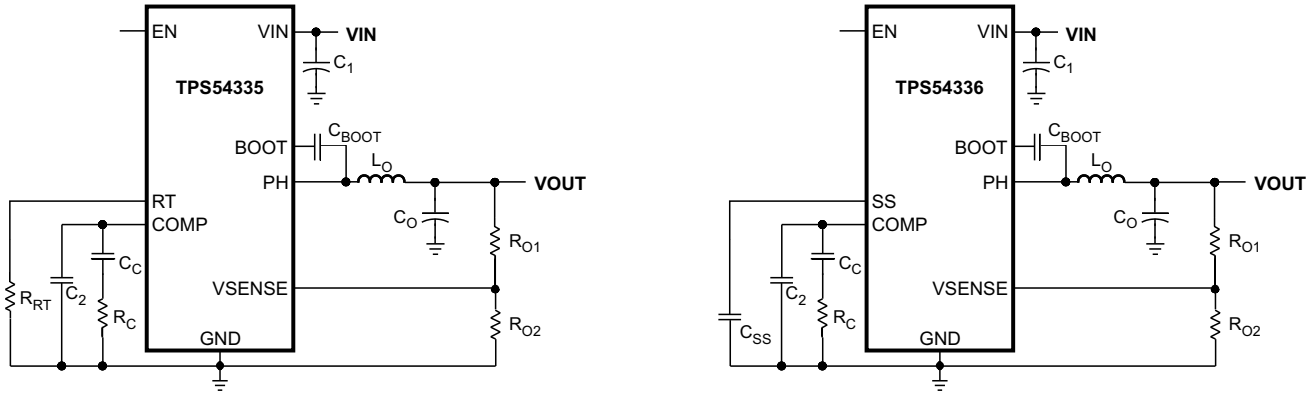
The TPS54335/6 enables small designs by integrating the MOSFETs and implementing current mode control to reduce external component count.

Efficiency is maximized through the integrated 128mΩ/84mΩ MOSFETs, low quiescent supply current and pulse skipping at light loads. Using the enable pin, shutdown supply current is reduced to 2 µA by entering a shutdown mode.

The TPS54335/6 provides accurate regulation for a variety of loads with an accurate 1.5% voltage reference over temperature.

Cycle by cycle current limiting on the high-side FET protects the TPS54335/6 in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. There is also a low-side sinking current limit which turns off the low-side MOSFET to prevent excessive reverse current. Hiccup protection will be triggered if the overcurrent condition has persisted for longer than the preset time. Thermal hiccup protection disables the part when die temperature exceeds thermal shutdown temperature and enables the part again after the built-in thermal hiccup time.

SIMPLIFIED SCHEMATICS



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1) (2)

T_J	PACKAGE	PART NUMBER
–40°C to +150°C	8-Pin SOIC PowerPAD™	TPS54335DDA
		TPS54336DDA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) The DDA package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54335DDAR). See applications section of data sheet for layout information.

ABSOLUTE MAXIMUM RATINGS(1) (2)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	30	V
	EN	–0.3	6	V
	BOOT	-0.3	(PH+7.5)	V
	VSENSE	–0.3	3	V
	COMP	–0.3	3	V
	RT	–0.3	3	V
	SS	–0.3	3	V
Output voltage	BOOT-PH	0	7.5	V
	PH	–1	30	V
	PH 10ns Transient	–3.5	30	V
Vdiff (GND to exposed Thermal Pad)		–0.2	0.2	V
Source current	EN	100	100	µA
	RT	100	100	µA
	PH		Current Limit	A
Sink current	PH		Current Limit	A
	COMP	200	200	µA
Electrostatic discharge (HBM) QSS 009-105 (JESD22-A114A)		2	2	kV
Electrostatic discharge (CDM) QSS 009-147 (JESD22-C101B.01)		500	500	V
Operating junction temperature		–40	150	°C
Storage temperature		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS54335/6 DDA (8 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	42.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	50.9	
θ_{JB}	Junction-to-board thermal resistance	31.8	
ψ_{JT}	Junction-to-top characterization parameter	8	
ψ_{JB}	Junction-to-board characterization parameter	13.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	7.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

The Electrical Ratings specified in this section will apply to all specifications in this document unless otherwise noted. These specifications will be interpreted as conditions that will not degrade the device's parametric or functional specifications for the life of the product containing it. T_J = –40°C to +150°C, VIN =4.5 TO 28V, (unless otherwise noted)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND UVLO (VIN PIN)					
Operating input voltage		4.5		28	V
Input UVLO threshold	Rising Vin		4	4.5	V
Input UVLO hysteresis			180	400	mV
VIN Shutdown supply current	EN = 0V		2	10	µA
VIN Operating – Non switching supply current	VSENSE = 810 mV		310	800	µA
ENABLE (EN PIN)					
Enable threshold	Rising		1.21	1.28	V
Enable threshold	Falling	1.1	1.17		V
Input current	EN= 1.1 V		1.15		µA
Hysteresis current	EN= 1.3 V		3.3		µA
VOLTAGE REFERENCE					
Reference	T_J =25°C	0.792	0.8	0.808	V
		0.788	0.8	0.812	
MOSFET					
High side switch resistance(1)	BOOT-PH= 3 V		160	280	mΩ
	BOOT-PH= 6 V		128	230	mΩ
Low Side Switch Resistance(1)	VIN = 12V		84	170	mΩ
ERROR AMPLIFIER					
Error amplifier transconductance (gm)	–2 µA < ICOMP < 2 µA V(COMP) = 1 V		1300		µmhos
Error amplifier dc gain(2)	VSENSE = 0.8 V	1000	3000		V/V
Error amplifier source/sink	V(COMP) = 1 V, 100 mV Overdrive		100		µA
Start switching peak current threshold			0.5		A
COMP to Iswitch gm			8		A/V
CURRENT LIMIT					
High side switch current limit threshold		4	4.9	6.5	A
Low side switch sourcing current limit		3.5	4.7	6.1	A
Low side switch sinking current limit			0		A
Hiccup wait time			512		Cycles
Hiccup time before re-start			16384		Cycles
THERMAL SHUTDOWN					
Thermal shutdown		160	175		°C
Thermal shutdown hysterisis			10		°C
Thermal shutdown hiccup time			32768		Cycles
PH (PH PIN)					
Minimum on time	Measured at 90% to 90% of VIN, I_{PH} = 2A		94	145	ns
Minimum off time	BOOT-PH ≥ 3V		0		%
BOOT (BOOT PIN)					
BOOT-PH UVLO			2.1	3	V

(1) Measured at pins
(2) Specified by design. Not production tested.

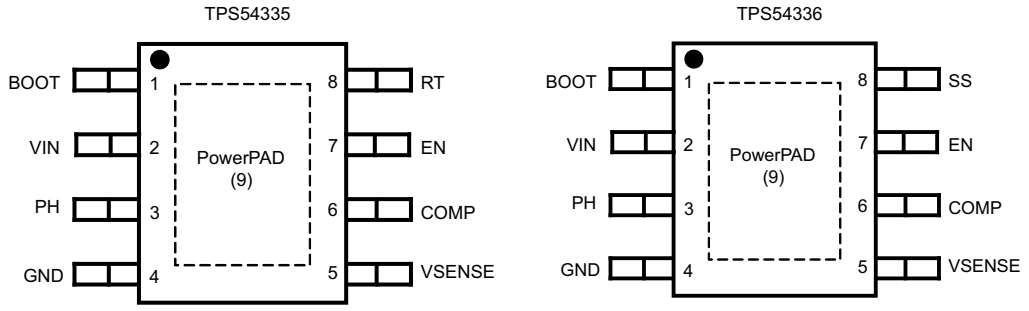
ELECTRICAL CHARACTERISTICS (continued)

The Electrical Ratings specified in this section will apply to all specifications in this document unless otherwise noted. These specifications will be interpreted as conditions that will not degrade the device's parametric or functional specifications for the life of the product containing it. T_J = –40°C to +150°C, VIN =4.5 TO 28V, (unless otherwise noted)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING FREQUENCY					
Switching frequency range	TPS54335	50		1500	kHz
	TPS54335, Rrt = 100 kΩ	384	480	576	kHz
	TPS54335, Rrt = 1000 kΩ, –40°C~105°C	40	50	60	kHz
	TPS54335, Rrt = 30 kΩ	1200	1500	1800	kHz
Internal switching frequency	TPS54336	272	340	408	kHz
SLOW START					
Internal slow start time	TPS54335		2		ms
Slow start charge current	TPS54336		2.3		µA

PIN ASSIGNMENTS

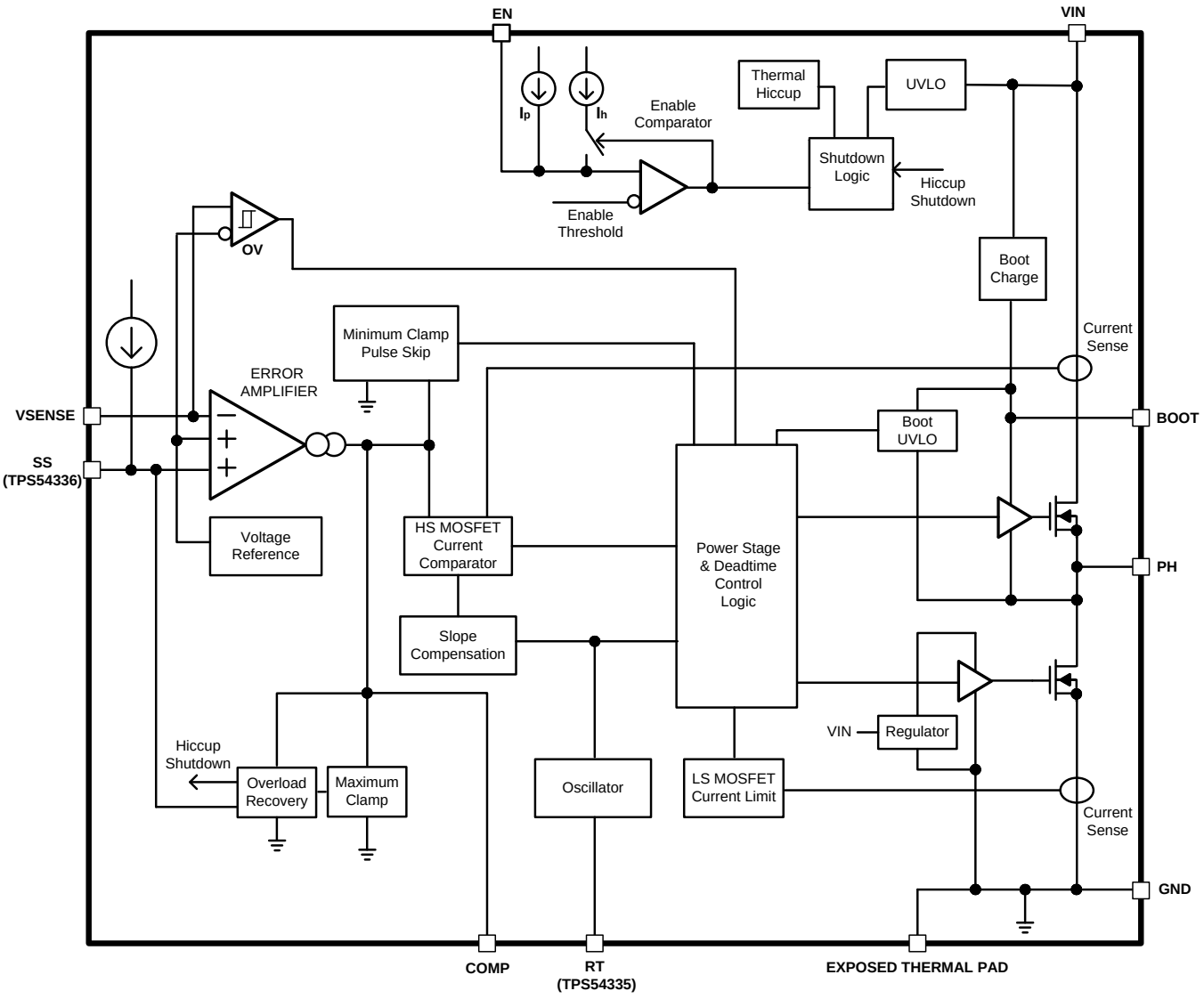
8-PIN SOIC WITH THERMAL PAD
(TOP VIEW)



PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NUMBER	
BOOT	1	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is refreshed.
Vin	2	Input supply voltage, 4.5 V to 28 V.
PH	3	The source of the internal high side power MOSFET.
GND	4	Ground.
VSENSE	5	Inverting node of the gm error amplifier.
COMP	6	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	7	Enable pin. Float to enable.
RT (TPS54335)	8	Connect to an external timing resistor to adjust the switching frequency of the device.
SS (TPS54336)	8	Slow-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference.
Powerpad	9	GND pin should be connected to the exposed thermal pad for proper operation. This thermal pad should be connected to any internal PCB ground plane using multiple vias for good thermal performance.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

HIGH-SIDE MOSFET ON RESISTANCE vs JUNCTION TEMPERATURE

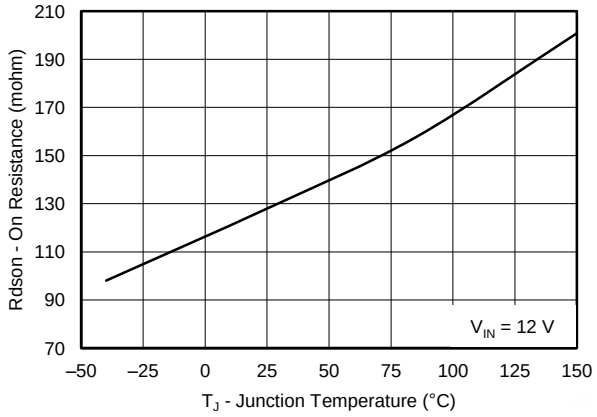


Figure 1.

LOW-SIDE MOSFET ON RESISTANCE vs JUNCTION TEMPERATURE

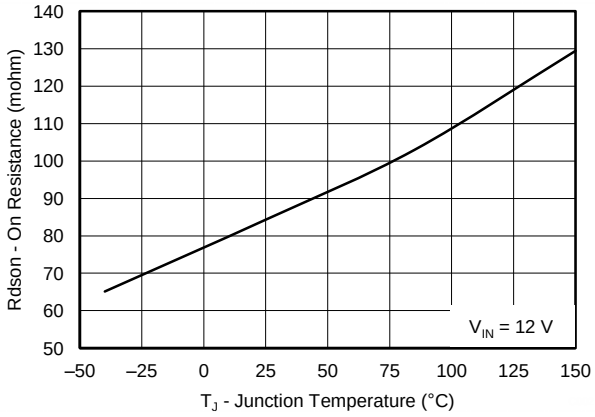


Figure 2.

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

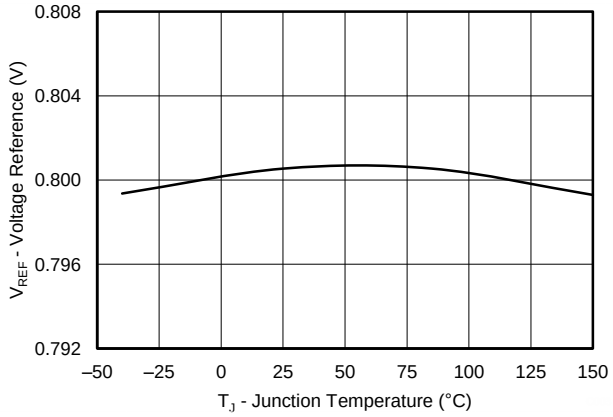


Figure 3.

OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

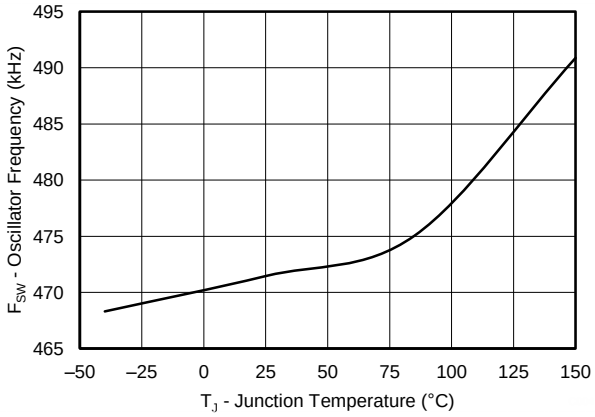


Figure 4.

UVLO THRESHOLD vs JUNCTION TEMPERATURE

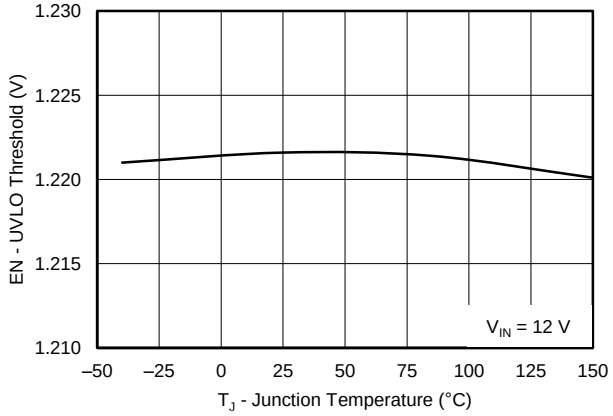


Figure 5.

HYSTERESIS CURRENT vs JUNCTION TEMPERATURE

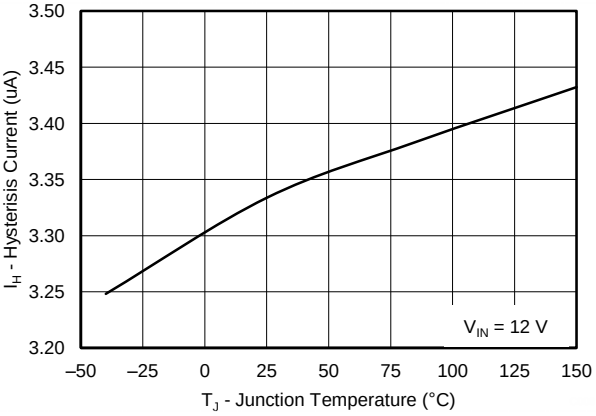


Figure 6.

TYPICAL CHARACTERISTICS (continued)

PULLUP CURRENT vs JUNCTION TEMPERATURE

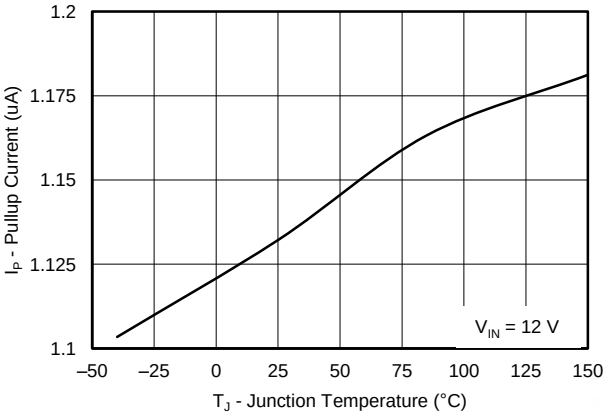


Figure 7.

NON-SWITCHING OPERATING QUIESCENT CURRENT vs INPUT VOLTAGE

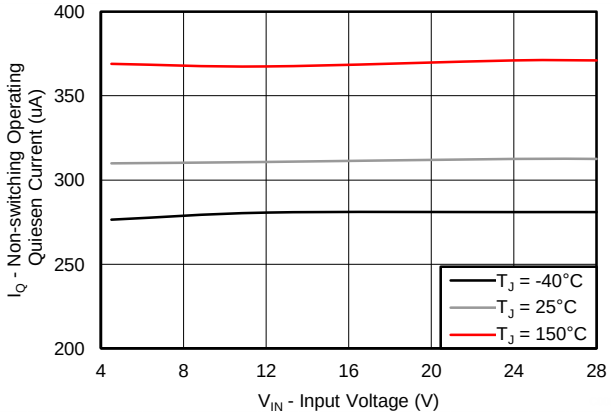


Figure 8.

SHUTDOWN QUIESCENT CURRENT vs INPUT VOLTAGE

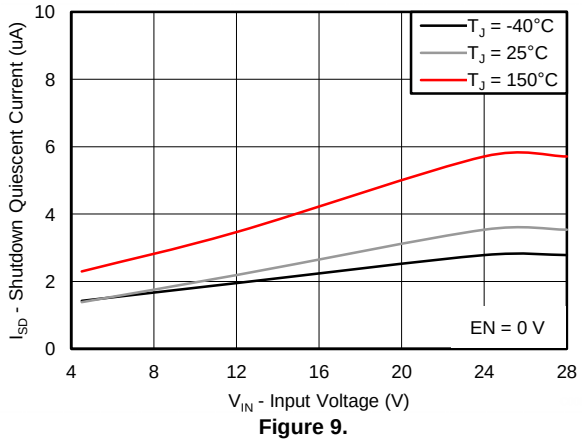


Figure 9.

SS CHARGE CURRENT vs JUNCTION TEMPERATURE

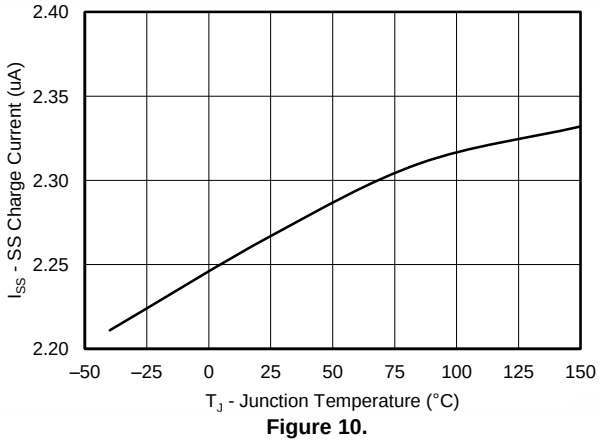


Figure 10.

MINIMUM CONTROLLABLE ON TIME vs JUNCTION TEMPERATURE

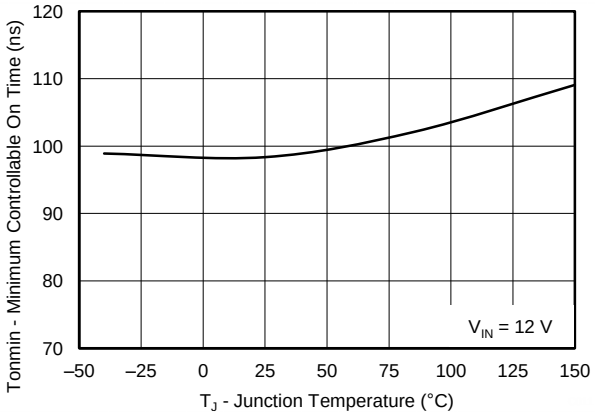


Figure 11.

MINIMUM CONTROLLABLE DUTY RATIO vs JUNCTION TEMPERATURE

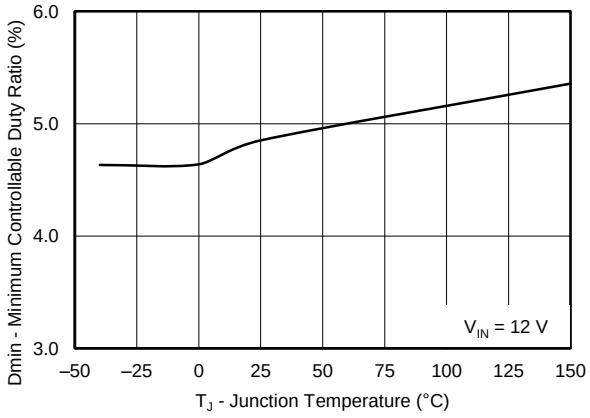


Figure 12.

TYPICAL CHARACTERISTICS (continued)

BOOT-PH UVLO THRESHOLD vs JUNCTION TEMPERATURE

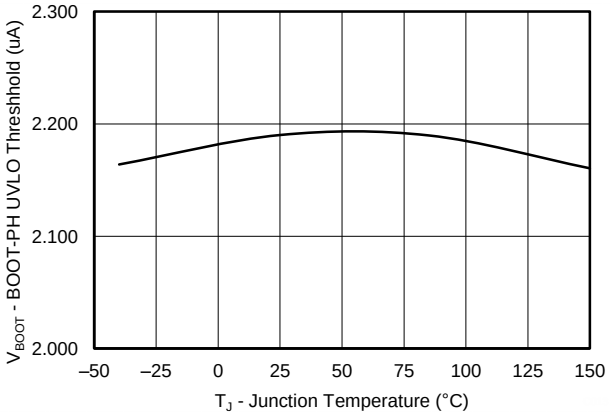


Figure 13.

CURRENT LIMIT THRESHOLD vs INPUT VOLTAGE

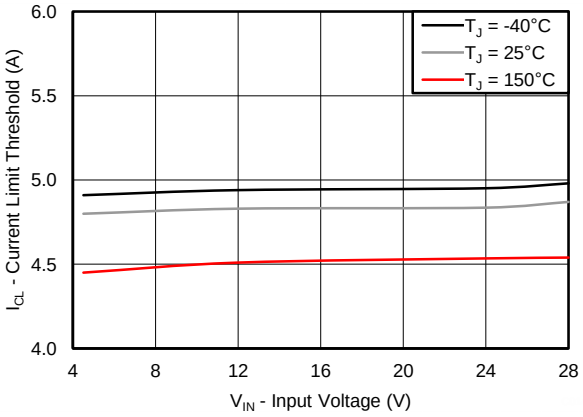


Figure 14.

OVERVIEW

The device is a 28-V, 3-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the device implements a constant frequency, peak current mode control which reduces output capacitance and simplifies external frequency compensation design.

The device has been designed for safe monotonic startup into pre-biased loads. It has a typical default start up voltage of 4.0 V. The EN pin has an internal pull-up current source that can provide a default condition when the EN pin is floating for the device to operate. The total operating current for the device is typically 310μA when not switching and under no load. When the device is disabled, the supply current is less than 5μA.

The integrated 128mΩ/84mΩ MOSFETs allow for high efficiency power supply designs with continuous output currents up to 3 amperes.

The device reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor between the BOOT and PH pins. The boot capacitor voltage is monitored by an UVLO circuit and turns off the high side MOSFET when the voltage falls below a preset threshold. The output voltage can be stepped down to as low as the 0.8 V reference.

The device minimizes excessive output over-voltage transients by taking advantage of the over-voltage power good comparator. When the regulated output voltage is greater than 106% of the nominal voltage, the over-voltage comparator is activated, and the high side MOSFET is turned off and masked from turning on until the output voltage is lower than 104%.

The TPS54335 has wide switching frequency of 50 kHz to 1500 kHz which allows for efficiency and size optimization when selecting the output filter components. The internal 2ms slow start time is implemented to minimize inrush currents.

The TPS54336 is fixed at 340kHz. It is able to adjust the slow start time by the SS pin.

DETAILED DESCRIPTION

FIXED FREQUENCY PWM CONTROL

The device uses a fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the COMP voltage level the high side power switch is turned off and the low side power switch is turned on. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level and also implements a minimum clamp for improved transient response performance.

LIGHT LOAD OPERATION

The device monitors the peak switch current of the high-side MOSFET. Once the peak switch current is lower than typically 0.5A, the device stops switching to boost the efficiency until the peak switch current again rises higher than typically 0.5A.

VOLTAGE REFERENCE

The voltage reference system produces a precise ±1.5% voltage reference over temperature by scaling the output of a temperature stable bandgap circuit.

ADJUSTING THE OUTPUT VOLTAGE

The output voltage is set with a resistor divider from the output node to the VSENSE pin. It is recommended to use divider resistors with 1% tolerance or better. Start with a 10 kΩ for the upper resistor divider, R1 and useEquation 1 to calculate R2. To improve efficiency at light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R2 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R1 \quad (1)$$

ENABLE AND ADJUSTING UNDERVOLTAGE LOCKOUT

The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state.

The EN pin has an internal pull-up current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 180mV.

If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in Figure 15. When using the external UVLO function it is recommended to set the hysteresis to be greater than 500mV.

The EN pin has a small pull-up current Ip which sets the default state of the pin to enable when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function since it increases by I_h once the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 2, and Equation 3.

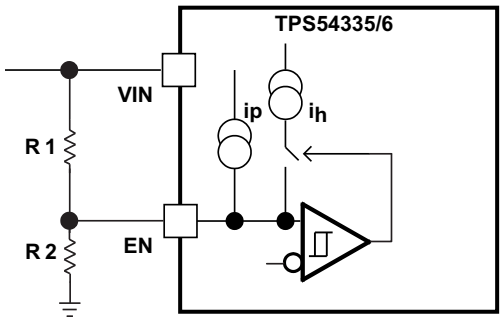


Figure 15. Adjustable VIN Undervoltage Lock Out

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (2)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \quad (3)$$

Where I_h = 3.3 µA, I_p = 1.15 µA, $V_{ENRISING}$ = 1.21 V, $V_{ENFALLING}$ = 1.17 V

ERROR AMPLIFIER

The device has a transconductance amplifier. The error amplifier compares the VSENSE voltage to the lower of the internal slow start voltage or the internal 0.8 V voltage reference. The transconductance of the error amplifier is 1300µA/V typically. The frequency compensation components are placed between the COMP pin and ground.

SLOPE COMPENSATION AND OUTPUT CURRENT

The device adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations as duty cycle increases. The available peak inductor current remains constant over the full duty cycle range.

SAFE START-UP INTO PRE-BIASED OUTPUTS

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, both high-side and low-side MOSFETs are not allowed to be turned on until the internal slow-start voltage (TPS54335), or SS pin voltage (TPS54336) is higher than V_{SENSE} pin voltage.

BOOTSTRAP VOLTAGE (BOOT)

The device has an integrated boot regulator, and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate drive voltage for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than VIN and BOOT-PH voltage is below regulation. The value of this ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage. When the voltage between BOOT and PH drops below the BOOT-PH UVLO threshold, which is typically 2.1V, the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged.

ADJUSTABLE SWITCHING FREQUENCY (TPS54335 ONLY)

To determine the RT resistance for a given switching frequency, use Equation 4 or the curve in Figure 16. To reduce the solution size one would set the switching frequency as high as possible, but tradeoffs of the supply efficiency and minimum controllable on time should be considered.

$$Rrt(k\Omega) = 55300 \times Fsw(kHz)^{-1.025} \quad (4)$$

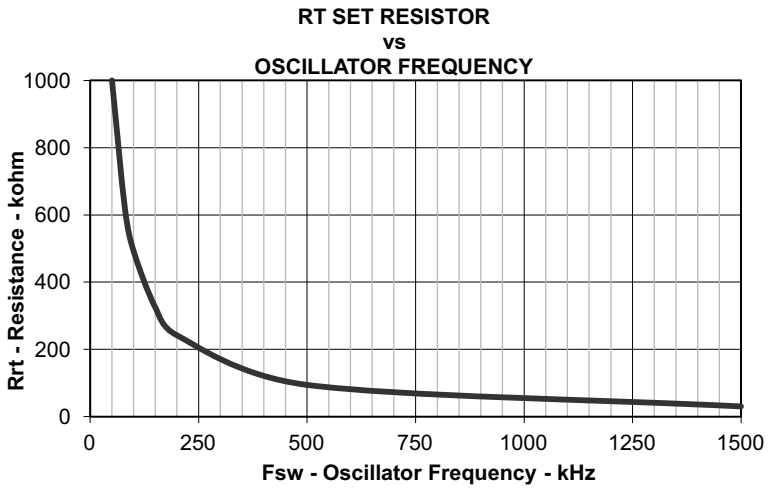


Figure 16. RT Set Resistor vs Switching Frequency

SLOW START (TPS54336 ONLY)

The device uses the lower voltage of the internal voltage reference or the SS pin voltage as the reference voltage and regulates the output accordingly. A capacitor on the SS pin to ground implements a slow start time. The device has an internal pull-up current source of 2.3 µA that charges the external slow start capacitor. The calculations for the slow start time (Tss, 10% to 90%) and slow start capacitor (Css) are shown in Equation 5. The voltage reference (Vref) is 0.8 V and the slow start charge current (Iss) is 2.3µA.

$$Tss(ms) = \frac{Css(nF) \times Vref(V)}{Iss(\mu A)} \quad (5)$$

When the input UVLO is triggered, the EN pin is pulled below 1.21V, or a thermal shutdown event occurs the device stops switching and enters low current operation. At the subsequent power up, when the shutdown condition is removed, the device does not start switching until it has discharged its SS pin to ground ensuring proper soft start behavior.

OUTPUT OVERVOLTAGE PROTECTION (OVP)

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the VSENSE pin voltage to the OVP threshold. If the VSENSE pin voltage is greater than the OVP threshold the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

OVERCURRENT PROTECTION

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

High-side MOSFET overcurrent protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle by cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference the high-side switch is turned off.

Low-side MOSFET overcurrent protection

While the low-side MOSFET is turned on its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current limit is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time which is programmed for 512 switching cycles, the device will shut down itself and restart after the hiccup time of 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

THERMAL SHUTDOWN

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C typically. Once the junction temperature drops below 165°C typically, the internal thermal hiccup timer will start to count. The device reinitiates the power up sequence after the built-in thermal shutdown hiccup time (32768 cycles) is over.

SMALL SIGNAL MODEL FOR LOOP RESPONSE

Figure 17 shows an equivalent model for the device control loop which can be modeled in a circuit simulation program to check frequency response and transient responses. The error amplifier is a transconductance amplifier with a gm of 1300µA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor Roea (3.07 MΩ) and capacitor Coea (20.7 pF) model the open loop gain and frequency response of the error amplifier. The 1-mV ac voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting a/c and c/b show the small signal responses of the power stage and frequency compensation respectively. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing the R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

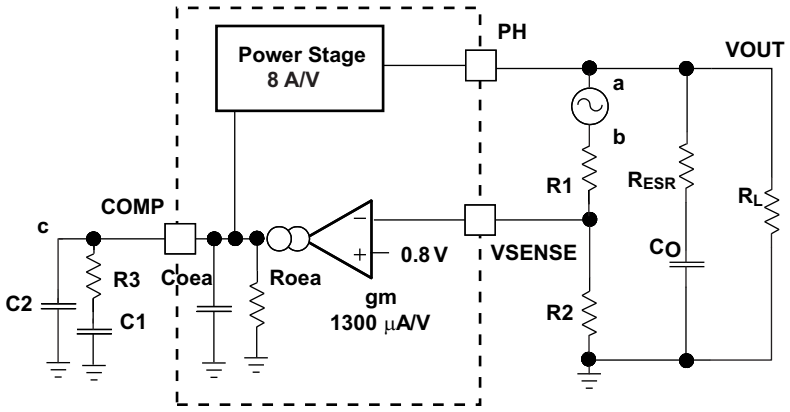


Figure 17. Small Signal Model for Loop Response

SIMPLE SMALL SIGNAL MODEL FOR PEAK CURRENT MODE CONTROL

Figure 18 is a simple small signal model that can be used to understand how to design the frequency compensation. The device power stage can be approximated to a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 6 and consists of a dc gain, one dominant pole and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 17) is the power stage transconductance (gm_{ps}) which is 8 A/V for the device. The DC gain of the power stage is the product of gm_{ps}

and the load resistance, R_L, as shown in Equation 7 with resistive loads. As the load current increases, the DC gain decreases. This variation with load may seem problematic at first glance, but fortunately the dominant pole moves with load current (see Equation 8). The combined effect is highlighted by the dashed line in Figure 19. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation.

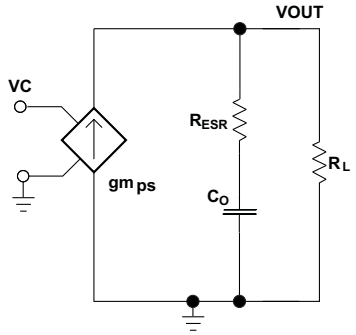


Figure 18. Simplified Small Signal Model for Peak Current Mode Control

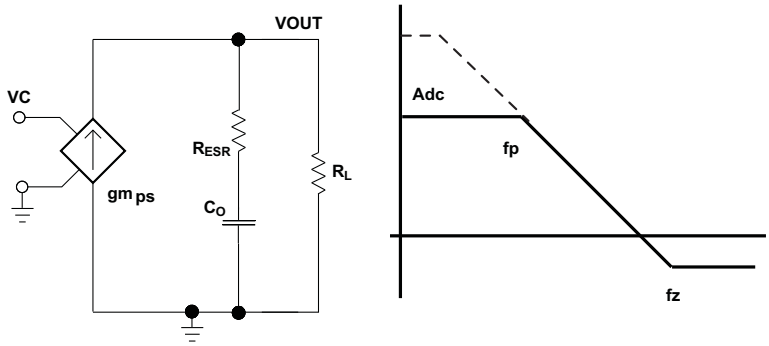


Figure 19. Simplified Frequency Response for Peak Current Mode Control

$$\frac{VOUT}{VC} = Adc \times \frac{\left(1+\frac{s}{2\pi \times fz}\right)}{\left(1+\frac{s}{2\pi \times fp}\right)} \quad (6)$$

$$Adc = gm_{ps} \times R_L \quad (7)$$

$$fp = \frac{1}{C_O \times R_L \times 2\pi} \quad (8)$$

$$fz = \frac{1}{C_O \times R_{ESR} \times 2\pi} \quad (9)$$

Where

gm_{ea} is the GM amplifier gain (1300µA/V)
gm_{ps} is the power stage gain (8 A/V).
R_L is the load resistance
C_O is the output capacitance.
R_{ESR} is the equivalent series resistance of the output capacitor.

SMALL SIGNAL MODEL FOR FREQUENCY COMPENSATION

The device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used Type II compensation circuits and a Type III frequency compensation circuit, as shown in Figure 20. In Type 2A, one additional high frequency pole, C6, is added to attenuate high frequency noise. In Type III, one additional capacitor, C11, is added to provide a phase boost at the crossover frequency. See *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352) for a complete explanation of Type III compensation.

The design guidelines below are provided for advanced users who prefer to compensate using the general method. The below equations only apply to designs whose ESR zero is above the bandwidth of the control loop. This is usually true with ceramic output capacitors.

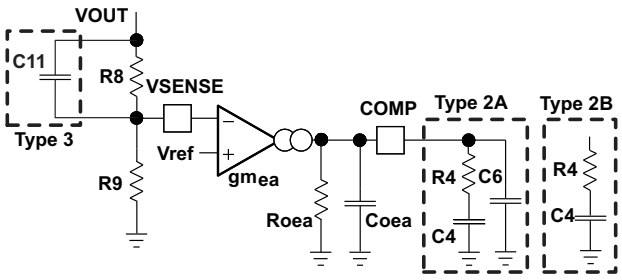


Figure 20. Types of Frequency Compensation

The general design guidelines for device loop compensation are as follows:

1. Determine the crossover frequency, fc. A good starting point is 1/10th of the switching frequency, fsw.
2. R4 can be determined by:

$$R4 = \frac{2\pi \times fc \times VOUT \times Co}{gm_{ea} \times Vref \times gm_{ps}} \quad (10)$$

   Where:

   gm_{ea} is the GM amplifier gain (1300 µA/V)
   gm_{ps} is the power stage gain (8 A/V)
   Vref is the reference voltage (0.8 V)

3. Place a compensation zero at the dominant pole: $\left(fp = \frac{1}{C_O \times R_L \times 2\pi} \right)$
   C4 can be determined by:

$$C4 = \frac{R_L \times Co}{R4} \quad (11)$$

4. C6 is optional. It can be used to cancel the zero from the ESR (Equivalent Series Resistance) of the output capacitor Co.

$$C6 = \frac{R_{ESR} \times Co}{R4} \quad (12)$$

5. Type III compensation can be implemented with the addition of one capacitor, C11. This allows for slightly higher loop bandwidths and higher phase margins. If used, C11 is calculated from Equation 13.

$$C11 = \frac{1}{(2 \cdot \pi \cdot R8 \cdot fc)} \quad (13)$$

APPLICATION INFORMATION

TPS54335 APPLICATION SCHEMATIC

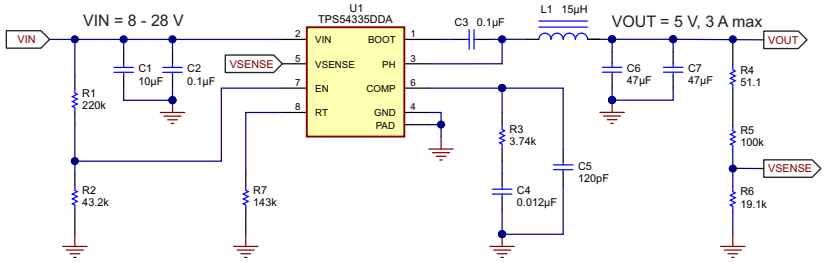


Figure 21. Typical Application Schematic, TPS54335

STEP BY STEP DESIGN PROCEDURE

The following design procedure can be used to select component values for the TPS54335 and TPS54336. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process using the TPS54335.

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

For this design example, use the following as the input parameters

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8 V to 28V
Output voltage	5 V
Transient response, 1.5 A load step	ΔVout = +/- 5 %
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	3 A
Operating Frequency	340 kHz

SWITCHING FREQUENCY

The switching frequency of the TPS54335 is set at 340 kHz to match the internally set frequency of the TPS54336 for this design. Use Equation 4 to calculate the required value for R7. The calculated value is 140.6 kΩ. Use the next higher standard value of 143 kΩ.

OUTPUT VOLTAGE SET POINT

The output voltage of the TPS54335 is externally adjustable using a resistor divider network. In the application circuit of Figure 21, this divider network is comprised of R5 and R6. The relationship of the output voltage to the resistor divider is given by Equation 14 and Equation 15:

$$R6 = \frac{R5 \times V_{REF}}{V_{OUT} - V_{REF}} \tag{14}$$

$$V_{OUT} = V_{REF} \times \left[\frac{R5}{R6} + 1\right] \tag{15}$$

Choose R5 to be approximately 100 kΩ. Slightly increasing or decreasing R5 can result in closer output voltage matching when using standard value resistors. In this design, R5 = 100 kΩ and R6 = 19.1 kΩ, resulting in a 4.988 V output voltage. The 51.1 ohm resistor R4 is provided as a convenient place to break the control loop for stability testing.

Under Voltage Lockout Set Point

The Under Voltage Lock Out (UVLO) can be adjusted using the external voltage divider network of R1 and R2. R1 is connected between VIN and the EN pin of the TPS54335 and R2 is connected between EN and GND . The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the minimum input voltage is 8 V, so the start voltage threshold is set to 7.15 V with 1 V hysteresis. Equation 2 and Equation 3 can be used to calculate the values for the upper and lower resistor values of R1 and R2.

INPUT CAPACITORS

The TPS54335 requires an input decoupling capacitor and depending on the application, a bulk input capacitor. The typical recommended value for the decoupling capacitor is 10 µF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. A smaller value may be used as long as all other requirements are met; however 10 µF has been shown to work well in a wide variety of circuits. Additionally, some bulk capacitance may be needed, especially if the TPS54335 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but should be rated to handle the maximum input voltage including ripple voltage, and should filter the output so that input ripple voltage is acceptable. For this design, a 10 µF, X7R dielectric capacitor rated for 35 V is used for the input decoupling capacitor. . The equivalent series resistance (ESR) is approximately 2mΩ, and the current rating is 3 A. Additionally, a small 0.1 µF capacitor is included for high frequency filtering.

This input ripple voltage can be approximated by Equation 16

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \tag{16}$$

Where $I_{OUT(MAX)}$ is the maximum load current, f_{SW} is the switching frequency, C_{BULK} is the bulk capacitor value and ESR_{MAX} is the maximum series resistance of the bulk capacitor.

The maximum RMS ripple current also needs to be checked. For worst case conditions, this can be approximated by Equation 17

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \tag{17}$$

In this case, the input ripple voltage would be 227 mV and the RMS ripple current would be 1.5 A. It is also important to note that the actual input voltage ripple will be greatly affected by parasitics associated with the layout and the output impedance of the voltage source. The actual input voltage ripple for this circuit is shown in Design Parameters and is larger than the calculated value. This measured value is still below the specified input limit of 400 mV. The maximum voltage across the input capacitors would be VIN max plus ΔVIN/2. The chosen bypass capacitor is rated for 35 V and the ripple current capacity is greater than 3 A, both providing ample margin. It is very important that the maximum ratings for voltage and current are not exceeded under any circumstance.

OUTPUT FILTER COMPONENTS

Two components need to be selected for the output filter, L_{OUT} and C_{OUT}. Since the TPS54335 is an externally compensated device, a wide range of filter component types and values can be supported.

Inductor Selection

To calculate the minimum value of the output inductor, use Equation 18

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{SW}} \quad (18)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. In general, this value is at the discretion of the designer; however, the following guidelines may be used. For designs using low ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.3 may be used. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results.

For this design example, use K_{IND} = 0.3 and the minimum inductor value is calculated to be 13.4 µH. For this design, a close standard value was chosen: 15 µH.

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from Equation 19

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8}\right)^2} \quad (19)$$

and the peak inductor current can be determined with Equation 20

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \quad (20)$$

For this design, the RMS inductor current is 3.002 A and the peak inductor current is 3.503 A. The chosen inductor is a Coilcraft 15 µH, XAL6060-153MEB. It has a saturation current rating of 5.8 A and an RMS current rating of 6.0 A, meeting these requirements. Smaller or larger inductor values can be used depending on the amount of ripple current the designer wishes to allow so long as the other design requirements are met. Larger value inductors will have lower ac current and result in lower output voltage ripple, while smaller inductor values will increase ac current and output voltage ripple. In general, inductor values for use with the TPS54335 are in the range of 0.68 µH to 100 µH.

Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of drop in the output voltage. Equation 21 shows the minimum output capacitance necessary to accomplish this.

$$Co > \frac{2 \cdot \Delta Iout}{fsw \cdot \Delta Vout} \quad (21)$$

Where ΔIout is the change in output current, Fsw is the regulators switching frequency and ΔVout is the allowable change in the output voltage. For this example, the transient load response is specified as a 5% change in Vout for a load step of 1.5 A. For this example, ΔIout = 1.5 A and ΔVout = 0.05 x 5.0 = 0.250 V. Using these numbers gives a minimum capacitance of 35.3 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 22 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, Voripple is the maximum allowable output voltage ripple, and Iripple is the inductor ripple current. In this case, the maximum output voltage ripple is 30 mV. Under this requirement Equation 22, yields 12.3 µF.

$$Co > \frac{1}{8 \cdot fsw} \cdot \frac{1}{\frac{Voripple}{Iripple}} \tag{22}$$

Equation 23 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 23 indicates the ESR should be less than 29.8 mΩ. In this case, the ceramic caps' ESR is much smaller than 29.8 mΩ.

$$Resr < \frac{Voripple}{Iripple} \tag{23}$$

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which increases this minimum value. For this example, two 47 µF 10V X5R ceramic capacitor with 3 mΩ of ESR are used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation 24 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 24 yields 116.2 mA for each capacitor.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT} \right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times N_C} \right) \tag{24}$$

COMPENSATION COMPONENTS

There are several possible methods to design closed loop compensation for dc/dc converters. For the ideal current mode control, the design equations can be easily simplified. The power stage gain is constant at low frequencies, and rolls off at -20 dB/decade above the modulator pole frequency. The power stage phase is 0 degrees at low frequencies and starts to fall one decade below the modulator pole frequency reaching a minimum of -90 degrees one decade above the modulator pole frequency. The modulator pole is a simple pole shown in Equation 25

$$fp\ mod = \frac{Ioutmax}{2\pi \times Vout \times Cout} \tag{25}$$

For the TPS54335 most circuits will have relatively high amounts of slope compensation. As more slope compensation is applied, the power stage characteristics will deviate from the ideal approximations. The phase loss of the power stage will now approach -180 degrees, making compensation more difficult. The power stage transfer function can be solved but it is a tedious hand calculation that does not lend itself to simple approximations. It is best to use Pspice to accurately model the power stage gain and phase so that a reliable compensation circuit can be designed. Alternately, a direct measurement of the power stage characteristics can be used. That is the technique used in this design procedure. For this design, L1 = 15 µH. C6 and C7 are set to 47µF each, and the ESR is 3 mΩ. Now the power stage characteristics are shown in Figure 22.

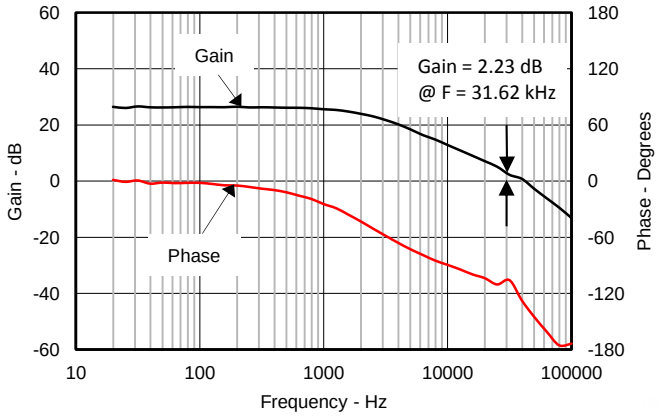


Figure 22. Power Stage Gain and Phase Characteristics

For this design, the intended crossover frequency is 31.62 kHz (there is an actual measured data point for that frequency). From the power stage gain and phase plots, the gain at 31.62 kHz is 2.23 dB and the phase is about -106 degrees. For 60 degrees of phase margin, additional phase boost from a feed forward capacitor in parallel with the upper resistor of the voltage set point divider is not needed. R3 sets the gain of the compensated error amplifier to be equal and opposite the power stage gain at crossover. The required value of R3 can be calculated from Equation 26.

$$R3 = \frac{10^{\frac{-G_{PWRSTG}}{20}}}{gm_{EA}} \cdot \frac{V_{REF}}{V_{OUT}} \tag{26}$$

To maximize phase gain, the compensator zero is placed one decade below the crossover frequency of 31.62 kHz. The required value for C4 is given by Equation 27.

$$C4 = \frac{1}{2 \cdot \pi \cdot R3 \cdot \frac{F_{CO}}{10}} \tag{27}$$

To maximize phase gain the high frequency pole is placed one decade above the crossover frequency of 31.62 kHz. The pole can also be useful to offset the ESR of aluminum electrolytic output capacitors. The value for C5 can be calculated from Equation 28.

$$C5 = \frac{1}{2 \cdot \pi \cdot R3 \cdot 10 \cdot F_{CO}} \tag{28}$$

For this design the calculated values for the compensation components are R3 = 3.74 kΩ ,C4 = 0.012 µF and C5 = 120 pF.

BOOTSTRAP CAPACITOR

Every TPS54335 design requires a bootstrap capacitor, C3. The bootstrap capacitor must be 0.1 µF. The bootstrap capacitor is located between the PH pins and BOOT pin. The bootstrap capacitor should be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

POWER DISSIPATION ESTIMATE

The following formulas show how to estimate the device power dissipation under continuous conduction mode operations. They should not be used if the device is working in the discontinuous conduction mode (DCM) or pulse skipping Eco-mode™.

The device power dissipation includes:

1) Conduction loss: $Pcon = Iout^2 \times R_{DS(on)} \times V_{OUT}/V_{IN}$

2) Switching loss: $Psw = 0.5 \times 10^{-9} \times V_{IN}^{\ 2} \times I_{OUT} \times Fsw$

3) Gate charge loss: $P_{gc} = 22.8 \times 10^{-9} \times F_{sw}$

4) Quiescent current loss: $P_q = 0.11 \times 10^{-3} \times V_{IN}$

Where:

I_{OUT} is the output current (A).

$R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω).

VOUT is the output voltage (V).

VIN is the input voltage (V).

Fsw is the switching frequency (Hz).

So

$P_{tot} = P_{con} + P_{sw} + P_{gc} + P_q$

For given T_A , $T_J = T_A + R_{th} \times P_{tot}$.

For given $T_{JMAX} = 150°C$, $T_{AMAX} = T_{JMAX} – R_{th} \times P_{tot}$.

Where:

P_{tot} is the total device power dissipation (W).

T_A is the ambient temperature (°C).

T_J is the junction temperature (°C) .

R_{th} is the thermal resistance of the package (°C/W).

T_{JMAX} is maximum junction temperature (°C).

T_{AMAX} is maximum ambient temperature (°C).

PCB LAYOUT

The VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connection. the VIN pin, and the GND pin of the IC. The typical recommended bypass capacitance is 10-µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN and GND pins of the device. See Figure 23 for a PCB layout example. The GND pin should be tied to the PCB ground plane at the pin of the IC. To facilitate close placement of the input bypass capacitors, The PH pin should be routed to a small copper area directly adjacent to the pin. Use vias to rout the PH signal to the bottom side or an inner layer. If necessary you can allow the top side copper area to extend slightly under the body of the closest input bypass capacitor. Make the copper trace on the bottom or internal layer short and wide as practical to reduce EMI issues. Connect the trace with vias back to the top side to connect with the output inductor as shown after the GND pin. In the same way use a bottom or internal layer trace to rout the PH signal across the VIN pin to connect to the BOOT capacitor as shown. Make the circulating loop from PH to the output inductor, output capacitors and back to GND as tight as possible while preserving adequate etch width to reduce conduction losses in the copper . For operation at full rated load, the ground area near the IC must provide adequate heat dissipating area. Connect the exposed thermal pad to bottom or internal layer ground plane using vias as shown. Additional vias may be used adjacent to the IC to tie top side copper to the internal or bottom layer copper. The additional external components can be placed approximately as shown. Use a separate ground trace to connect the feed back, compensation, UVLO and RT (SS for TPS54336) returns. Connect this ground trace to the main power ground at a single point to minimize circulating currents. It may be possible to obtain acceptable performance with alternate layout schemes, however this layout has been shown to produce good results and is intended as a guideline.

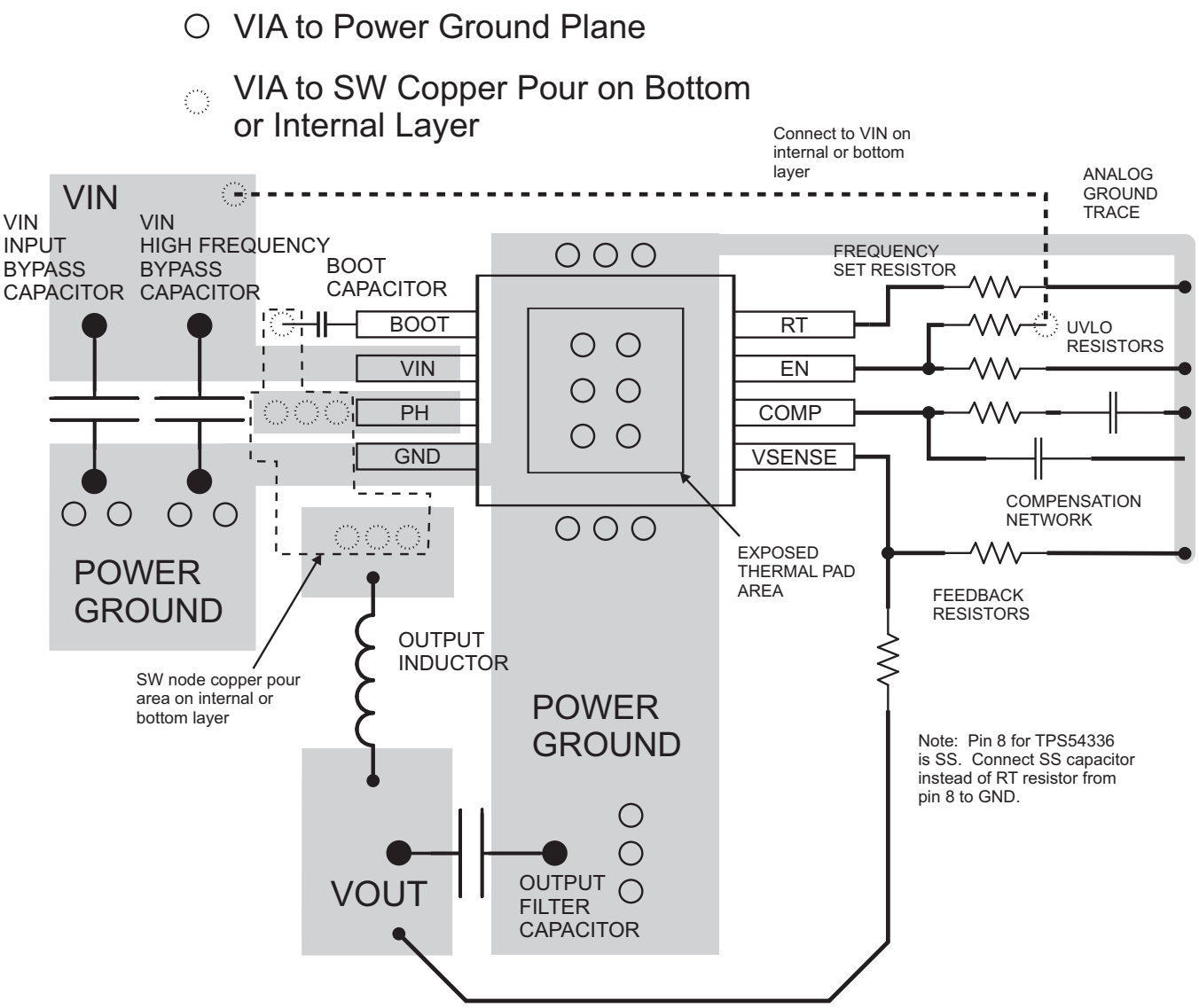


Figure 23. TPS54335DDA Board Layout

TPS54335 APPLICATION CURVES

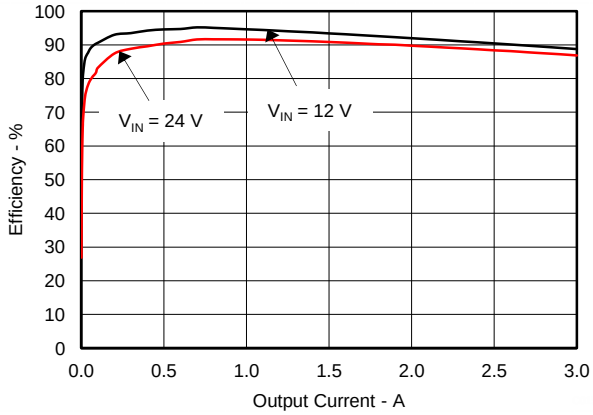


Figure 24. TPS54335 Efficiency

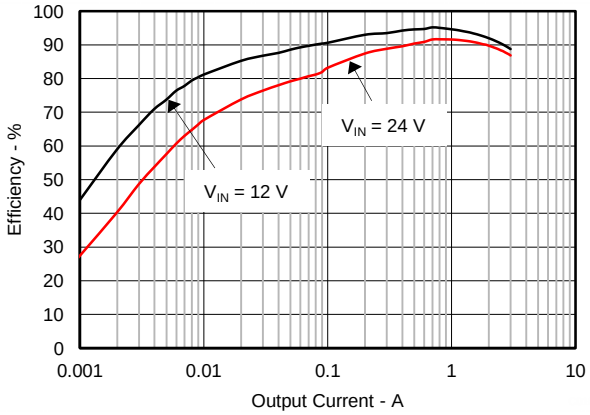


Figure 25. TPS54335 Low Current Efficiency

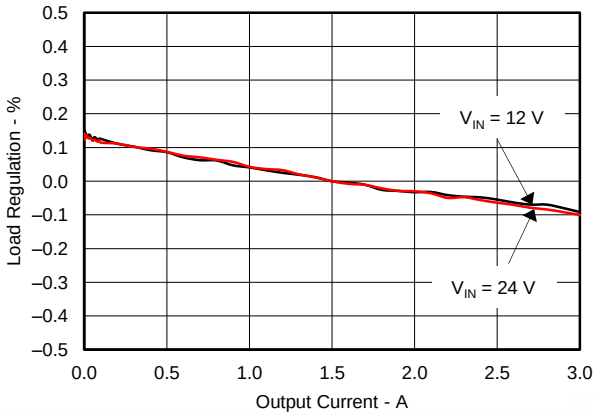


Figure 26. TPS54335 Load Regulation

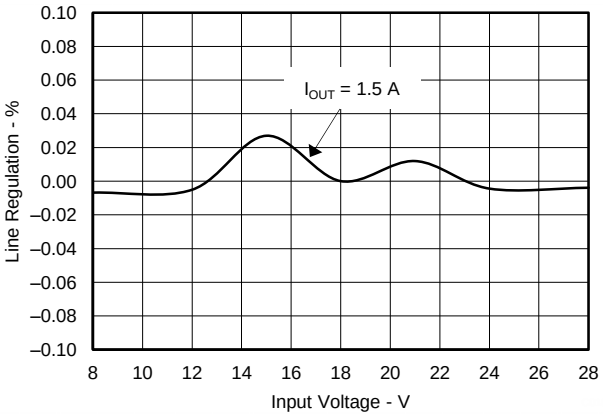


Figure 27. TPS54335 Line Regulation

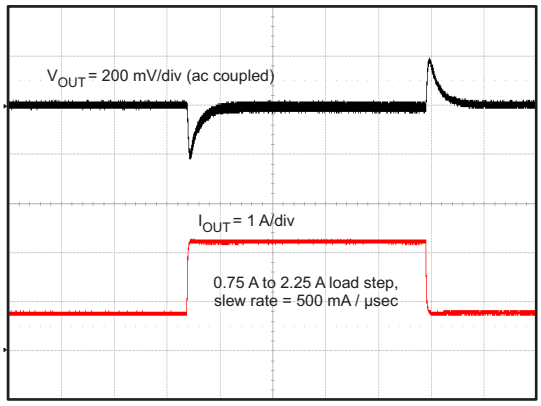


Figure 28. TPS54335 Transient Response

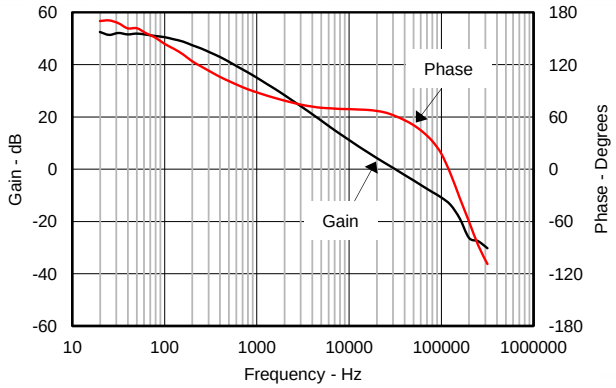


Figure 29. TPS54335 Loop Response

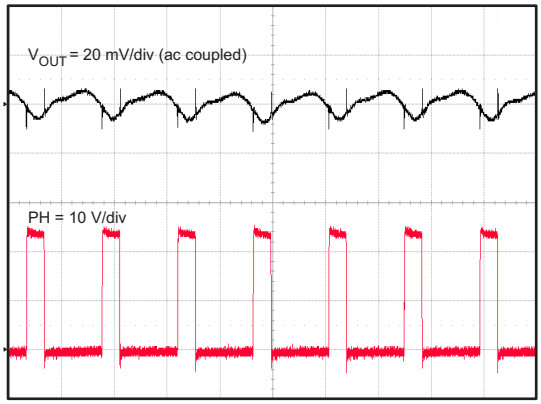


Figure 30. TPS54335 Full Load Output Ripple

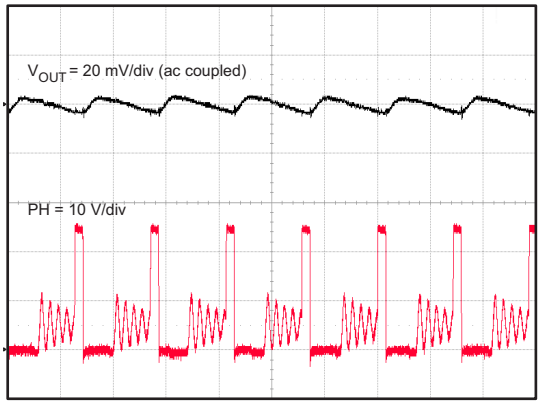


Figure 31. TPS54335 100 mA Output Ripple

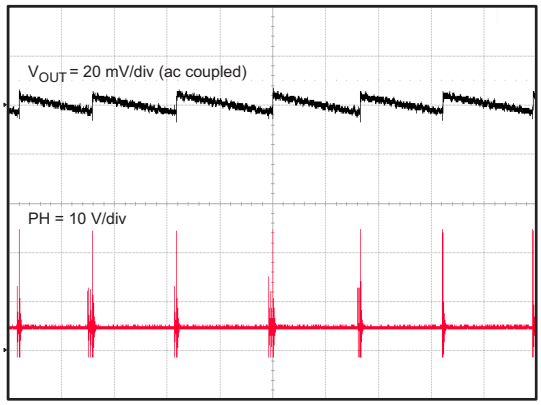


Figure 32. TPS54335 No Load Output Ripple

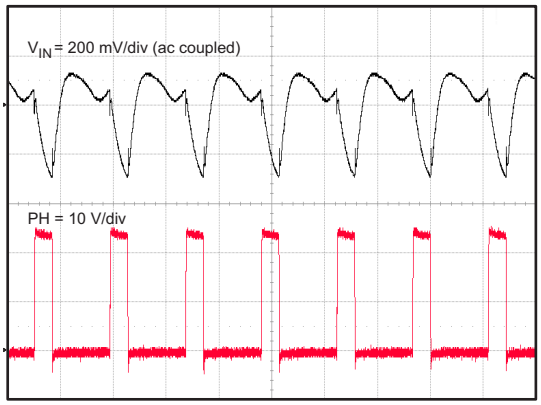


Figure 33. TPS54335 Full Load Input Ripple

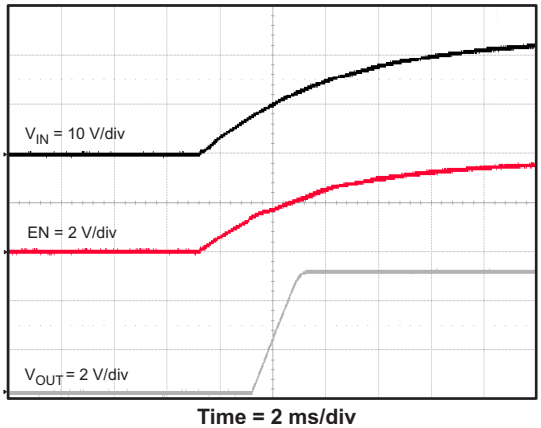


Figure 34. TPS54335 Start Up Relative to VIN

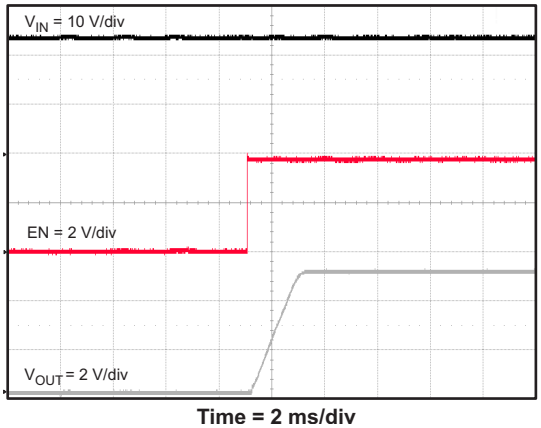


Figure 35. TPS54335 Start-up Relative to Enable

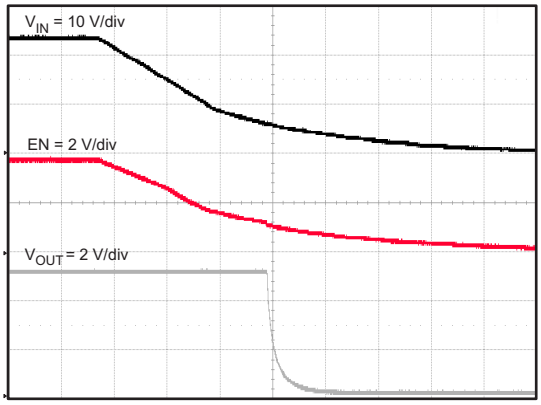


Figure 36. TPS54335 Shut Down Relative to VIN

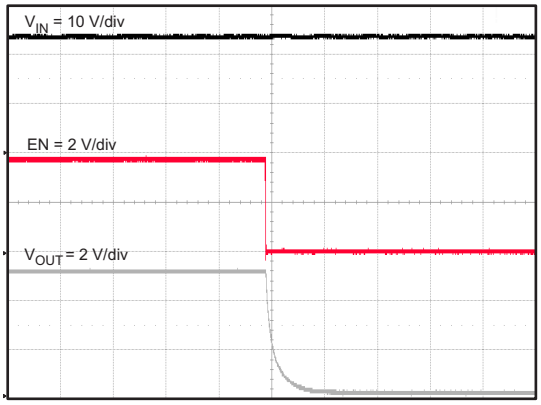


Figure 37. TPS54335 Shut Down Relative to EN

TPS54336 APPLICATION SCHEMATIC

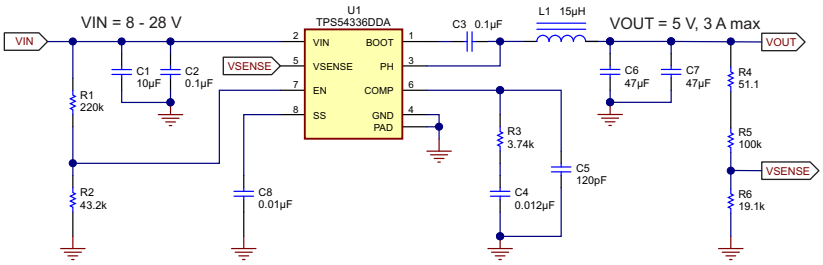


Figure 38. Typical Application Schematic, TPS54336

TPS54336 DESIGN

The design procedure for the TPS54336 is identical to the TPS54335, except the TPS54336 utilizes a slow start circuit rather than an externally set switching frequency at pin 8. The switching frequency is internally set for 340 kHz.

SLOW START CAPACITOR

The slow start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54336 reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. The soft start capacitor value can be calculated using Equation 5. For the example circuit, the soft start time is not too critical since the output capacitor value is 2 x 47 µF which does not require much current to charge to 5 V. The example circuit has the soft start time set to an arbitrary value of 3.5 ms which requires a 10 nF capacitor. In TPS54336, Iss is 2.3 µA and Vref is 0.8V.

TPS54336 APPLICATION CURVES

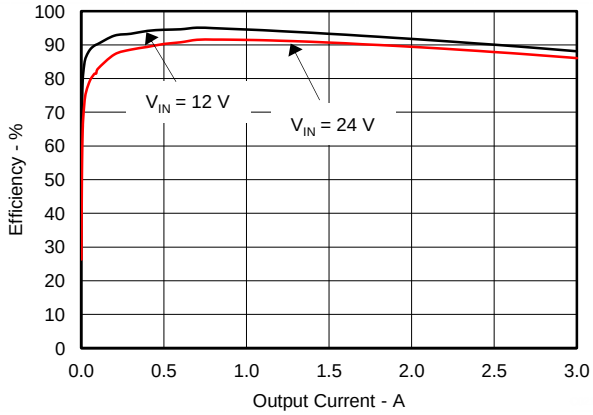


Figure 39. TPS54336 Efficiency

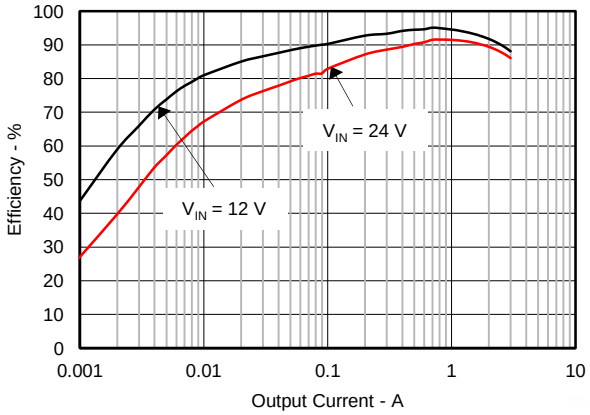


Figure 40. TPS54336 Low Current Efficiency

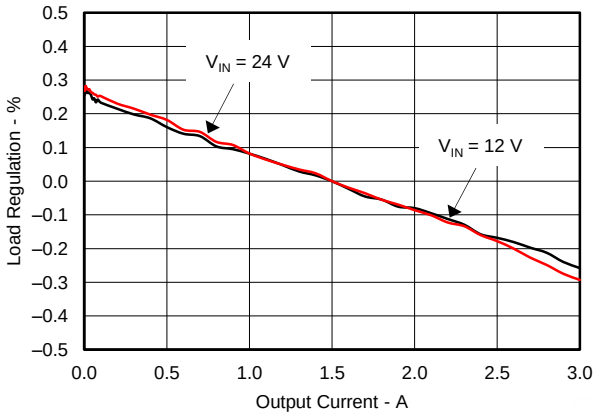


Figure 41. TPS54336 Load Regulation

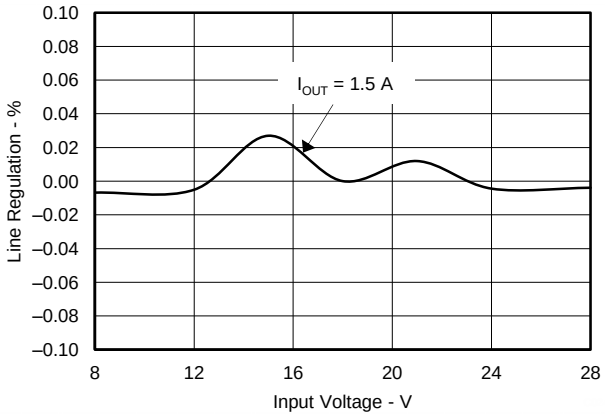


Figure 42. TPS54336 Line Regulation

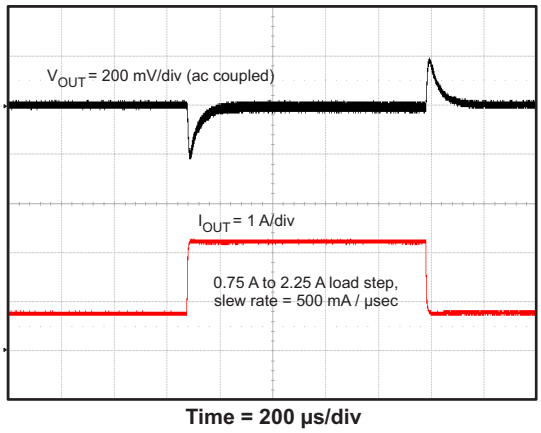


Figure 43. TPS54336 Transient Response

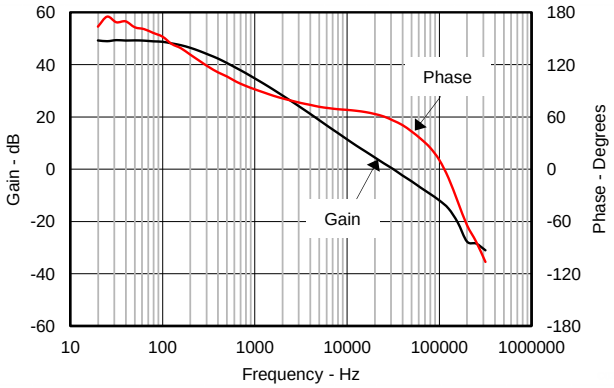


Figure 44. TPS54336 Loop Response

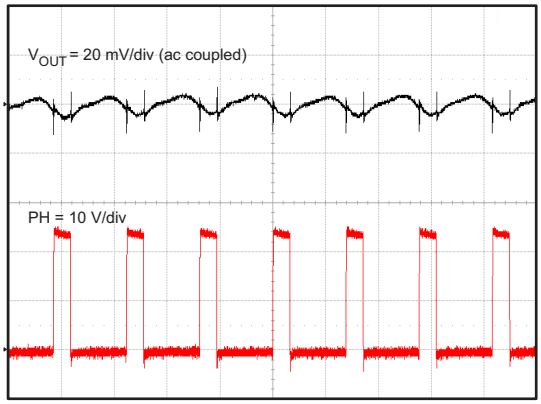


Figure 45. TPS54336 Full Load Output Ripple

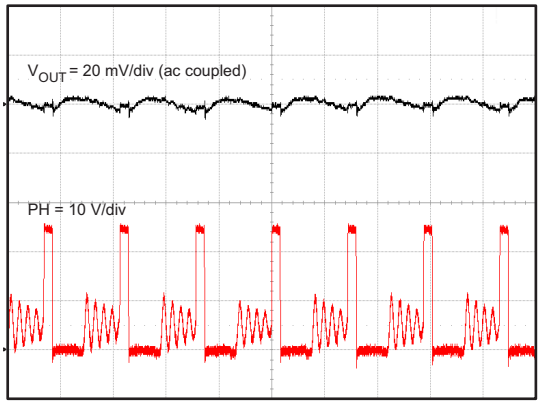


Figure 46. TPS54336 100 mA Output Ripple

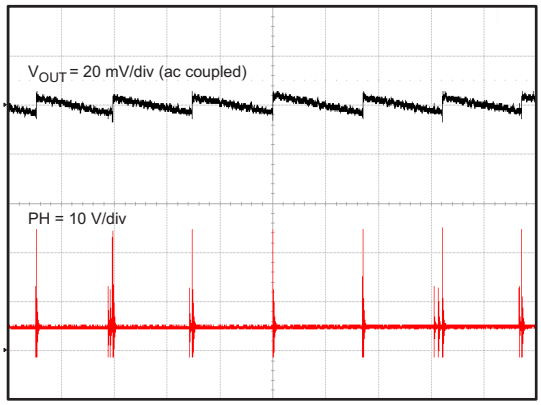


Figure 47. TPS54336 No Load Output Ripple

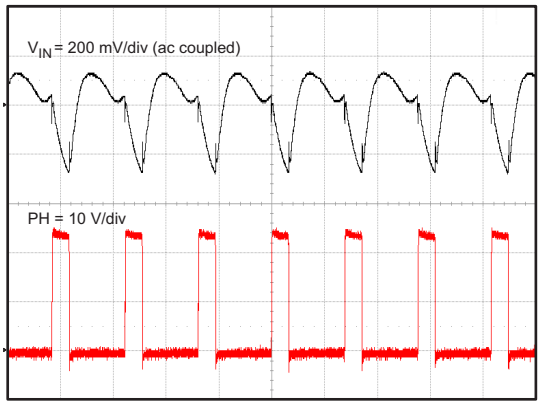


Figure 48. TPS54336 Full Load Input Ripple

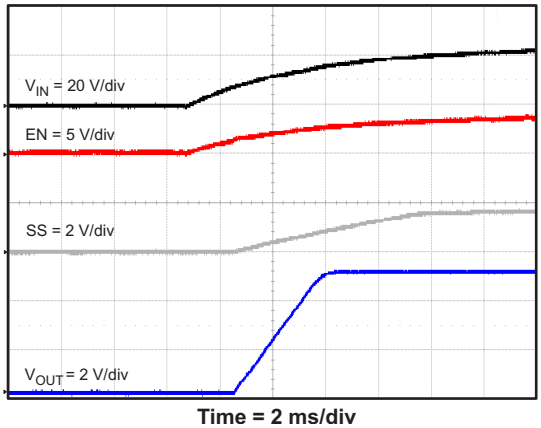


Figure 49. TPS54336 Start Up Relative to VIN

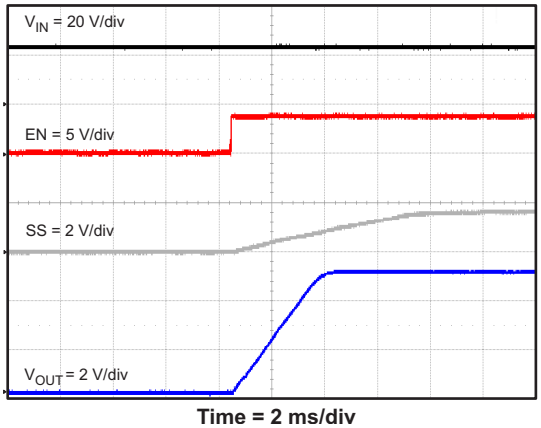


Figure 50. TPS54336 Start-up Relative to Enable

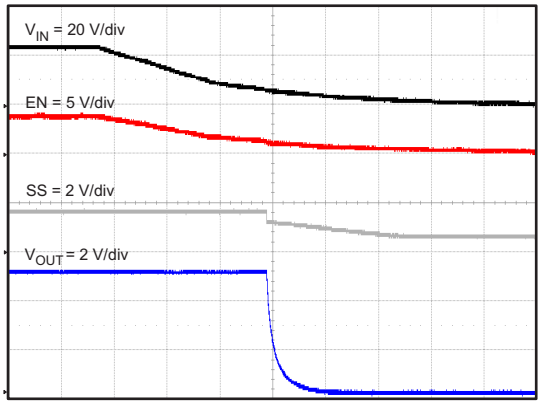


Figure 51. TPS54336 Shut Down Relative to VIN

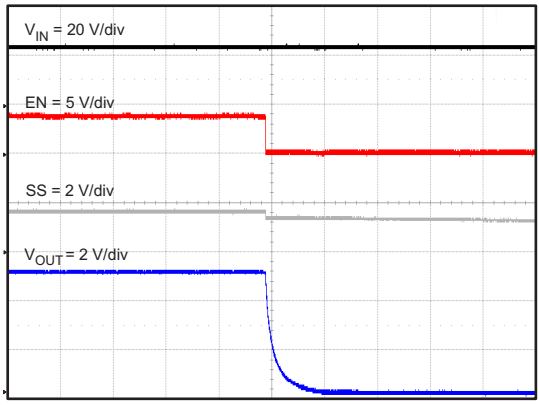
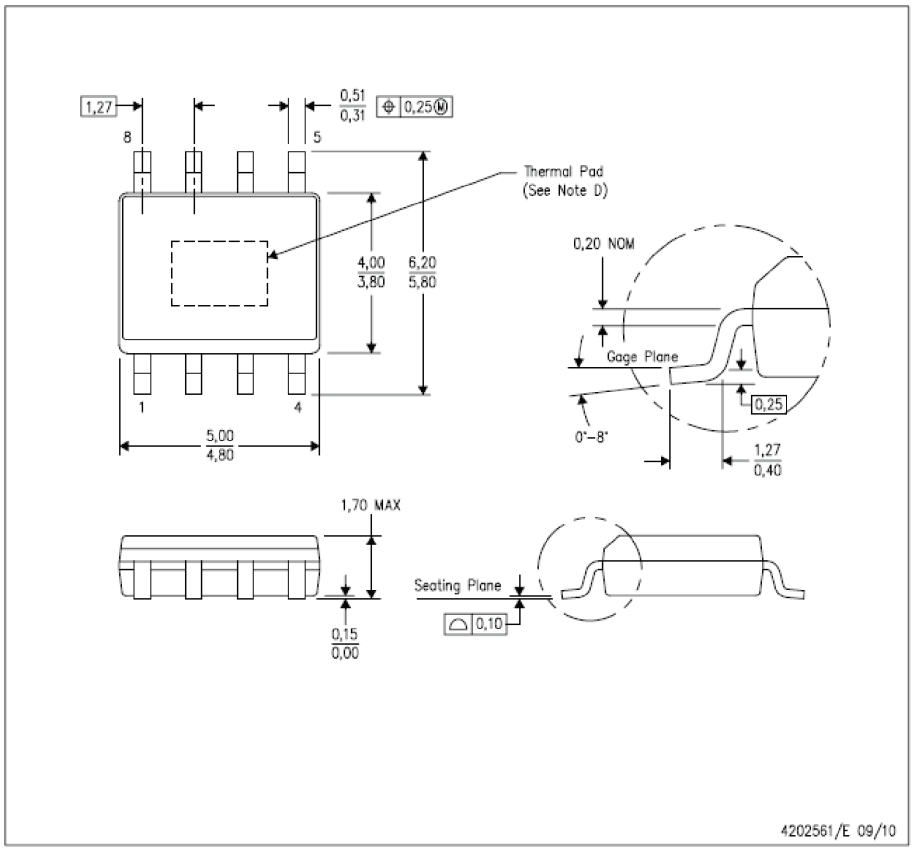


Figure 52. TPS54336 Shut Down Relative to EN

MECHANICAL PACKAGE DRAWING

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. This package complies to JEDEC MS–012 variation BA

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54335DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	54335	Samples
TPS54335DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	54335	Samples
TPS54336DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	54336	Samples
TPS54336DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	54336	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

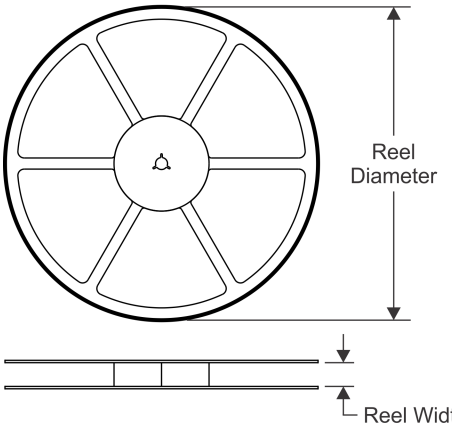
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

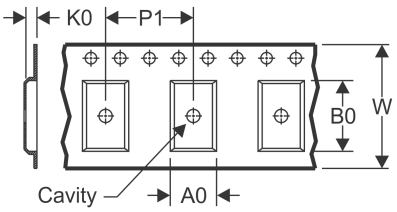
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

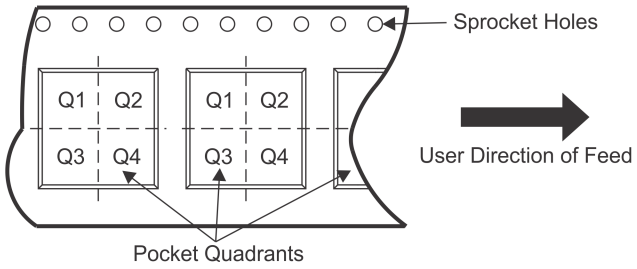


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

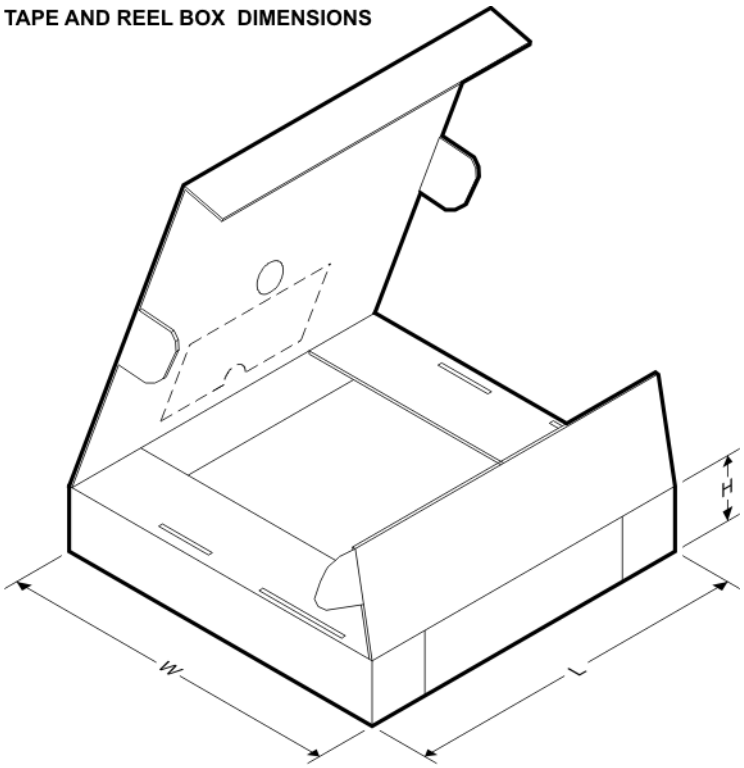
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54335DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS54336DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

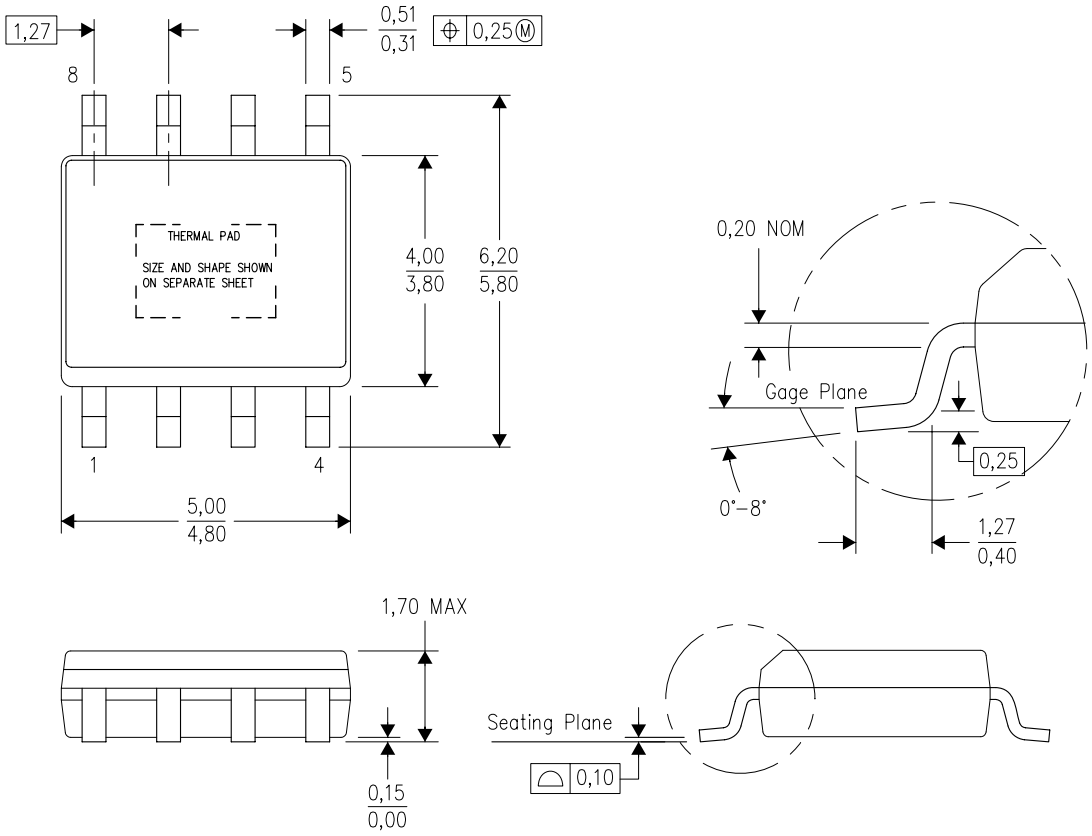
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54335DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TPS54336DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

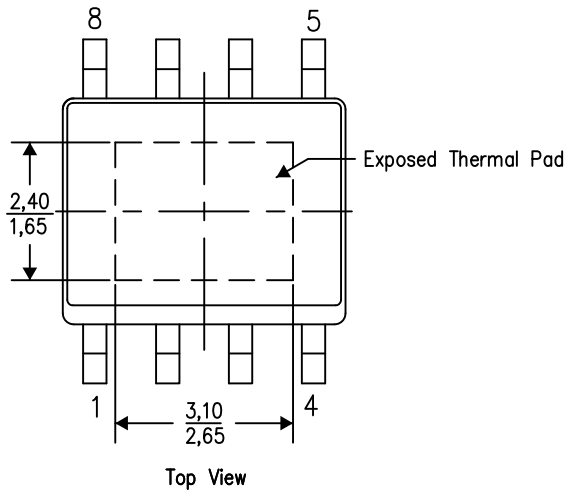
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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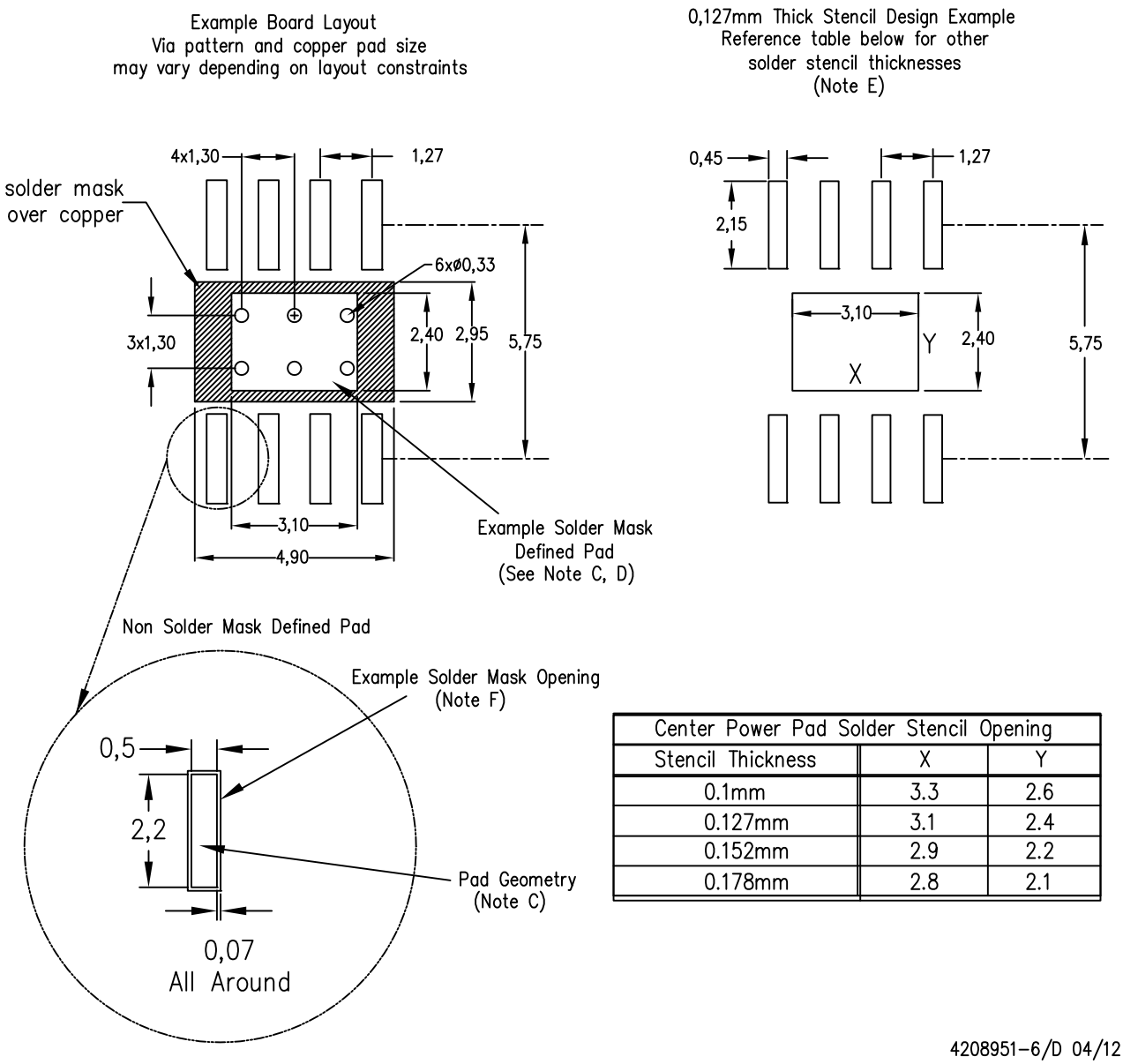
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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