TPS7A37 1% High-Accuracy, 1-A, Low-Dropout Regulator With Reverse Current Protection

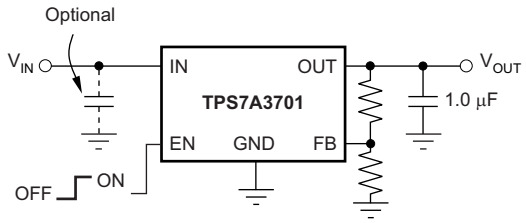
1 Features

- Stable with 1-µF or Larger Ceramic Output Capacitor
- Input Voltage Range: 2.2 V to 5.5 V
- Ultralow Dropout Voltage:
  - 200-mV Maximum at 1 A
- Excellent Load Transient Response—Even With Only 1-µF Output Capacitor
- NMOS Topology Delivers Low Reverse Leakage Current
- Excellent Accuracy:
  - 0.23% Nominal Accuracy
  - 1% Overall Accuracy Over Line, Over Load, and Over Temperature
- Less Than 20-nA typical I_Q in Shutdown Mode
- Thermal Shutdown and Current Limit for Fault Protection

2 Applications

- Point of Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors
- Post-Regulation for Switching Supplies
- Portable and Battery-Powered Equipment

Typical Application Circuit (Adjustable Version)



3 Description

The TPS7A37 family of linear low-dropout (LDO) voltage regulators uses an NMOS pass element in a voltage-follower configuration. This topology is relatively insensitive to output capacitor value and ESR, allowing a wide variety of load configurations. Load transient response is excellent, even with a small 1-µF ceramic output capacitor. The NMOS topology also allows very low dropout.

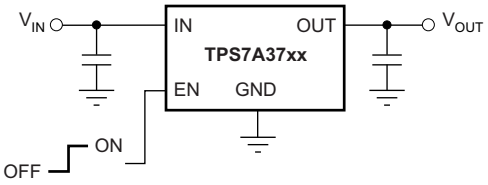
The TPS7A37 family uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 20 nA and ideal for portable applications. These devices are protected by thermal shutdown and foldback current limit.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A37	WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit (Fixed Version)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2013) to Revision B — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed Internal Reference (VFB) parameter typ value ... 5

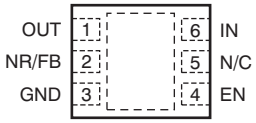
Changes from Original (March 2013) to Revision A — **Page**

- Changed device status to Production Data ... 1

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5 Pin Configuration and Functions

DRV Package
6-Pin WSON
Top View



Power dissipation may limit operating range. Check *Thermal Information* table.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	4	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to the *Shutdown* section under *Applications Information* for more details. EN must not be left floating and can be connected to IN if not used.
FB	2	I	Adjustable voltage version only—this pin is the input to the control loop error amplifier, and is used to set the output voltage of the device.
GND	3, Pad	—	Ground
IN	6	I	Unregulated input supply
N/C	5	—	Not connected
NR/FB	2	—	Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
OUT	1	O	Regulator output. A 1.0-µF or larger capacitor of any type is required for stability.
PowerPAD	—	—	

6 Specifications

6.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
Voltage	IN	–0.3	6	V
	EN	–0.3	6	V
	OUT	–0.3	5.5	V
	NR, FB	–0.3	6	V
Current	Peak output current	Internally limited		A
	Output short-circuit duration	Indefinite		A
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{IN}	2.2		5.5	V
V_{OUT}	V_{FB}		5.5 – V_{DO}	V
V_{EN}	0		V_{IN}	
I_{OUT}	0		1	A
C_{IN}		1		µF
C_{OUT} (1)	1			µF
C_{NR}		10		nF
R_1 (2)		$V_{OUT(nom)}$ × 15.833		kΩ
C_{FF}		10	100	nF

(1) If the product of COUT × ESR < 50 nΩ-F, the part may ring after a transient.
(2) This nominal value is for the best accuracy.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A37 DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	87.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 1 V(1), I_{OUT} = 10 mA, V_{EN} = 2.2 V, and C_{OUT} = 2.2 µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)(2)			2.2		5.5	V
V_{FB}	Internal reference		T_J = 25°C	1.192	1.204	1.216	V
V_{OUT}	Output voltage range		TPS7A3701(3)	V_{FB}		5.5 – V_{DO}	V
	Accuracy(1), (4)	Nominal	T_J = 25°C		0.23%		
		over V_{IN}, I_{OUT}, and T_J= –40°C to 125°C	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V; 10 mA ≤ I_{OUT} ≤ 1 A	–1%		+1.0%	
$\Delta V_{O(\Delta VI)}$	Line regulation(1)		$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V		0.01	0.03	%/V
$\Delta V_{O(\Delta IO)}$	Load regulation		0.1 mA ≤ I_{OUT} ≤ 300 mA		0.25%	0.35%	
					3	5	mV
			10 mA ≤ I_{OUT} ≤ 1 A		0.5%		
V_{DO}	Dropout voltage(5) (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)		I_{OUT} = 1 A		130	200	mV
Z_O(DO)	Output impedance in dropout		2.2 V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(nom)}$	1.05	1.6	2.2	A
I_{SC}	Short-circuit current		V_{OUT} = 0 V		450		mA
I_{REV}	Reverse leakage current(6) (–I_{IN})		V_{EN} ≤ 0.5 V, 0 V ≤ V_{IN} ≤ V_{OUT}		0.1		µA
I_{GND}	GND pin current		I_{OUT} = 10 mA (I_Q)		400		µA
			I_{OUT} = 1 A		1300		
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.5 V, V_{OUT} ≤ V_{IN} ≤ 5.5 V		20		nA
I_{FB}	FB pin current		TPS7A3701		0.1	0.6	µA
PSRR	Power-supply rejection ratio (ripple rejection)		f = 100 Hz, I_{OUT} = 1 A		58		dB
			f = 10 kHz, I_{OUT} = 1 A		37		
V_N	Output noise voltage BW = 10 Hz to 100 kHz		C_{OUT} = 10 µF		27 × V_{OUT}		μV_{RMS}
t_{STR}	Startup time		V_{OUT} = 3 V, R_L = 30 Ω, C_{OUT} = 1 µF		600		µs
$V_{EN(HI)}$	EN pin high (enabled)			1.7		V_{IN}	V
$V_{EN(LO)}$	EN pin low (shutdown)			0		0.5	V
$I_{EN(HI)}$	EN pin current (enabled)		V_{EN} = 5.5 V		20		nA
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		160		°C
			Reset, temperature decreasing		140		
T_J	Operating junction temperature			–40		125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.2 V, whichever is greater.
(2) For $V_{OUT(nom)}$ < 1.6 V, when V_{IN} ≤ 1.6 V, the output will lock to V_{IN} and may result in an over-voltage condition on the output. To avoid this situation, disable the device before powering down V_{IN}.
(3) TPS7A3701 is tested at V_{OUT} = 1.2 V.
(4) Tolerance of external resistors not included in this specification.
(5) V_{DO} is not measured for fixed output versions with $V_{OUT(nom)}$ < 2.3 V since minimum V_{IN} = 2.2 V.
(6) Fixed-voltage versions only; refer to the *Application Information* section for more information.

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6.6 Typical Characteristics

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 10 mA, V_{EN} = 2.2 V, and C_{OUT} = 2.2 µF, unless otherwise noted.

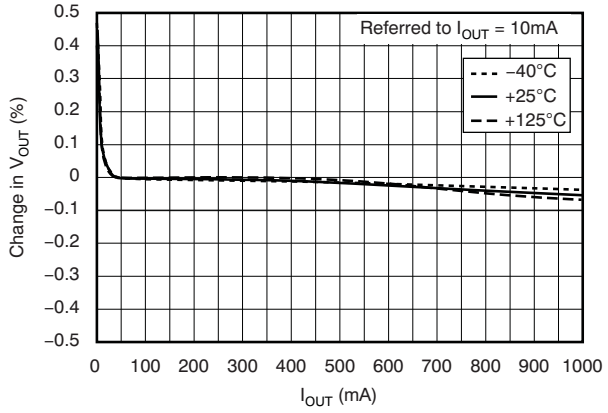


Figure 1. Load Regulation

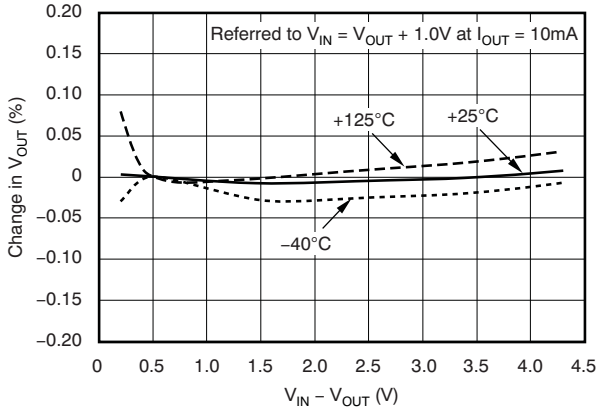


Figure 2. Line Regulation

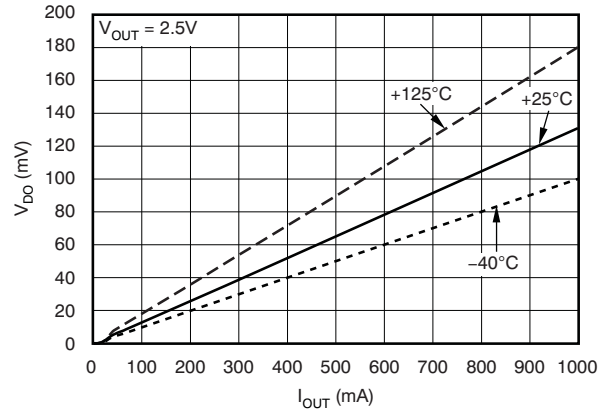


Figure 3. Dropout Voltage vs Output Current

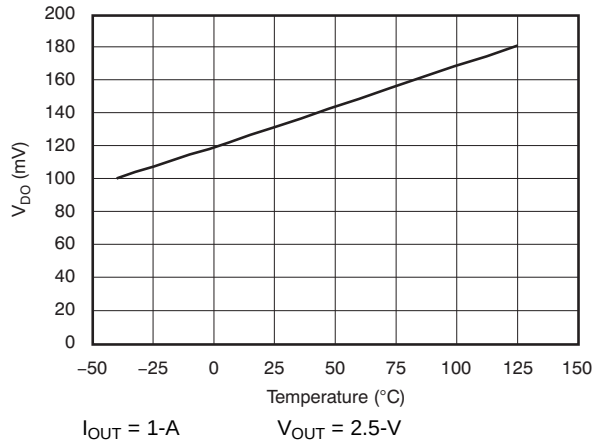


Figure 4. Dropout Voltage vs Temperature

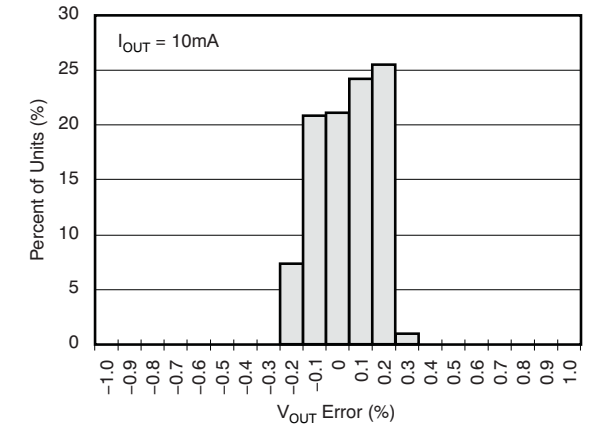


Figure 5. Output Voltage Histogram

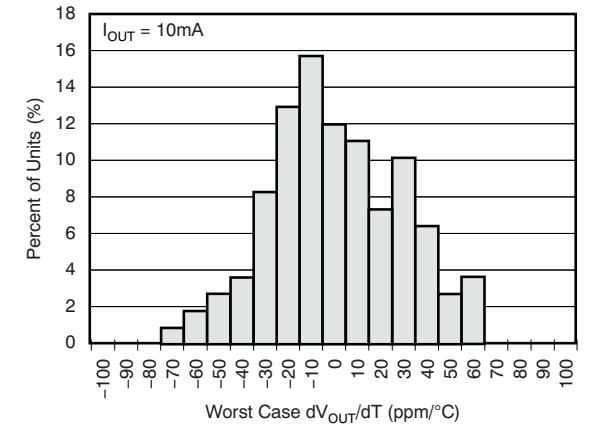


Figure 6. Output Voltage Drift Histogram

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Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 10 mA, V_{EN} = 2.2 V, and C_{OUT} = 2.2 µF, unless otherwise noted.

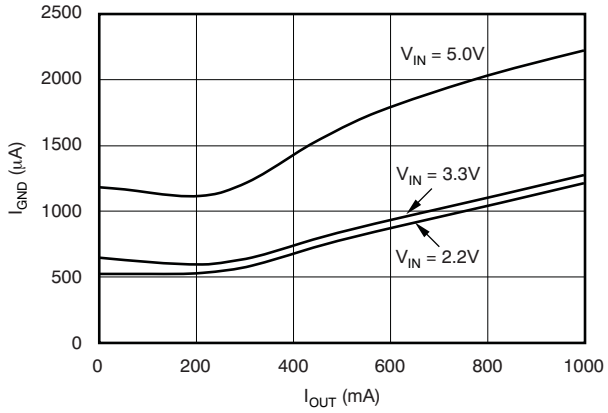


Figure 7. Ground Pin Current vs Output Current

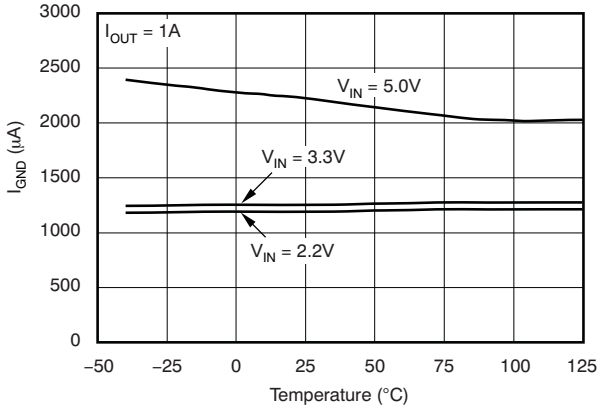


Figure 8. Ground Pin Current vs Temperature

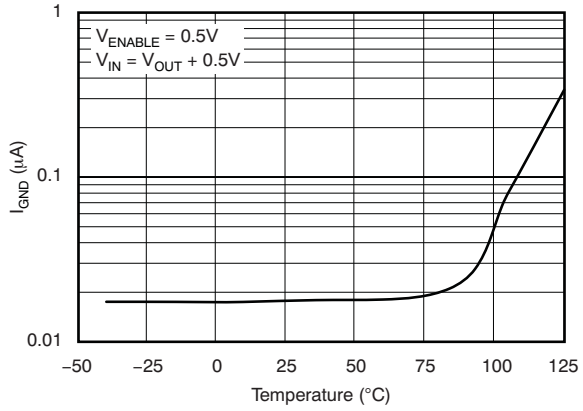


Figure 9. Ground Pin Current in Shutdown vs Temperature

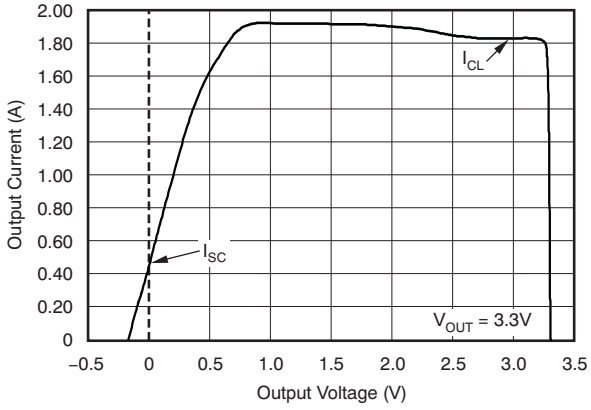


Figure 10. Current Limit vs V_{OUT} (Foldback)

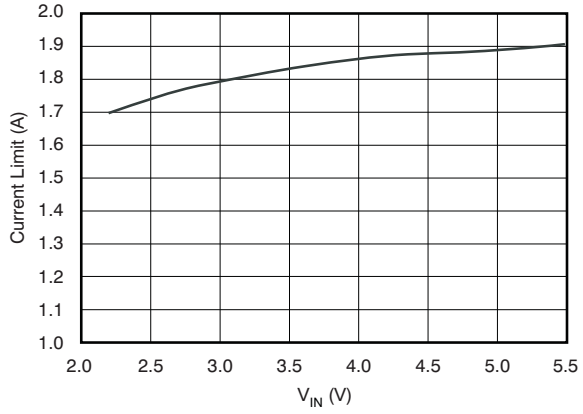


Figure 11. Current Limit vs V_{IN}

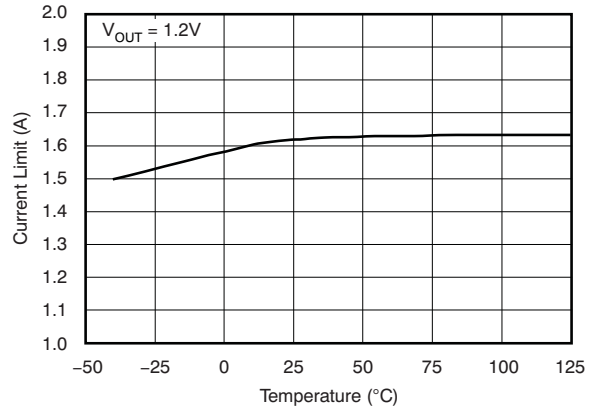


Figure 12. Current Limit vs Temperature

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Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 10 mA, V_{EN} = 2.2 V, and C_{OUT} = 2.2 µF, unless otherwise noted.

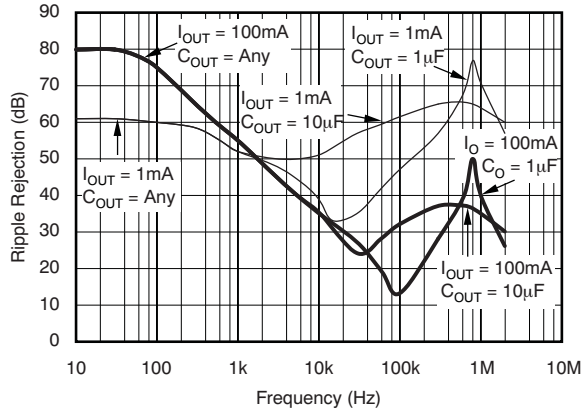


Figure 13. PSRR (Ripple Rejection) vs Frequency

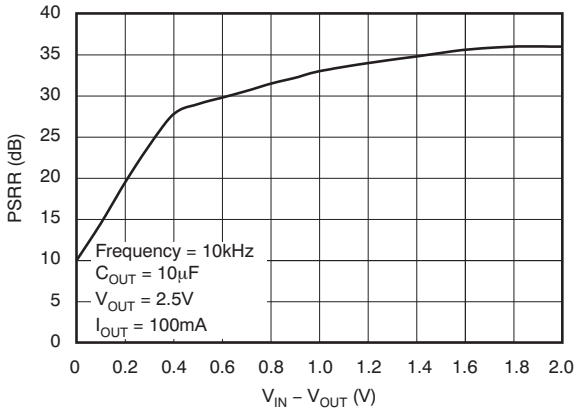


Figure 14. PSRR (Ripple Rejection) vs V_{IN} – V_{OUT}

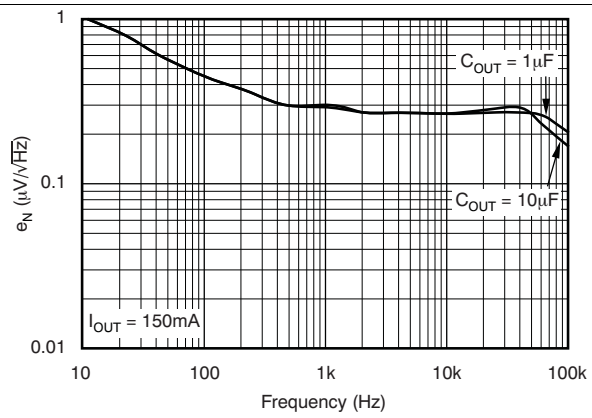


Figure 15. Noise Spectral Density

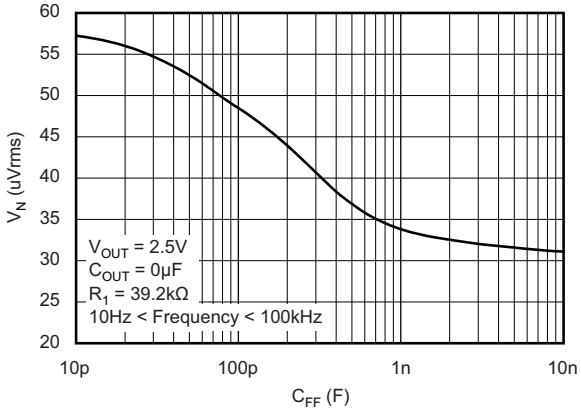


Figure 16. TPS7A3701: RMS Noise Voltage vs C_{FF}

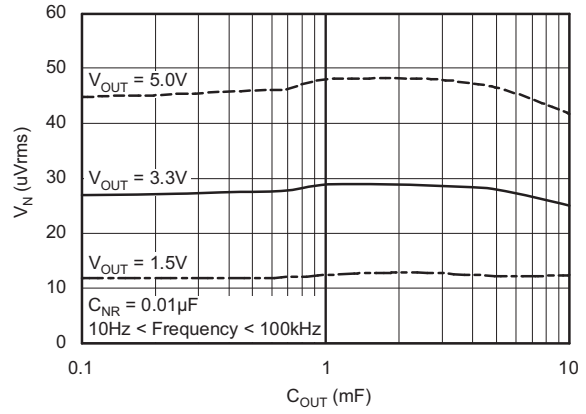


Figure 17. RMS Noise Voltage vs C_{OUT}

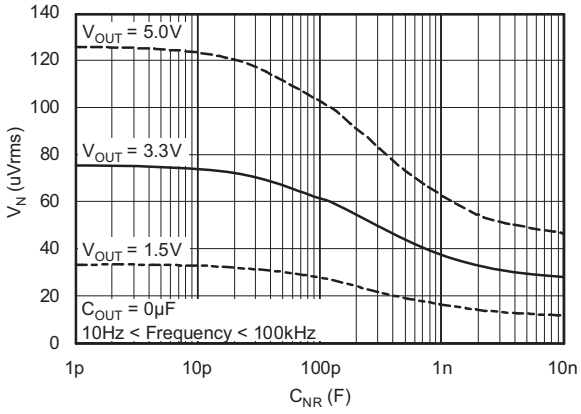
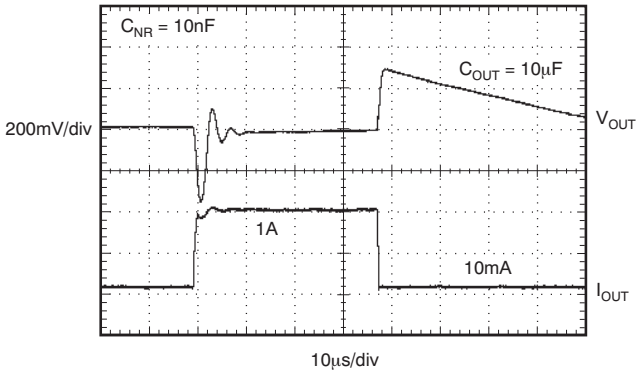


Figure 18. RMS Noise Voltage vs C_{NR}

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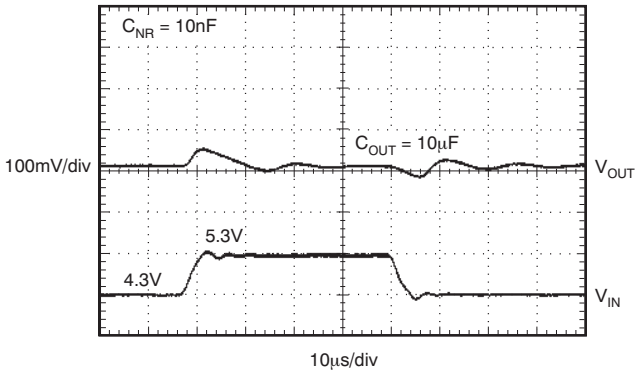
Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 10 mA, V_{EN} = 2.2 V, and C_{OUT} = 2.2 µF, unless otherwise noted.



V_{OUT} = 3.3V

Figure 19. TPS7A3701: Load Transient Response



V_{OUT} = 3.3V

Figure 20. TPS7A3701: Line Transient Response

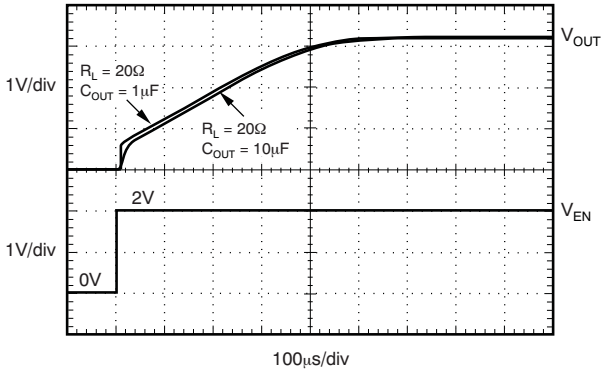


Figure 21. TPS7A3701: Turn-on Response

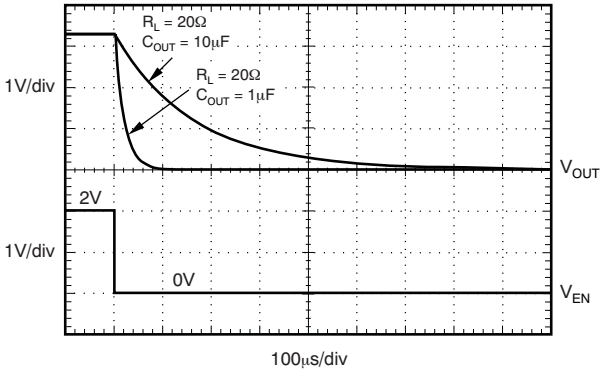


Figure 22. TPS7A3701: Turn-off Response

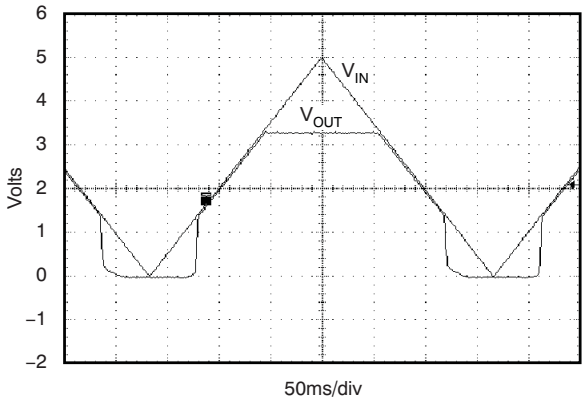


Figure 23. TPS7A3701: Power-up/Power-down (V_{OUT} = 3.3 V)

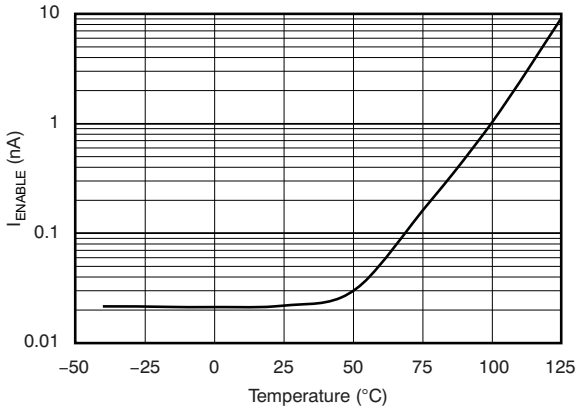


Figure 24. I_{ENABLE} vs Temperature

Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 10 mA, V_{EN} = 2.2 V, and C_{OUT} = 2.2 µF, unless otherwise noted.

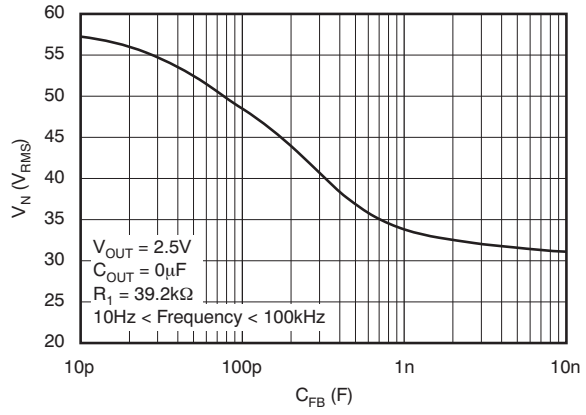


Figure 25. TPS7A3701: RMS Noise Voltage vs C_{FB}

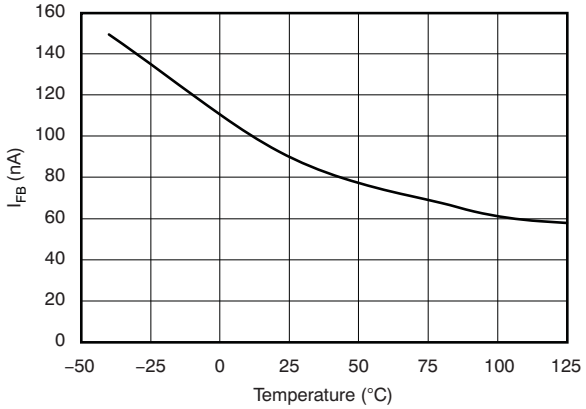


Figure 26. TPS7A3701: I_{FB} vs Temperature

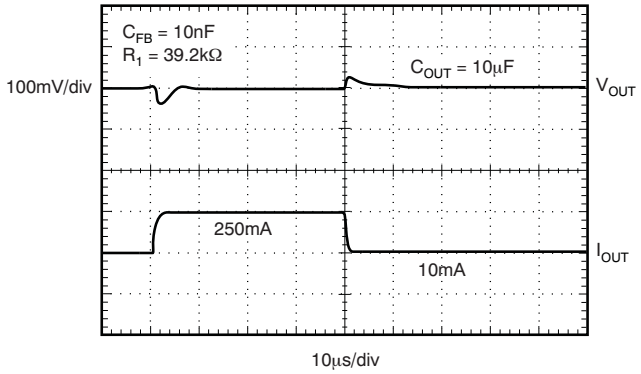


Figure 27. TPS7A3701: Load Transient, Adjustable Version

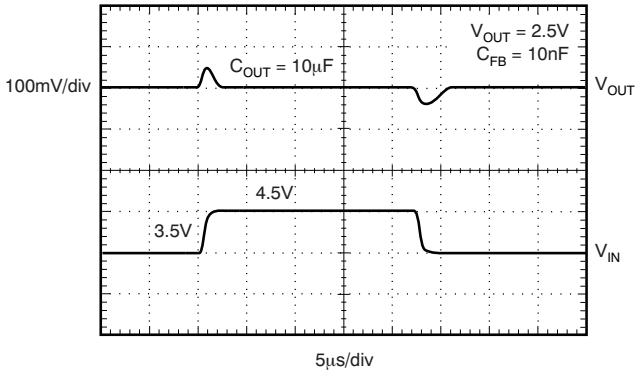


Figure 28. TPS7A3701: Line Transient, Adjustable Version

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7 Detailed Description

7.1 Overview

The TPS7A37 belongs to a family of LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance and reverse current protection. These features combined with an enable input make the TPS7A37 ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

7.2 Functional Block Diagrams

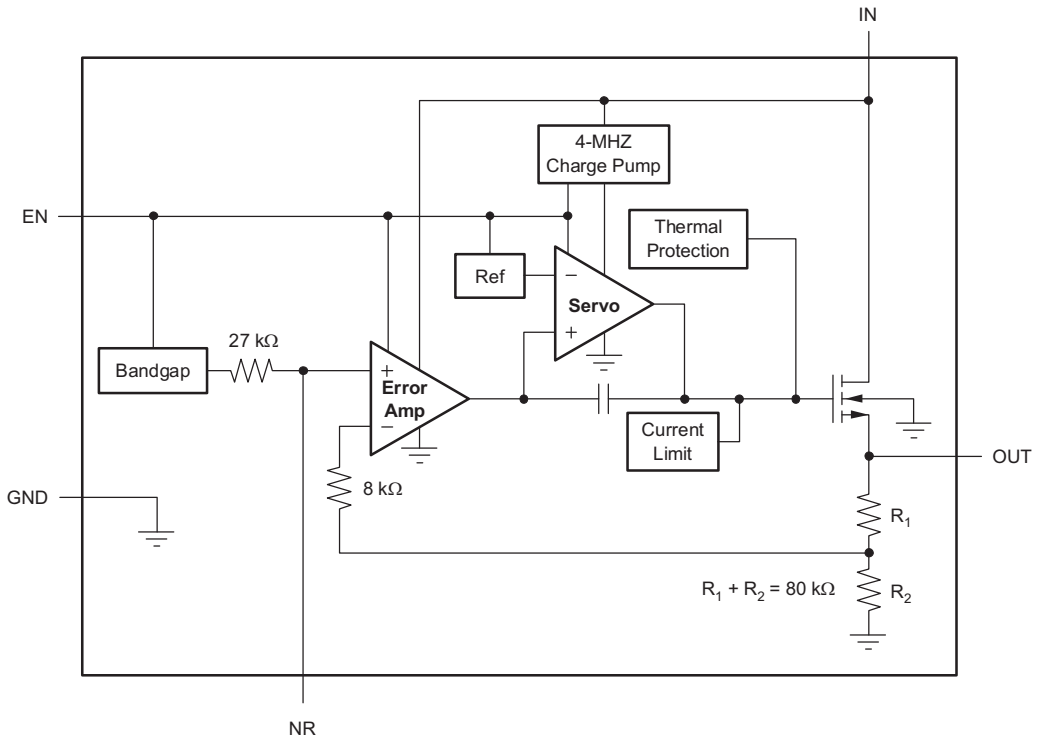
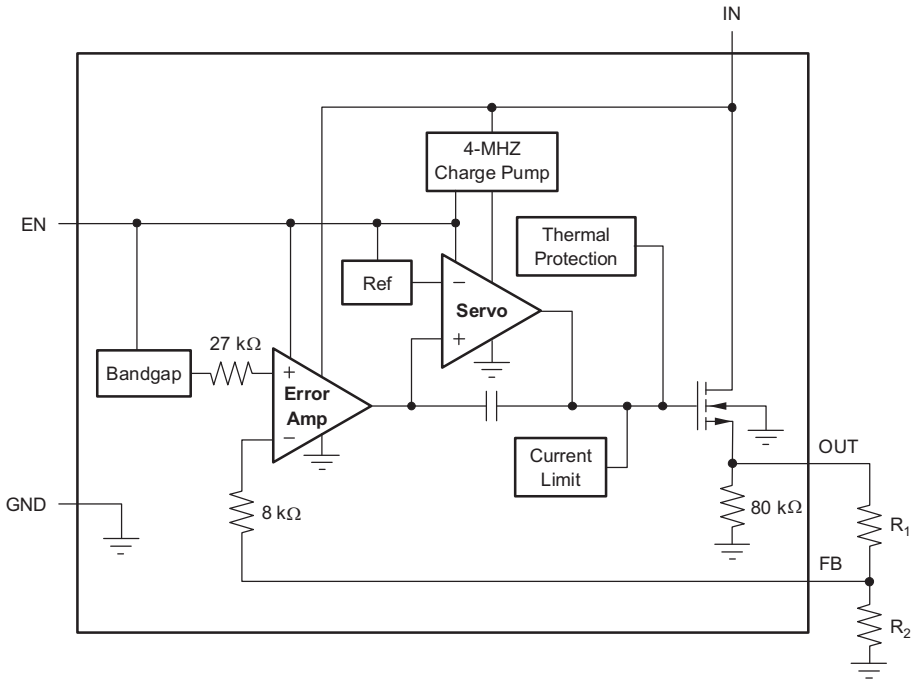


Figure 29. Fixed Voltage Version

Functional Block Diagrams (continued)



Standard 1% Resistor Values for Common Output Voltages

V_O	R_1	R_2
1.2 V	Short	Open
1.5 V	23.2 kΩ	95.3 kΩ
1.8 V	28.0 kΩ	56.2 kΩ
2.5 V	39.2 kΩ	36.5 kΩ
2.8 V	44.2 kΩ	33.2 kΩ
3.0 V	46.4 kΩ	30.9 kΩ
3.3 V	52.3 kΩ	30.1 kΩ

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$; $R_1 \parallel R_2 \cong 19\ k\Omega$ for best accuracy.

Figure 30. Adjustable Voltage Version

7.3 Feature Description

7.3.1 Internal Current Limit

The TPS7A37 internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5 V. See Figure 10 in the *Typical Characteristics* section.

Note from Figure 10 that approximately –0.2 V of V_{OUT} results in a current limit of 0 mA. Therefore, if OUT is forced below –0.2 V before EN goes high, the device may not start up. In applications that work with both a positive and negative voltage supply, the TPS7A37 should be enabled first.

7.3.2 Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A V_{EN} below 0.5 V (max) turns the regulator off and drops the GND pin current to approximately 10 nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate, and the output ramps back up to a regulated V_{OUT} (see Figure 21).

When shutdown capability is not required, EN can be connected to V_{IN}. However, the pass gate may not be discharged using this configuration, and the pass transistor may be left on (enhanced) for a significant time after V_{IN} has been removed. This scenario can result in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power-up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output may overshoot upon power-up.

Note that current limit foldback can prevent device start-up under some conditions. See the *Internal Current Limit* section for more information.

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Feature Description (continued)

7.3.3 Reverse Current

The NMOS pass element of the TPS7A37 provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the EN pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on because of stored charge on the gate.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin because of voltage applied on the OUT pin. There will be additional current flowing into the OUT pin as a result of the 80-kΩ internal resistor divider to ground (see Figure 29 and Figure 30).

For the TPS7A3701, reverse current may flow when V_{FB} is more than 1.0 V above V_{IN}.

7.4 Device Functional Modes

Driving the EN pin over 1.7 V turns on the regulator. Driving the EN pin below 0.5 V causes the regulator to enter shutdown mode. In shutdown, the current consumption of the device is reduced to 20 nA, typically.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability if input impedance is very low, it is good analog design practice to connect a 0.1-µF to 1-µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS7A37 requires a 1-µF output capacitor for stability. It is designed to be stable for all available types and values of capacitors. In applications where multiple low ESR capacitors are in parallel, ringing may occur when C_{OUT} × ESR < 50 nΩ-F. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance will meet this requirement.

8.1.2 Output Noise

A precision bandgap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS7A37 and it generates approximately 32 μV_{RMS} (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Since the value of V_{REF} is 1.2V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (2)$$

for the case of no C_{NR}.

An internal 27-kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10 nF, the total noise in the 10-Hz to 100-kHz bandwidth is reduced by a factor of ~3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) x\ V_{OUT}(V) \quad (3)$$

for C_{NR} = 10 nF.

This noise reduction effect is shown as RMS Noise Voltage vs C_{NR} in the *Typical Characteristics* section.

The TPS7A3701 adjustable version does not have the NR pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the feedback pin (FB) reduces output noise and improve load transient performance. This capacitor should be limited to 0.1 µF.

The TPS7A37 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates ~250 µV of switching noise at ~4 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

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Application Information (continued)

8.1.3 Dropout Voltage

The TPS7A37 uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS, ON}$ of the NMOS pass element.

For large step changes in load current, the TPS7A37 requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of V_{IN} – V_{OUT} above this line ensure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to dc dropout levels], the TPS7A37 can take a couple of hundred microseconds to return to the specified regulation accuracy.

8.1.4 Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without a 1.0-µF output capacitor. As with any regulator, the addition of additional capacitance from the OUT pin to ground reduces undershoot magnitude but increases its duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the OUT pin to the FB pin will also improve the transient response.

The TPS7A37 does not have active pull-down when the output is over-voltage. This architecture allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This architecture also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal/external load resistance. The rate of decay is given by:

(Fixed voltage version)

$$\frac{dV}{dT} = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}} \quad (4)$$

(Adjustable voltage version)

$$\frac{dV}{dT} = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \quad (5)$$

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8.2 Typical Applications

8.2.1 Typical Application Schematic

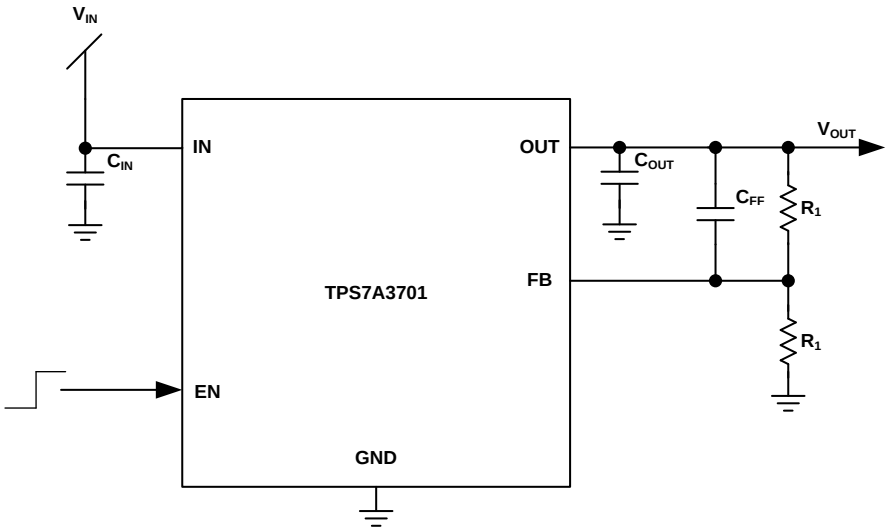


Figure 31. Typical Application Schematic

8.2.1.1 Design Requirements

Table 1 lists the design parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.6 V
Output voltage	3.3 V
DC output current	100 mA
Peak output current	1 A

8.2.1.2 Detailed Design Procedure

Due to the transients in this application input and output capacitors should be used. A C_{IN} = C_{OUT} = 10-uF capacitor has been selected.

The ESR of the chosen capacitor can be checked by looking the magnitude of the complex impedance over frequency. When |Zc| reaches a minimum the DC ESR is the value of |Zc| at that frequency. The ESR of the chosen capacitor is 10 mΩ, which gives us a product of 10 mΩ * 10 uF = 100 nΩ-F > 50 nΩ-F, minimizing the ringing during transients.

As the V_{IN} - V_{OUT} change is only 300 mV with a 100-mA DC current, the expected junction temperature rise over the ambient, on a JEDEC standard board, is 67.2 C/W × 0.3V × 0.1 A = 2 C.

To ensure best accuracy, R1 = 52.3 kΩ and R2 = 30.1 kΩ, and a 10-nF C_{FF} is used to reduce output noise.

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8.2.1.3 Application Curves

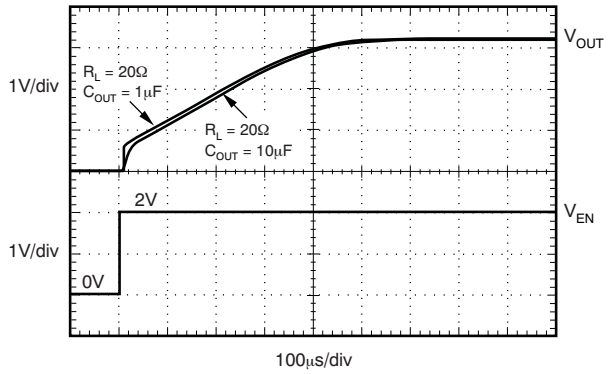


Figure 32. TPS7A3701: Turn-on Response

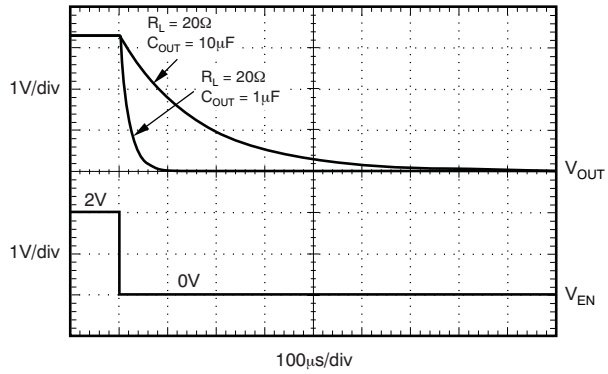


Figure 33. TPS7A3701: Turn-off Response

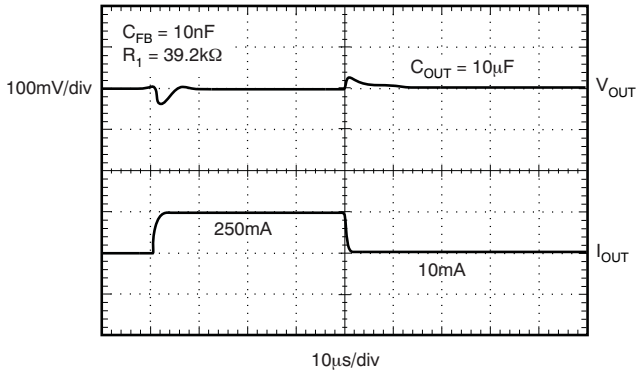


Figure 34. TPS7A3701: Load Transient, Adjustable Version

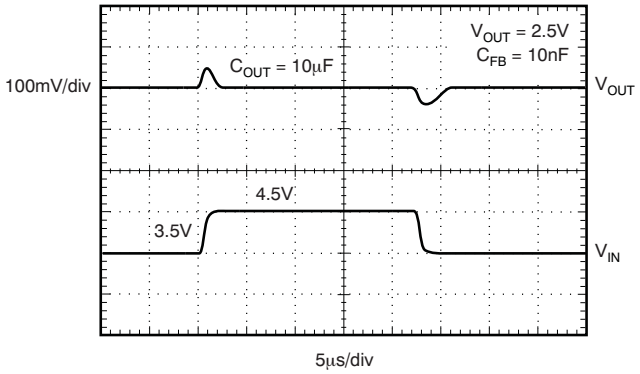


Figure 35. TPS7A3701: Line Transient, Adjustable Version

8.2.2 Fixed-Voltage Version

Figure 36 shows the basic circuit connections for the fixed voltage models.

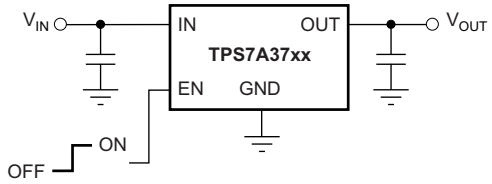


Figure 36. Typical Application Circuit for Fixed-Voltage Version

8.2.3 Adjustable Operation

Figure 37 gives the connections for the adjustable output version, TPS7A3701 .

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 37. Sample resistor values for common output voltages are shown in Figure 30.

For best accuracy, make the parallel combination of R_1 and R_2 approximately equal to 19 kΩ. This 19 kΩ, in addition to the internal 8-kΩ resistor, presents the same impedance to the error amp as the 27-kΩ bandgap reference output. This impedance helps compensate for leakages into the error amp terminals.

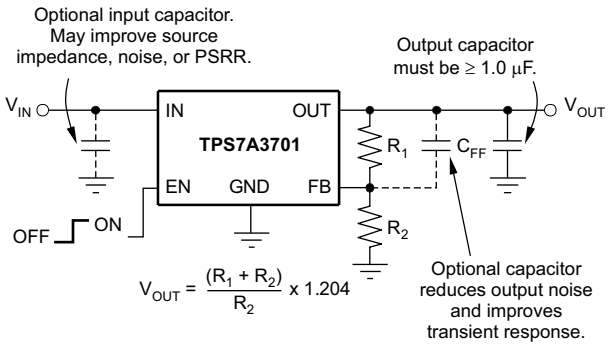


Figure 37. Typical Application Circuit for Adjustable-Voltage Version(1)

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9 Power Supply Recommendations

The input supply for the LDO must be within its recommended operating conditions (that is, between 2.2 V to 5.5 V). The input voltage must provide adequate headroom in order for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output transient performance.

10 Layout

10.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

The GND pin should be tied directly to the PowerPAD under the IC. The PowerPAD should be connected to any internal PCB ground planes using multiple vias directly under the IC.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits may impact system performance negatively, and even cause instability.

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance (such as PSRR, output noise, and transient response), TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane star connected only at the GND pin of the device.

10.2 Layout Example

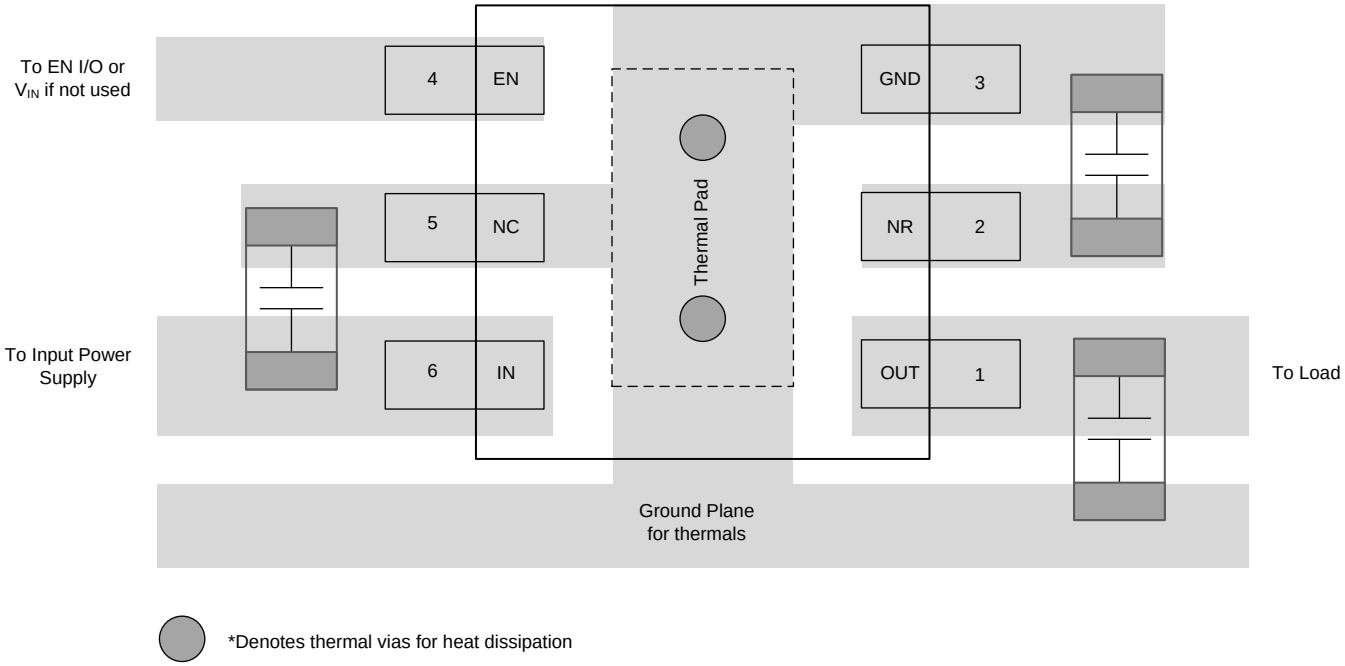


Figure 38. Fixed Voltage Layout

Layout Example (continued)

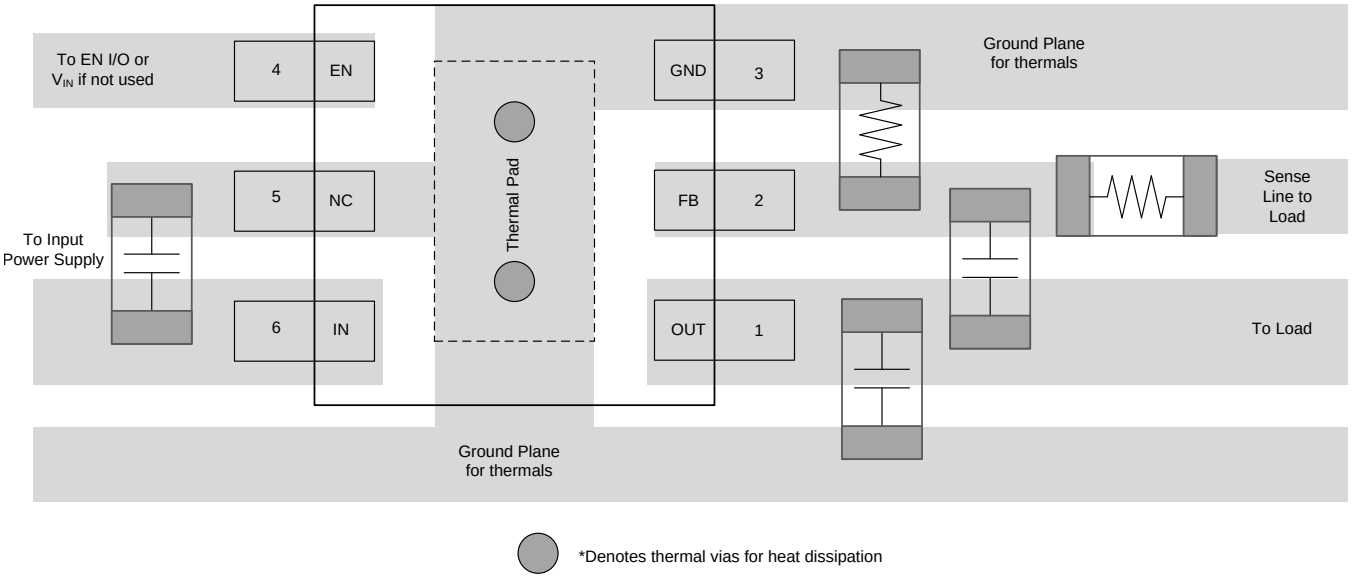


Figure 39. Adjustable Voltage Layout

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A37 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A37 into thermal shutdown degrades device reliability.

10.4 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 6:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

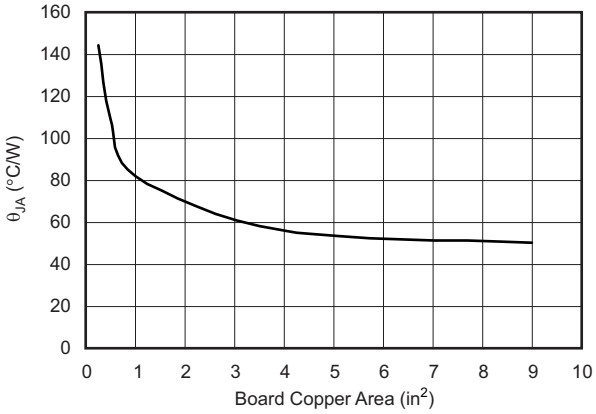
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Power Dissipation (continued)

On the WSON (DRV) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. That tab should be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 7:

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \tag{7}$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 40.



Note: θ_{JA} value at board size of $9in^2$ (that is, 3in × 3in) is a JEDEC standard.

Figure 40. DRV (WSON) Package θ_{JA} vs Board Size

Figure 40 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

NOTE

When the device is mounted on an application PCB, it is strongly recommended to use Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

10.5 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 8). For backwards compatibility, an older $\theta_{JC,Top}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{8}$$

Where P_D is the power dissipation shown by Equation 6, T_T is the temperature at the center-top of the IC package, and T_B is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (as Figure 42 shows).

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

Estimating Junction Temperature (continued)

For more information about measuring T_T and T_B, see the application note SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com.

By looking at Figure 41, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 8 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

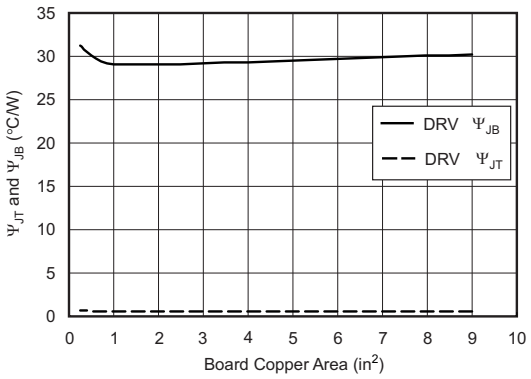
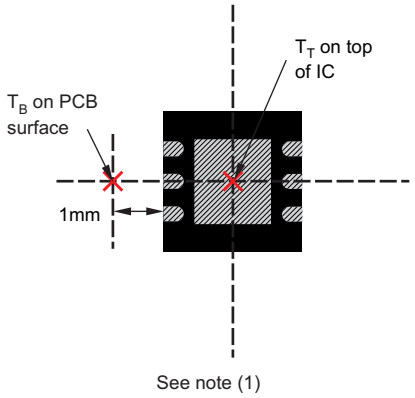


Figure 41. DRV (WSON) Package Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, refer to application report SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com. For further information, refer to application report SPRA953, *Semiconductor and IC Package Thermal Metrics*, also available on the TI website.



(1) Power dissipation may limit operating range. Check *Thermal Information* table.

(2) Example DRV (SON) Package Measurement

Figure 42. Measuring Points for T_T and T_B

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- *Using New Thermal Metrics*, SBVA025
- *TPS7A37xxEVM-529 Evaluation Module*, SLVU850

11.1.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A3701DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJI	Samples
TPS7A3701DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJI	Samples
TPS7A3721DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIX	Samples
TPS7A3721DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIX	Samples
TPS7A3725DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJH	Samples
TPS7A3725DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

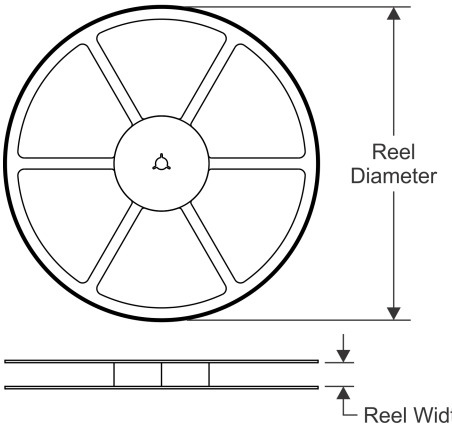
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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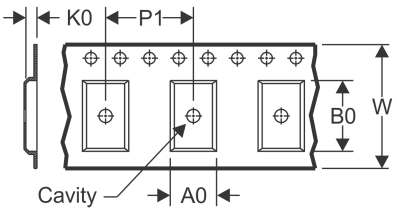
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

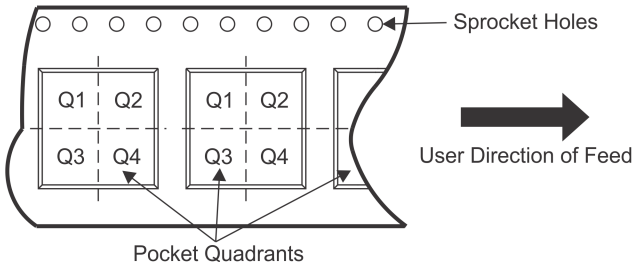


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

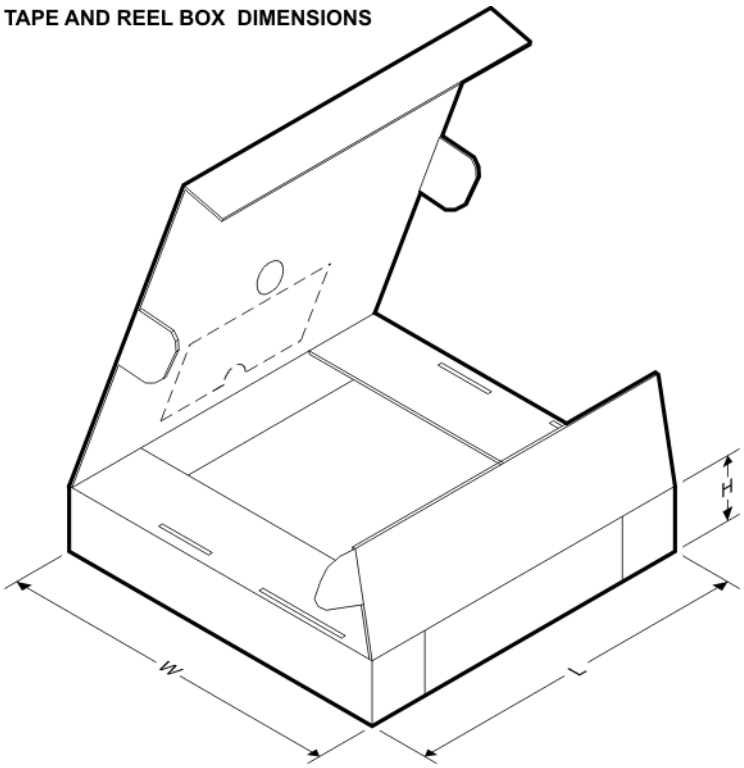
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A3701DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS7A3701DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS7A3721DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS7A3721DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS7A3725DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS7A3725DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

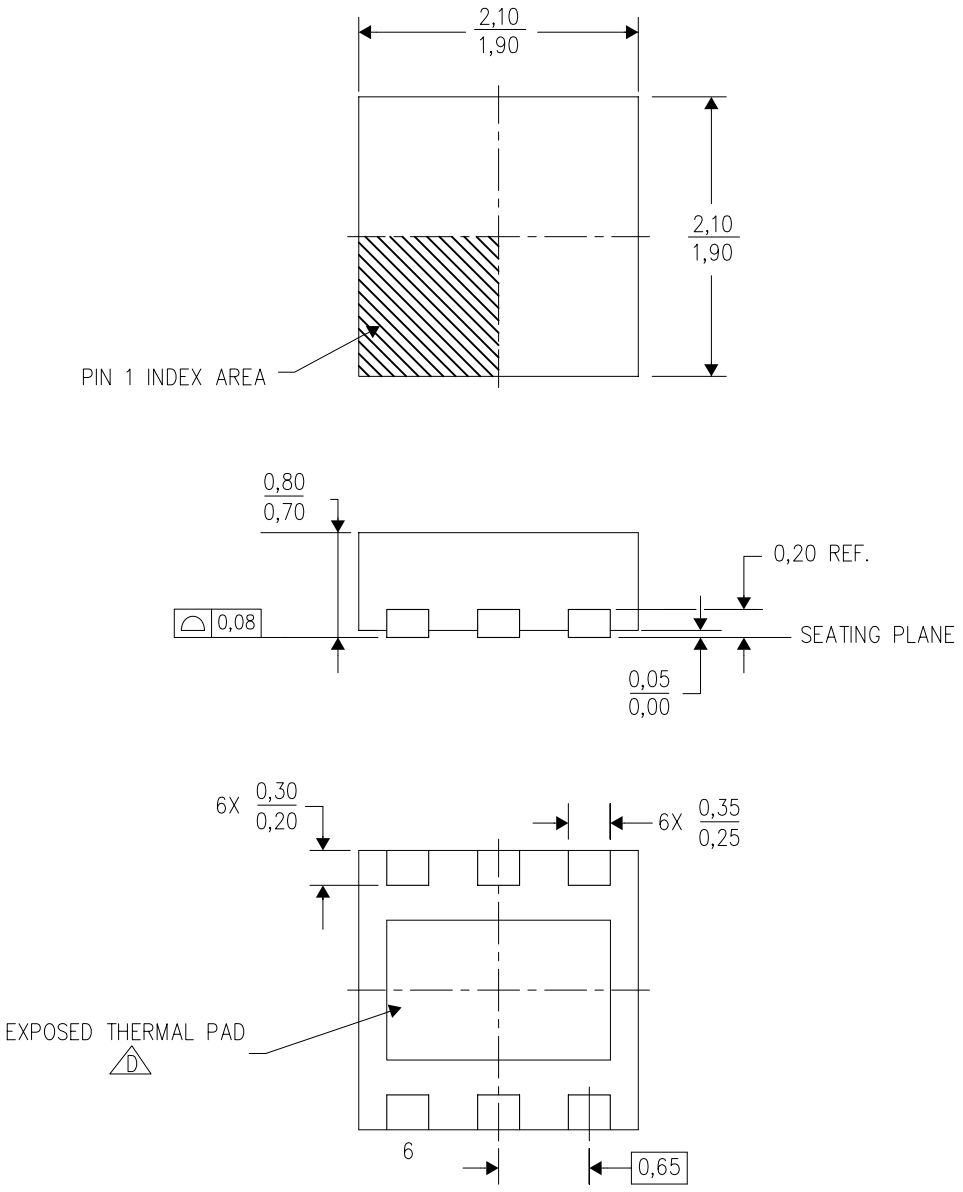
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A3701DRVR	WSON	DRV	6	3000	195.0	200.0	45.0
TPS7A3701DRVT	WSON	DRV	6	250	195.0	200.0	45.0
TPS7A3721DRVR	WSON	DRV	6	3000	195.0	200.0	45.0
TPS7A3721DRVT	WSON	DRV	6	250	195.0	200.0	45.0
TPS7A3725DRVR	WSON	DRV	6	3000	195.0	200.0	45.0
TPS7A3725DRVT	WSON	DRV	6	250	195.0	200.0	45.0

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

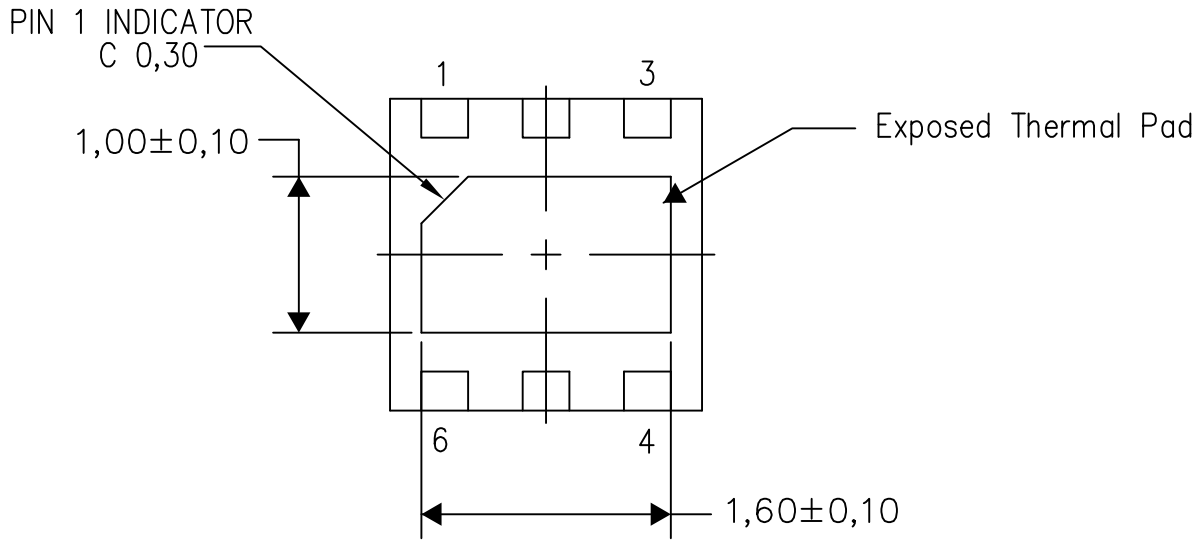
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



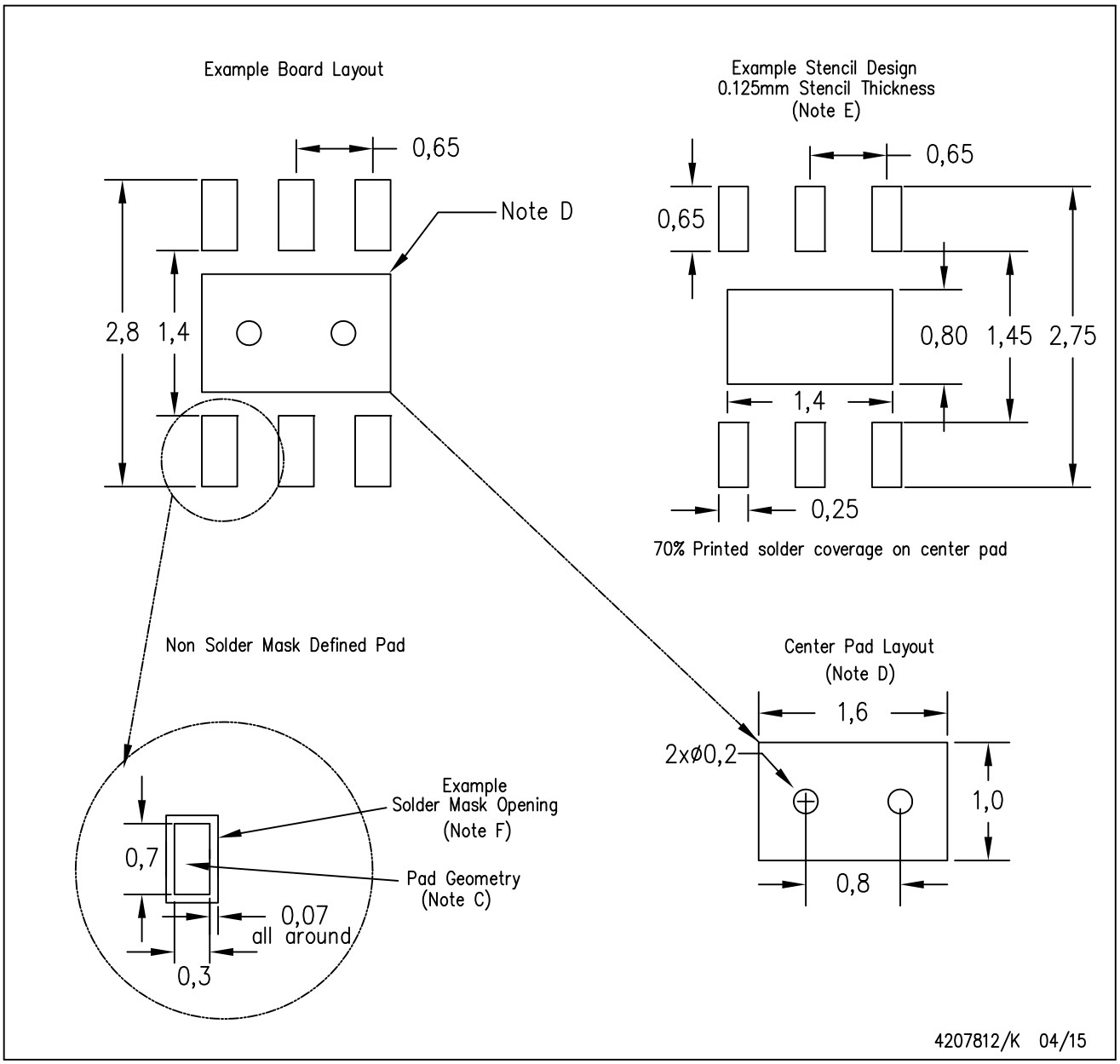
Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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