19-3430; Rev 0; 10/04

EVALUATION KIT AVAILABLE

Triple-Output TFT-LCD DC-DC Converters

General Description

The MAX1748/MAX8726 triple-output DC-DC converters in a low-profile TSSOP package provide the regulated voltages required by active-matrix, thin-film transistor (TFT) liquid-crystal displays (LCDs). One high-power DC-DC converter and two low-power charge pumps convert the +3.3V to +5V input supply voltage into three independent output voltages.

The primary 1MHz DC-DC converter generates a boosted output voltage (V_{MAIN}) up to 13V using ultra-small inductors and ceramic capacitors. The low-power BiCMOS control circuitry and the low on-resistance (0.35Ω) of the integrated power MOSFET allows efficiency up to 93%.

The dual charge pumps independently regulate one positive output (V_{POS}) and one negative output (V_{NEG}). These low-power outputs use external diode and capacitor stages (as many stages as required) to regulate output voltages up to +40V and down to -40V. A proprietary regulation algorithm minimizes output ripple, as well as capacitor sizes for both charge pumps.

For both the MAX1748 and MAX8726, the supply sequence is V_{MAIN} first, V_{NEG} next, and finally V_{POS}. The MAX1748 soft-starts each supply as soon as the previous supply finishes. The MAX8726 adds a delay between the startups of V_{MAIN} and V_{NEG} and also between V_{NEG} and V_{POS}.

The MAX1748/MAX8726 are available in the ultra-thin TSSOP package (1.1mm max height).

Applications

TFT Active-Matrix LCD Displays

Passive-Matrix LCD Displays

PDAs

Digital Still Cameras

Camcorders

Typical Operating Circuit appears at end of data sheet.

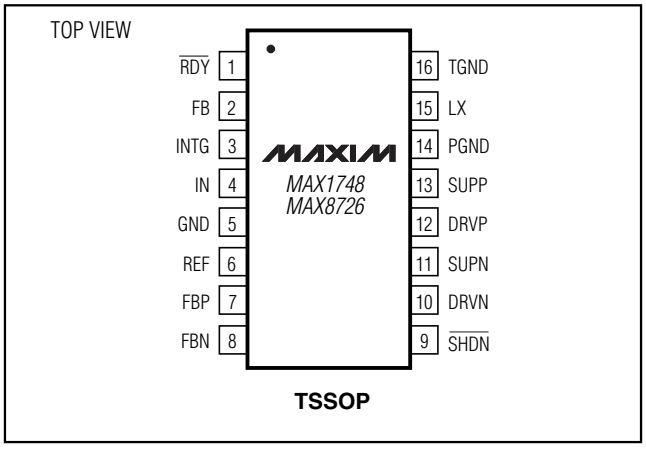
Features

- **Three Integrated DC-DC Converters**
- **1MHz Current-Mode PWM Boost Regulator**
  - **Up to +13V Main High-Power Output**
  - **±1% Accuracy**
  - **High Efficiency (93%)**
- **Dual Charge-Pump Outputs**
  - **Up to +40V Positive Charge-Pump Output**
  - **Down to -40V Negative Charge-Pump Output**
- **Internal Supply Sequencing**
- **Internal Power MOSFETs**
- **+2.7V to +5.5V Input Supply**
- **0.1µA Shutdown Current**
- **0.6mA Quiescent Current**
- **Internal Soft-Start**
- **Power-Ready Output**
- **Ultra-Small External Components**
- **Thin TSSOP Package (1.1mm max)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1748EUE	-40°C to +85°C	16 TSSOP
MAX8726EUE	-40°C to +85°C	16 TSSOP

Pin Configuration



For free samples and the latest literature, visit www.maxim-ic.com or phone 1-800-998-8800.
For small orders, phone 1-800-835-8769.

Triple-Output TFT-LCD DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDN}$, TGND to GND .....-0.3V to +6V
DRVN to GND .....-0.3V to (V_{SUPN} + 0.3V)
DRVP to GND .....-0.3V to (V_{SUPP} + 0.3V)
PGND to GND .....±0.3V
$\overline{RDY}$ to GND .....-0.3V to +14V
LX, SUPP, SUPN to PGND .....-0.3V to +14V
INTG, REF, FB, FBN, FBP to GND .....-0.3V to (V_{IN} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP (derate 9.4mW/°C above +70°C) 755mW
Operating Temperature Range
MAX1748EUE/MAX8726EUE .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = 10V, TGND = PGND = GND, C_{REF} = 0.22µF, C_{INTG} = 470pF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range	V_{IN}		2.7		5.5	V
Input Undervoltage Threshold	V_{UVLO}	V_{IN} rising, 40mV hysteresis (typ)	2.2	2.4	2.6	V
IN Quiescent Supply Current	I_{IN}	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = -0.2V		0.6	1	mA
SUPP Quiescent Current	I_{SUPP}	V_{FBP} = 1.5V		0.4	0.8	mA
SUPN Quiescent Current	I_{SUPN}	V_{FBN} = -0.1V		0.4	0.8	mA
IN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{IN} = 5V		0.1	10	µA
SUPP Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPP} = 13V		0.1	10	µA
SUPN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPN} = 13V		0.1	10	µA
MAIN BOOST CONVERTER						
Output Voltage Range	V_{MAIN}		V_{IN}		13	V
FB Regulation Voltage	V_{FB}	T_A = 0°C to +85°C	1.235	1.248	1.261	V
FB Input Bias Current	I_{FB}	V_{FB} = 1.25V, INTG = GND	-50		+50	nA
Operating Frequency	f_{OSC}		0.85	1	1.15	MHz
Oscillator Maximum Duty Cycle			78	85	90	%
Load Regulation		I_{MAIN} = 0 to 200mA, V_{MAIN} = 10V		0.2		%
Line Regulation				0.1		%/V
Integrator Gm				320		µmho
LX Switch On-Resistance	$R_{LX(ON)}$	I_{LX} = 100mA		0.35	0.7	Ω
LX Leakage Current	I_{LX}	V_{LX} = 13V		0.01	20	µA
LX Current Limit	$I_{LX(MAX)}$	Phase I = soft-start (1.0ms)	0.275	0.380	0.500	A
		Phase II = soft-start (1.0ms)		0.75		
		Phase III = soft-start (1.0ms)		1.12		
		Phase IV = fully on (after 3.0ms)	1.1	1.5	2.0	
Maximum RMS LX Current				1		A
Soft-Start Period	t_{SS}	Power-up to the end of phase III		3072 / f_{OSC}		s
FB Fault Trip Level			1.07	1.1	1.14	V
POSITIVE CHARGE PUMP						
V_{SUPP} Input Supply Range	V_{SUPP}		2.7		13.0	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = 10V, TGND = PGND = GND, C_{REF} = 0.22µF, C_{INTG} = 470pF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency				0.5 x f_{OSC}		Hz
FBP Regulation Voltage	V_{FBP}		1.20	1.25	1.30	V
FBP Input Bias Current	I_{FBP}	V_{FBP} = 1.5V	-50		+50	nA
DRVP PCH On-Resistance				3	10	Ω
DRVP NCH On-Resistance		V_{FBP} = 1.213V		1.5	4	Ω
		V_{FBP} = 1.275V	20			kΩ
FBP Power-Ready Trip Level		Rising edge	1.091	1.125	1.159	V
FBP Fault Trip Level		Falling edge		1.11		V
Maximum RMS DRVP Current				0.1		A
NEGATIVE CHARGE PUMP						
V_{SUPN} Input Supply Range	V_{SUPN}		2.7		13.0	V
Operating Frequency				0.5 x f_{OSC}		Hz
FBN Regulation Voltage	V_{FBN}		-50	0	+50	mV
FBN Input Bias Current	I_{FBN}	V_{FBN} = -0.05V	-50		+50	nA
DRVN PCH On-Resistance				3	10	Ω
DRVN NCH On-Resistance		V_{FBN} = 0.035V		1.5	4	Ω
		V_{FBN} = -0.025V	20			kΩ
FBN Power-Ready Trip Level		Rising edge	80	110	165	mV
FBN Fault Trip Level		Falling edge		130		mV
Maximum RMS DRVN Current				0.1		A
REFERENCE						
Reference Voltage	V_{REF}	-2µA < I_{REF} < +50µA	1.231	1.25	1.269	V
Reference Undervoltage Threshold		V_{REF} rising	0.9	1.05	1.2	V
LOGIC SIGNALS						
$\overline{SHDN}$ Input Low Voltage		0.4V hysteresis (typ)			0.9	V
$\overline{SHDN}$ Input High Voltage			2.1			V
$\overline{SHDN}$ Input Current	$I_{\overline{SHDN}}$			0.01	1	µA
$\overline{RDY}$ Output Low Voltage		I_{SINK} = 2mA		0.25	0.5	V
$\overline{RDY}$ Output High Voltage		$V_{\overline{RDY}}$ = 13V		0.01	1	µA

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = 10V, TGND = PGND = GND, C_{REF} = 0.22µF, C_{INTG} = 470pF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Supply Range	V_{IN}		2.7	5.5	V
Input Undervoltage Threshold	V_{UVLO}	V_{IN} rising, 40mV hysteresis (typ)	2.2	2.6	V
IN Quiescent Supply Current	I_{IN}	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = -0.2V		1	mA
SUPP Quiescent Current	I_{SUPP}	V_{FBP} = 1.5V		0.8	mA
SUPN Quiescent Current	I_{SUPN}	V_{FBN} = -0.1V		0.8	mA
IN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{IN} = 5V		10	µA
SUPP Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPP} = 13V		10	µA
SUPN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPN} = 13V		10	µA
MAIN BOOST CONVERTER					
Output Voltage Range	V_{MAIN}		V_{IN}	13.0	V
FB Regulation Voltage	V_{FB}		1.222	1.271	V
FB Input Bias Current	I_{FB}	V_{FB} = 1.25V, INTG = GND	-50	+50	nA
Operating Frequency	F_{OSC}		0.75	1.25	MHz
Oscillator Maximum Duty Cycle			78	90	%
LX Switch On-Resistance	$R_{LX(ON)}$	I_{LX} = 100mA		0.7	Ω
LX Leakage Current	I_{LX}	V_{LX} = 13V		20	µA
LX Current Limit	$I_{LX(MAX)}$	Phase I = soft-start (1.0ms)	0.275	0.500	A
		Phase IV = fully on (after 3.0ms)	1.1	2.0	
FB Fault Trip Level			1.07	1.14	V
POSITIVE CHARGE PUMP					
SUPP Input Supply Range	V_{SUPP}		2.7	13.0	V
FBP Regulation Voltage	V_{FBP}		1.20	1.30	V
FBP Input Bias Current	I_{FBP}	V_{FBP} = 1.5V	-50	+50	nA
DRVP PCH On-Resistance				10	Ω
DRVP NCH On-Resistance		V_{FBP} = 1.213V		4	Ω
		V_{FBP} = 1.275V	20		kΩ
FBP Power-Ready Trip Level		Rising edge	1.091	1.159	V
NEGATIVE CHARGE PUMP					
SUPN Input Supply Range	V_{SUPN}		2.7	13.0	V
FBN Regulation Voltage	V_{FBN}		-50	+50	mV
FBN Input Bias Current	I_{FBN}	V_{FBN} = -0.05V	-50	+50	nA
DRVN PCH On-Resistance				10	Ω
DRVN NCH On-Resistance		V_{FBN} = 0.035V		4	Ω
		V_{FBN} = -0.025V	20		kΩ
FBN Power-Ready Trip Level		Rising edge	80	165	mV
REFERENCE					
Reference Voltage	V_{REF}	-2µA < I_{REF} < +50µA	1.223	1.269	V
Reference Undervoltage		V_{REF} rising	0.9	1.2	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = 10V, TGND = PGND = GND, C_{REF} = 0.22µF, C_{INTG} = 470pF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

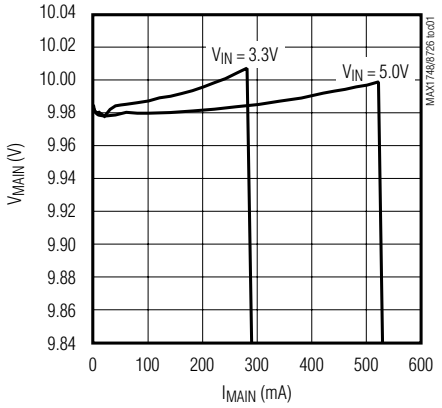
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
LOGIC SIGNALS					
$\overline{SHDN}$ Input Low Voltage		0.45V hysteresis (typ)		0.9	V
$\overline{SHDN}$ Input High Voltage			2.1		V
$\overline{SHDN}$ Input Current	$I_{\overline{SHDN}}$			1	µA
$\overline{RDY}$ Output Low Voltage		I_{SINK} = 2mA		0.5	V
$\overline{RDY}$ Output High Leakage		$V_{\overline{RDY}}$ = 13V		1	µA

Note 1: Specifications from 0°C to -40°C are guaranteed by design, not production tested.

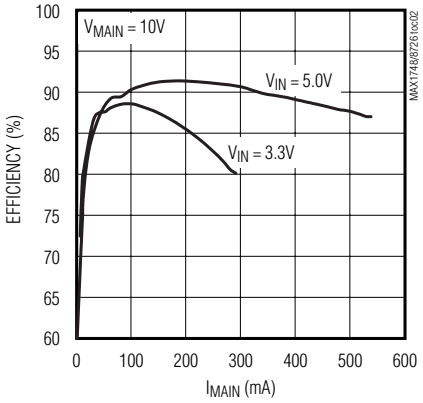
Typical Operating Characteristics

(Circuit of Figure 5, V_{IN} = 3.3V, T_A = +25°C, unless otherwise noted.)

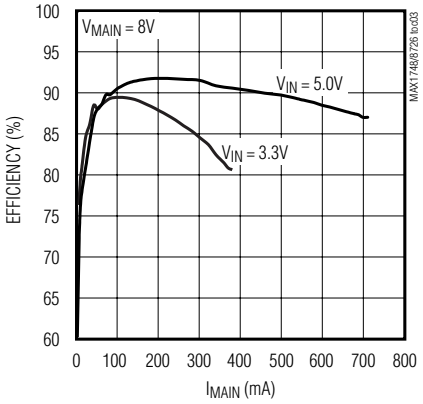
MAIN OUTPUT VOLTAGE vs. LOAD CURRENT



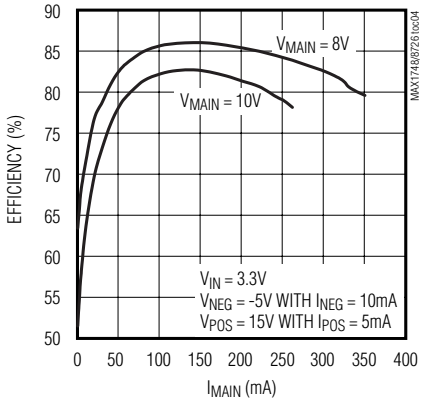
MAIN STEP-UP CONVERTER EFFICIENCY vs. LOAD CURRENT (BOOST ONLY)



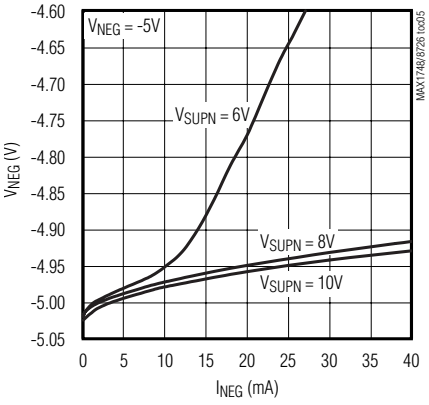
MAIN STEP-UP CONVERTER EFFICIENCY vs. LOAD CURRENT (BOOST ONLY)



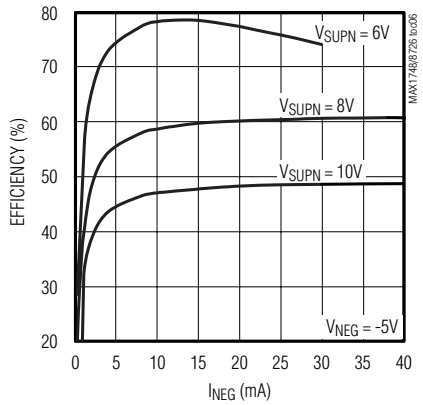
EFFICIENCY vs. LOAD CURRENT (BOOST CONVERTER AND CHARGE PUMPS)



NEGATIVE CHARGE-PUMP OUTPUT VOLTAGE vs. LOAD CURRENT



NEGATIVE CHARGE-PUMP EFFICIENCY vs. LOAD CURRENT

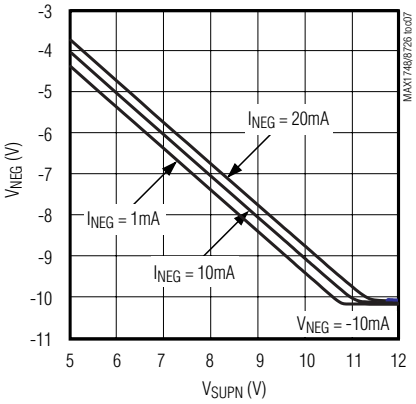


Triple-Output TFT-LCD DC-DC Converters

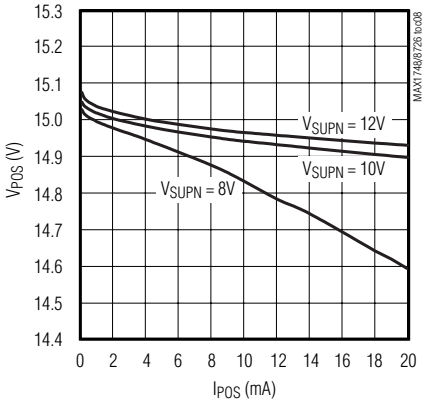
Typical Operating Characteristics (continued)

(Circuit of Figure 5, V_{IN} = 3.3V, T_A = +25°C, unless otherwise noted.)

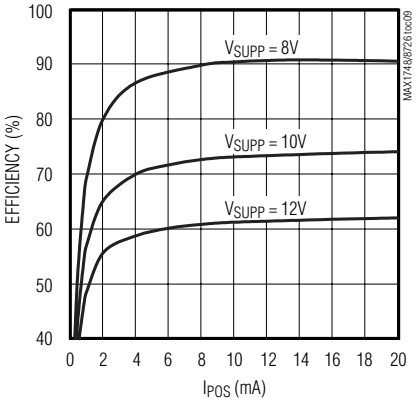
MAXIMUM NEGATIVE CHARGE-PUMP OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



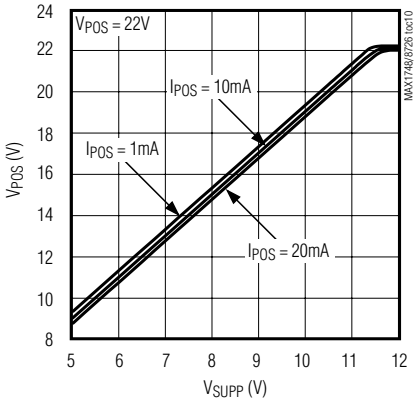
POSITIVE CHARGE-PUMP OUTPUT VOLTAGE vs. LOAD CURRENT



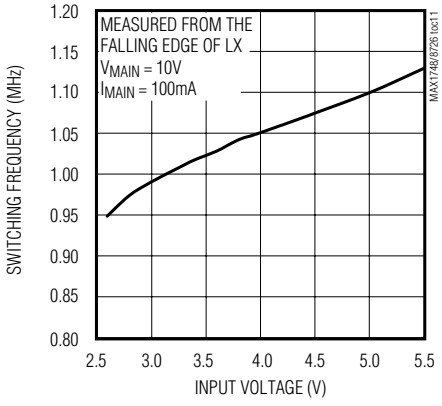
POSITIVE CHARGE-PUMP EFFICIENCY vs. LOAD CURRENT



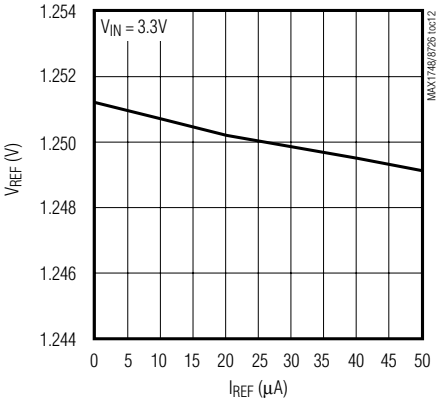
MAXIMUM POSITIVE CHARGE-PUMP OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



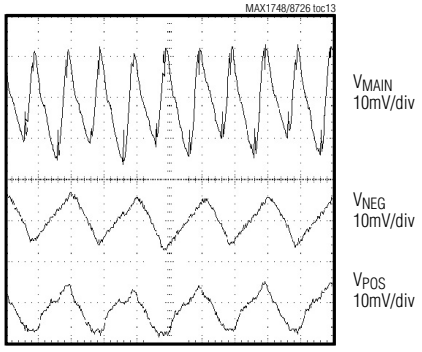
SWITCHING FREQUENCY vs. INPUT VOLTAGE



REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT

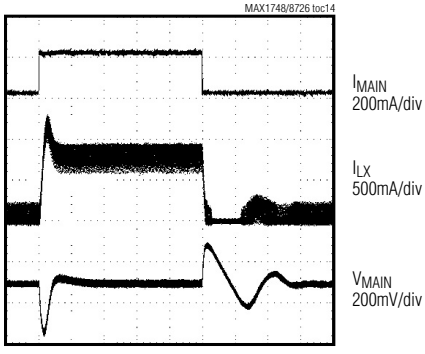


RIPPLE WAVEFORMS



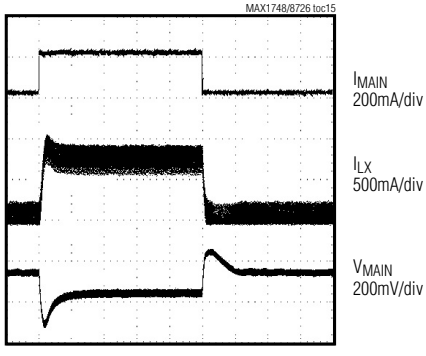
V_{MAIN} = 10V, I_{MAIN} = 200mA,
V_{NEG} = -5V, I_{NEG} = 10mA,
V_{POS} = 15V, I_{POS} = 10mA

LOAD-TRANSIENT RESPONSE



V_{IN} = 3.3V, V_{MAIN} = 10V,
R_{MAIN} = 500Ω TO 50Ω (20mA TO 200mA)

LOAD-TRANSIENT RESPONSE WITHOUT INTEGRATOR

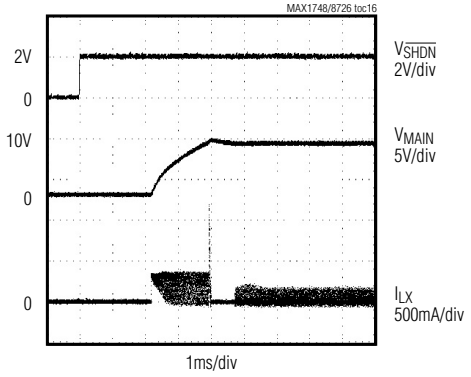


V_{IN} = 3.3V, V_{MAIN} = 10V, INTG = REF,
R_{MAIN} = 500Ω TO 50Ω (20mA TO 200mA)

Typical Operating Characteristics (continued)

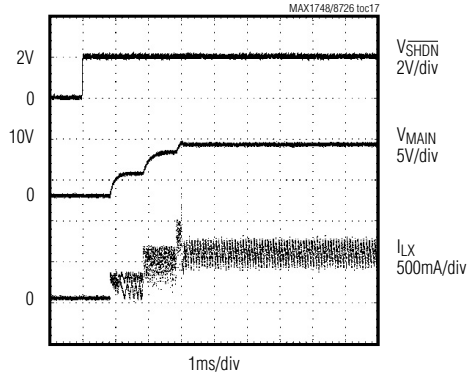
(Circuit of Figure 5, V_{IN} = 3.3V, T_A = +25°C, unless otherwise noted.)

MAIN BOOST STARTUP WAVEFORM



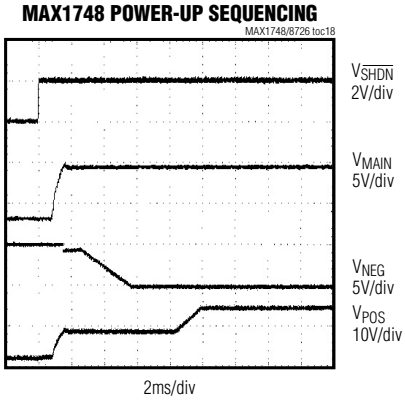
R_{MAIN} = 1kΩ, V_{MAIN} = 10V

MAIN BOOST STARTUP WAVEFORM WITH LOAD



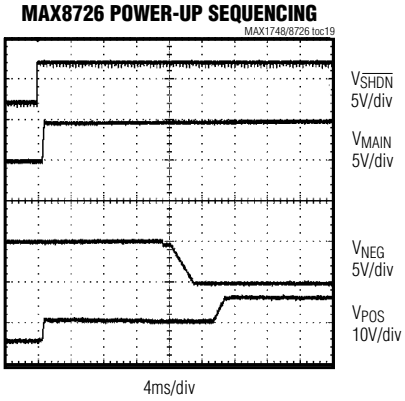
V_{MAIN} = 10V, R_{MAIN} = 50Ω (200mA)

MAX1748 POWER-UP SEQUENCING



V_{MAIN} = 10V, V_{NEG} = -5V, V_{POS} = 15V

MAX8726 POWER-UP SEQUENCING



V_{MAIN} = 10V, V_{NEG} = -5V, V_{POS} = 15V

Pin Description

PIN	NAME	FUNCTION
1	$\overline{RDY}$	Active-Low, Open-Drain Output. Indicates all outputs are ready. The on-resistance is 125Ω (typ).
2	FB	Main Boost Regulator Feedback Input. Regulates to 1.248V nominal. Connect feedback resistive divider to analog ground (GND).
3	INTG	Main Boost Integrator Output. If used, connect 470pF to analog ground (GND). To disable integrator, connect to REF.
4	IN	Supply Input. +2.7V to +5.5V input range. Bypass with a 0.1µF capacitor between IN and GND, as close to the pins as possible.
5	GND	Analog Ground. Connect to power ground (PGND) underneath the IC.
6	REF	Internal Reference Bypass Terminal. Connect a 0.22µF capacitor from this terminal to analog ground (GND). External load capability to 50µA.
7	FBP	Positive Charge-Pump Regulator Feedback Input. Regulates to 1.25V nominal. Connect feedback resistive divider to analog ground (GND).

Triple-Output TFT-LCD DC-DC Converters

Pin Description (continued)

PIN	NAME	FUNCTION
8	FBN	Negative Charge-Pump Regulator Feedback Input. Regulates to 0V nominal.
9	$\overline{SHDN}$	Active-Low Logic-Level Shutdown Input. Connect $\overline{SHDN}$ to IN for normal operation.
10	DRVN	Negative Charge-Pump Driver Output. Output high level is V_{SUPN}, and low level is PGND.
11	SUPN	Negative Charge-Pump Driver Supply Voltage. Bypass to PGND with a 0.1µF capacitor.
12	DRVP	Positive Charge-Pump Driver Output. Output high level is V_{SUPP}, and low level is PGND.
13	SUPP	Positive Charge-Pump Driver Supply Voltage. Bypass to PGND with a 0.1µF capacitor.
14	PGND	Power Ground. Connect to GND underneath the IC.
15	LX	Main Boost Regulator Power MOSFET n-Channel Drain. Connect output diode and output capacitor as close to PGND as possible.
16	TGND	Must be connected to ground.

Detailed Description

The MAX1748/MAX8726 are highly efficient triple-output power supplies for TFT-LCD applications. These devices contain one high-power step-up converter and two low-power charge pumps. The primary boost converter uses an internal n-channel MOSFET to provide maximum efficiency and to minimize the number of external components. The output voltage of the main boost converter (V_{MAIN}) can be set from V_{IN} to 13V with external resistors.

The dual charge pumps independently regulate a positive output (V_{POS}) and a negative output (V_{NEG}). These low-power outputs use external diode and capacitor stages (as many stages as required) to regulate output voltages up to +40V and down to -40V. A proprietary regulation algorithm minimizes output ripple as well as capacitor sizes for both charge pumps.

Also included in the MAX1748/MAX8726 is a precision 1.25V reference that sources up to 50µA, logic shutdown, soft-start, power-up sequencing, fault detection, and an active-low open-drain ready output.

Main Boost Converter

The MAX1748/MAX8726 main step-up converter switches at a constant 1MHz internal oscillator frequency to allow the use of small inductors and output capacitors. The MOSFET switch pulse width is modulated to control the power transferred on each switching cycle and to regulate the output voltage.

During PWM operation, the internal clock's rising edge sets a flip-flop, which turns on the n-channel MOSFET (Figure 1). The switch turns off when the sum of the voltage-error, slope-compensation, and current-feedback signals trips the multi-input comparator and resets the flip-flop. The switch remains off for the rest of the clock cycle. Changes in the output-voltage error signal shift the switch current trip level, consequently modulating the MOSFET duty cycle.

Dual Charge-Pump Regulator

The MAX1748/MAX8726 contain two individual low-power charge pumps. One charge pump inverts the supply voltage (SUPN) and provides a regulated negative output voltage. The second charge pump doubles the supply voltage (SUPP) and provides a regulated positive output voltage. The MAX1748/MAX8726 contain internal p-channel and n-channel MOSFETs to control the power transfer. The internal MOSFETs switch at a constant 500kHz ($0.5 \times f_{OSC}$).

Negative Charge Pump

During the first half-cycle, the p-channel MOSFET turns on and the flying capacitor C5 charges to V_{SUPN} minus a diode drop (Figure 2). During the second half-cycle, the p-channel MOSFET turns off, and the n-channel MOSFET turns on, level shifting C5. This connects C5 in parallel with the reservoir capacitor C6. If the voltage across C6 minus a diode drop is lower than the voltage across C5, charge flows from C5 to C6 until the diode (D5) turns off. The amount of charge transferred to the output is controlled by the variable n-channel on-resistance.

Positive Charge Pump

During the first half-cycle, the n-channel MOSFET turns on and charges the flying capacitor C3 (Figure 3). This initial charge is controlled by the variable n-channel on-resistance. During the second half-cycle, the n-channel MOSFET turns off and the p-channel MOSFET turns on, level shifting C3 by V_{SUPP} volts. This connects C3 in parallel with the reservoir capacitor C4. If the voltage across C4 plus a diode drop ($V_{POS} + V_{DIODE}$) is smaller than the level-shifted flying capacitor voltage ($V_{C3} + V_{SUPP}$), charge flows from C3 to C4 until the diode (D3) turns off.

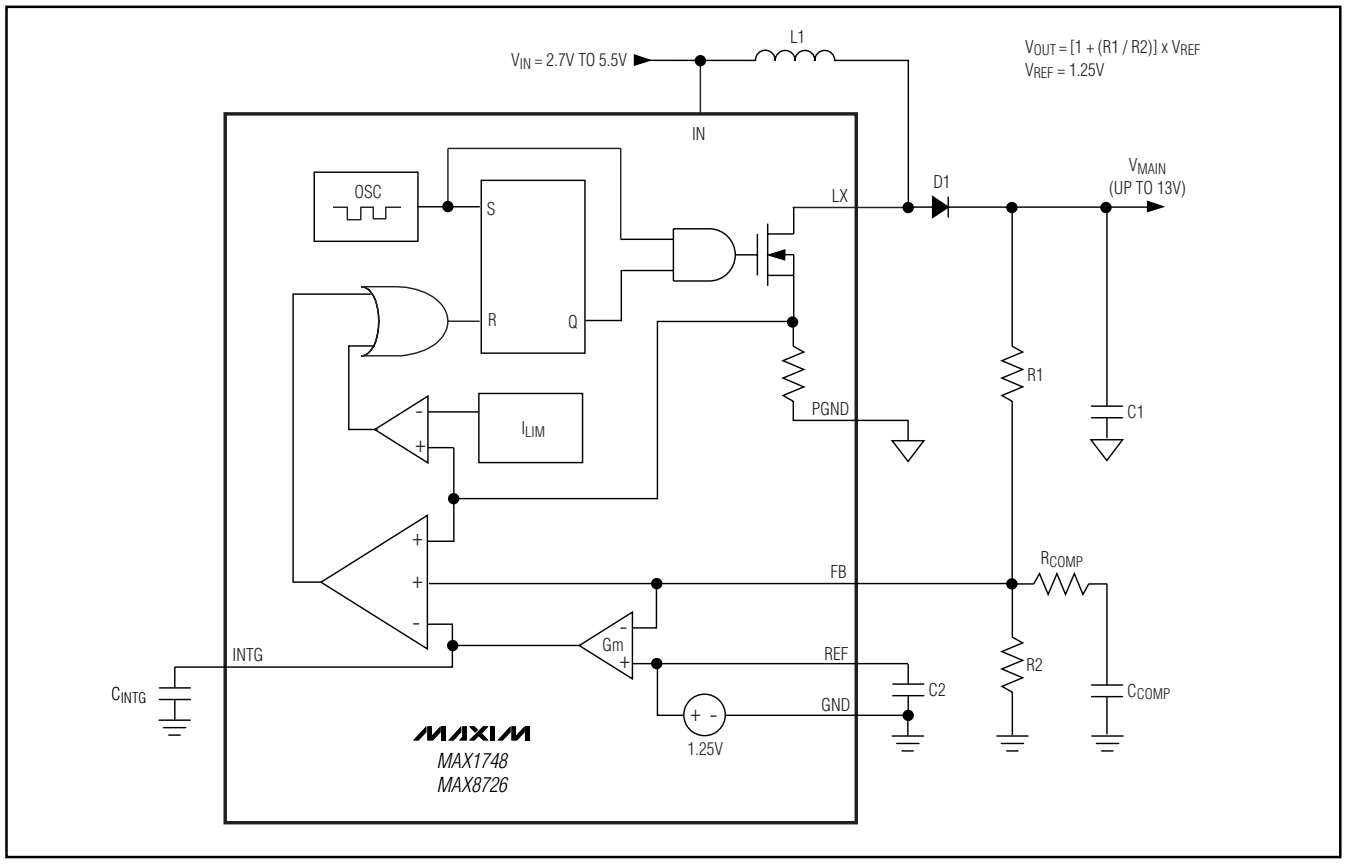


Figure 1. PWM Boost Converter Block Diagram

Soft-Start

For the main boost regulator, soft-start allows a gradual increase of the internal current-limit level during startup to reduce input surge currents. The MAX1748/MAX8726 divide the soft-start period into four phases. During phase 1, the MAX1748/MAX8726 limit the current limit to only 0.38A (see the *Electrical Characteristics* tables), approximately a quarter of the maximum current limit ($I_{LX(MAX)}$). If the output does not reach regulation within 1ms, soft-start enters phase II and the current limit is increased by another 25%. This process is repeated for phase III. The maximum 1.5A (typ) current limit is reached within 3.0ms or when the output reaches regulation, whichever occurs first (see the startup waveforms in the *Typical Operating Characteristics*).

For the charge pumps, soft-start is achieved by controlling the rise rate of the output voltage. The output voltage regulates within 4ms, regardless of output capacitance and load, limited only by the regulator's output impedance.

Shutdown

A logic-low level on $\overline{SHDN}$ disables all three MAX1748/MAX8726 converters and the reference. When shut down, supply current drops to 0.1µA to maximize battery life and the reference is pulled to ground. The output capacitance and load current determine the rate at which each output voltage will decay. A logic-level high on $\overline{SHDN}$ power activates the MAX1748/MAX8726 (see the *Power-Up Sequencing* section). Do not leave $\overline{SHDN}$ floating. If unused, connect $\overline{SHDN}$ to IN.

Power-Up Sequencing

Upon power-up or exiting shutdown, the MAX1748 and MAX8726 start their respective power-up sequences.

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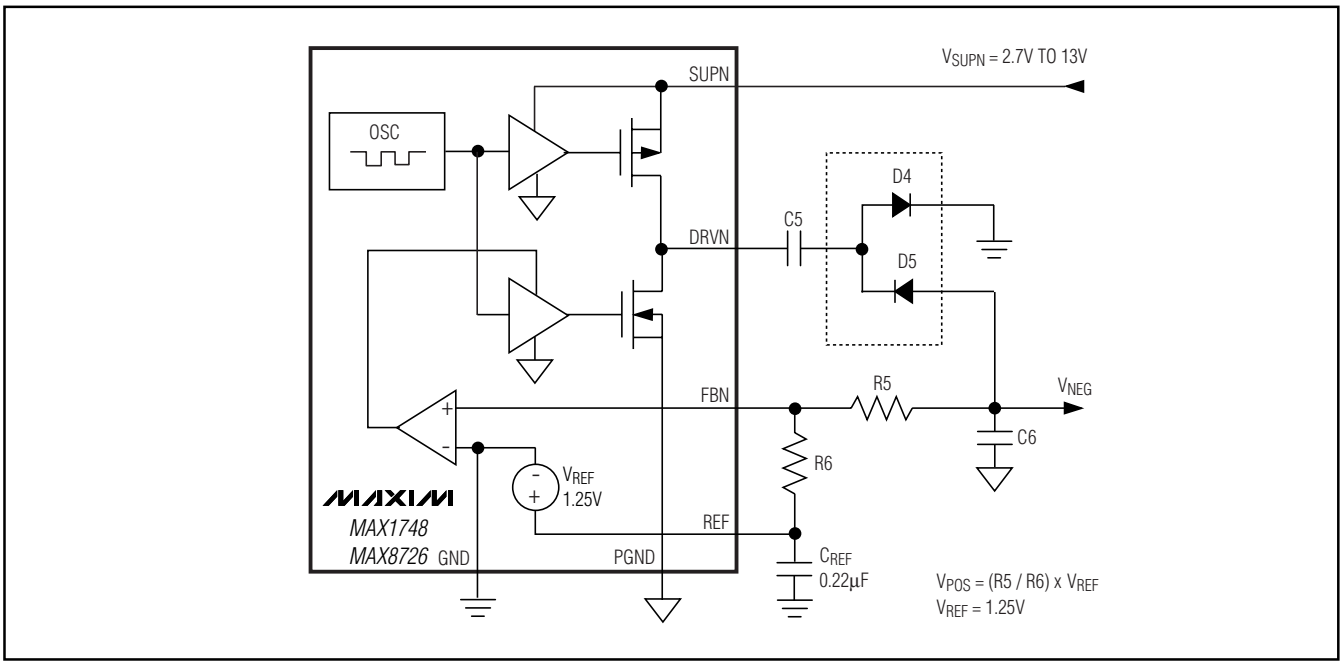


Figure 2. Negative Charge-Pump Block Diagram

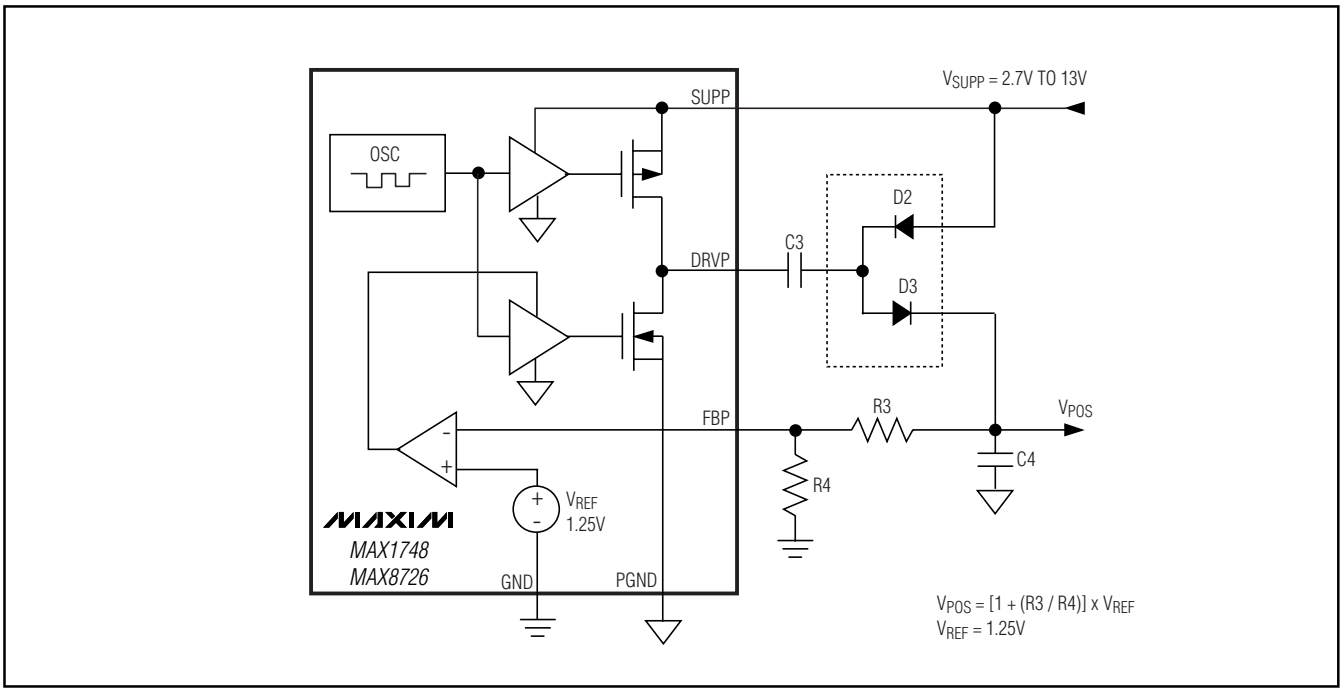


Figure 3. Positive Charge-Pump Block Diagram

In the MAX1748, the reference powers up first, then the main DC-DC step-up converter powers up with soft-start enabled. Once the main step-up converter reaches regulation, the negative charge pump turns on. When the negative output voltage reaches approximately 88% of its nominal value (V_{FBN} < 110mV), the positive charge pump starts up. Finally, when the positive output voltage reaches 90% of its nominal value (V_{FBP} > 1.125V), the active-low ready signal ($\overline{RDY}$) goes low (see the *Power Ready* section).

In the MAX8726, the reference powers up first. After the reference is in regulation, the main DC-DC step-up converter powers up with soft-start enabled. The negative charge pump is enabled when the main step-up converter reaches regulation, and at least 16ms (typ) after the main step-up converter has been enabled. The positive charge pump is enabled when the negative output voltage reaches approximately 88% of its nominal value (V_{FBN} < 110mV), and at least 4ms (typ) after the negative charge pump has been enabled. Finally, when the positive output voltage reaches 90% of its nominal value (V_{FBP} > 1.125V), the active-low ready signal ($\overline{RDY}$) goes low (see the *Power Ready* section).

Power Ready

Power ready is an open-drain output. When the power-up sequence is properly completed, the MOSFET turns on and pulls $\overline{RDY}$ low with a typical 125Ω on-resistance. If a fault is detected, the internal open-drain MOSFET appears as a high impedance. Connect a 100kΩ pullup resistor between $\overline{RDY}$ and IN for a logic-level output.

Fault Detection

Once $\overline{RDY}$ is low and if any output falls below its fault-detection threshold, $\overline{RDY}$ goes high impedance.

For the reference, the fault threshold is 1.05V. For the main boost converter, the fault threshold is 88% of its nominal value (V_{FB} < 1.1V). For the negative charge pump, the fault threshold is approximately 90% of its nominal value (V_{FBN} < 130mV). For the positive charge pump, the fault threshold is 88% of its nominal value (V_{FBP} < 1.11V).

Once an output faults, all outputs later in the power sequence shut down until the faulted output rises above its power-up threshold. For example, if the negative charge-pump output voltage falls below the fault-detection threshold, the main boost converter remains active while the positive charge pump stops switching and its output voltage decays, depending on output capacitance and load. The positive charge-pump output will not power up until the negative charge-pump output voltage rises above its power-up threshold (see the *Power-Up Sequencing* section).

Voltage Reference

The voltage at REF is nominally 1.25V. The reference can source up to 50µA with good load regulation (see the *Typical Operating Characteristics*). Connect a 0.22µF bypass capacitor between REF and GND.

Design Procedure

Main Boost Converter

Output Voltage Selection

Adjust the output voltage by connecting a voltage-divider from the output (V_{MAIN}) to FB to GND (see the *Typical Operating Circuit*). Select R2 in the 10kΩ to 20kΩ range. Higher resistor values improve efficiency at low output current but increase output voltage error due to the feedback input bias current. Calculate R1 with the following equations:

$$R1 = R2\ [(V_{MAIN} / V_{REF}) - 1]$$

where V_{REF} = 1.25V. V_{MAIN} can range from V_{IN} to 13V.

Feedback Compensation

For stability, add a pole-zero pair from FB to GND in the form of a series resistor (R_{COMP}) and capacitor (C_{COMP}). The resistor should be half the value of the R2 feedback resistor.

Inductor Selection

Inductor selection depends on input voltage, output voltage, maximum current, switching frequency, size, and availability of inductor values. Other factors can include efficiency and ripple voltage. Inductors are specified by their inductance (L), peak current (I_{PEAK}), and resistance (R_L). The following boost-circuit equations are useful in choosing inductor values based on the application. They allow the trading of peak current and inductor value while allowing for consideration of component availability and cost.

The following equation includes a constant LIR, which is the ratio of the inductor peak-to-peak AC current to maximum average DC inductor current. A good compromise between the size of the inductor, loss, and output ripple is to choose an LIR of 0.3 to 0.5. The peak inductor current is then given by:

$$I_{PEAK} = \frac{I_{MAIN(MAX)} \times V_{MAIN}}{Efficiency \times V_{IN(MIN)}} \times \left[1 + (LIR/2)\right]$$

Triple-Output TFT-LCD DC-DC Converters

The inductance value is then given by:

$$L = \frac{V_{IN(MIN)}^2 \times \text{Efficiency} \times (V_{MAIN} - V_{IN(MIN)})}{V_{(MAIN)}^2 \times LIR \times I_{MAIN(MAX)} \times f_{OSC}}$$

Considering the typical application circuit, the maximum DC load current ($I_{MAIN(MAX)}$) is 200mA with a 10V output. A 6.8µH inductance value is then chosen, based on the above equations and using 85% efficiency and a 1MHz operating frequency. Smaller inductance values typically offer a smaller physical size for a given series resistance and current rating, allowing the smallest overall circuit dimensions. However, due to higher peak inductor currents, the output voltage ripple (I_{PEAK} x output filter capacitor ESR) will be higher.

Use inductors with a ferrite core or equivalent; powder iron cores are not recommended for use with the MAX1748/MAX8726s' high switching frequencies. The inductor's maximum current rating should exceed I_{PEAK}. Under fault conditions, inductor current may reach up to 2.0A. The MAX1748/MAX8726s' fast current-limit circuitry allows the use of soft-saturation inductors while still protecting the IC.

The inductor's DC resistance significantly affects efficiency. For best performance, select inductors with resistance less than the internal n-channel FET resistance. To minimize radiated noise in sensitive applications, use a shielded inductor.

The inductor should have as low a series resistance as possible. For continuous inductor current, the power loss in the inductor resistance, P_{LR}, is approximated by:

$$P_{LR} \cong (I_{MAIN} \times V_{MAIN} / V_{IN})^2 \times R_L$$

where R_L is the inductor series resistance.

Output Capacitor

A 10µF capacitor works well in most applications. The equivalent series resistance (ESR) of the output-filter capacitor affects efficiency and output ripple. Output voltage ripple is largely the product of the peak inductor current and the output capacitor ESR. Use low-ESR ceramic capacitors for best performance. Low-ESR, surface-mount tantalum capacitors with higher capacity may be used for load transients with high peak currents. Voltage ratings and temperature characteristics should be considered.

Input Capacitor

The input capacitor (C_{IN}) in boost designs reduces the current peaks drawn from the input supply and reduces noise injection. The value of C_{IN} is largely determined by the source impedance of the input supply. High source impedance requires high input capacitance, particularly as the input voltage falls. Since step-up DC-DC converters act as "constant-power" loads to their input supply, input current rises as input voltage falls. A good starting point is to use the same capacitance value for C_{IN} as for C_{OUT}. Table 1 lists suggested component suppliers.

Integrator Capacitor

The MAX1748/MAX8726 contain an internal current integrator that improves the DC load regulation but increases the peak-to-peak transient voltage (see the load-transient waveforms in the *Typical Operating Characteristics*). For highly accurate DC load regulation, enable the current integrator by connecting a 470pF capacitor to INTG. To minimize the peak-to-peak transient voltage at the expense of DC regulation, disable the integrator by connecting INTG to REF and adding a 100kΩ resistor to GND.

Rectifier Diode

Use a Schottky diode with an average current rating equal to or greater than the peak inductor current, and a voltage rating at least 1.5 times the main output voltage (V_{MAIN}).

Table 1. Component Suppliers

SUPPLIER	PHONE	FAX
INDUCTORS		
Coilcraft	847-639-6400	847-639-1469
Coiltronics	561-241-7876	561-241-9339
Sumida USA	847-956-0666	847-956-0702
Toko	847-297-0070	847-699-1194
CAPACITORS		
AVX	803-946-0690	803-626-3123
Kemet	408-986-0424	408-986-1442
Sanyo	619-661-6835	619-661-1055
Taiyo Yuden	408-573-4150	408-573-4159
DIODES		
Central Semiconductor	516-435-1110	516-435-1824
International Rectifier	310-322-3331	310-322-3332
Motorola	602-303-5454	602-994-6430
Nihon	847-843-7500	847-843-2798
Zetex	516-543-7100	516-864-7630

Charge Pump

Efficiency Considerations

The efficiency characteristics of the MAX1748/MAX8726 regulated charge pumps are similar to a linear regulator. They are dominated by quiescent current at low output currents and by the input voltage at higher output currents (see the *Typical Operating Characteristics*). So the maximum efficiency can be approximated by:

$$\text{Efficiency} \cong V_{NEG} / [V_{IN} \times N];$$
for the negative charge pump

$$\text{Efficiency} \cong V_{POS} / [V_{IN} \times (N + 1)];$$
for the positive charge pump

where N is the number of charge-pump stages.

Output Voltage Selection

Adjust the positive output voltage by connecting a voltage-divider from the output (V_{POS}) to FBP to GND (see the *Typical Operating Circuit*). Adjust the negative output voltage by connecting a voltage-divider from the output (V_{NEG}) to FBN to REF. Select R4 and R6 in the 50kΩ to 100kΩ range. Higher resistor values improve efficiency at low output current but increase output-voltage error due to the feedback input bias current. Calculate the remaining resistors with the following equations:

$$R3 = R4 [(V_{POS} / V_{REF}) - 1]$$

$$R5 = R6 (V_{NEG} / V_{REF})$$

where V_{REF} = 1.25V. V_{POS} can range from V_{SUPP} to 40V, and V_{NEG} can range from 0 to -40V.

Flying Capacitor

Increasing the flying capacitor's value reduces the output current capability. Above a certain point, increasing the capacitance has a negligible effect because the output current capability becomes dominated by the internal switch resistance and the diode impedance. Start with 0.1µF ceramic capacitors. Smaller values can be used for low-current applications.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. Use the following equation to approximate the required capacitor value:

$$C_{OUT} \geq [I_{OUT} / (500kHz \times V_{RIPPLE})]$$

Charge-Pump Input Capacitor

Use a bypass capacitor with a value equal to or greater than the flying capacitor. Place the capacitor as close to the IC as possible. Connect directly to PGND.

Rectifier Diode

Use Schottky diodes with a current rating equal to or greater than 4 times the average output current, and a voltage rating at least 1.5 times V_{SUPP} for the positive charge pump and V_{SUPN} for the negative charge pump.

PC Board Layout and Grounding

Careful printed circuit layout is extremely important to minimize ground bounce and noise. First, place the main boost-converter output diode and output capacitor less than 0.2in (5mm) from the LX and PGND pins with wide traces and no vias. Then place 0.1µF ceramic bypass capacitors near the charge-pump input pins (SUPP and SUPN) to the PGND pin. Keep the charge-pump circuitry as close to the IC as possible, using wide traces and avoiding vias when possible. Locate all feedback resistive dividers as close to their respective feedback pins as possible. The PC board should feature separate GND and PGND areas connected at only one point under the IC. To maximize output power and efficiency and to minimize output-power ripple voltage, use extra wide power ground traces and solder the IC's power ground pin directly to it. Avoid having sensitive traces near the switching nodes and high-current lines.

Refer to the MAX1748/MAX8726 evaluation kit for an example of proper board layout.

Applications Information

Boost Converter Using a Cascoded MOSFET

For applications that require output voltages greater than 13V, cascode an external n-channel MOSFET (Figure 4). Place the MOSFET as close to the LX pin as possible. Connect the gate to the input voltage (V_{IN}) and the source to LX.

MOSFET Selection

Choose a MOSFET with an on-resistance ($R_{DS(ON)}$) lower than the internal n-channel MOSFET. Lower $R_{DS(ON)}$ will improve efficiency. The external n-channel MOSFET must have a drain-voltage rating higher than the main output voltage (V_{MAIN}).

Chip Information

TRANSISTOR COUNT: 2846

Triple-Output TFT-LCD DC-DC Converters

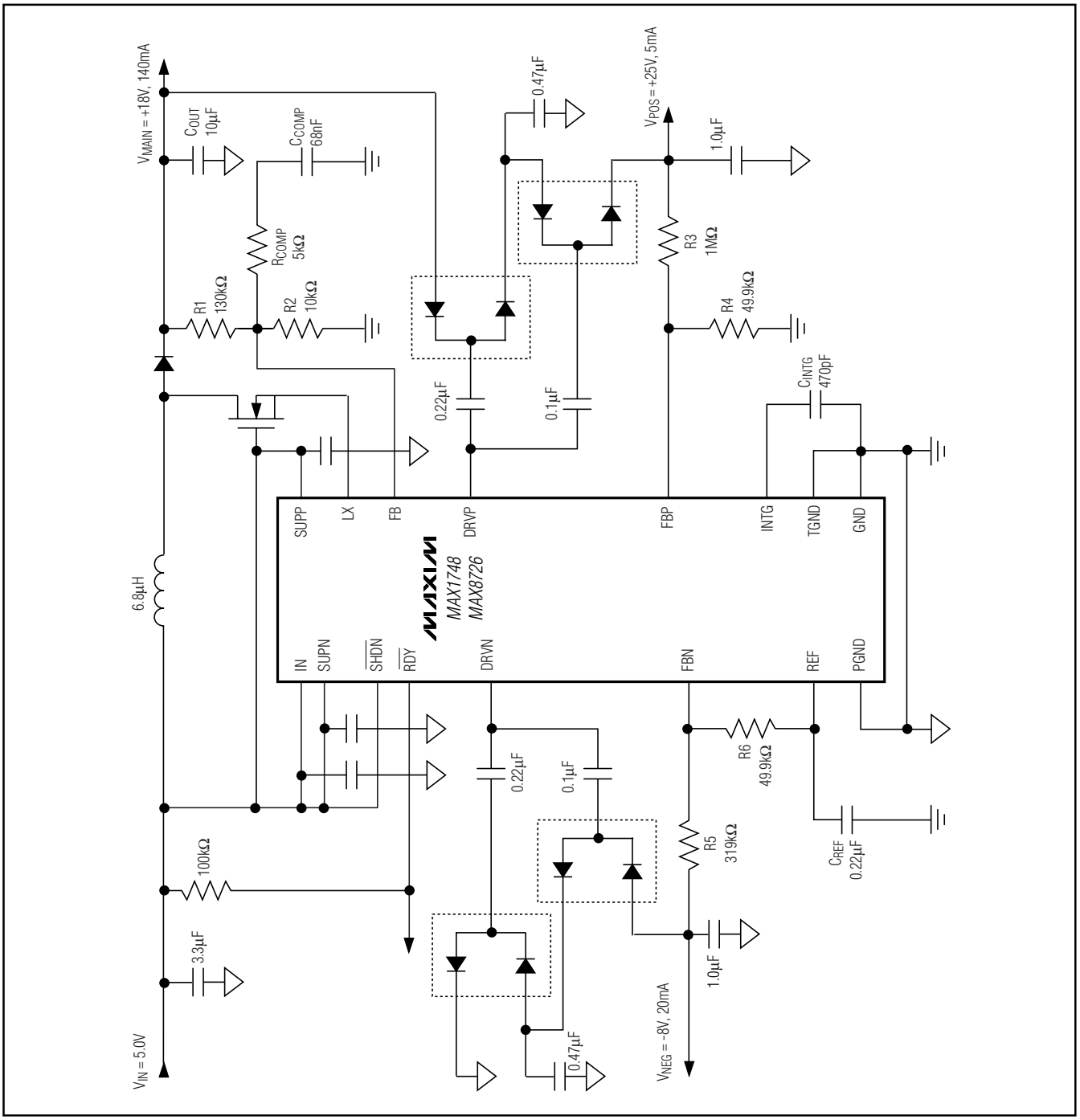
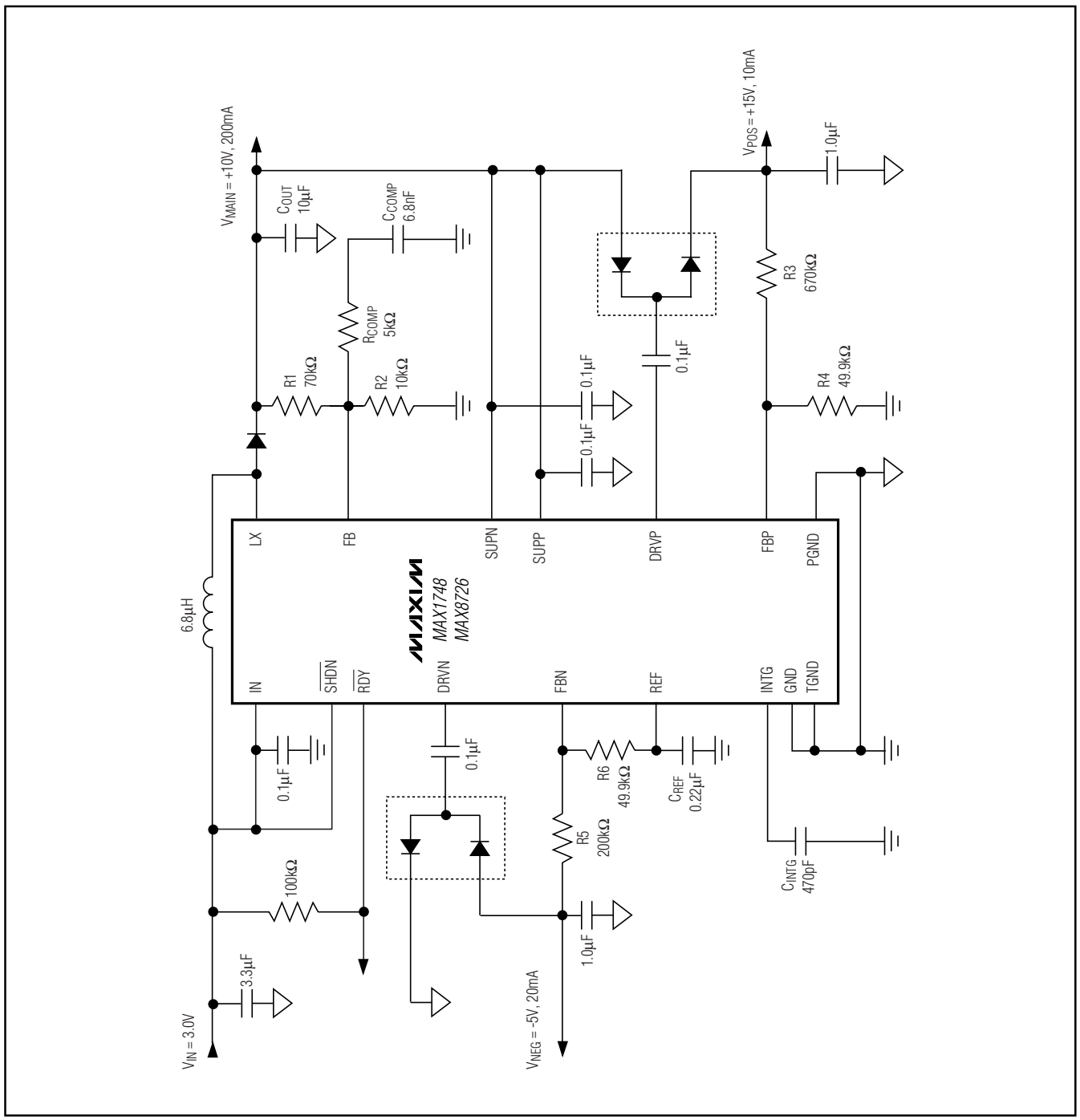


Figure 4. Power Supply Using Cascoded MOSFET

Typical Operating Circuit

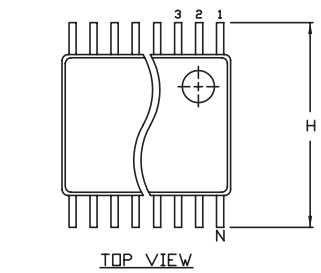


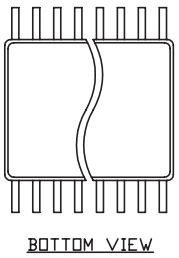
Triple-Output TFT-LCD DC-DC Converters

Package Information

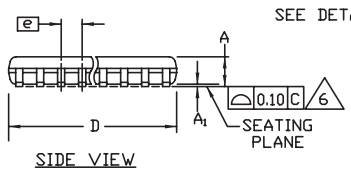
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

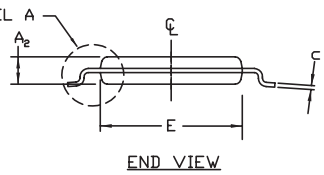
TSSOP4.40mm.EPS



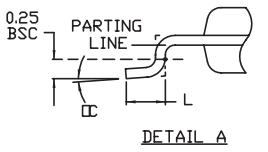


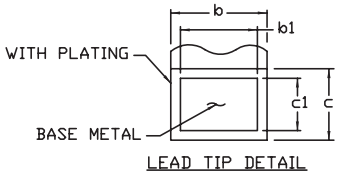
SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°





JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386





NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1

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