Document Title

4M x 16Bit Asynchronous / Page Mode StRAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	Oct. 23 , 2007	Preliminary

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4M x16 Bit Async./Page StRAM

FEATURES

- Single power supply voltage of 2.6 to 3.3V
- Direct TTL compativility for all inputs and outputs.
- Deep power-down mode : Memory cell data invalid.
- Supplied in KGD(Known Good Die) form.
- Page operation mode
  Page read operation by 8 words.
- Logic compatible with SRAM R/W pin.
- Standby Current
  Standby 150 uA
  Deep power-down standby 10uA
- Access Time

Access Time	65ns
$\overline{CE1}$ Access Time	65ns
$\overline{OE}$ Access Time	25ns
Page Access Time	20NS

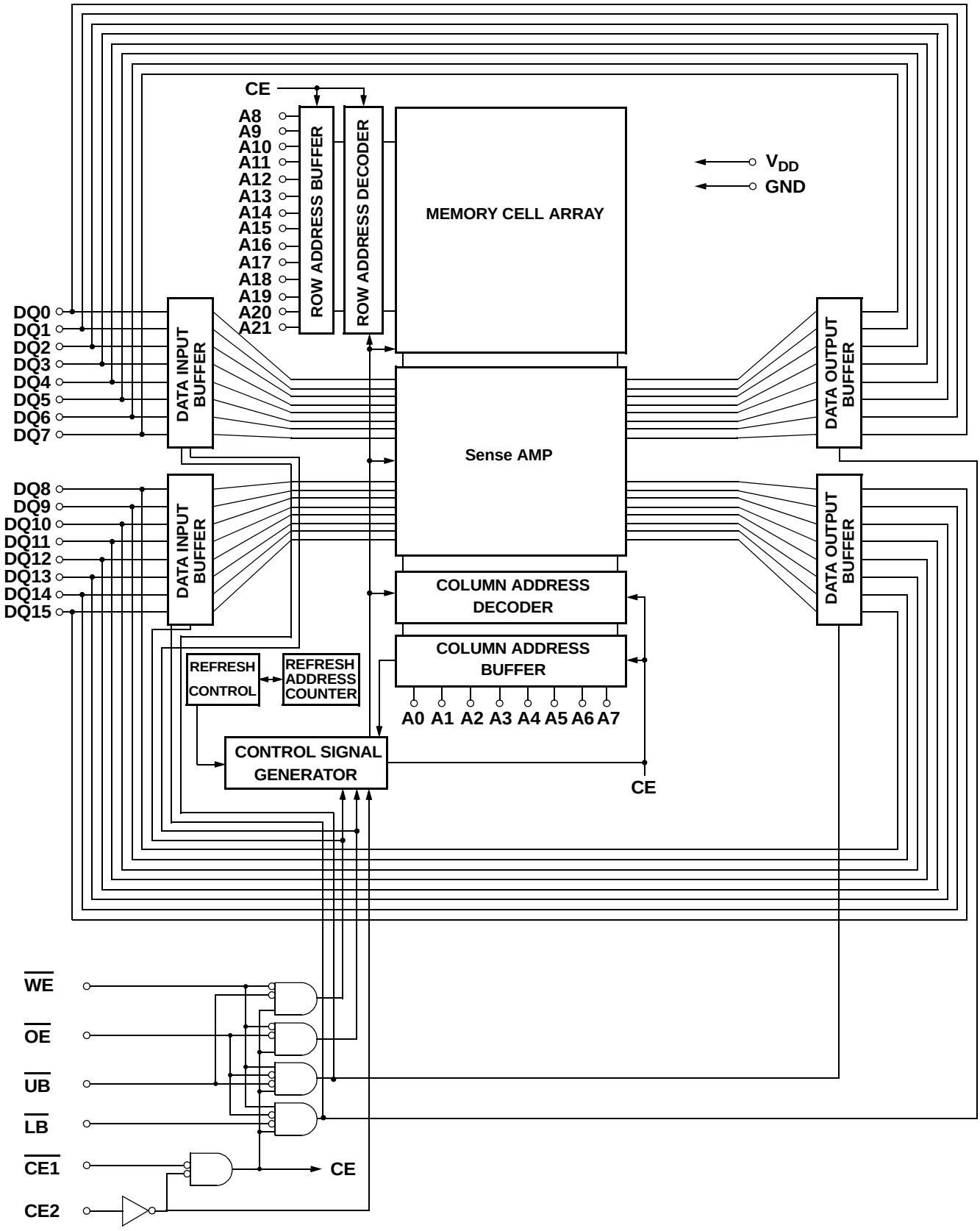
GENERAL DISCRIPTION

The EM7643SU16H is a 64M-bit StRAM organized as 4M words by 16 bits. It provides high density, high speed and low power. The device operates single power supply. The device also features SRAM-like W/R timing whereby the device is controlled by $\overline{CE1}$, $\overline{OE}$ and $\overline{WE}$ on asynchronous. The device has the page access operation. Page size is 8 words. The device also supports deep power-down mode, realizing low-power standby.

PAD DESCRIPTION

SYMBOL	DESCRIPTION
A0~A21	Address input
A0~A2	Page Address input
$\overline{CE1}$	Chip Enable Input1, Low : Enable
CE2	Chip Enable Input2, High:Enable, Low:Enter Power Down mode
$\overline{WE}$	Write Enable input, Low :Enable
$\overline{OE}$	Output Enable input, Low :Enable
$\overline{LB}$	Lower byte write control
$\overline{UB}$	Upper byte write control
DQ0~DQ15	Data inputs/outputs
V_{DD}	Device Power supply
V_{SS}	V_{SS} must be connected ground
V_{DDQ}	I/O Power supply
V_{SSQ}	V_{SS} must be connected ground
NC	Not Connection

FUNCTION BLOCK DIAGRAM



OPERATION MODE

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Add	DQ_0 to DQ_7	DQ_8 to DQ_{15}	Mode	Power
L	H	L	H	L	L	X	Data Out	Data Out	Read(Word)	IDD0
L	H	L	H	L	H	X	Data Out	High-Z	Read(Lower Byte)	IDD0
L	H	L	H	H	L	X	High-Z	Data Out	Read(Upper Byte)	IDD0
L	H	X	L	L	L	X	Data In	Data In	Write(Word)	IDD0
L	H	X	L	L	H	X	Data In	Invalid	Write(Lower Byte)	IDD0
L	H	X	L	H	L	X	Invalid	Data In	Write(Upper Byte)	IDD0
L	H	H	H	X	X	X	High-Z	High-Z	Outputs Disabled	IDD0
H	H	X	X	X	X	X	High-Z	High-Z	Standby	IDDS
H	L	X	X	X	X	X	High-Z	High-Z	Deep Power-down Standby	IDDSD

Note: X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS (SEE NOTE1)

SYMBOL	RATING	VALUE	UNIT
VDD	Device Power Supply Voltage	-1.0 to 3.6	V
VIN	Input Voltage	-1.0 to 3.6	V
VOUT	Output Voltage	-1.0 to 3.6	V
Topr.	Operating Temperature	-25 to 85	℃
Tstrg.	Stroage Temperature	-55 to 150	℃
PD	Power Dissipation	0.6	W
IOUT	Short Circuit Output Current	50	mA

DC RECOMMENDED OPERATING CONDITIONS(Ta = -25℃ to 85 ℃)

SYMBOL	PARAMETER	MIN	TYP	Max	Unit
VDD	Device Power Supply Voltage	2.6	2.75	3.3	V
VIH	Input High Voltage	0.8*VDD	-	VDD + 0.3	
VIL	Input Low Voltage	-0.3	-	0.15*VDD	

VIH(Max) VDD+1.0V with 10ns pulse width
VIL(Min)-1.0V with 10ns pulse width

DC CHARACTERISTICS(Ta = -25℃ to 85 ℃, VDD=2.6 to 3.3V) (SEE NOTE 3 to 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=0 to V_{DD}	-1	-	1	uA
Output leakage current	I_{LO}	Output disable, VOUT= 0V to VDD	-1	-	1	uA
Operating current	I_{DDO1}	tRC= Min, $\overline{CE1}$=V_{IL} , CE2=V_{IH} , I_{OUT}=0mA	-	-	50	mA
Page Access Operating current	I_{DDO2}	tPC = Min, $\overline{CE1}$=V_{IL}, CE2=V_{IH} , I_{OUT}=0mA, Page add. cycling.	-	-	25	mA
Output high voltage	V_{OH}	I_{OH} = -0.5mA	0.8*V_{DD}	-	-	V
Output low voltage	V_{OL}	I_{OL} = 1.0mA, V_{CC}=V_{CCmin}	-	-	0.15*V_{CCQ}	V
Standby Current (CMOS)	I_{DDS}	$\overline{CE1}$≥V_{DD}-0.2V, CE2=V_{DD} -0.2V	-	-	150	uA
Deep Power-down Standby Curret	V_{DDSD} (*1, *2)	CE2 = 0.2V	-	-	10	uA

Note
*1. Max VIL of signals(i.e. A0~A21, DQ1~DQ16, CE1#, CE2, WE#, OE#, LB#, UB#) can be 0.2V to 0.616V.
*2. For deep power-down, CE2<=0.2V is essential. If max VIL of CE2 is from 0.2V to 0.616V, the 10uA deep-power current will not be guaranteed, and the deep-power current might go high as 20uA.

CAPACITANCE (f =1MHz, T_A=25^{o}C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=VSS	-	10	pF
Ouput capacitance	C_{OUT}	V_{OUT}=VSS	-	30	pF

Note : This parameter is sampled periodically and is not 100% tested

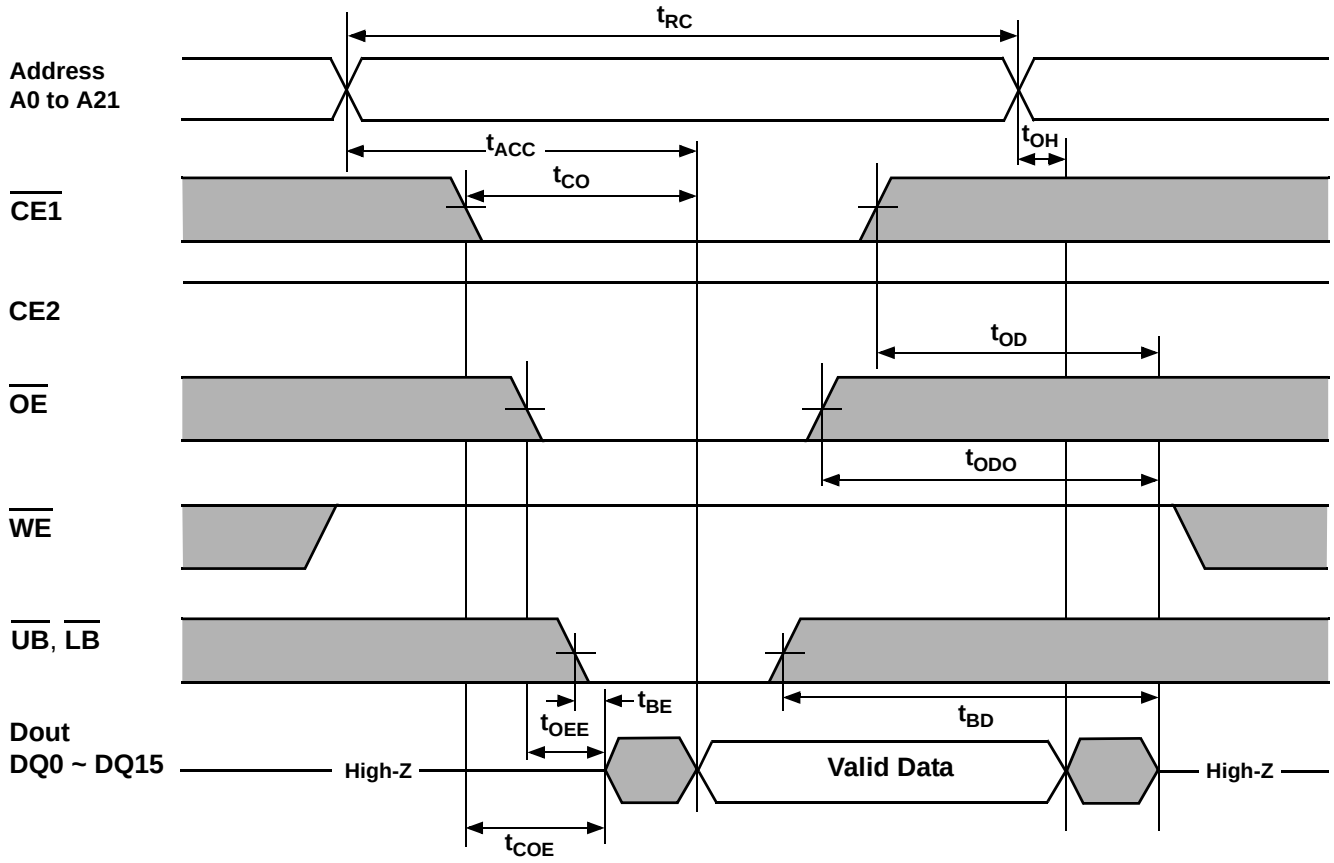
AC TEST CONDITIONS

PARAMETER	CONDITION
Output load	50 ohm+0.5 * VDD
Input pulse level	VDD-0.2V, 0.2V
Timing measurements	VDD * 0.5
Reference level	VDD * 0.5
tR, tF	5 ns

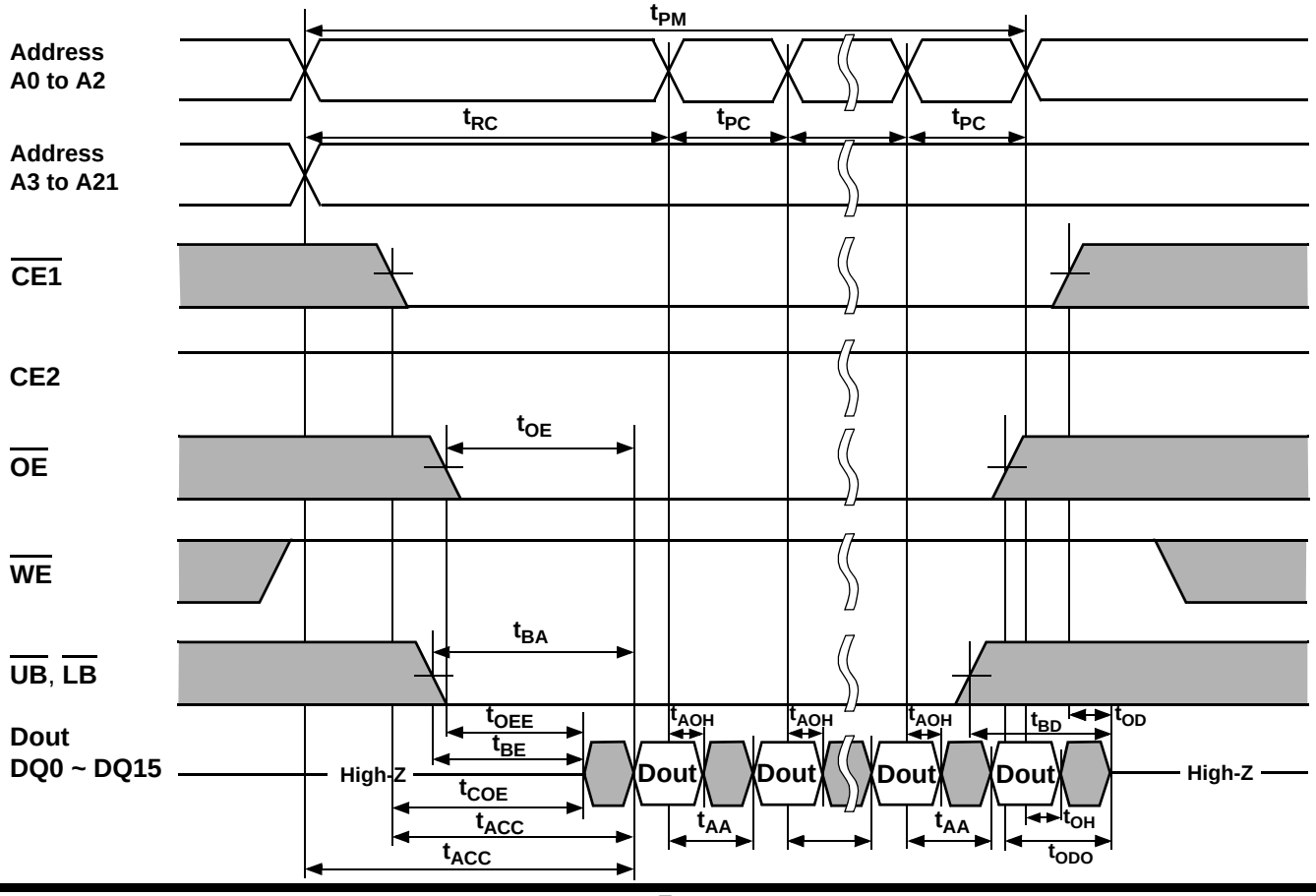
AC CHARACTERISTICS (V_{cc} = 2.6 to 3.3V, Gnd = 0V, T_A = -25°C to +85°C) (SEE NOTE 5-11)

Symbol	Parameter List	Speed		Unit
		Min	Max	
t_{RC}	Read Cycle Time	65	10000	ns
t_{ACC}	Address Access Time	-	65	ns
t_{CO}	Chip Enable($\overline{CE1}$) Access Time	-	65	ns
t_{OE}	Output Enable Access Time	-	25	ns
t_{BA}	Data Byte Control Access Time	-	65	ns
t_{COE}	Chip Enable Low to Output Active	10	-	ns
t_{OEE}	Output Enable Low to Output Active	0	-	ns
t_{BE}	Data Byte Control Low to Output Active	0	-	ns
t_{OD}	Chip Enable High to Ouput High-Z	-	20	ns
t_{ODO}	Output Enable High to Output High-Z	-	20	ns
t_{BD}	Data Byte Control High to Output High-Z	-	20	ns
t_{OH}	Output Data Hold Time	5	-	ns
t_{PM}	Page Mode Time	65	10000	ns
t_{PC}	Page Mode Cycle Time	20	-	ns
t_{AA}	Page Mode Address Access Time	-	20	ns
t_{AOH}	Page Mode Output Data Hold Time	5	-	ns
t_{WC}	Write Cycle Time	65	10000	ns
t_{WP}	Write Pulse Width	50	-	ns
t_{CW}	Chip Enable to End of Write	65	-	ns
t_{BW}	Data Byte Control to End of Write	60	-	ns
t_{AW}	Address Valid to End of Write	60	-	ns
t_{AS}	Address Set-up Time	0	-	ns
t_{WR}	Write Recovery Time	0	-	ns
t_{CEH}	Chip Enable High Pulse Width	10	-	ns
t_{WEH}	Write Enable High Pulse Width	6	-	ns
t_{ODW}	$\overline{WE}$ Low to Output High-Z	-	20	ns
t_{OEW}	WE High to Output Active	0	-	ns
t_{DS}	Data Set-up Time	30	-	ns
t_{DH}	Data Hold Time	0	-	ns
t_{CS}	CE2 Set-up Time	0	-	ns
t_{CH}	CE2 Hold Time	300	-	us
t_{DPD}	CE2 Pulse Width	10	-	ms
t_{CHC}	CE2 Hold from $\overline{CE1}$	0	-	ns
t_{CHP}	CE2 Hold from Power On	30	-	us

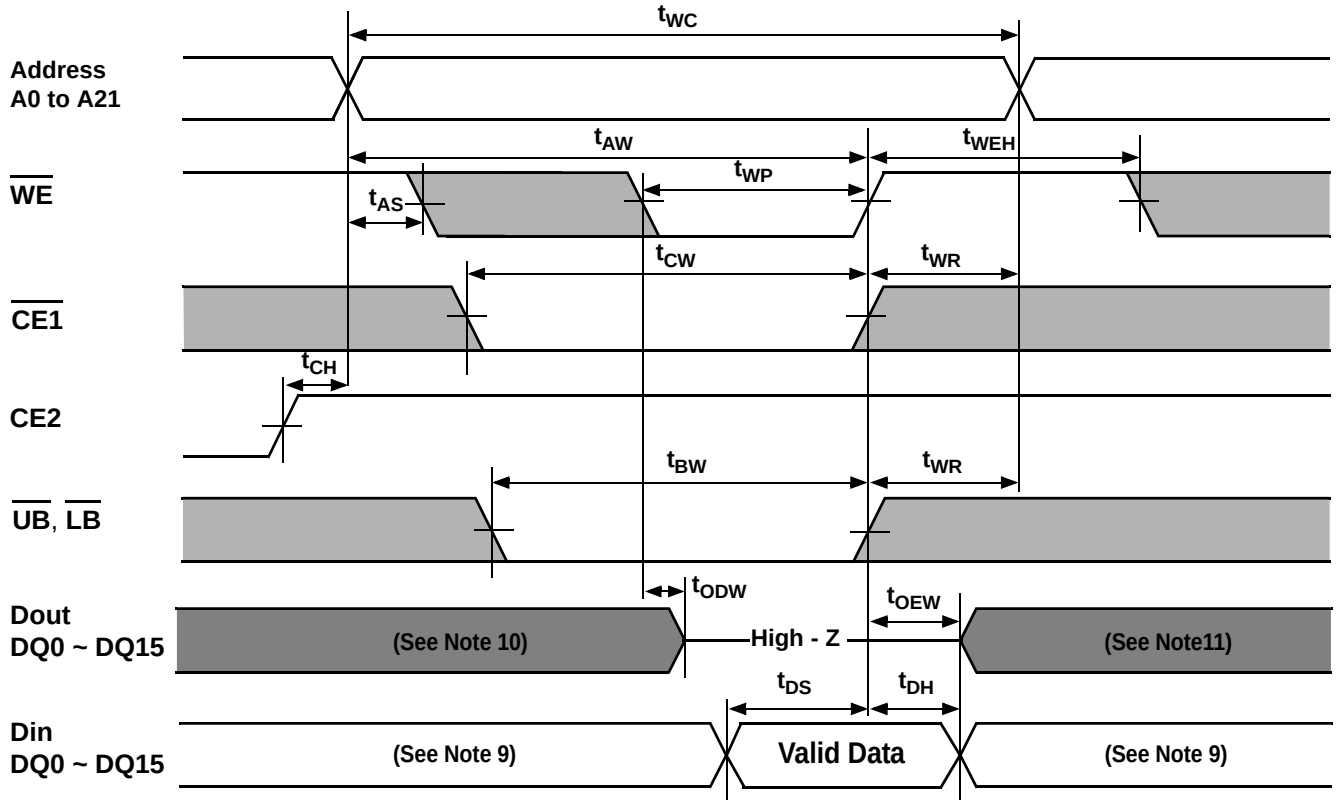
TIMING WAVEFORM OF READ CYCLE



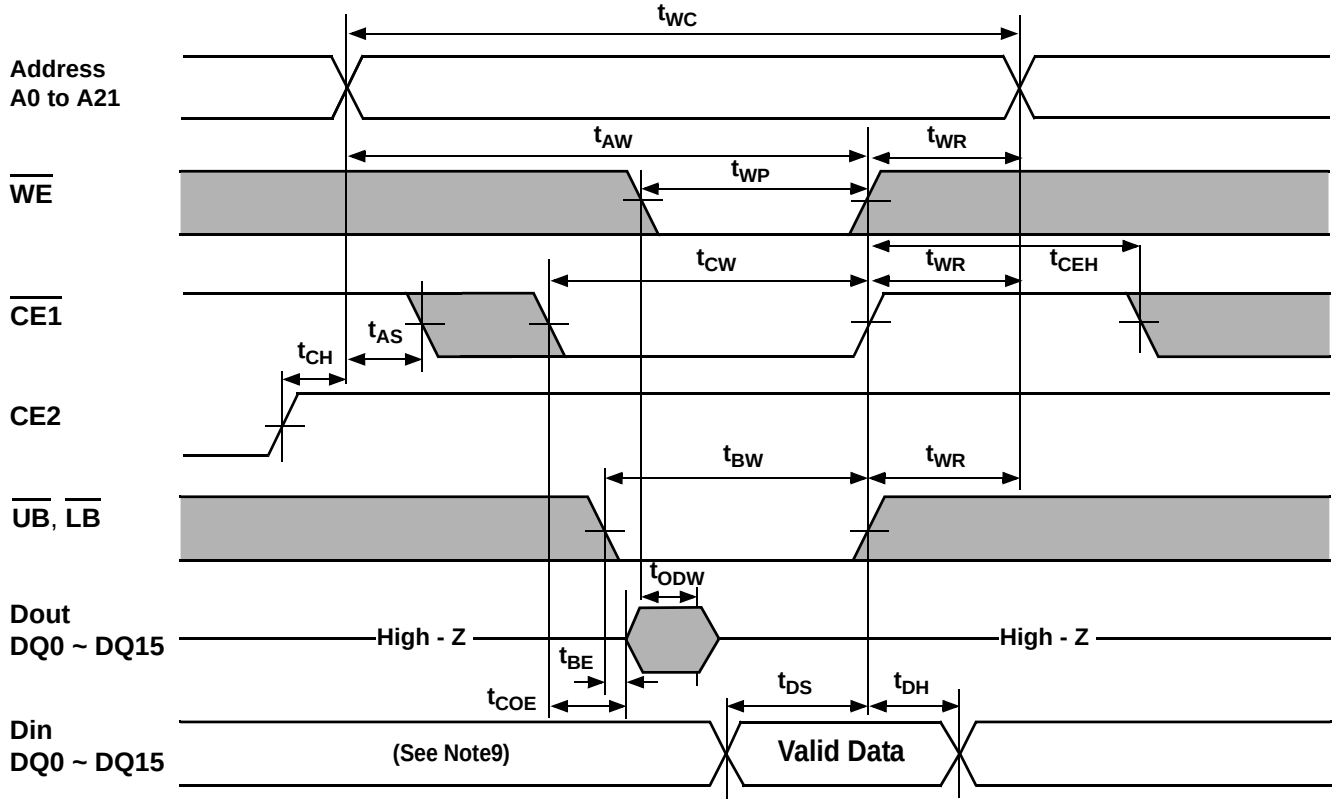
TIMING WAVEFORM OF PAGE READ CYCLE (8 words access)



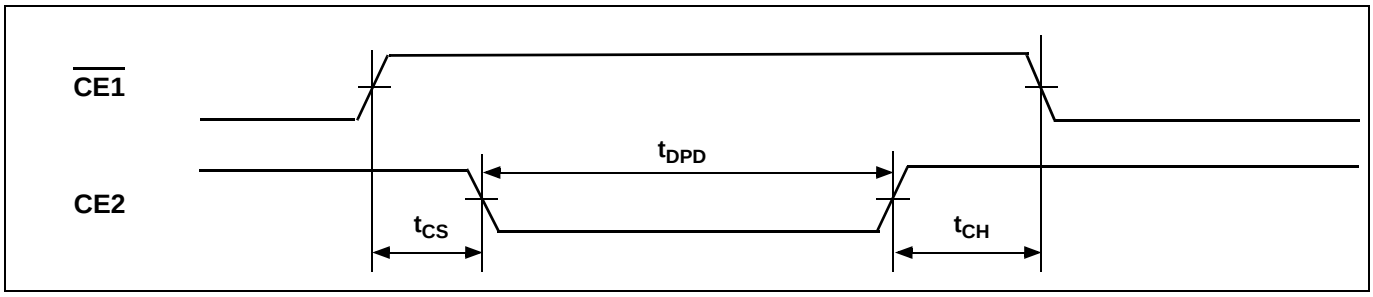
TIMING WAVEFORM OF WRITE CYCLE1 ($\overline{WE}$ CONTROLLED) (SEE NOTE 8)



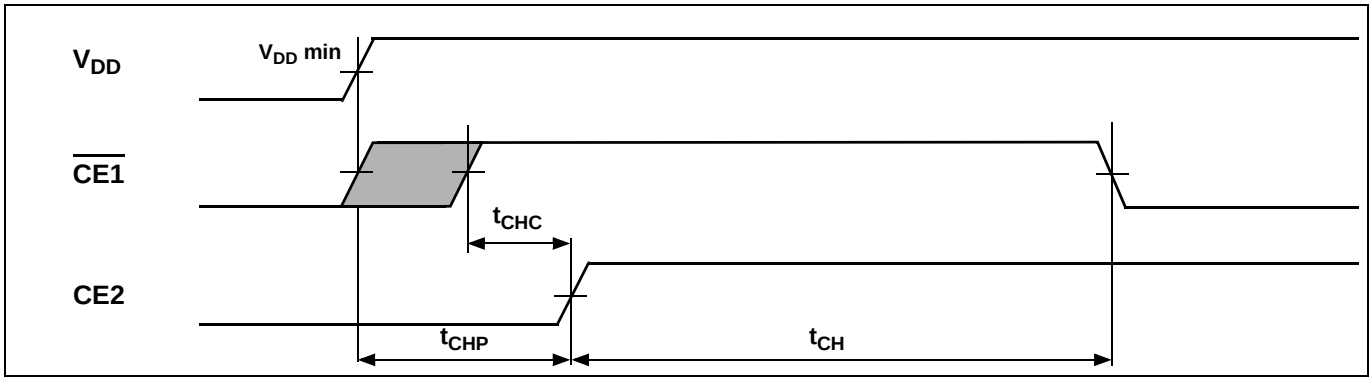
TIMING WAVEFORM OF WRITE CYCLE 2 ($\overline{CE}$ CONTROLLED) (SEE NOTE 8)



DEEP POWER-DOWN TIMING



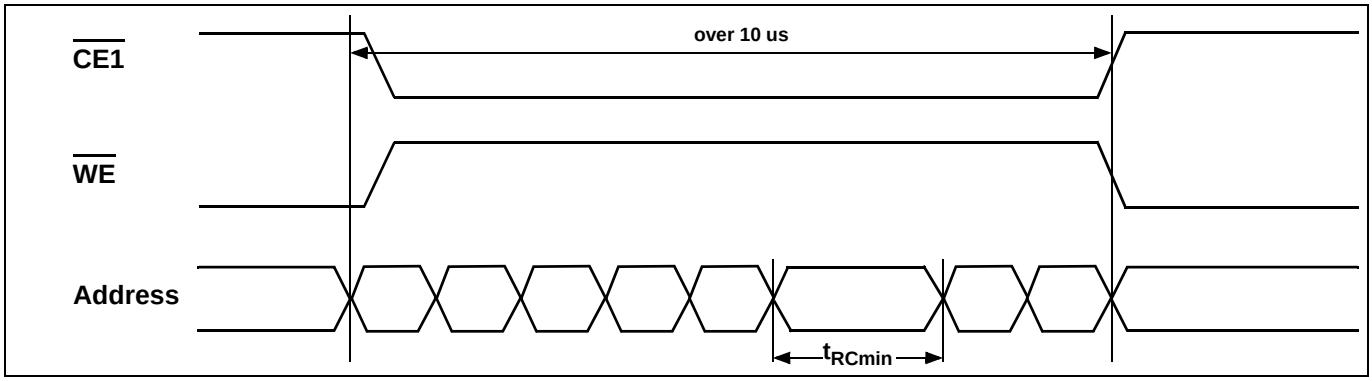
POWER_ON TIMING



PROVISIONS OF ADDRESS SKEW

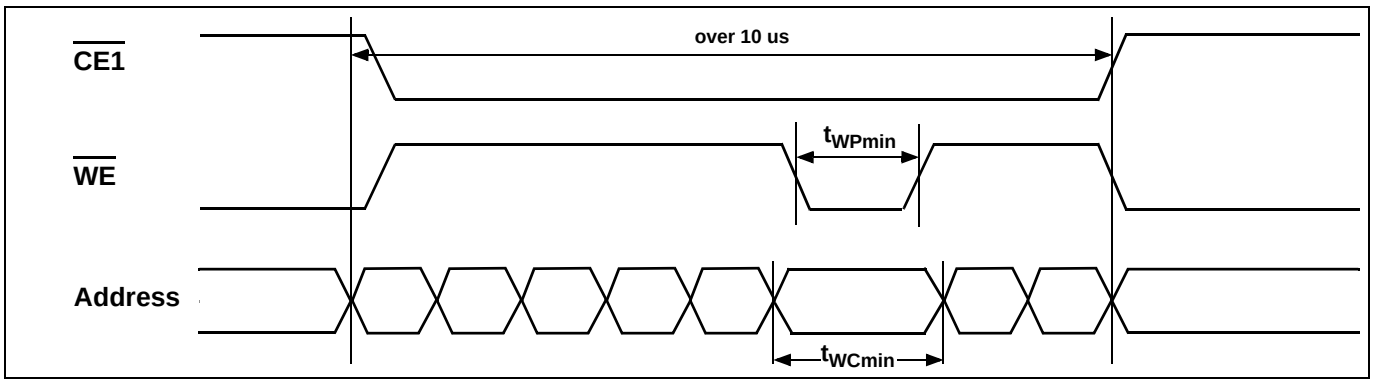
Read

In case, multiple invalid address cycles shorter than tRC_min sustain over 10us in a active status, as least one valid address cycle over tRC_min must be needed during 10us.



Write

In case, multiple invalid address cycles shorter than tWC_min sustain over 10us in a active status, as least one valid address cycle over tRC_min with tWP_min must be needed during 10us.



Notes :
1. Stresses greater than listed under “Absolute Maximum Ratings” may cause permanet damage to the device.
2. All voltages are reference to VSS.
3. IDD0 depends on the cycle time.
4. IDD0 depends on output loading. Specified values are defined with the output open condition.
5. AC measurement are assumed tR, tF = 5ns.
6. Parameters tOD, tODO, tBD and tODW define the time at which the output goes the open condition and are not output voltage reference levels
7. Data cannot be retained at deep power-down stand-by mode.
8. If $\overline{OE}$ is high during the write cycle, the outputs will remain at high impedence.
9. During the output state of DQ signals, input signals of reverse polarity must not be applied.
10. If $\overline{CE1}$ or $\overline{LB}$ / $\overline{UB}$ goes LOW coincident with or after $\overline{WE}$ goes LOW, the outputs will remain at high impedence.
11. If $\overline{CE1}$ or $\overline{LB}$./$\overline{UB}$ goes HIGH coincident with or before $\overline{WE}$ goes HIGH, the outputs will remain at high impedence.

MEMORY FUNCTION GUIDE

EM X XX X X X XX X X X - XX XX

1. EMLSI Memory
2. Device Type
3. Density
4. Function
5. Technology
6. Operating Voltage
7. Organization
8. Version
9. Option
10. PKG
11. Speed
12. Power

1. Memory Component

2. Device Type
- 6 ---------- Low Power SRAM
- 7 ---------- STRAM
- C ---------- CellularRAM

3. Density
- 4 ---------- 4M
- 8 ---------- 8M
- 16 ---------- 16M
- 32 ---------- 32M
- 64 ---------- 64M
- 28 ---------- 128M

4. Function
- 2 ----Multiplexed async.
- 3-----Demultiplexed async. with page mode
- 4-----Demultiplexed async. with direct DPD
- 5-----Multiplexed sync.
- 6-----Optional mux/demuxed sync.

5. Technology
- S ---------- Single Transistor & Trench Cell

6. Operating Voltage
- V ---------- 3.3V
- U ---------- 3.0V
- S ---------- 2.5V
- R ---------- 2.0V
- P ---------- 1.8V
- L ---------- 1.5V

7. Organization
- 8 ---------- x8 bit
- 16 ---------- x16 bit
- 32 ---------- x32 bit

8. Version
- Blank ---------- Mother die
- A ---------- 2'nd generation
- B ---------- 3'rd generation
- C ---------- 4'th generation
- D ---------- 5'th generation

9. Option
- Blank ---- No optional mode
- H ---------- Demultiplexed with DPD
- J ---------- Demultiplexed with DPD & RBC
- K ---------- Multiplexed with RBC
- L ---------- Multiplexed with DPD & RBC

10. Package
- Blank ---------- Wafer
- S ---------- 32 sTSOP1
- T ---------- 32 TSOP1
- U ---------- 44 TSOP2
- P ---------- 48 FPBGA
- Z ---------- 52 FPBGA
- Y ---------- 54 FPBGA
- V ---------- 90 FPBGA

11. Speed (@async.)
- 45 ---------- 45ns
- 55 ---------- 55ns
- 70 ---------- 70ns
- 85 ---------- 85ns
- 90 ---------- 90ns
- 10 ---------- 100ns
- 12 ---------- 120ns

12. Power
- LL ---------- Low Low Power
- LF ---------- Low Low Power (Pb-Free&Green)
- L ---------- Low Power