# TMP103 Low-Power, Digital Temperature Sensor With Two-Wire Interface in WCSP

## 1 Features

- Multiple Device Access (MDA):
  - Global Read/Write Operations
- $I^2C$™ and SMBus™-Compatible Interface
- Resolution: 8 Bits
- Accuracy: ±1°C Typical (–10°C to 100°C)
- Low Quiescent Current:
  - 3-µA Active $I_Q$ at 0.25 Hz
  - 1-µA Shutdown
- Supply Range: 1.4 V to 3.6 V
- Digital Output
- 4-Ball WCSP (DSBGA) Package

## 2 Applications

- Handsets
- Notebooks
- SSDs
- Servers
- Telecom
- Set Top Boxes
- Low Power Environmental
- Sensors

## 3 Description

The TMP103 is a digital output temperature sensor in a four-ball wafer chip-scale package (WCSP). The TMP103 is capable of reading temperatures to a resolution of 1°C.

The TMP103 features a two-wire interface that is compatible with both $I^2C$ and SMBus interfaces. In addition, the interface supports multiple device access (MDA) commands that allow the master to communicate with multiple devices on the bus simultaneously, eliminating the need to send individual commands to each TMP103 on the bus.

Up to eight TMP103s can be tied together in parallel and easily read by the host. The TMP103 is especially suitable for space-constrained, power-sensitive applications with multiple temperature measurement zones that must be monitored.

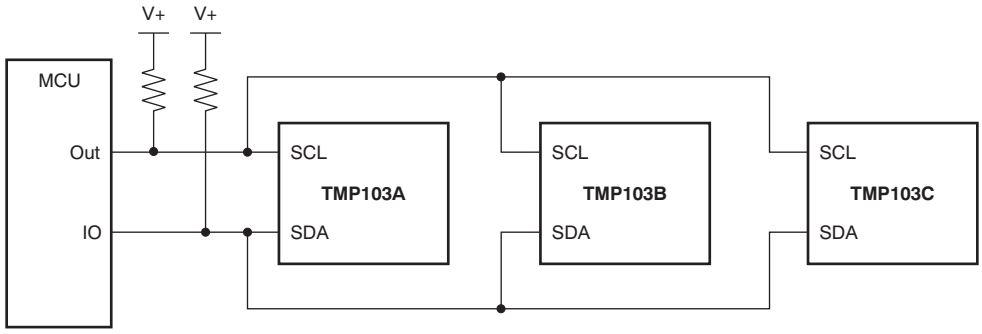
The TMP103 is specified for operation over a temperature range of –40°C to 125°C.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TMP103 | DSBGA (4) | 0.76 mm × 0.76 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Typical Application Diagram**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (March 2011) to Revision B** — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added SSDs, Servers, Telecom, Set Top Boxes, Low Power Environmental, and Sensors to *Applications* section ... 1

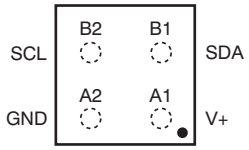
**Changes from Original (February 2011) to Revision A** — **Page**

- Changed Package-Lead from WCSP-4 to DSBGA-4 in *Device Information* table ... 1


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# 5 Pin Configurations and Functions

**YFF Package**
**4-Ball DSBGA**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| A1 | $V^+$ | I | Supply voltage |
| A2 | GND | I | Ground |
| B1 | SDA | I/O | Input/output data pin |
| B2 | SCL | I | Input clock pin |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V^+$ | Supply voltage | | 3.6 | V |
| | Input voltage(2) | –0.3 | ($V^+$) + 0.3 | V |
| | Operating temperature | –55 | 150 | °C |
| $T_J$ | Junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature | –60 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input voltage rating applies to all TMP103 input voltages.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | |
| | | Machine model (MM) | ±200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V^+$ | Supply voltage | 1.4 | 3.6 | V |
| $T_A$ | Operating free-air temperature | –40 | 125 | °C |

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## 6.4 Thermal Information

| THERMAL METRIC[1] | | TMP103 YFF (DSBGA) 4 BALLS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 160 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 75 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 76 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 74 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

at $T_A$ = 25°C and $V^+$ = 1.4 V to 3.6 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **TEMPERATURE INPUT** | | | | | | |
| Range | | | –40 | | 125 | °C |
| Accuracy (temperature error) | | –10°C to 100°C, $V^+$ = 1.8 V | –2 | 0 | 2 | °C |
| | | –40°C to 125°C, $V^+$ = 1.8 V | –3 | ±1 | 3 | °C |
| vs supply | | | –0.5 | ±0.2 | 0.5 | °C/V |
| Resolution | | | | 1 | | °C |
| **DIGITAL INPUT/OUTPUT** | | | | | | |
| Input logic levels | $V_{IH}$ | | 0.7 ($V^+$) | | $V^+$ | V |
| | $V_{IL}$ | | –0.5 | | 0.3 ($V^+$) | V |
| Input current | $I_{IN}$ | 0 < $V_{IN}$ < ($V^+$) + 0.3 V | | | 1 | µA |
| Output logic levels | $V_{OL}$ SDA | $V^+$ > 2 V, $I_{OL}$ = 2 mA | 0 | | 0.4 | V |
| | | $V^+$ < 2 V, $I_{OL}$ = 2 mA | 0 | | 0.2 ($V^+$) | V |
| Resolution | | | | 8 | | Bit |
| Conversion time | | | | 26 | 35 | ms |
| Conversion modes | | CR1 = 0, CR0 = 0 (default) | | 0.25 | | Conv/s |
| | | CR1 = 0, CR0 = 1 | | 1 | | Conv/s |
| | | CR1 = 1, CR0 = 0 | | 4 | | Conv/s |
| | | CR1 = 1, CR0 = 1 | | 8 | | Conv/s |
| Timeout time | | | | 30 | 40 | ms |
| **POWER SUPPLY** | | | | | | |
| Operating supply range | | | 1.4 | | 3.6 | V |
| Quiescent current | $I_Q$ | Serial bus inactive, CR1 = 0, CR0 = 0 (default), $V^+$ = 1.8 V | | 1.5 | 3 | µA |
| | | Serial bus active, SCL frequency = 400 kHz | | 15 | | µA |
| | | Serial bus active, SCL frequency = 3.4 MHz | | 85 | | µA |
| Shutdown current | $I_{SD}$ | Serial bus inactive, $V^+$ = 1.8 V | | 0.5 | 1 | µA |
| | | Serial bus active, SCL frequency = 400 kHz | | 10 | | µA |
| | | Serial bus active, SCL frequency = 3.4 MHz | | 80 | | µA |
| **TEMPERATURE** | | | | | | |
| Specified range | | | –40 | | 125 | °C |
| Operating range | | | –55 | | 150 | °C |


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## 6.6 Timing Requirements

See (1)

| | | FAST MODE | | HIGH-SPEED MODE | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $f_{(SCL)}$ | SCL operating frequency, $V_S$ > 1.7 V | 0.001 | 0.4 | 0.001 | 3.4 | MHz |
| $f_{(SCL)}$ | SCL operating frequency, $V_S$ < 1.7 V | 0.001 | 0.4 | 0.001 | 2.75 | MHz |
| $t_{(BUF)}$ | Bus free time between STOP and START condition | 600 | | 160 | | ns |
| $t_{(HDSTA)}$ | Hold time after repeated START condition. After this period, the first clock is generated. | 100 | | 100 | | ns |
| $t_{(SUSTA)}$ | Repeated START condition setup time | 100 | | 100 | | ns |
| $t_{(SUSTO)}$ | STOP condition setup Time | 100 | | 100 | | ns |
| $t_{(HDDAT)}$ | Data hold time | 20 | 400 | 10 | 125 | ns |
| $t_{(SUDAT)}$ | Data setup time | 100 | | 10 | | ns |
| $t_{(LOW)}$ | SCL clock low period, $V_S$ > 1.7 V | 1300 | | 160 | | ns |
| $t_{(LOW)}$ | SCL clock low period, $V_S$ < 1.7 V | 1300 | | 200 | | ns |
| $t_{(HIGH)}$ | SCL clock high period | 600 | | 60 | | ns |
| $t_F$ | Clock/data fall time | | 300 | | | ns |
| $t_R$ | Clock/data rise time | | 300 | | 160 | ns |
| $t_R$ | Clock/data rise time for SCLK ≤ 100 kHz | | 1000 | | | ns |

(1) Values based on a statistical analysis of a one-time sample of devices. Minimum and maximum values are not guaranteed and not production tested.

The TMP103 is two-wire and SMBus compatible. Figure 1 to Figure 5 describe the various operations on the TMP103. Parameters for Figure 1 are defined in Timing Requirements. Bus definitions are:

**Bus Idle:** Both SDA and SCL lines remain high.

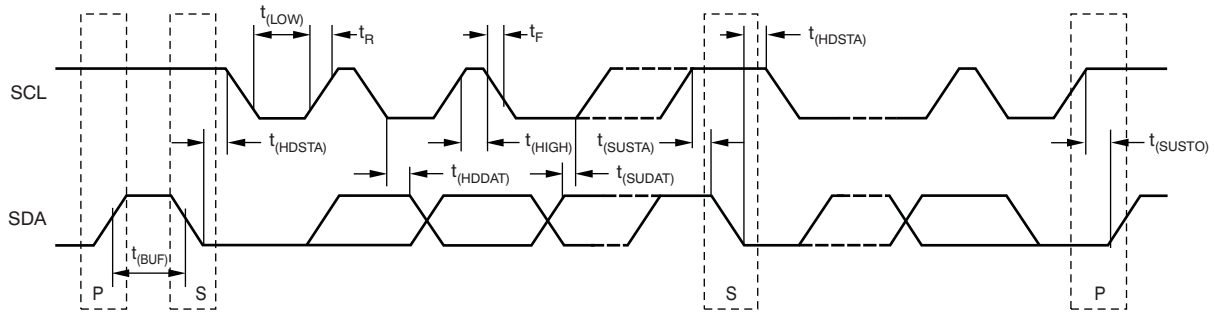
**Start Data Transfer:** A change in the state of the SDA line, from high to low, while the SCL line is high, defines a START condition. Each data transfer is initiated with a START condition.

**Stop Data Transfer:** A change in the state of the SDA line from low to high while the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

**Data Transfer:** The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device.

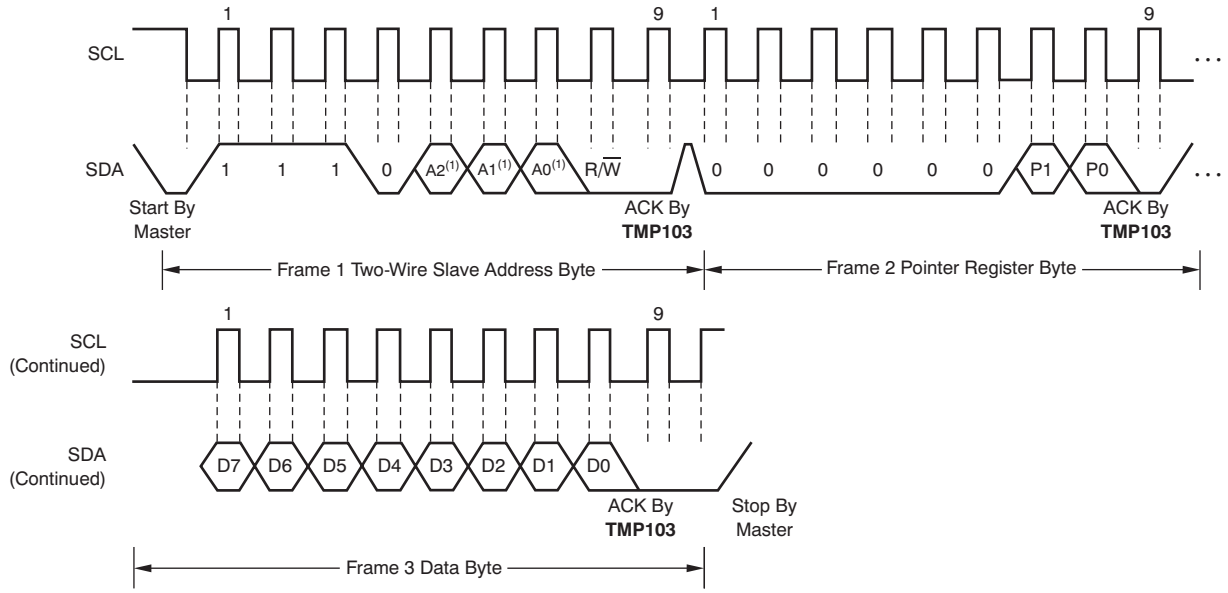
**Acknowledge:** Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a *Not-Acknowledge* (1) on the last byte transmitted by the slave.

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NOTE: P = STOP, S = START.

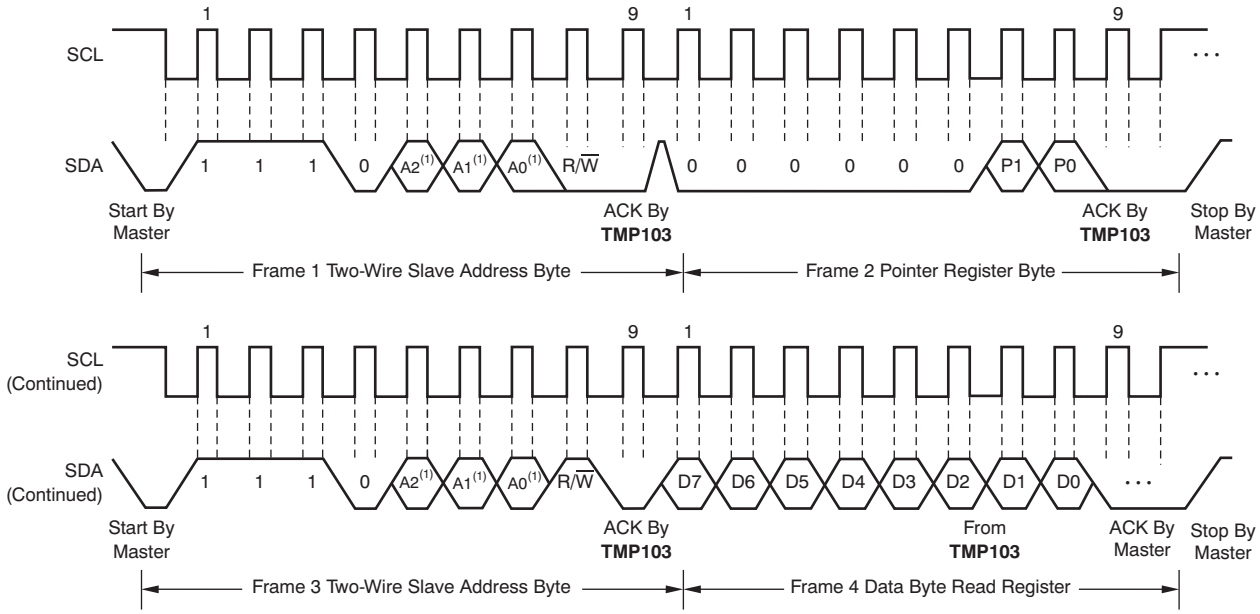
**Figure 1. Two-Wire Timing Diagram**




(1) The value of A0, A1, and A2 are determined by the TMP103 version; see Table 2.

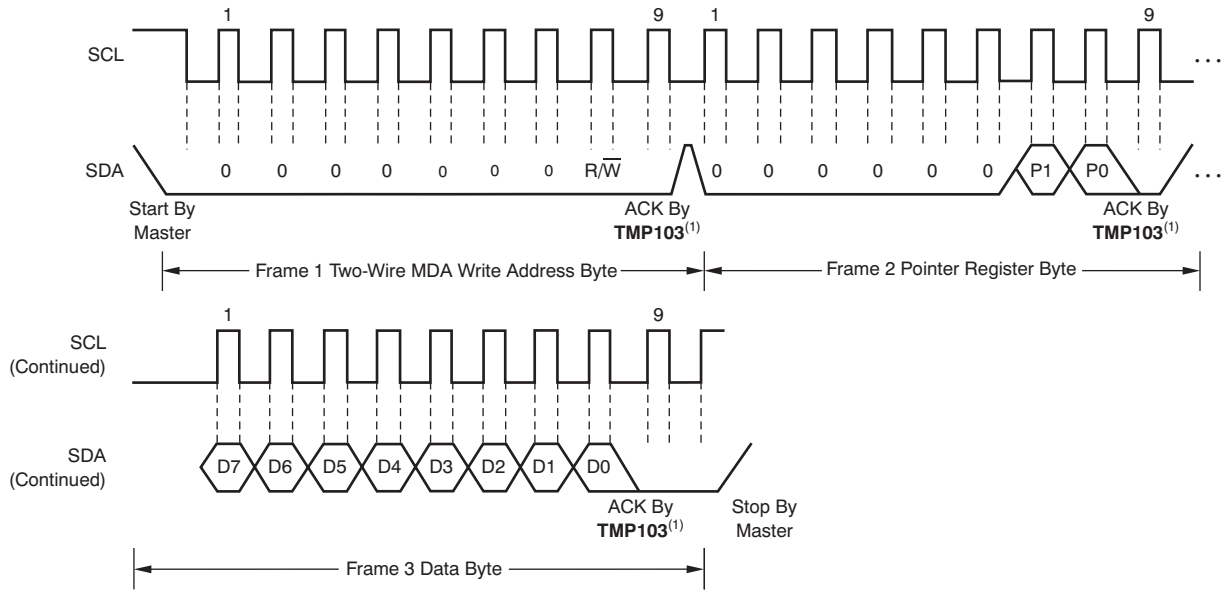
**Figure 2. Two-Wire Timing Diagram for Write Word Format**


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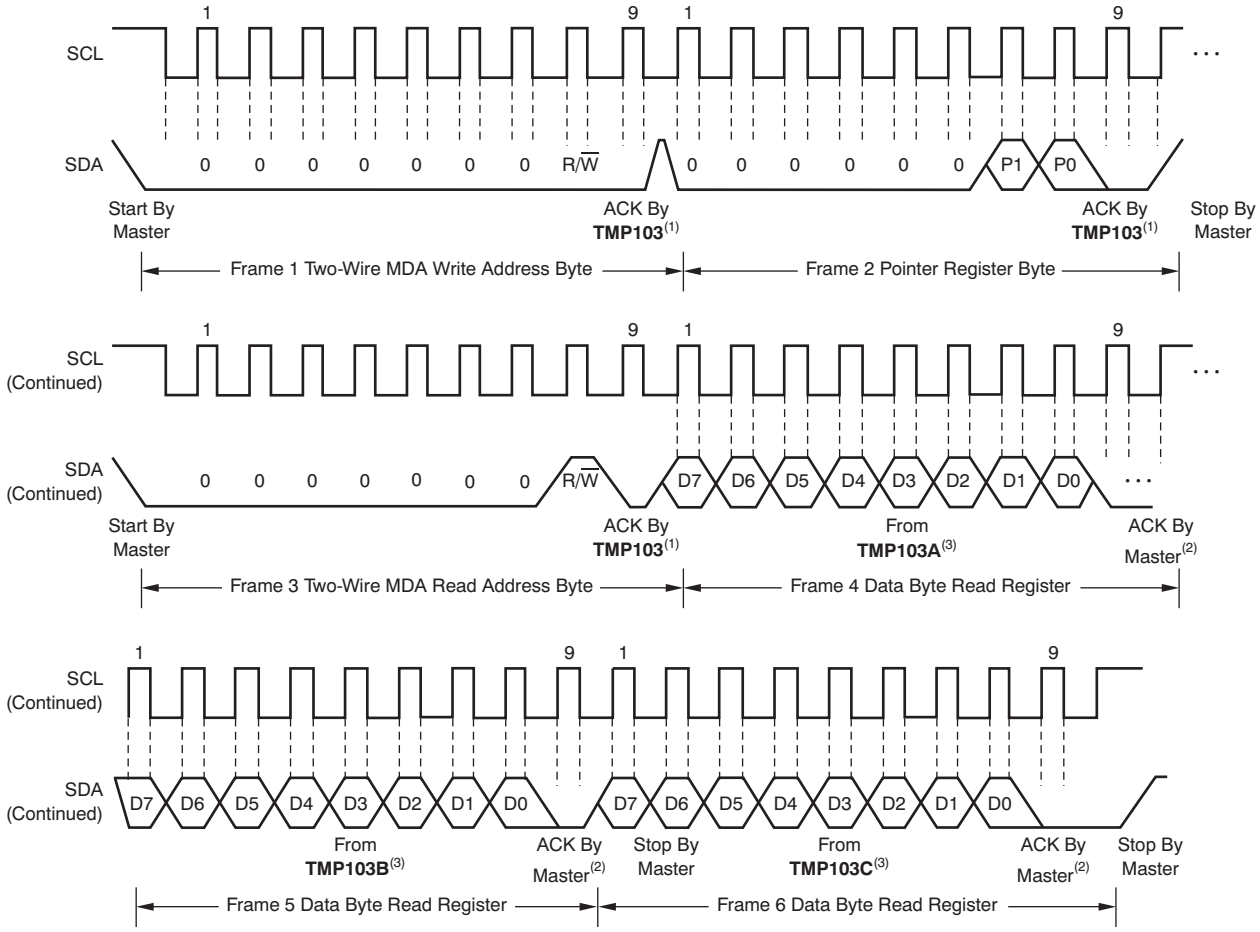

(1) The value of A0, A1, and A2 are determined by the TMP103 version; see Table 2.

**Figure 3. Two-Wire Timing Diagram for Read Word Format**




(1) All TMP103 devices on the bus acknowledge the byte.

**Figure 4. Two-Wire Timing Diagram MDA Write Word Format**




(1) All TMP103 devices on the bus acknowledge the byte.

(2) The master must issue an acknowledge for each byte read to read all of the TMP103 devices on the bus.

(3) Three TMP103 devices used in this case; up to eight devices can be used (see Table 2).

**Figure 5. Two-Wire Timing Diagram MDA Read Word Format Using Figure 16 (Typical Application)**


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## 6.7 Typical Characteristics

At $T_A$ = 25°C and $V^+$ = 1.8 V, unless otherwise noted.

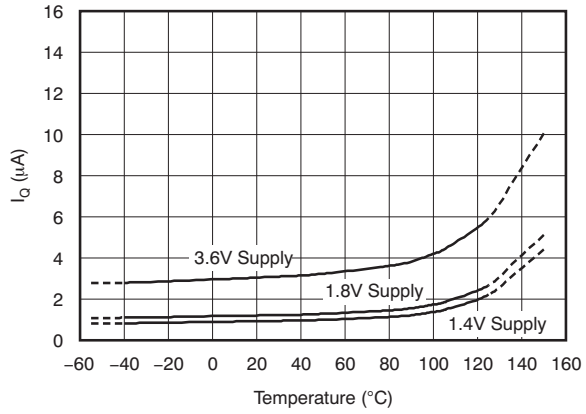



**Figure 6. Quiescent Current vs Temperature (0.25 Conversions Per Second)**

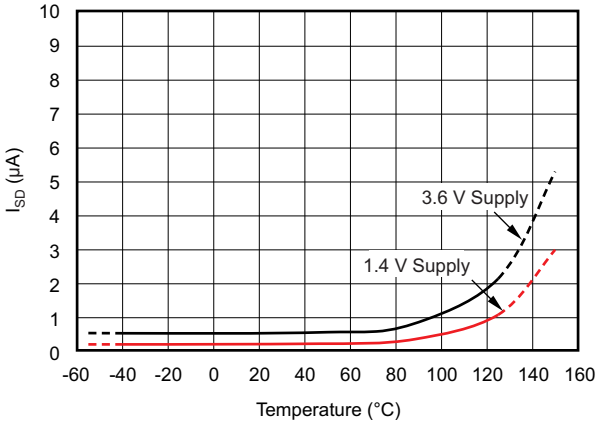



**Figure 7. Shutdown Current vs Temperature**

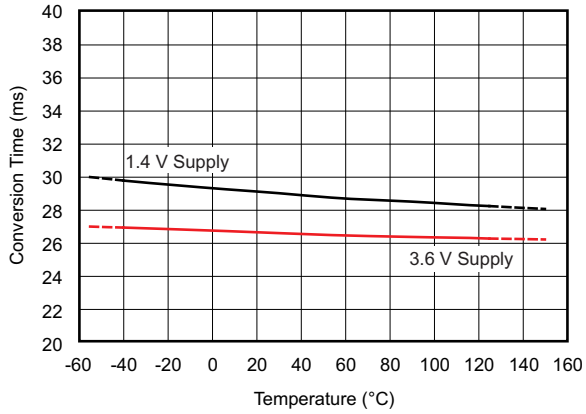



**Figure 8. Conversion Time vs Temperature**

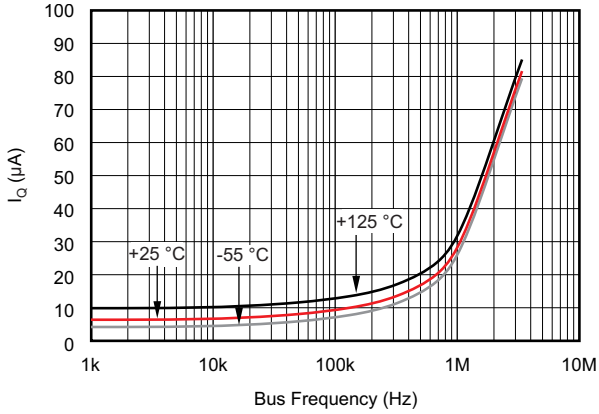



**Figure 9. Quiescent Current vs Bus Frequency (Temperature at 3.3-V Supply)**

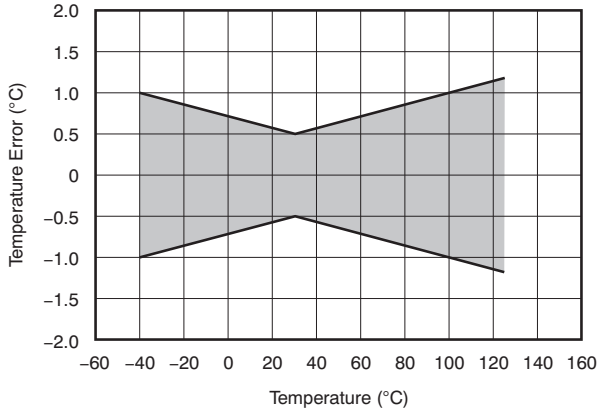



**Figure 10. Temperature Error vs Temperature**

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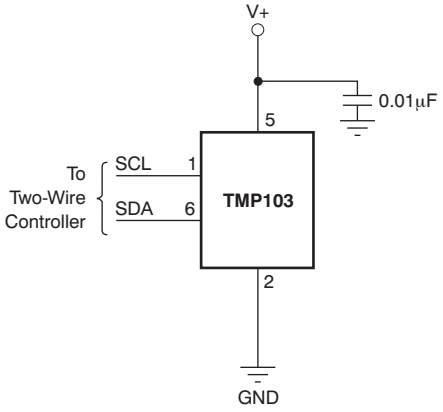
# 7 Detailed Description

## 7.1 Overview

The TMP103 is a digital output temperature sensor in a wafer chip-scale package (WCSP) that is optimal for thermal management and thermal profiling. The TMP103 includes a two-wire interface that is compatible with both $I^2C$ and SMBus interfaces. In addition, the TMP103 has the capability of executing multiple device access (MDA) commands that allow multiple TMP103 devices to respond to a single global bus command. MDA commands reduce communication time and power in a bus that contains multiple TMP103 devices. The TMP103 is specified over a temperature range of –40ºC to 125 ºC.

The TMP103 serial interface is designed to support up to eight TMP103 devices on a single bus. The TMP103 is offered with eight internal interface addresses. Each unique address option can be used as a location or temperature zone designator. The TMP103 responds to standard $I^2C$ and SMBus slave protocols that allow the internal registers to be written to or read from on an individual basis. The TMP103 also responds to MDA commands that allow all the devices on the bus to be written to or read from, without having to send the individual address and commands to each device.

Pullup resistors are required on SCL and SDA. TI also recommends a 0.01-µF bypass capacitor, as shown in Figure 11.



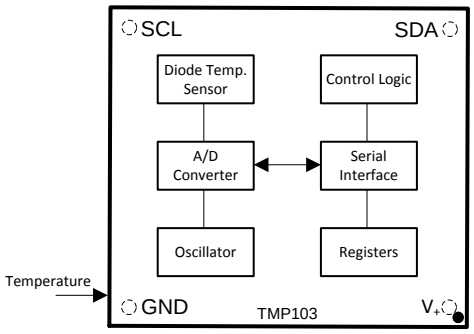

NOTE: SCL and SDA pins require pullup resistors.

**Figure 11. Typical Connections**

The temperature sensor in the TMP103 is the chip itself. Thermal paths run through the package bumps as well as the package. The lower thermal resistance of metal causes the bumps to provide the primary thermal path.

To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package from ambient air temperature.

## 7.2 Functional Block Diagram





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## 7.3 Feature Description

The TMP103 is a 1°C resolution digital output temperature sensor offered in a four-ball wafer chip-scale package (WCSP). The TMP103 features a two-wire interface that is compatible with both $I^2C$ and SMBus interfaces.

The serial interface supports multiple device access (MDA) commands that allow the master to communicate with multiple devices on the bus simultaneously, eliminating the need to send individual commands to each TMP103 device on the bus. Up to eight TMP103 devices can be tied together in parallel and easily read by the host.

The TMP103 is an ideal choice for space-constrained and power-sensitive applications with multiple temperature measurement zones to be monitored.

## 7.4 Device Functional Modes

### 7.4.1 Shutdown Mode

Shutdown mode saves maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 0.5 µA. For details on how to enter shutdown mode, see *Shutdown Mode (M1 = 0, M0 = 0)* in *Programming*.

### 7.4.2 One-Shot Mode

The TMP103 features a One-Shot Temperature Measurement mode. When the device is in Shutdown mode, the device can be instructed to complete a one-time temperature measurement before returning to the shutdown state. This feature is useful for reducing power consumption in the TMP103 when continuous temperature monitoring is not required.

As a result of the short conversion time, the TMP103 can achieve a higher conversion rate. A single conversion typically takes 26 ms and a read can take place in less than 20 µs. When using One-Shot mode, 30 or more conversions per second are possible.

For details on how to enter One-Shot mode, see *One-Shot (M1 = 0, M0 = 1)* in *Programming*.

### 7.4.3 Continuous Conversion Mode

In Continuous Conversion mode, the TMP103 performs temperature conversion at a rate determined by the conversion rate bits (CR1 and CR0) set in the configuration register. Because the actual temperature conversion takes only 26 mS, the TMP103 powers down in between conversions and waits for the appropriate delay. For details on how to enter One-Shot mode, see *Continuous Conversion Mode (M1 = 1)* and *Conversion Rate* in *Programming*.

## 7.5 Programming

### 7.5.1 Temperature Watchdog Function

The TMP103 contains a watchdog function that monitors device temperature and compares the result to the values stored in the temperature limit registers ($T_{HIGH}$ and $T_{LOW}$) to determine if the device temperature is within these set limits. If the temperature of the TMP103 becomes greater than the value in the $T_{HIGH}$ register, then the flag-high bit (FH) in the configuration register is set to 1. If the temperature falls below the value in the $T_{LOW}$ register, then the flag-low bit (FL) is set to 1. If both flag bits remain 0, then the temperature is within the temperature *window* set by the temperature limit registers, as shown in Figure 12.

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## Programming (continued)

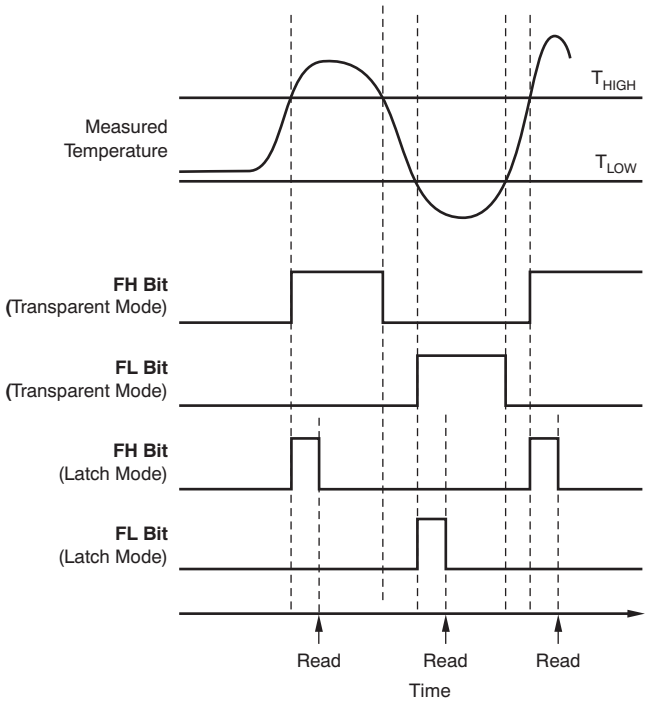



**Figure 12. Temperature Flag Functional Diagram**

The latch bit (LC) in the configuration register is used to latch the value of the flag bits (FH and FL) until the master issues a read command to the configuration register. The flag bits are set to 0 if a read command is received by the TMP103, or if LC = 0 and the temperature is within the temperature limits. The power-on default values for these bits are FH = 0, FL = 0, and LC = 0.

### 7.5.2 Conversion Rate

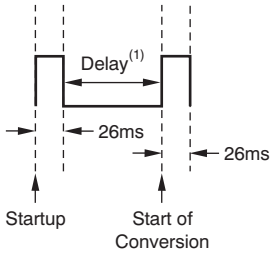
The conversion rate bits, CR1 and CR0 located in the Configuration Register, configure the TMP103 for conversion rates of 8 Hz, 4 Hz, 1 Hz, or 0.25 Hz (default). The TMP103 has a typical conversion time of 26 ms. To achieve different conversion rates, the TMP103 performs a single conversion and then powers down and waits for the appropriate delay set by CR1 and CR0. Table 1 lists the settings for CR1 and CR0.

**Table 1. Conversion Rate Settings**

| CR1 | CR0 | CONVERSION RATE |
|---|---|---|
| 0 | 0 | 0.25 Hz (default) |
| 0 | 1 | 1 Hz |
| 1 | 0 | 4 Hz |
| 1 | 1 | 8 Hz |


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After power up or general-call reset, the TMP103 immediately starts a conversion, as shown in Figure 13. The first result is available after 26 ms (typical). The active quiescent current during conversion is 40 µA (typical at 27°C, $V^+$ = 1.8 V). The quiescent current during delay is 1 µA (typical at 27°C, $V^+$ = 1.8 V).




(1) Delay is set by CR1 and CR0.

**Figure 13. Conversion Start**

### 7.5.3 Shutdown Mode (M1 = 0, M0 = 0)

Shutdown mode saves maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 0.5 µA. Shutdown mode is enabled when bits M1 and M0 (in the Configuration Register) = 00. The device shuts down when the current conversion is completed.

### 7.5.4 One-Shot (M1 = 0, M0 = 1)

The TMP103 features a One-Shot Temperature Measurement mode. When the device is in Shutdown mode, writing a 01 to bits M1 and M0 starts a single temperature conversion. During the conversion, bits M1 and M0 read 01. The device returns to the shutdown state at the completion of the single conversion. After the conversion, bits M1 and M0 read 00. This feature is useful for reducing power consumption in the TMP103 when continuous temperature monitoring is not required.

As a result of the short conversion time, the TMP103 can achieve a higher conversion rate. A single conversion typically takes 26 ms and a read can take place in less than 20 µs. When using One-Shot mode, 30 or more conversions per second are possible.

### 7.5.5 Continuous Conversion Mode (M1 = 1)

When the TMP103 is in Continuous Conversion mode (M1 = 1), a single conversion is performed at a rate determined by the conversion rate bits, CR1 and CR0 (in the Configuration Register). The TMP103 performs a single conversion and then powers down and waits for the appropriate delay set by CR1 and CR0. See Table 1 for CR1 and CR0 settings.

### 7.5.6 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data line (SDA) from a high to low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of the clock, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge Bit. During data transfer, SDA must remain stable while SCL is high, because any change in SDA while SCL is high is interpreted as a START or STOP signal.

Once all data have been transferred, the master generates a STOP condition indicated by pulling SDA from low to high, while SCL is high.

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### 7.5.7 Serial Interface

The TMP103 operates as a slave device only on the two-wire bus and SMBus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP103 supports the transmission protocol for both fast (1 kHz to 400 kHz) and high-speed (1 kHz to 3.4 MHz) modes. All data bytes are transmitted MSB first.

### 7.5.8 Serial Bus Address

To communicate with the TMP103, the master must first address slave devices through a slave address byte. The slave address byte consists of seven address bits, and a direction bit that indicates the intent of executing a read or write operation.

The TMP103 is available in eight versions, each with a different slave address, as shown in Table 2. These addresses can be used as either a location or a temperature zone designator.

**Table 2. Device Slave Addresses**

| PRODUCT | TWO-WIRE ADDRESS | TEMPERATURE ZONE |
|---|---|---|
| TMP103A | 1110000 | Zone1 |
| TMP103B | 1110001 | Zone2 |
| TMP103C | 1110010 | Zone3 |
| TMP103D | 1110011 | Zone4 |
| TMP103E | 1110100 | Zone5 |
| TMP103F | 1110101 | Zone6 |
| TMP103G | 1110110 | Zone7 |
| TMP103H | 1110111 | Zone8 |

### 7.5.9 Writing and Reading Operation

Accessing a particular register on the TMP103 is accomplished by writing the appropriate value to the Pointer Register. The value for the Pointer Register is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the TMP103 requires a value for the Pointer Register (see Figure 2).

When reading from the TMP103, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer Register. This action is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit low, followed by the Pointer Register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. See Figure 3 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the Pointer Register bytes; the TMP103 remembers the Pointer Register value until it is changed by the next write operation, or the TMP103 is reset.

### 7.5.10 Slave Mode Operations

The TMP103 can operate as a slave receiver or slave transmitter. As a slave device, the TMP103 never drives the SCL line.

#### *7.5.10.1 Slave Receiver Mode*

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit low. The TMP103 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer Register. The TMP103 then acknowledges reception of the Pointer Register byte. The next byte is written to the register addressed by the Pointer Register. The TMP103 acknowledges reception of the data byte. The master can terminate data transfer by generating a START or STOP condition.


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#### 7.5.10.2 Slave Transmitter Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave of the register indicated by the Pointer Register. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a *Not-Acknowledge* on reception of the data byte, or generating a START or STOP condition.

### 7.5.11 General Call

The TMP103 responds to a two-wire General Call address (0000000) if the eighth bit is 0. The device acknowledges the General Call address and responds to commands in the second byte. If the second byte is 00000110, the TMP103 internal registers are reset to power-up values. The TMP103 does not support the General Address acquire command.

### 7.5.12 High-Speed (Hs) Mode

For the two-wire bus to operate at frequencies greater than 400 kHz, the master device must issue an Hs-mode master code (00001xxx) as the first byte after a START condition to switch the bus to high-speed operation. The TMP103 does not acknowledge this byte, but switches its input filters on SDA and SCL and its output filters on SDA to operate in Hs-mode, allowing transfers at up to 3.4 MHz. After the Hs-mode master code has been issued, the master transmits a START condition followed by a two-wire slave address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP103 switches the input and output filters back to the default fast-mode operation.

### 7.5.13 Timeout Function

The TMP103 resets the serial interface if SCL is held low for 30 ms (typical). The TMP103 releases the bus if it is pulled low and waits for a START condition. To avoid activating the timeout function, it is necessary to maintain a communication speed of at least 1 kHz for SCL operating frequency.

### 7.5.14 Multiple Device Access

The TMP103 supports Multiple Device Access (MDA), which allows the master to communicate with multiple TMP103 devices on the same bus interface with one interface transaction. MDA commands consist of an MDA read address (00000001) and an MDA write address (00000000). The device acknowledges the MDA address and responds to the command accordingly. For the MDA to function correctly, different product versions of the TMP103 must be used in the system; see Table 2.

#### 7.5.14.1 Multiple Device Access Write

The master transmits an MDA write address followed by the pointer address of the register to be accessed; see Table 4. Following the pointer, all of the TMP103 devices on the bus acknowledge and wait for the next byte of data to be written to the addressed registers. When the data byte is received by the TMP103 devices, they store and acknowledge the transmitted byte. The TMP103 devices store the same data on all devices on the bus in one transaction; see Figure 4.

#### 7.5.14.2 Multiple Device Access Read

Before an MDA read transaction can begin, the master must first send an MDA write transaction to set the appropriate pointer address of the register to be accessed, as stated in the previous section. The master can then transmit an MDA read address followed by a read byte for each TMP103 used on the bus. For example, if a TMP103A and TMP103B are used on the same bus and an MDA read address is sent, the address must be followed by two bytes of data and two master acknowledges. The TMP103A sends data on the first byte and the TMP103B sends data on the second byte. The master must issue an acknowledge for each byte read to read all of the TMP103 devices on the bus; see Figure 5. If the master does not acknowledge each byte of data, the TMP103s stop sending subsequent data for any remaining devices.

Up to eight TMP103 devices can be on the same bus and respond to MDA commands; see Table 2.

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**NOTE**

If the bus contains an incomplete sequence of TMP103 device addresses, the master must transmit all required dummy bytes for the missing device address to allow for normal MDA read operation. For example, if the TMP103A, TMP103B, and TMP103D devices are on the bus, the master must transmit an MDA read address followed by four bytes and four acknowledges to complete the MDA read transaction.

### 7.5.15 NOISE

The TMP103 is a very low-power device and generates very low noise on the supply bus. Applying an RC filter to the $V^+$ pin of the TMP103 can further reduce any noise the TMP103 might propagate to other components. $R_F$ in Figure 14 should be less than 5 kΩ and $C_F$ should be greater than 10 nF.

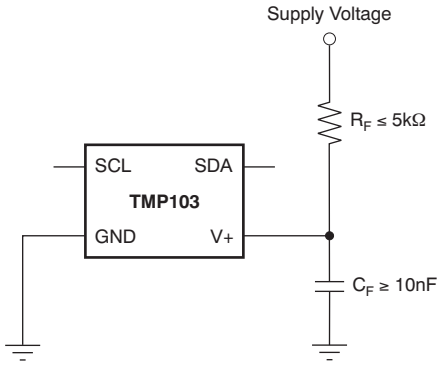



**Figure 14. Noise Reduction**

## 7.6 Register Maps

### 7.6.1 Pointer Register

Figure 15 shows the internal register structure of the TMP103. The 8-bit Pointer Register of the device is used to address a given data register. The Pointer Register uses the two LSBs to identify which of the data registers should respond to a read or write command. Table 3 identifies the bits of the Pointer Register byte. During a write command, P2 through P7 must always be 0. Table 4 describes the pointer address of the registers available in the TMP103. Power-up reset value of P1/P0 is 00. By default, the TMP103 reads the temperature on power up.

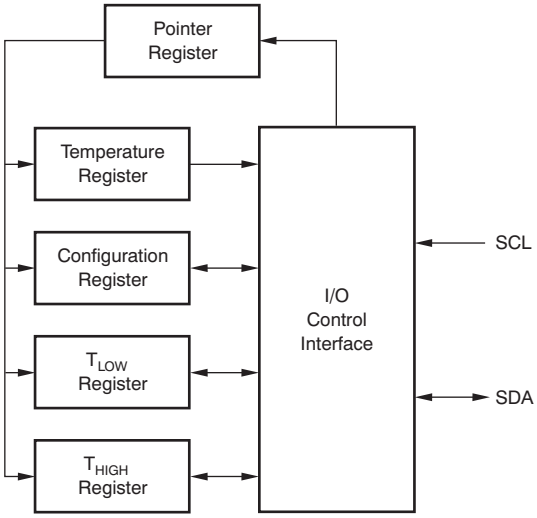



**Figure 15. Internal Register Structure**


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## Register Maps (continued)

**Table 3. Pointer Register Byte**

| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | Register Bits | |

**Table 4. Pointer Addresses**

| P1 | P0 | REGISTER |
|---|---|---|
| 0 | 0 | Temperature Register (Read Only) |
| 0 | 1 | Configuration Register (Read/Write) |
| 1 | 0 | $T_{LOW}$ Register (Read/Write) |
| 1 | 1 | $T_{HIGH}$ Register (Read/Write) |

### 7.6.2 Temperature Register

The Temperature Register of the TMP103 device is configured as an eight-bit, read-only register that stores the output of the most recent conversion. A single byte must be read to obtain data, and is described in Table 5. The data format for temperature is summarized in Table 6. One LSB equals 1°C.

**Table 5. Temperature Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |

Negative numbers are represented in binary twos complement format. Following power up or reset, the Temperature Register reads 0°C until the first conversion is complete.

**Table 6. 8-Bit Temperature Data Format(1)**

| TEMPERATURE (°C) | DIGITAL OUTPUT (BINARY) | HEX |
|---|---|---|
| 128 | 0111 1111 | 7F |
| 127 | 0111 1111 | 7F |
| 100 | 0110 0100 | 64 |
| 80 | 0101 0000 | 50 |
| 75 | 0100 1011 | 4B |
| 50 | 0011 0010 | 32 |
| 25 | 0001 1001 | 19 |
| 0 | 0000 0000 | 00 |
| –1 | 1111 1111 | FF |
| –25 | 1110 0111 | E7 |
| –55 | 1100 1001 | C9 |

(1) The resolution for the ADC is 1°C/count, where *count* is equal to the digital output of the ADC.

For positive temperatures (for example, 50°C):

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code, left-justified format. Denote a positive number with MSB = 0.

Example: (50°C)/(1°C/count) = 50 = 32h = 0011 0010

For negative temperatures (for example, –25°C):

Generate the twos complement of a negative number by complementing the absolute value binary number and adding 1. Denote a negative number with MSB = 1.

Example: (|–25°C|)/(1°C/count) = 25 = 19h = 0001 1001

Twos complement format: 1110 0110 + 1 = 1110 0111

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### 7.6.3 Configuration Register

The Configuration Register is an eight-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. The format and power-up and reset value of the Configuration Register is shown in Table 7. All registers are updated at the end of the data byte.

**Table 7. Configuration and Power-Up and Reset Format**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| ID | CR1 | CR0 | FH | FL | LC | M1 | M0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

### 7.6.4 Temperature Limit Registers

The $T_{HIGH}$ and $T_{LOW}$ registers are used to store the temperature limit thresholds for the TMP103 watchdog function. At the end of each temperature measurement, the TMP103 compares the temperature results to each of these limits. If the temperature result is greater than the $T_{HIGH}$ limit, then the FH bit in the configuration register is set to 1. If the temperature result is less than the $T_{LOW}$ limit, then the FL bit in the configuration register is set to 1; see Figure 12.

Table 8 and Table 9 describe the format for the $T_{HIGH}$ and $T_{LOW}$ registers. Power-up reset values for $T_{HIGH}$ and $T_{LOW}$ are: $T_{HIGH}$ = 60°C and $T_{LOW}$ = –10°C. The format of the data for $T_{HIGH}$ and $T_{LOW}$ is the same as for the Temperature Register.

**Table 8. $T_{HIGH}$ Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| H7 | H6 | H5 | H4 | H3 | H2 | H1 | H0 |

**Table 9. $T_{LOW}$ Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| L7 | L6 | L5 | L4 | L3 | L2 | L1 | L0 |


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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TMP103 is a digital output temperature sensor in a DSBGA package that is optimal for thermal management and thermal profiling. The TMP103 includes a two-wire interface that is compatible with both $I^2C$ and SMBus interfaces. In addition, the TMP103 has the capability of executing multiple device access (MDA) commands that allows multiple TMP103 devices to respond to a single global bus command. MDA commands reduce communication time and power in a bus that contains multiple TMP103 devices. The TMP103 is specified over a temperature range of –40ºC to 125ºC.

The TMP103 serial interface is designed to support up to eight TMP103 devices on a single bus. The TMP103 is offered with eight internal interface addresses. Each unique address option can be used as a location or temperature zone designator. The TMP103 responds to standard $I^2C$ and SMBus slave protocols that allow the internal registers to be written to or read from on an individual basis. The TMP103 also responds to MDA commands that allow all the devices on the bus to be written to or read from, without having to send the individual address and commands to each device.

## 8.2 Typical Application

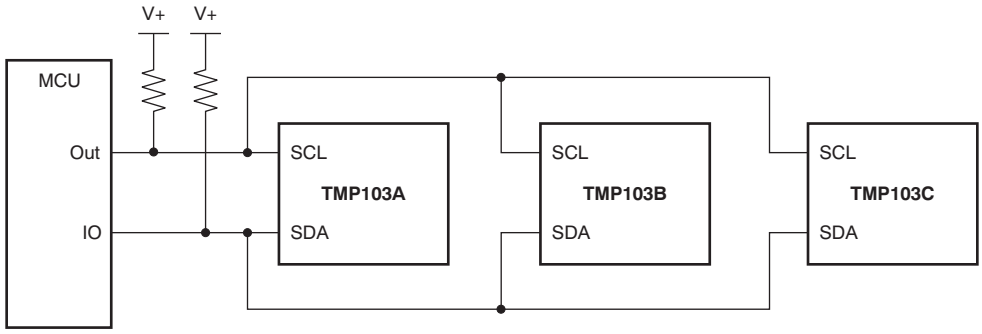



**Figure 16. Typical Application Diagram**

### 8.2.1 Design Requirements

The TMP103 device requires pullup resistors on the SCL and SDA pins. The pullup resistor values must be selected such that the maximum current sinking capability of I/O pins is not violated. TI recommends a 0.01-µF bypass capacitor on the supply.

### 8.2.2 Detailed Design Procedure

The TMP103 devices must be placed in close proximity to the heat source that must be monitored, with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package and leads from ambient air temperature. The TMP103 device is a very low-power device and generates very low noise on the supply bus. Applying an RC filter to the $V^+$ pin of the TMP103 device can further reduce any noise that the TMP103 device might propagate to other components.

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## Typical Application (continued)

### 8.2.3 Application Curve

Table 9 shows the step response of the TMP103 device to a submersion in an oil bath of 100ºC from room temperature (25ºC). The time-constant, or the time for the output to reach 63% of the input step, is 1.4 s. The time-constant result depends on the printed-circuit-board (PCB) that the TMP103 device is mounted. For this test, there are eight TMP103 devices soldered to a two-layer PCB that measured 2 in × 2 in, and the PCB thickness is 64 mils.

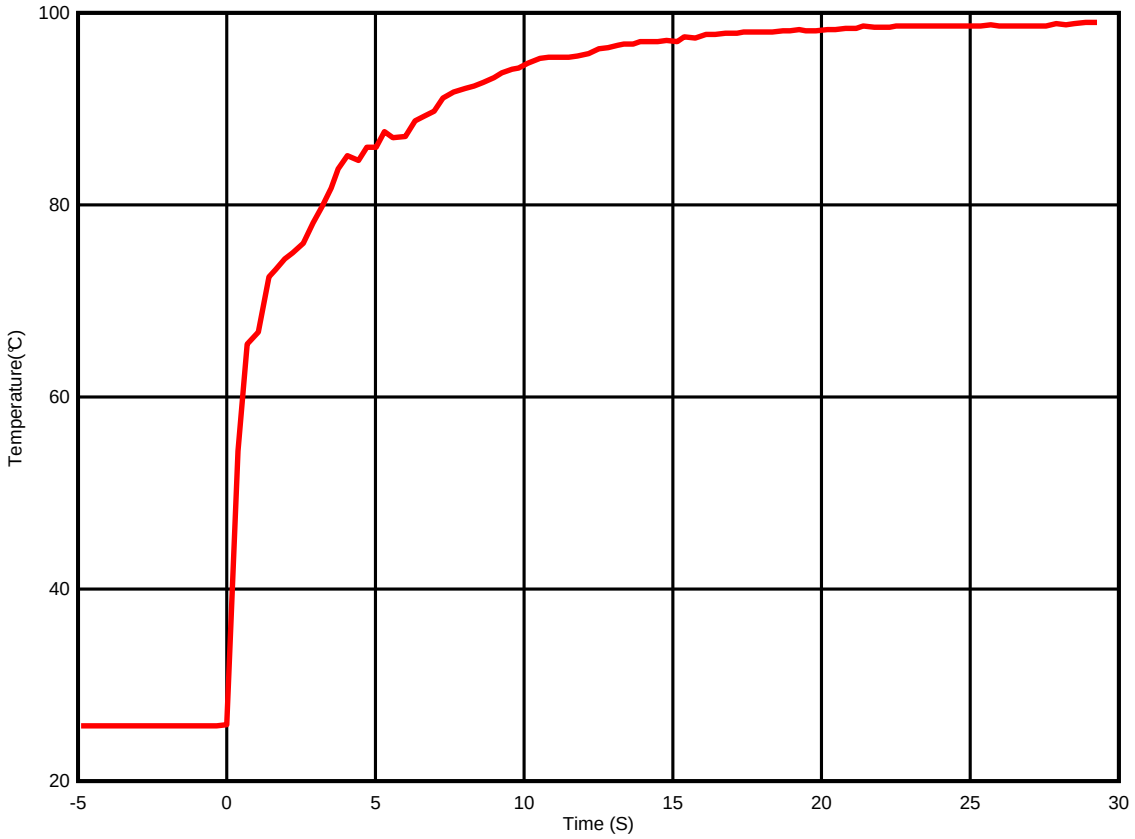



**Figure 17. Temperature vs Time**


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# 9 Power Supply Recommendations

The TMP103 device operates with power supply in the range of 1.4 V to 3.6 V. The device is optimized for operation at 3.3-V supply but can measure temperature accurately in the full supply range. A power-supply bypass capacitor is required for proper operation. Place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

# 10 Layout

## 10.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply pin. The recommended value of this bypass capacitor is 0.01 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. Pull up the SDA and SCL pins through 5-kΩ pullup resistors.

## 10.2 Layout Example

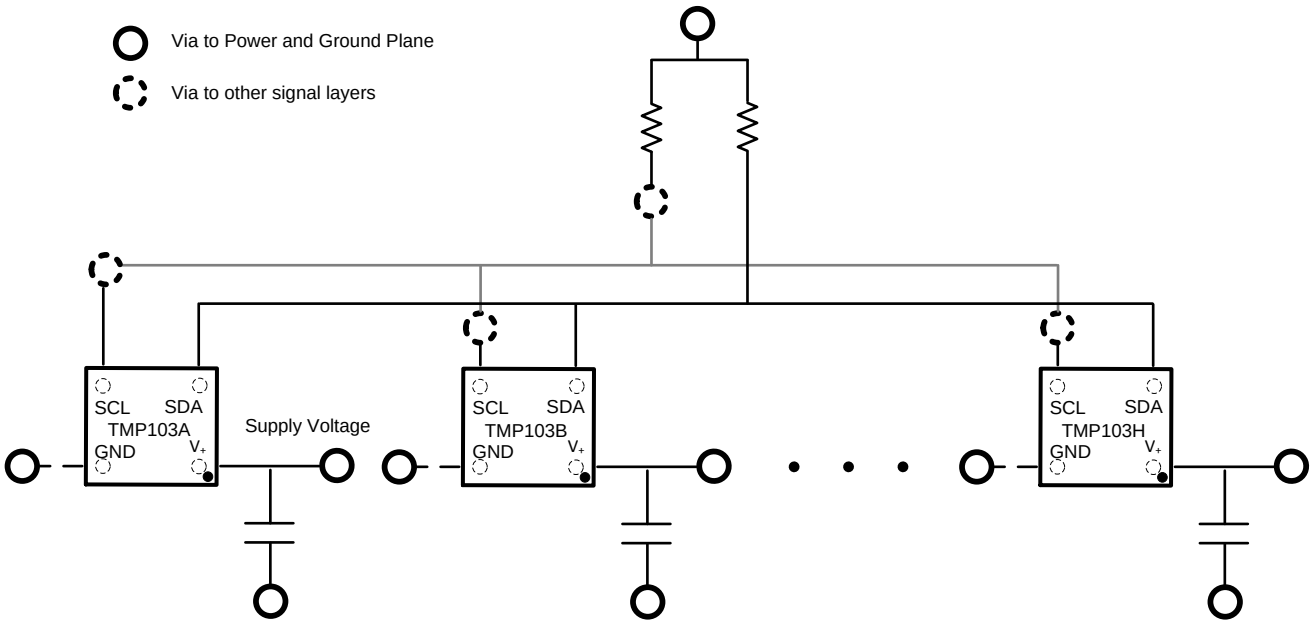



**Figure 18. Recommended Layout Example**

# 11 Device and Documentation Support

## 11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.2 Trademarks

E2E is a trademark of Texas Instruments.
SMBus is a trademark of Intel.
$I^2C$ is a trademark of NXP Semiconductors.
All other trademarks are the property of their respective owners.

## 11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMP103AYFFR | ACTIVE | DSBGA | YFF | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TA | Samples |
| TMP103AYFFT | ACTIVE | DSBGA | YFF | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TA | Samples |
| TMP103BYFFR | ACTIVE | DSBGA | YFF | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TB | Samples |
| TMP103BYFFT | ACTIVE | DSBGA | YFF | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TB | Samples |
| TMP103CYFFR | ACTIVE | DSBGA | YFF | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TC | Samples |
| TMP103CYFFT | ACTIVE | DSBGA | YFF | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TC | Samples |
| TMP103DYFFR | ACTIVE | DSBGA | YFF | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TD | Samples |
| TMP103DYFFT | ACTIVE | DSBGA | YFF | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TD | Samples |
| TMP103EYFFR | ACTIVE | DSBGA | YFF | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TE | Samples |
| TMP103EYFFT | ACTIVE | DSBGA | YFF | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TE | Samples |
| TMP103FYFFR | ACTIVE | DSBGA | YFF | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TF | Samples |
| TMP103FYFFT | ACTIVE | DSBGA | YFF | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TF | Samples |
| TMP103GYFFR | ACTIVE | DSBGA | YFF | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TG | Samples |
| TMP103GYFFT | ACTIVE | DSBGA | YFF | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TG | Samples |
| TMP103HYFFR | ACTIVE | DSBGA | YFF | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TH | Samples |
| TMP103HYFFT | ACTIVE | DSBGA | YFF | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | TH | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

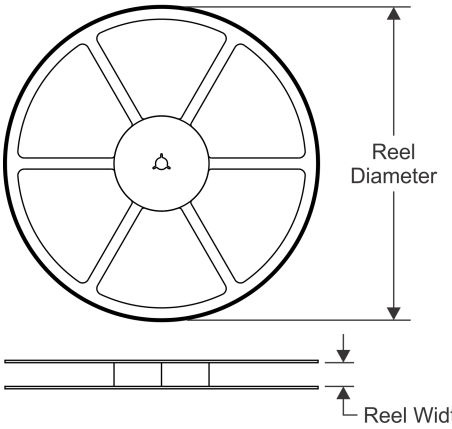
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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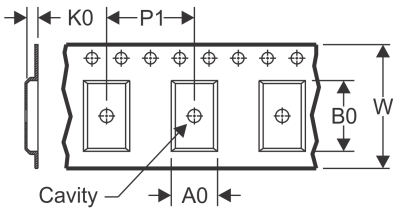
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

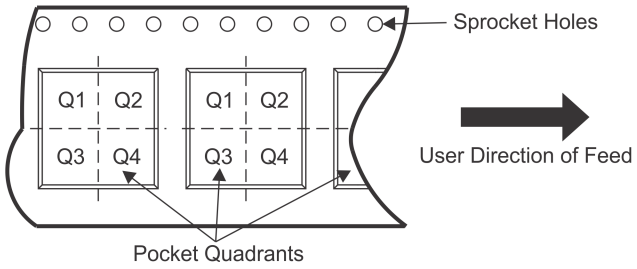



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

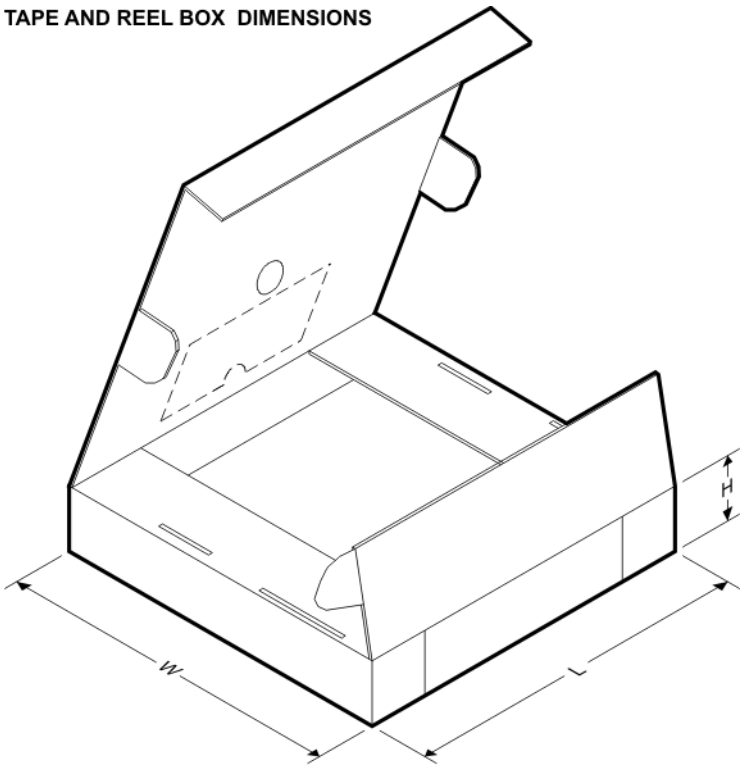
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMP103AYFFR | DSBGA | YFF | 4 | 3000 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TMP103AYFFT | DSBGA | YFF | 4 | 250 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TMP103BYFFR | DSBGA | YFF | 4 | 3000 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TMP103BYFFT | DSBGA | YFF | 4 | 250 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TMP103CYFFR | DSBGA | YFF | 4 | 3000 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TMP103CYFFT | DSBGA | YFF | 4 | 250 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TMP103DYFFR | DSBGA | YFF | 4 | 3000 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TMP103DYFFT | DSBGA | YFF | 4 | 250 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TMP103EYFFR | DSBGA | YFF | 4 | 3000 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TMP103EYFFT | DSBGA | YFF | 4 | 250 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TMP103FYFFR | DSBGA | YFF | 4 | 3000 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TMP103FYFFT | DSBGA | YFF | 4 | 250 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TMP103GYFFR | DSBGA | YFF | 4 | 3000 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TMP103GYFFT | DSBGA | YFF | 4 | 250 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TMP103HYFFR | DSBGA | YFF | 4 | 3000 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TMP103HYFFT | DSBGA | YFF | 4 | 250 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

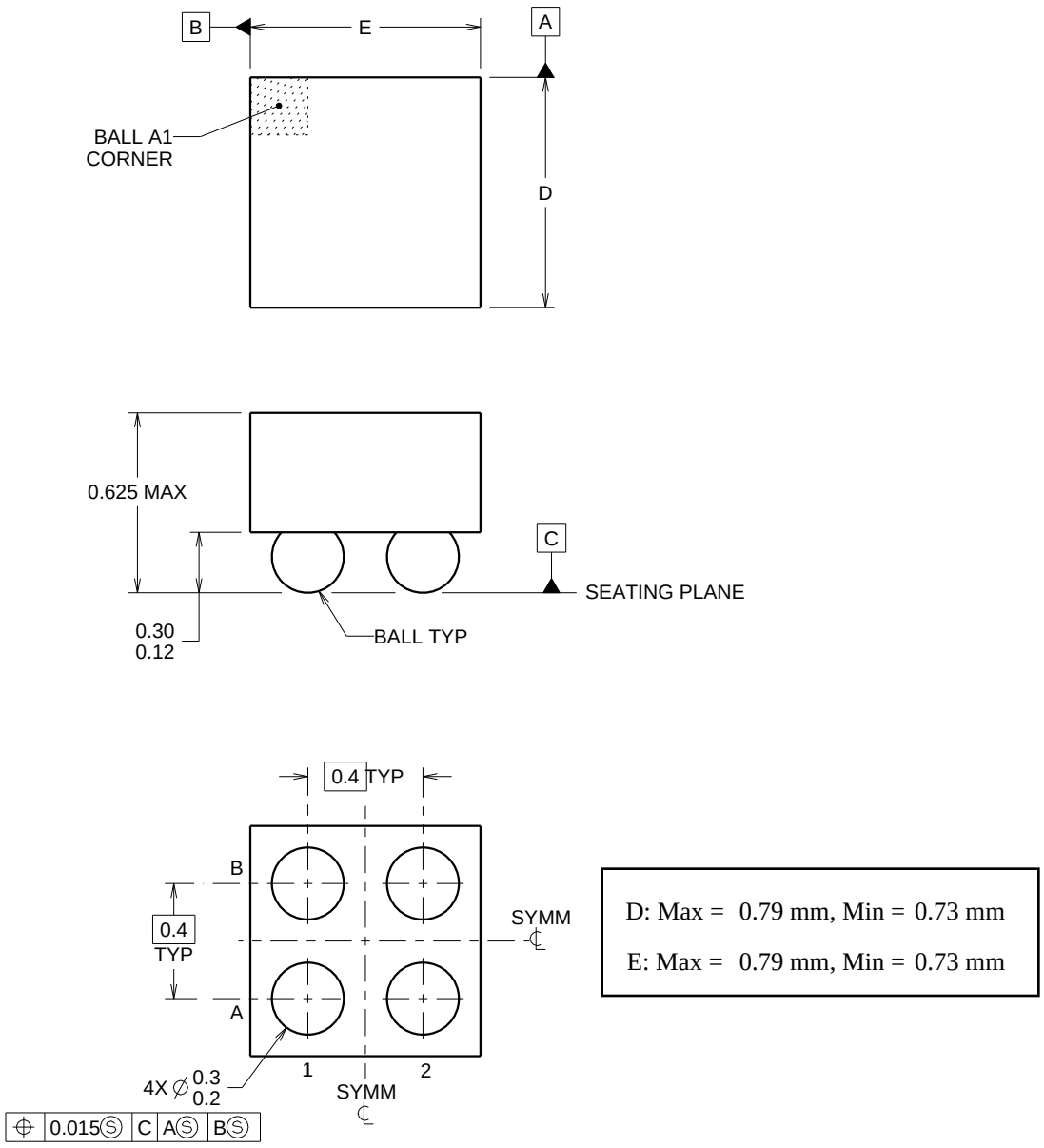
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TMP103AYFFR | DSBGA | YFF | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TMP103AYFFT | DSBGA | YFF | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TMP103BYFFR | DSBGA | YFF | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TMP103BYFFT | DSBGA | YFF | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TMP103CYFFR | DSBGA | YFF | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TMP103CYFFT | DSBGA | YFF | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TMP103DYFFR | DSBGA | YFF | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TMP103DYFFT | DSBGA | YFF | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TMP103EYFFR | DSBGA | YFF | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TMP103EYFFT | DSBGA | YFF | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TMP103FYFFR | DSBGA | YFF | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TMP103FYFFT | DSBGA | YFF | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TMP103GYFFR | DSBGA | YFF | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TMP103GYFFT | DSBGA | YFF | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TMP103HYFFR | DSBGA | YFF | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TMP103HYFFT | DSBGA | YFF | 4 | 250 | 182.0 | 182.0 | 20.0 |

# PACKAGE OUTLINE

## YFF0004

## DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY




D: Max = 0.79 mm, Min = 0.73 mm

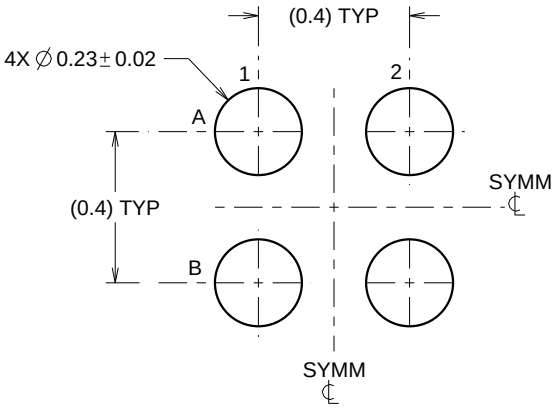
E: Max = 0.79 mm, Min = 0.73 mm

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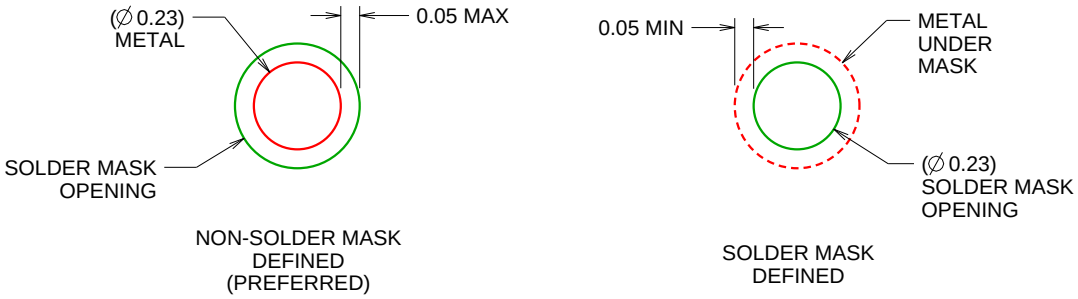
NOTES:

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1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.




LAND PATTERN EXAMPLE
SCALE:50X




SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

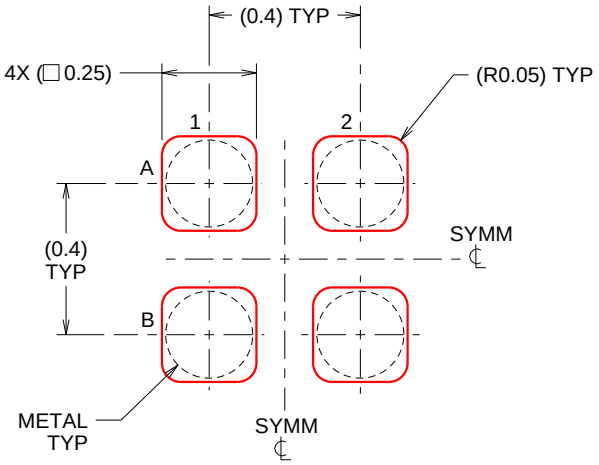
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

# EXAMPLE STENCIL DESIGN

## YFF0004

## DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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