

March 1997

**2K x 8 CMOS RAM**

## Features

- Low Power Standby . . . . . 275 $\mu$ W Max
- Low Power Operation . . . . . 55mW/MHz Max
- Fast Access Time. . . . . 120/200ns Max
- Industry Standard Pinout
- Single Supply . . . . . 5.0V V<sub>CC</sub>
- TTL Compatible
- Static Memory Cells
- High Output Drive
- On-Chip Address Latches
- Easy Microprocessor Interfacing

## Description

The HM-6516 is a CMOS 2048 x 8 Static Random Access Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, which also gives fast access times. The pinout of the HM-6516 is the popular 24 pin, 8-bit wide JEDEC standard, which allows easy memory board layouts, flexible enough to accommodate a variety of PROMs, RAMs, EPROMs, and ROMs.

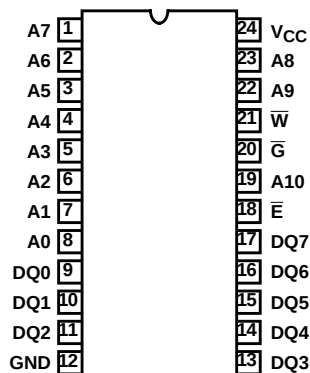
The HM-6516 is ideally suited for use in microprocessor based systems. The byte wide organization simplifies the memory array design, and keeps operating power down to a minimum, because only one device is enabled at a time. The address latches allow very simple interfacing to recent generation microprocessors which employ a multiplexed address/data bus. The convenient output enable control also simplifies multiplexed bus interfacing by allowing the data outputs to be controlled independent of the chip enable.

## Ordering Information

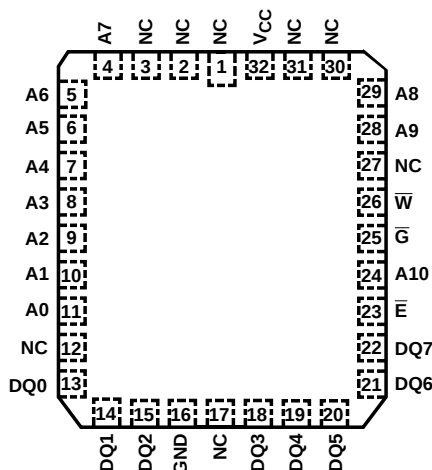
| 120ns       | 200ns      | TEMP. RANGE     | PACKAGE | PKG. NO. |
|-------------|------------|-----------------|---------|----------|
| HM1-6516B-9 | HM1-6516-9 | -40°C to +85°C  | CERDIP  | F24.6    |
| -           | 29102BJA   | -55°C to +125°C | JAN#    | F24.6    |
| 8403607JA   | 8403601JA  | -55°C to +125°C | SMD#    | F24.6    |
| -           | HM4-6516-9 | -40°C to +85°C  | CLCC    | J32.A    |
| 8403607ZA   | 8403601ZA  | -55°C to +125°C | SMD#    | J32.A    |

## Pinouts

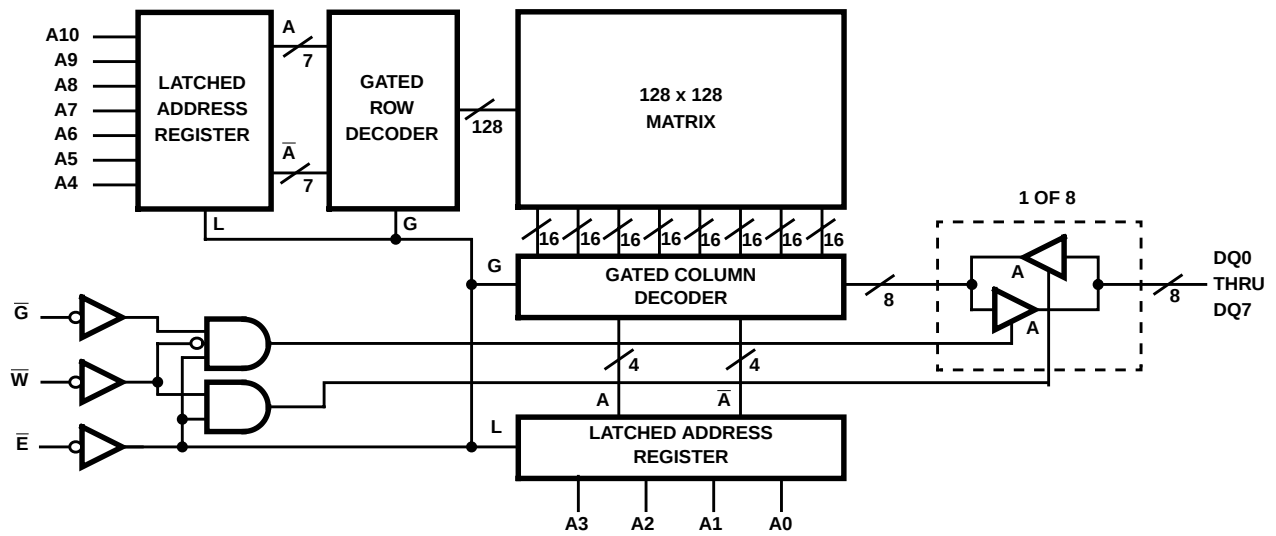
HM-6516  
(CERDIP)  
TOP VIEW



HM-6516  
(CLCC)  
TOP VIEW



| PIN                  | DESCRIPTION            |
|----------------------|------------------------|
| NC                   | No Connect             |
| A0 - A10             | Address Inputs         |
| $\bar{E}$            | Chip Enable/Power Down |
| V <sub>SS</sub> /GND | Ground                 |
| DQ0 - DQ7            | Data In/Data Out       |
| V <sub>CC</sub>      | Power (+5V)            |
| $\bar{W}$            | Write Enable           |
| $\bar{G}$            | Output Enable          |

**Functional Diagram**

# HM-6516

## Absolute Maximum Ratings

Supply Voltage .....+7.0V  
 Input or Output Voltage Applied for all Grades .....GND -0.3V to  $V_{CC} + 0.3V$   
 ESD Classification ..... Class 1

## Thermal Information

Thermal Resistance  
 CERDIP Package .....  $\theta_{JA}$  48°C/W  $\theta_{JC}$  8°C/W  
 CLCC Package ..... 66°C/W 12°C/W  
 Maximum Storage Temperature Range ..... -65°C to +150°C  
 Maximum Junction Temperature ..... +175°C  
 Maximum Lead Temperature (Soldering 10s) ..... +300°C

## Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V  
 Operating Temperature Ranges:  
 HM-6516B-9, HM-6516-9 ..... -40°C to +85°C

## Die Characteristics

Gate Count ..... 25953 Gates

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## DC Electrical Specifications $V_{CC} = 5V \pm 10\%$ ; $T_A = -40^\circ C$ to $+85^\circ C$ (HM-6516B-9, HM-6516-9)

| SYMBOL          | PARAMETER                         | LIMITS         |                | UNITS   | TEST CONDITIONS                                                                   |
|-----------------|-----------------------------------|----------------|----------------|---------|-----------------------------------------------------------------------------------|
|                 |                                   | MIN            | MAX            |         |                                                                                   |
| ICCSB           | Standby Supply Current            | -              | 50             | $\mu A$ | IO = 0mA, VI = $V_{CC}$ or GND, $V_{CC} = 5.5V$ , HM-6516B-9                      |
|                 |                                   | -              | 100            | $\mu A$ | IO = 0mA, VI = $V_{CC}$ or GND, HM-6516-9                                         |
| ICCOP           | Operating Supply Current (Note 1) | -              | 10             | mA      | f = 1MHz, IO = 0mA, $\bar{G} = V_{CC}$ , $V_{CC} = 5.5V$ , VI = $V_{CC}$ or GND   |
| ICCDR           | Data Retention Supply Current     | -              | 25             | $\mu A$ | $V_{CC} = 2.0V$ , IO = 0mA, VI = $V_{CC}$ or GND, $\bar{E} = V_{CC}$ , HM-6516B-9 |
|                 |                                   | -              | 50             | $\mu A$ | $V_{CC} = 2.0V$ , IO = 0mA, VI = $V_{CC}$ or GND, $\bar{E} = V_{CC}$ , HM-6516-9  |
| VCCDR           | Data Retention Supply Voltage     | 2.0            | -              | V       |                                                                                   |
| II              | Input Leakage Current             | -1.0           | +1.0           | $\mu A$ | VI = $V_{CC}$ or GND, $V_{CC} = 5.5V$                                             |
| IIOZ            | Input/Output Leakage Current      | -1.0           | +1.0           | $\mu A$ | VIO = $V_{CC}$ or GND, $V_{CC} = 5.5V$                                            |
| V <sub>IL</sub> | Input Low Voltage                 | -0.3           | 0.8            | V       | $V_{CC} = 4.5V$                                                                   |
| V <sub>IH</sub> | Input High Voltage                | 2.4            | $V_{CC} + 0.3$ | V       | $V_{CC} = 5.5V$                                                                   |
| VOL             | Output Low Voltage                | -              | 0.4            | V       | IO = 3.2mA, $V_{CC} = 4.5V$                                                       |
| VOH1            | Output High Voltage               | 2.4            | -              | V       | IO = -1.0mA, $V_{CC} = 4.5V$                                                      |
| VOH2            | Output High Voltage (Note 2)      | $V_{CC} - 0.4$ | -              | V       | IO = -100 $\mu A$ , $V_{CC} = 4.5V$                                               |

## Capacitance $T_A = +25^\circ C$

| SYMBOL | PARAMETER                         | MAX | UNITS | TEST CONDITIONS                                         |
|--------|-----------------------------------|-----|-------|---------------------------------------------------------|
| CI     | Input Capacitance (Note 2)        | 8   | pF    | f = 1MHz, All measurements are referenced to device GND |
| CIO    | Input/Output Capacitance (Note 2) | 10  | pF    |                                                         |

### NOTES:

- Typical derating 5mA/MHz increase in ICCOP.
- Tested at initial design and after major design changes.

## HM-6516

### AC Electrical Specifications $V_{CC} = 5V \pm 10\%$ ; $T_A = -40^{\circ}C$ to $+85^{\circ}C$ (HM-6516B-9, HM-6516-9)

| SYMBOL     | PARAMETER                        | LIMITS     |     |           |     | UNITS | TEST<br>CONDITIONS |
|------------|----------------------------------|------------|-----|-----------|-----|-------|--------------------|
|            |                                  | HM-6516B-9 |     | HM-6516-9 |     |       |                    |
|            |                                  | MIN        | MAX | MIN       | MAX |       |                    |
| (1) TELQV  | Chip Enable Access Time          | -          | 120 | -         | 200 | ns    | (Notes 1, 3)       |
| (2) TAVQV  | Address Access Time              | -          | 120 | -         | 200 | ns    | (Notes 1, 3, 4)    |
| (3) TELQX  | Chip Enable Output Enable Time   | 10         | -   | 10        | -   | ns    | (Notes 2, 3)       |
| (4) TWLQZ  | Write Enable Output Disable Time | -          | 50  | -         | 80  | ns    | (Notes 2, 3)       |
| (5) TEHQZ  | Chip Enable Output Disable Time  | -          | 50  | -         | 80  | ns    | (Notes 2, 3)       |
| (6) TGLQV  | Output Enable Output Valid Time  | -          | 80  | -         | 80  | ns    | (Notes 1, 3)       |
| (7) TGLQX  | Output Enable Output Enable Time | 10         | -   | 10        | -   | ns    | (Notes 2, 3)       |
| (8) TGHQZ  | Output Enable Output DisableTime | -          | 50  | -         | 80  | ns    | (Notes 2, 3)       |
| (9) TELEH  | Chip Enable Pulse Negative Width | 120        | -   | 200       | -   | ns    | (Notes 1, 3)       |
| (10) TEHEL | Chip Enable Pulse Positive Width | 50         | -   | 80        | -   | ns    | (Notes 1, 3)       |
| (11) TAVEL | Address Setup Time               | 0          | -   | 0         | -   | ns    | (Notes 1, 3)       |
| (12) TELAX | Address Hold Time                | 30         | -   | 50        | -   | ns    | (Notes 1, 3)       |
| (13) TWLWH | Write Enable Pulse Width         | 120        | -   | 200       | -   | ns    | (Notes 1, 3)       |
| (14) TWLEH | Write Enable Pulse Setup Time    | 120        | -   | 200       | -   | ns    | (Notes 1, 3)       |
| (15) TELWH | Write Enable Pulse Hold Time     | 120        | -   | 200       | -   | ns    | (Notes 1, 3)       |
| (16) TDVWH | Data Setup Time                  | 50         | -   | 80        | -   | ns    | (Notes 1, 3)       |
| (17) TWHDX | Data Hold Time                   | 10         | -   | 10        | -   | ns    | (Notes 1, 3)       |
| (18) TELEL | Read or Write Cycle Time         | 170        | -   | 280       | -   | ns    | (Notes 1, 3)       |

#### NOTES:

- Input pulse levels: 0.8V to  $V_{CC} - 2.0V$ ; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent,  $C_L = 50pF$  (min) - for  $C_L$  greater than 50pF, access time is derated by 0.15ns per pF.
- Tested at initial design and after major design changes.
- $V_{CC} = 4.5V$  and  $5.5V$ .
- $TAVQV = TELQV + TAVEL$ .



The write cycle is initiated on the falling edge of  $\bar{E}$  ( $T = 0$ ), which latches the address information in the on-chip registers. If a write cycle is to be performed where the output is not to become active,  $\bar{G}$  can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of  $\bar{G}$ . If  $\bar{E}$  and  $\bar{G}$  fall before  $\bar{W}$  falls (read mode), a possible bus conflict may exist. If  $\bar{E}$  rises before  $\bar{W}$

rises, reference data setup and hold times to the  $\bar{E}$  rising edge. The write operation is terminated by the first rising edge of  $\bar{W}$  ( $T = 2$ ) or  $\bar{E}$  ( $T = 3$ ). After the minimum  $\bar{E}$  high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the  $\bar{W}$  line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising of  $\bar{E}$ .

### Typical Performance Curve

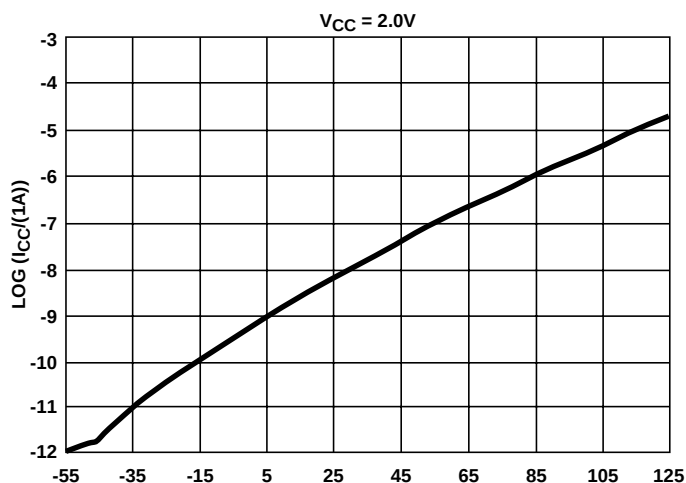


FIGURE 3. TYPICAL ICCDR vs T<sub>A</sub>

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