DATA SHEET

SA8027

2.5 GHz low voltage, low power RF fractional-N/IF integer frequency synthesizer

Product data
Supersedes data of 2001 Jul 18

2001 Aug 21

Philips Semiconductors

PHILIPS

2.5 GHz low voltage, low power RF fractional-N/IF integer frequency synthesizer

SA8027

GENERAL DESCRIPTION

The SA8027 BICMOS device integrates programmable dividers, charge pumps and phase comparators to implement phase-locked loops. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at VCO input frequencies up to 2.5 GHz. The synthesizer has fully programmable main, auxiliary and reference dividers. All divider ratios are supplied via a 3-wire serial programming bus. The main divider is a fractional-N divider with programmable integer ratios from 512 to 65535.

Separate power and ground pins are provided to the charge pumps and digital circuits. The ground pins should be externally connected to prevent large currents from flowing across the die and causing damage. V_{DDCP} must be equal to or greater than V_{DD}.

The charge pump current (gain) is fully programmable, while I_{SET} is set by an external resistance at the R_{SET} pin (refer to section 1.5, Main Output Charge Pumps and Fractional Compensation Currents). The phase/frequency detector charge pump outputs allow for implementing a passive loop filter.

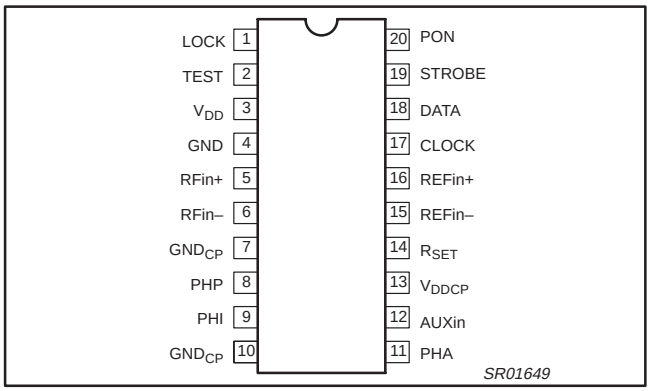


Figure 1. TSSOP20 Pin Configuration

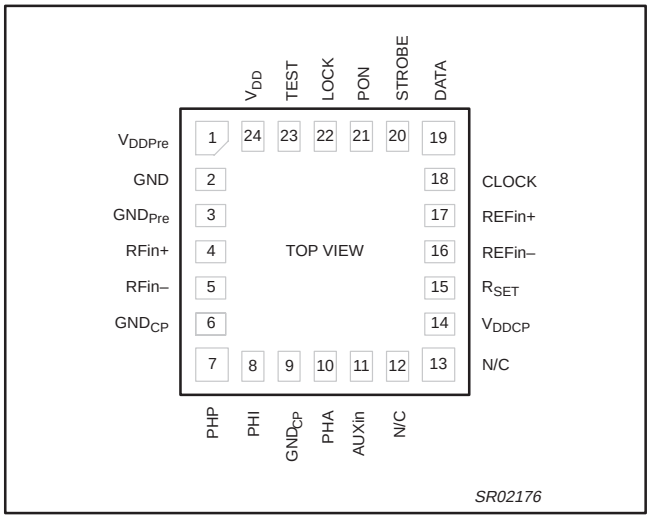


Figure 2. HBCC24 Pin configuration

FEATURES

- Low phase noise
- Low power
- Fully programmable main and auxiliary dividers
- Programmable Normal & Integral charge pumps outputs
- Fast Locking Adaptive mode design
- Internal fractional spurious compensation
- Hardware and software power down
- Split supply for V_{DD} and V_{DDCP}
- Loop filter bandwidth programmability

APPLICATIONS

- 500 to 2500 MHz wireless equipment
- Cellular phones (all standards)
- WLAN
- Portable battery-powered radio equipment.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage		2.7	–	3.6	V
V_{DDCP}	Analog supply voltage	$V_{DDCP} \geq V_{DD}$	2.7	–	3.6	V
$I_{DDCP}+I_{DD}$	Supply current	Main and Aux. on	–	7.7	–	mA
$I_{DDCP}+I_{DD}$	Total supply current in power-down mode		–	1	–	µA
f_{VCO}	Input frequency		500	–	2500	MHz
f_{AUX}	Input frequency		100	–	550	MHz
f_{REF}	Crystal reference input frequency		5	–	40	MHz
f_{PC}	Maximum phase comparator frequency		–		4	MHz
T_{amb}	Operating ambient temperature		–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA8027DH	TSSOP20	Plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
SA8027W	HBCC24	Plastic, heatsink bottom chip carrier; 24 terminals; body 4 x 4 x 0.65 mm (Note 1)	SOT564-1

NOTE:
1. The SA8027W will be released for production Q2, 2001.

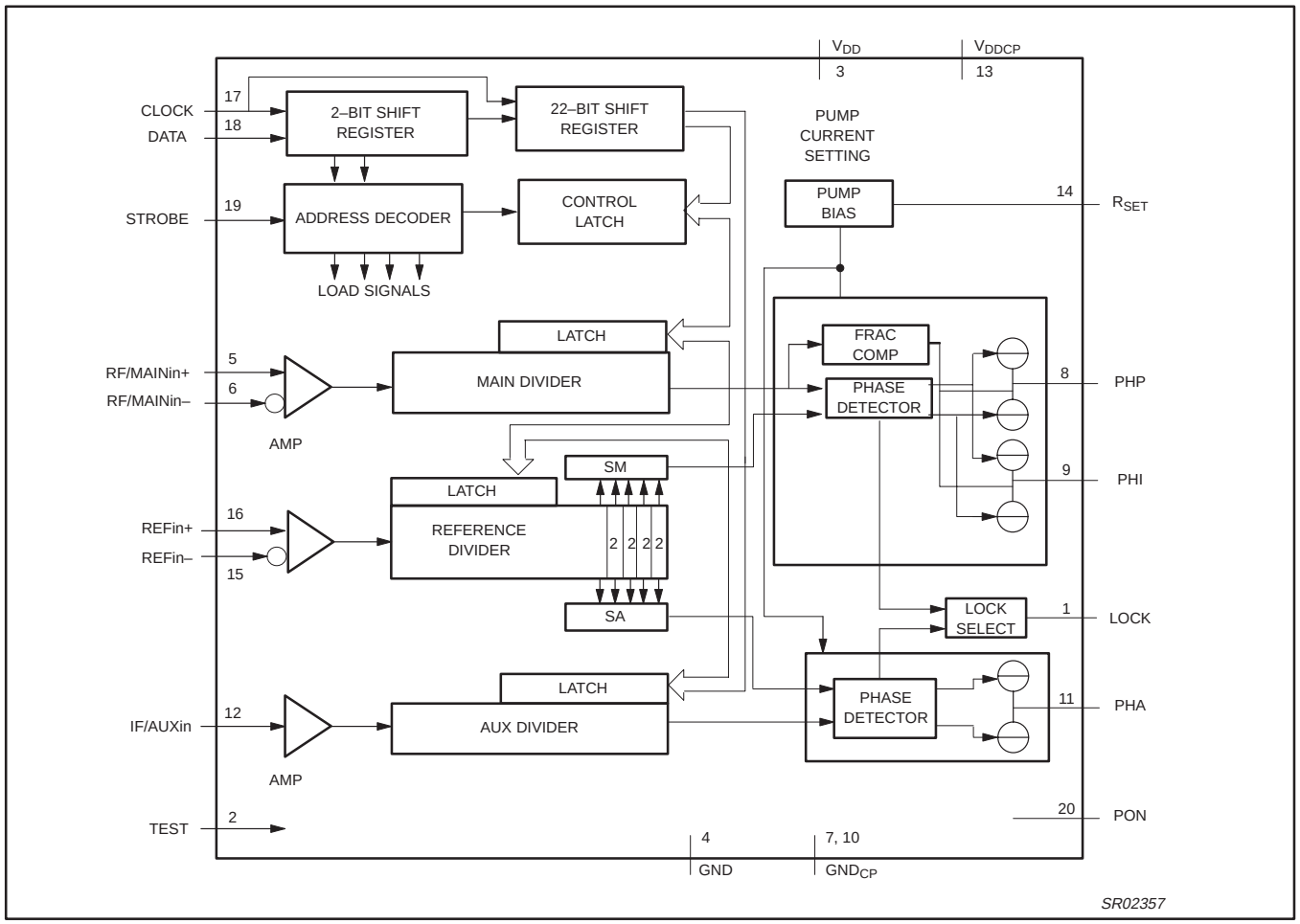


Figure 3. Block Diagram (TSSOP20)

TSSOP20 PIN DESCRIPTION

SYMBOL	PIN	DESCRIPTION
LOCK	1	Lock detect output
TEST	2	Test (should be either grounded or connected to V_{DD})
V_{DD}	3	Digital supply
GND	4	Digital ground
RFin+	5	RF input to main divider
RFin–	6	RF input to main divider
GND_{CP}	7	Charge pump ground
PHP	8	Main normal charge pump
PHI	9	Main integral charge pump
GND_{CP}	10	Charge pump ground

SYMBOL	PIN	DESCRIPTION
PHA	11	Auxiliary charge pump output
AUXin	12	Input to auxiliary divider
V_{DDCP}	13	Charge pump supply voltage
R_{SET}	14	External resistor from this pin to ground sets the charge pump current
REFin–	15	Reference input
REFin+	16	Reference input
CLOCK	17	Programming bus clock input
DATA	18	Programming bus data input
STROBE	19	Programming bus enable input
PON	20	Power down control

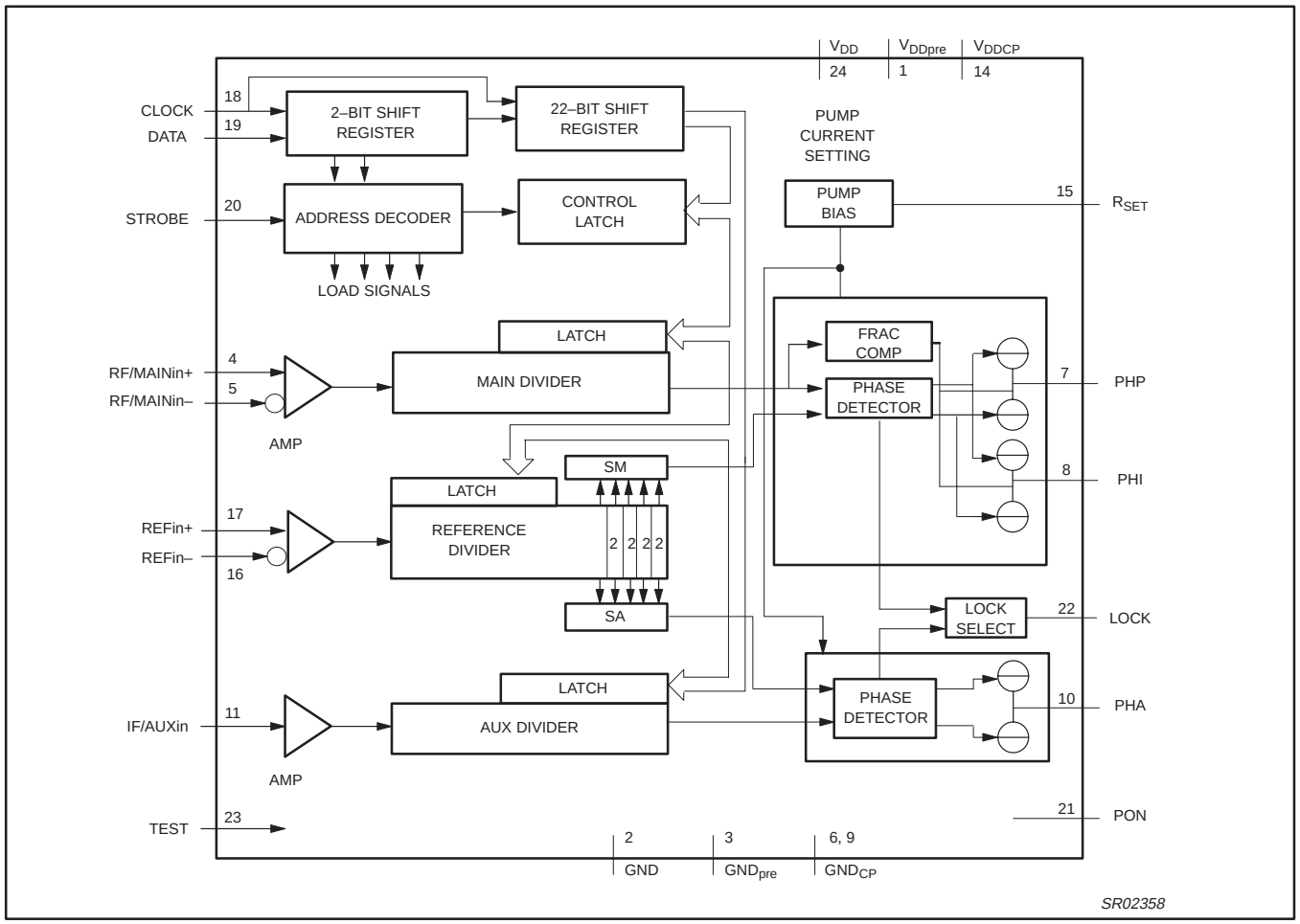


Figure 4. Block Diagram (HBCC24)

HBCC24 PIN DESCRIPTION

SYMBOL	PIN	DESCRIPTION
V_{DDPre}	1	Prescaler supply voltage
GND	2	Digital ground
GND_{Pre}	3	Prescaler ground
RFin+	4	RF input to main divider
RFin–	5	RF input to main divider
GND_{CP}	6	Charge pump ground
PHP	7	Main normal charge pump
PHI	8	Main integral charge pump
GND_{CP}	9	Charge pump ground
PHA	10	Auxiliary charge pump output
AUXin	11	Input to auxiliary divider
N/C	12	Not connected
N/C	13	Not connected

SYMBOL	PIN	DESCRIPTION
V_{DDCP}	14	Charge pump supply voltage
R_{SET}	15	External resistor from this pin to ground sets the charge pump current
REFin–	16	Reference input
REFin+	17	Reference input
CLOCK	18	Programming bus clock input
DATA	19	Programming bus data input
STROBE	20	Programming bus enable input
PON	21	Power down control
LOCK	22	Lock detect output
TEST	23	Test (should be either grounded or connected to V_{DD})
V_{DD}	24	Digital supply

Limiting values

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Digital supply voltage	–0.3	+3.6	V
V_{DDCP}	Analog supply voltage	–0.3	+3.6	V
$\Delta(V_{DDCP}–V_{DD})$	Difference in voltage between V_{DDCP} and V_{DD} ($V_{DDCP} \geq V_{DD}$)	–0.3	+0.9	V
Vi_n	All input pins	–0.3	V_{DD} + 0.3	V
ΔV_{GND}	Difference in voltage between GND_{CP} and GND (these pins should be connected together)	–0.3	+0.3	V
T_{stg}	Storage temperature	–55	+125	°C
T_{amb}	Operating ambient temperature	–40	+85	°C
T_j	Maximum junction temperature		150	°C

Thermal characteristics

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j–a}$	Thermal resistance from junction to ambient in free air	135	K/W

CHARACTERISTICS

V_{DDCP} = V_{DD} = +3.0 V, T_{amb} = +25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	Digital supply voltage		2.7	–	3.6	V
V_{DDCP}	Analog supply voltage	$V_{DDCP} \geq V_{DD}$	2.7	–	3.6	V
I_{Total}	Synthesizer operational supply current	V_{DD} = +3.0 V (with main and aux on)	–	7.7	–	mA
$I_{Standby}$	Total supply current in power-down mode	logic levels 0 or V_{DD}	–	1	–	µA
RFin main divider input						
f_{VCO}	VCO input frequency		500	–	2500	MHz
V_{RFin}	AC-coupled input signal level	R_{in} (external) = R_S = 50 Ω; single-ended drive; max. limit is indicative @ 500 to 2500 MHz	–18	–	0	dBm
			80	–	632	mV_{PP}
Z_{RFin}	Input impedance (real part)	f_{VCO} = 2.4 GHz	–	300	–	Ω
C_{RFin}	Typical pin input capacitance	f_{VCO} = 2.4 GHz	–	1	–	pF
N_{main}	Main divider ratio		512	–	65535	
f_{PCmax}	Maximum loop comparison frequency	indicative, not tested	–	–	4	MHz
AUX divider input						
f_{AUXin}	Input frequency range		100	–	550	MHz
V_{AUXin}	AC-coupled input signal level	R_{in} (external) = R_S = 50 Ω; max. limit is indicative	–15	–	0	dBm
			112	–	632	mV_{PP}
Z_{AUXin}	Input impedance (real part)	f_{VCO} = 500 MHz	–	3.9	–	kΩ
C_{AUXin}	Typical pin input capacitance	f_{VCO} = 500 MHz	–	0.5	–	pF
N_{AUX}	Auxiliary division ratio		128	–	16383	
Reference divider input						
f_{REFin}	Input frequency range from TCXO		5	–	40	MHz
V_{REFin}	AC-coupled input signal level	single-ended drive; max. limit is indicative	360	–	1300	mV_{PP}
Z_{REFin}	Input impedance (real part)	f_{REF} = 20 MHz	–	10	–	kΩ
C_{REFin}	Typical pin input capacitance	f_{REF} = 20 MHz	–	1	–	pF
R_{REF}	Reference division ratio	SA = SM = ”000”	4	–	1023	
Charge pump current setting resistor input						
R_{SET}	External resistor from pin to ground		6	7.5	15	kΩ
V_{SET}	Regulated voltage at pin	R_{SET} = 7.5 kΩ	–	1.22	–	V
Charge pump outputs; R_{SET} = 7.5 kΩ						
I_{CP}	Charge pump current ratio to I_{SET}[1]	Current gain = I_{PH}/I_{SET}	–15		+15	%
I_{MATCH}	Sink-to-source current matching	V_{PH} = 1/2 V_{DDCP}	–10		+10	%
I_{ZOUT}	Output current variation versus V_{PH}[2]	V_{PH} in compliance range	–10		+10	%
I_{LPH}	Charge pump off leakage current	V_{PH} = 1/2 V_{DDCP}	–10		+10	nA
V_{PH}	Charge pump voltage compliance		0.6	–	V_{DDCP}–0.7	V

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Phase noise (condition R_{SET} = 7.5 kΩ, CP = 00)						
$\mathcal{L}_{(f)}$	Synthesizer's contribution to close-in phase noise of 900 MHz RF signal at 1 kHz offset.	GSM f_{REF} = 13MHz, TCXO, f_{COMP} = 1MHz indicative, not tested	–	–90	–	dBc/Hz
	Synthesizer's contribution to close-in phase noise of 1800 MHz RF signal at 1 kHz offset.		–	–83	–	dBc/Hz
	Synthesizer's contribution to close-in phase noise of 800 MHz RF signal at 1 kHz offset.	TDMA f_{REF} = 19.44MHz, TCXO, f_{COMP} = 240kHz indicative, not tested	–	–85	–	dBc/Hz
	Synthesizer's contribution to close-in phase noise of 2100 MHz RF signal at 1 kHz offset.		–	–77	–	dBc/Hz
Interface logic input signal levels						
V_{IH}	HIGH level input voltage		0.7*V_{DD}	–	V_{DD}+0.3	V
V_{IL}	LOW level input voltage		–0.3	–	0.3*V_{DD}	V
I_{LEAK}	Input leakage current	logic 1 or logic 0	–0.5	–	+0.5	µA
Lock detect output signal (in push/pull mode)						
V_{OL}	LOW level output voltage	I_{sink} = 2 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{source} = –2 mA	V_{DD}–0.4	–	–	V

NOTES:

1. $I_{SET} = \frac{V_{SET}}{R_{SET}}$ bias current for charge pumps
2. The relative output current variation is defined as:
   $\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \times \frac{(I_2 - I_1)}{|I_2 + I_1|}$; with I_1 @ V_1 = 0.6 V, I_2 @ V_2 = V_{DDCP} –0.7 V (See Figure 5.)

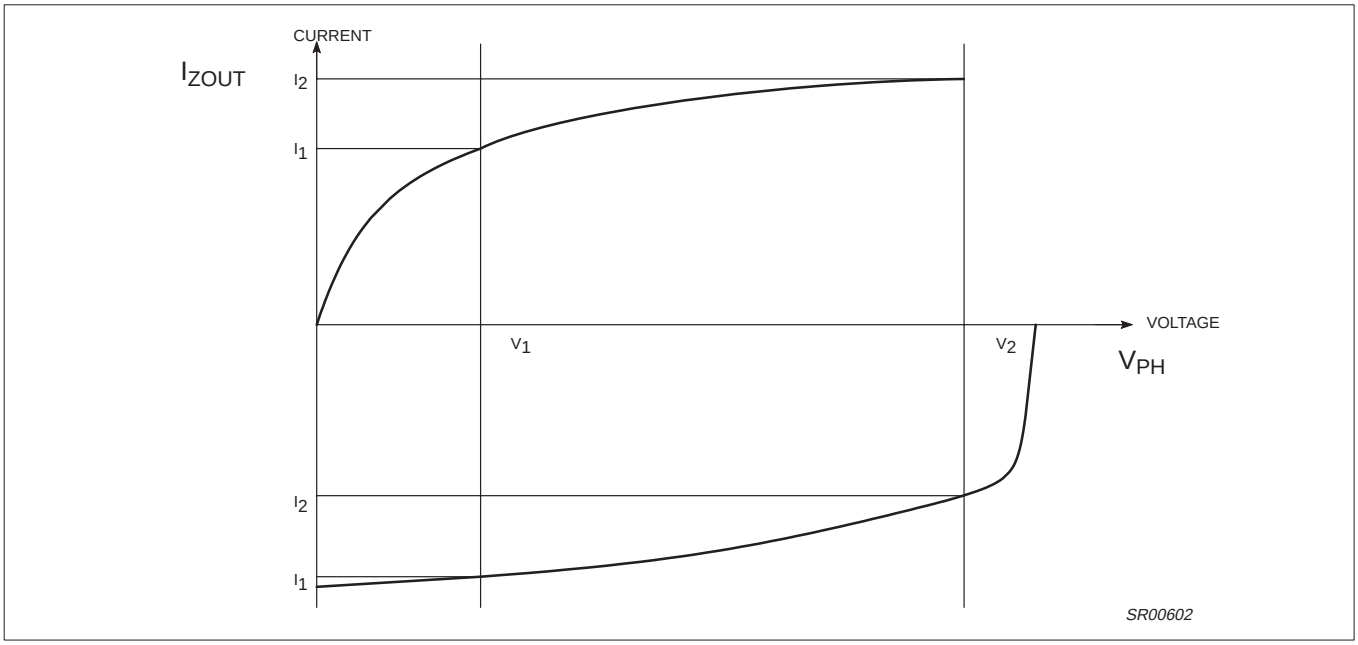


Figure 5. Relative Output Current Variation

1.0 FUNCTIONAL DESCRIPTION

1.1 Main Fractional-N divider

The RFin inputs drive a pre-amplifier to provide the clock to the first divider stage. For single ended operation, the signal should be fed to one of the inputs while the other one is AC grounded. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from –18 dBm to 0 dBm, and at frequencies as high as 2.5 GHz. The divider consists of a fully programmable bipolar prescaler followed by a CMOS counter. Total divide ratios range from 512 to 65535.

The fractional modulus is selected by programming FMOD in the A word. There are 2 modulus to select from: when FMOD = 0, modulo 8 is selected; when FMOD = 1, modulo 5 is selected.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented by the value of NF. The accumulator works with modulo set by FMOD. When the accumulator overflows, the overall division ratio N will be increased by 1, to N + 1. The average division ratio over modulo main divider cycles (either 5 or 8) will be

$$Nfrac = \left(N + \frac{NF}{f_{MOD}}\right)$$

The output of the main divider will be modulated with a fractional phase ripple. The phase ripple is proportional to the contents of the fractional accumulator and is nulled by the fractional compensation charge pump. Thus, $f_{VCO} = f_{comp} * \left(N + \frac{NF}{f_{MOD}}\right)$.

The reloading of a new main divider ratio is synchronized to the state of the main divider to avoid introducing a phase disturbance.

1.2 Auxiliary divider

The AUXin input drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from –15 dBm to 0 dBm (112 to 632 mVpp), and at frequencies as high as 550 MHz. The divider consists of a fully programmable bipolar prescaler followed by a CMOS counter. Total divide ratios range from 128 to 16383.

1.3 Reference divider

The reference divider consists of a divider with programmable values between 4 and 1023 followed by a three bit binary counter. The 3 bit SM (SA) register (see Figure 6) determines which one of the 5 output pulses are selected as the main (auxiliary) phase detector input, thus allowing the main PFD and auxiliary PFD to operate at different frequencies.

1.4 Phase detector (see Figure 7)

The reference and main (aux) divider outputs are connected to a phase/frequency detector that controls the charge pump. The pump current is set by an external resistor in conjunction with control bits CP0 and CP1 in the C-word (see Table 1). The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by forcing the pumps ON for a minimum time (τ) at every cycle (backlash time) providing improved linearity.

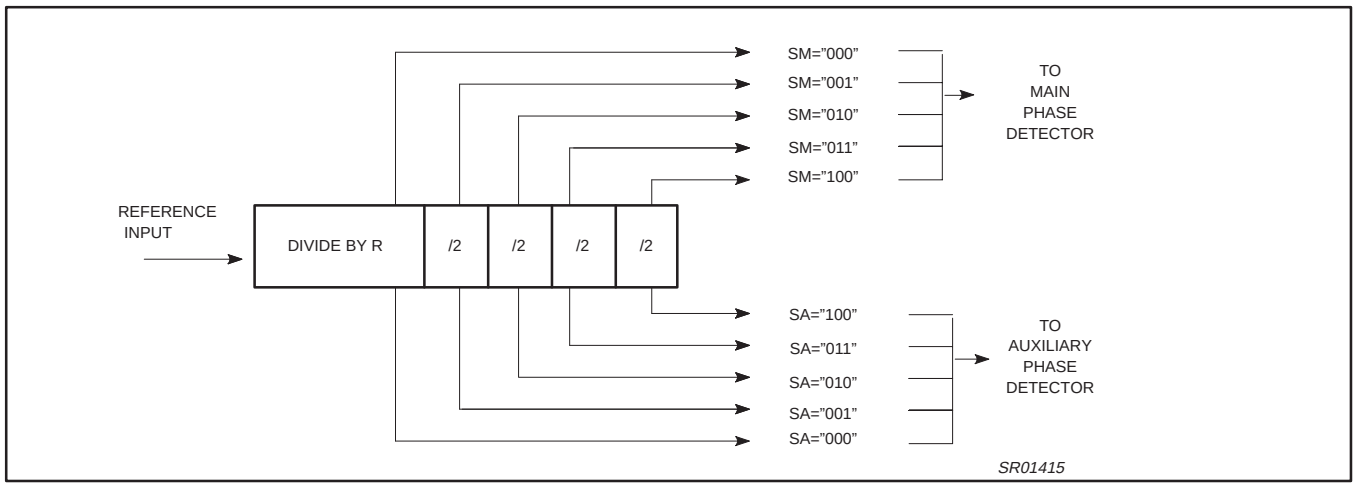


Figure 6. Reference Divider

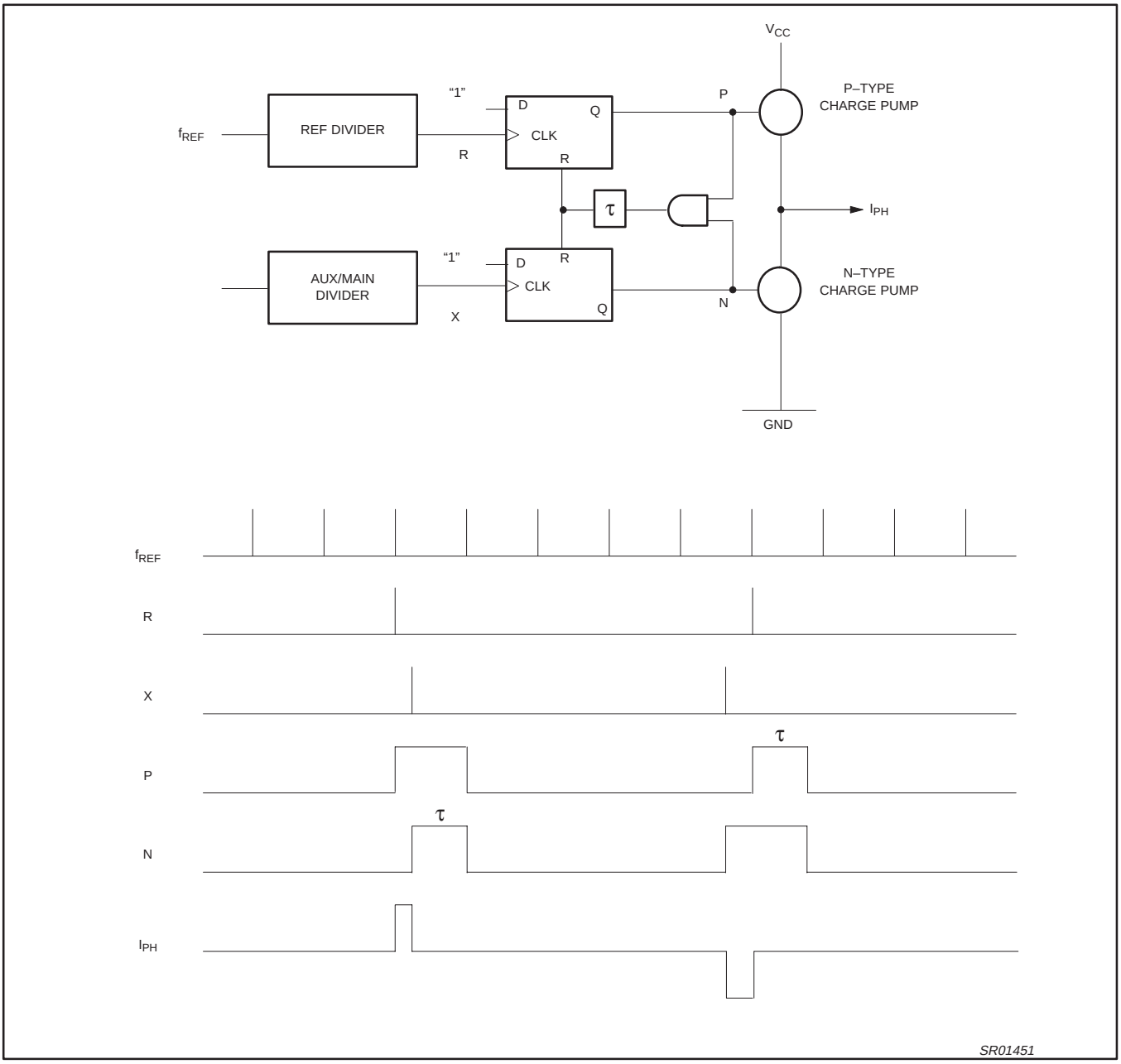


Figure 7. Phase Detector Structure with Timing

1.5 Main Output Charge Pumps and Fractional Compensation Currents (see Figure 8)

The main charge pumps on pins PHP and PHI are driven by the main phase detector and the charge pump current values are determined by the current at pin R_{SET} in conjunction with bits CP0, CP1 in the C-word (see Table 1). The main charge pumps will enter speed up mode after the A-word is set and strobe goes High. When strobe goes Low, charge pump will exit speed up mode. The fractional compensation is derived from the current at R_{SET}, the contents of the fractional accumulator (FRD) and by the program value of the FDAC. The timing for the fractional compensation is derived from the main divider.

1.6 Principle of Fractional Compensation

The fractional compensation is designed into the circuit as a means of reducing or eliminating fractional spurs that are caused by the fractional phase ripple of the main divider. If I_{COMP} is the compensation current and I_{PUMP} is the pump current, then for each charge pump:

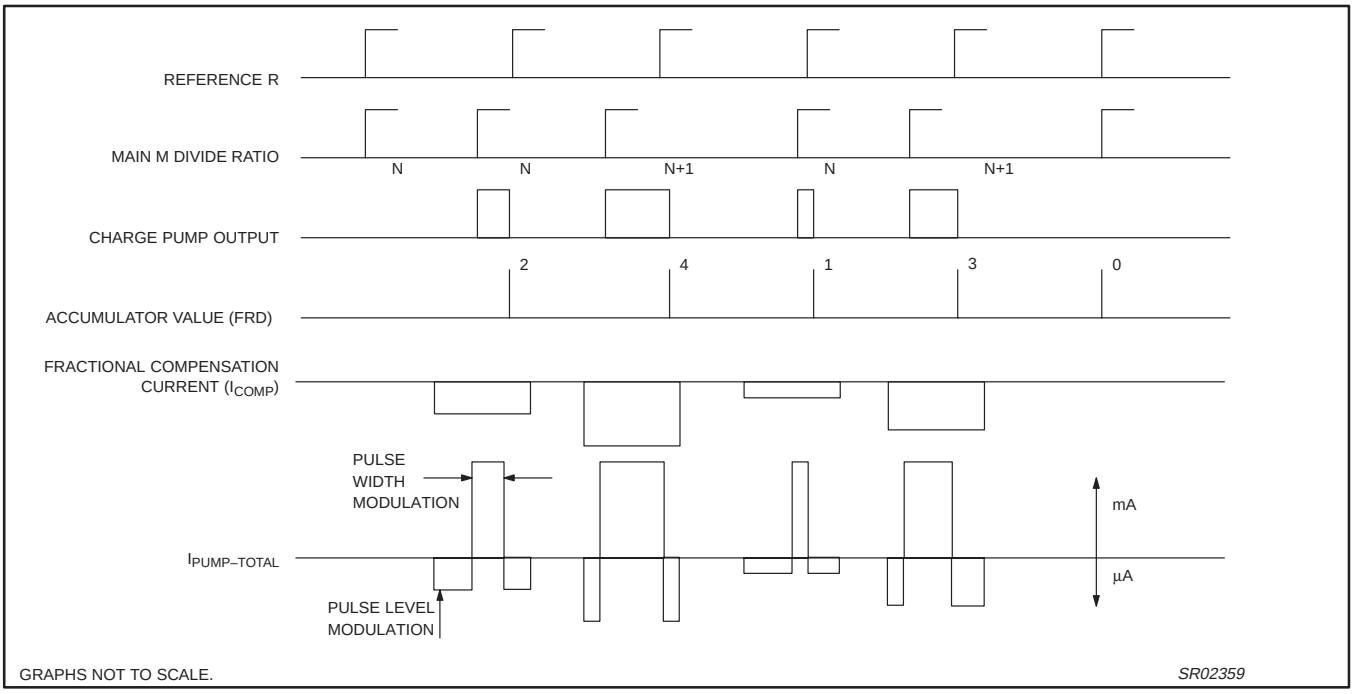
$$I_{PUMP\_TOTAL} = I_{PUMP} + I_{COMP}.$$

The compensation is done by sourcing a small current, I_{COMP}, see Figure 9, that is proportional to the fractional error phase. For proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the fractional charge pump ripple. The width of the fractional compensation pulse is fixed to 128 VCO cycles, the amplitude is proportional to the fractional accumulator value and is adjusted by FDAC values (bits FC7–0 in the B-word). The fractional compensation current is derived from the main charge pump in that it follows all the current scaling through external resistor setting, R_{SET}, programming or speed-up operation. For a given charge pump,

$$I_{COMP} = (I_{PUMP} / 128) * (FDAC / 5*128) * FRD$$

FRD is the fractional accumulator value and is automatically updated.

The theoretical values for FDAC are: 128 for FMOD = 1 (modulo 5) and 80 for FMOD = 0 (modulo 8).



NOTE: For a proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump output.

Figure 8. Waveforms for NF = 2 Modulo 5 → fraction = $^2/_5$

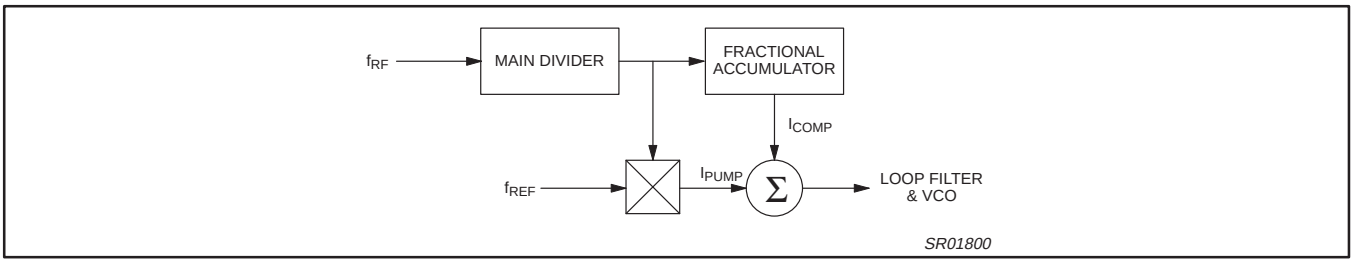


Figure 9. Current Injection Concept

1.7 Charge Pumps

The PHP and PHI charge pumps are driven by the main phase detector, while the PHA charge pump is driven by the auxiliary phase detector. The I_{SET} value (refer to Table 1) is determined by the external resistor attached to the R_{SET} pin.

The charge pump, by default, will automatically go into speed-up mode (which can deliver up to 15*I_{SET} for PHP_SU, and 36*I_{SET} for PHI), based on the strobe pulse width following the A word, to reduce switching speed for large tuning voltage steps (i.e., large frequency steps). Figure 10 shows the recommended passive loop filter configuration. Note: This charge pump architecture eliminates the need for added active switches and reduces external component count. Furthermore, the programmable charge pump gains provide some programmability to the loop filter bandwidth.

The duration of speed-up mode is determined by the strobe pulse width following the A word. Recommended optimal strobe width is equal to the total loop filter capacitance charge time from state 1 to state 2. The strobe width must not exceed this charge time. The strobe width is controlled by the CPU (× number of clock cycles).

In addition, charge pumps will stay in speed-up mode continuously while Tspu = 1 (in D word). The speed-up mode can also be disabled by programming $T_{dis\text{-}spu}$ = 1 (in D word).

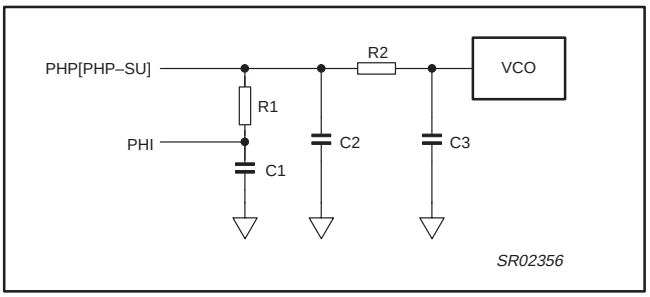


Figure 10. Typical passive 3-pole loop filter

Table 1. Main and auxiliary charge pump currents

CP1	CP0	I_{PHA}	I_{PHP}	$I_{PHP–SU}$	I_{PHI}
0	0	1.5xI_{SET}	3xI_{SET}	15xI_{SET}	36xI_{SET}
0	1	0.5xI_{SET}	1xI_{SET}	5xI_{SET}	12xI_{SET}
1	0	1.5xI_{SET}	3xI_{SET}	15xI_{SET}	0
1	1	0.5xI_{SET}	1xI_{SET}	5xI_{SET}	0

NOTES:
1. $I_{SET} = V_{SET}/R_{SET}$: bias current for charge pumps.
2. CP1 is used to disable the PHI pump, $I_{PHP–SU}$ is the total current at pin PHP during speed up condition.

1.8 Lock Detect

The output LOCK maintains a logic ‘1’ when the auxiliary phase detector (AND/ORed) with the main phase detector indicates a lock condition. The lock condition for the main and auxiliary synthesizers is defined as a phase difference of less than ±1 period of the frequency at the input $REF_{in+,\ -}$. One counter can fulfill the lock condition when the other counter is powered down. Out of lock (logic ‘0’) is indicated when both counters are powered down.

1.9 Power-down mode

The power-down signal can be either hardware (PON) or software (PD). The PON signal is exclusively ORed with the PD bits in B-word. If PON = 0, then the part is powered up when PD = 1. PON can be used to invert the polarity of the software bit PD. When the synthesizer is reactivated after power-down, the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

2.0 SERIAL PROGRAMMING BUS

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program all counter divide ratios, fractional compensation DAC, selection and enable bits. The programming data is structured into 24 bit words; each word includes 2 or 3 address bits. Figure 11 shows the timing diagram of the serial input. When the STROBE goes active HIGH, the clock is disabled and the data in the shift register remains unchanged. Depending on the address bits, the data is latched into the selected working registers or temporary registers. In order to fully program the synthesizer, 3 words must be sent: C, B, and A, in that order. A typical programming sequence is illustrated in Figure 12. Table 2 shows the format and the contents of each word. The D word is used for testing purposes and should be initially set to 0 for normal operation. When sending the B-word, data bits FC7–0 for the fractional compensation DAC are not loaded immediately. Instead they are stored in temporary registers. Only when the A-word is loaded, these temporary registers are loaded together with the main divider ratio.

2.1 Serial bus timing characteristics (see Figure 11)

$V_{DD} = V_{DDCP}$ =+3.0 V; T_{amb} = +25 °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	Input rise time	–	10	40	ns
t_f	Input fall time	–	10	40	ns
T_{cy}	Clock period	100	–	–	ns
Enable programming; STROBE					
t_{START}	Delay to rising clock edge	40	–	–	ns
t_W	Minimum inactive pulse width	$1/f_{COMP}$	–	–	ns
$t_{SU;\overline{E}}$	Enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	Input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	Input data to clock hold time	20	–	–	ns

Application information

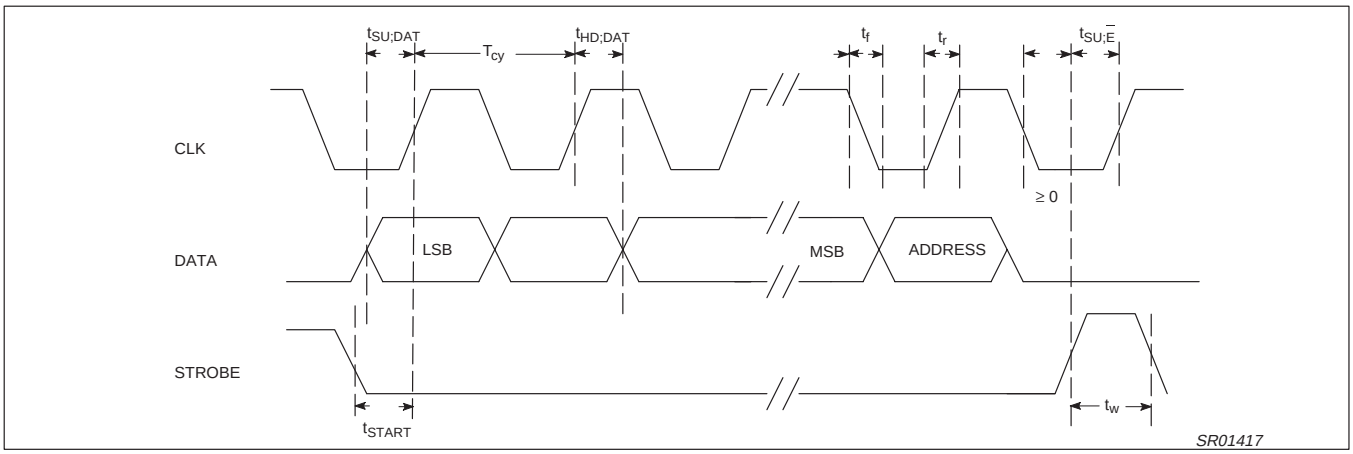


Figure 11. Serial Bus Timing Diagram

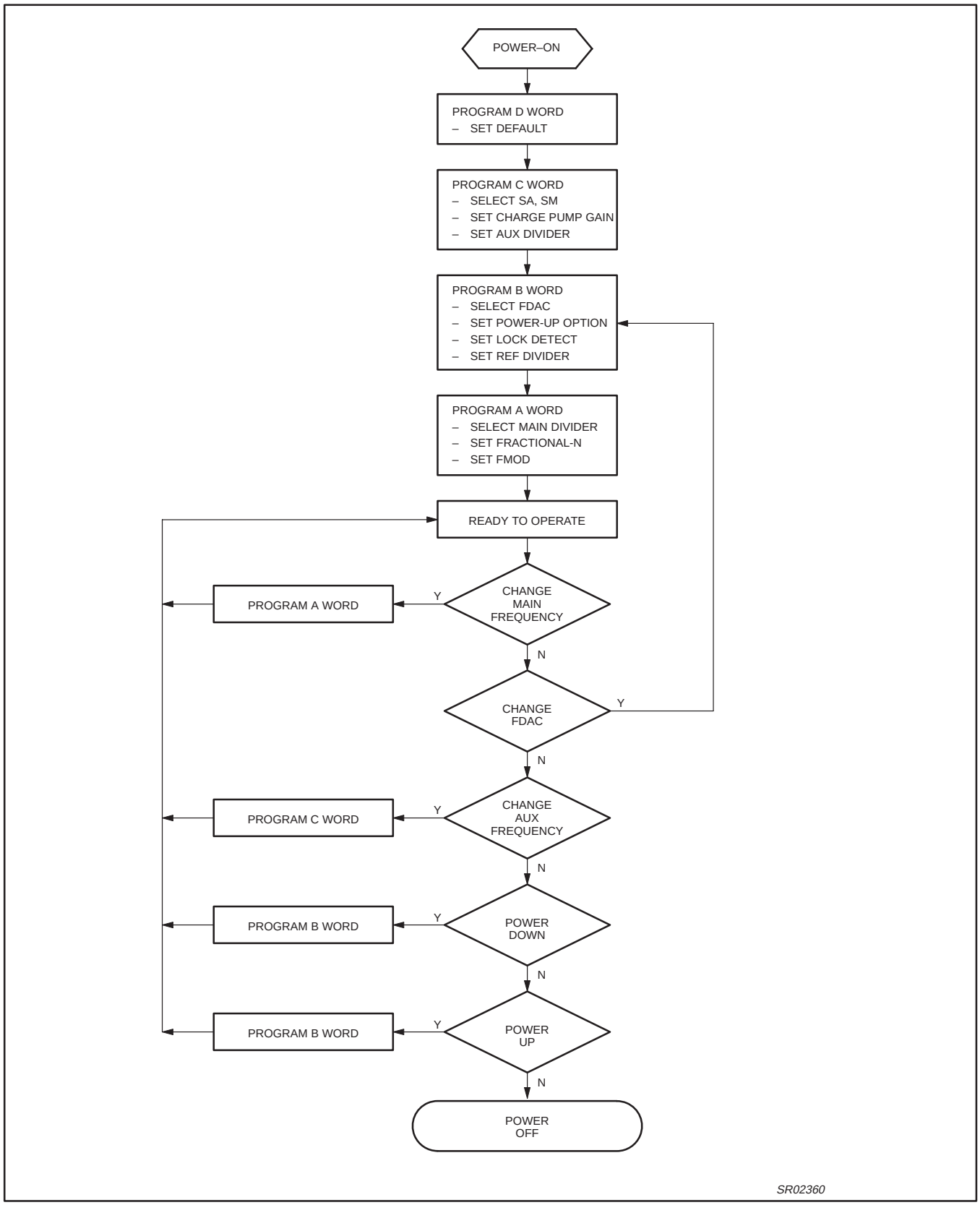


Figure 12. Typical programming sequence

Data format

Table 2. Format of programmed data

Last In		MSB	Serial Programming Format				First In LSB
p23	p22	p21	p20	../..	../..	p1	p0

Table 3. A word, length 24 bits

Last In					MSB															LSB	First In	
Address		fmod	Fractional-N			Main Divider ratio															Spare	
0	0	fmod	NF2	NF1	NF0	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	SK1	SK2
Default		0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0

A word address	Fixed to 00.
Fractional Modulus select	fmod = 0 is modulo 8; fmod = 1 is modulo 5.
Fractional-N Increment	Fractional-N Increment values 000 to 111 (0 to 7). NF is a 3-bit word.
N-Divider	N0..N15, Main divider values 512 to 65535 allowed for divider ratio.
Spare	SK1, SK2 must be set to 0.

Table 4. B word, length 24 bits

Address		Reference Divider										Lock		PD		FDAC (Fractional Compensation DAC)							
0	1	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	L1	L0	Main	Aux	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
Default		0	0	0	1	0	1	0	0	0	1	0	0	1	1	0	1	0	1	0	0	0	0

B word address	Fixed to 01	
REF-Divider	R0..R9, Reference divider values 4 to 1023 allowed for divider ratio. R <9:0>.	
Lock detect output	L1 L0 0 0 Combined main, aux. lock detect signal present at the LOCK pin (push/pull). 0 1 Combined main, aux, lock detect signal present at the LOCK pin (open drain). 1 0 Main lock detect signal present at the LOCK pin (push/pull). 1 1 Auxiliary loop lock detect signal present at the LOCK pin (push/pull). When auxiliary loop and main loop are in power down mode, the lock indicator is low.	
Power down (PD)	PON pin is tied to GND	Main = 1: power-on to Main PLL. Main = 0: power-down to Main PLL. Aux = 1: power-on to Aux PLL. Aux = 0: power-down to Aux PLL.
	PON pin is tied to V_{DD}	Main = 0: power-on to Main PLL. Main = 1: power-down to Main PLL. Aux = 0: power-on to Aux PLL. Aux = 1: power-down to Aux PLL.
Fractional Compensation	FC7..0 Fractional Compensation charge pump current DAC, values 0 to 255.	

Table 5. C word, length 24 bits

Address		Auxiliary Divider														CP		SM			SA		
1	0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	CP1	CP0	SM2	SM1	SM0	SA2	SA1	SA0
Default		0	0	0	0	0	1	1	1	0	0	1	0	1	0	1	1	0	0	0	0	0	0

C word address	Fixed to 10
A-Divider	A0..A13, Auxiliary divider values 128 to 16383 allowed for divider ratio.
Charge pump current Ratio	CP1, CP0: Charge pump current ratio, see Table 1.
Main comparison select	SM comparison divider select for main phase detector.
Aux comparison select	SA Comparison divider select for auxiliary phase detector.

Table 6. D word, length 24 bits

Address			Synthesizer Test Bits																				
1	1	0	–	–	–	–	$T_{dis-spu}$	Tspu	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Default			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D word address	Fixed to 110.
$T_{dis-spu}$ = 1	Speed-up mode disabled. **NOTE**: All other test bits must be set to 0 for normal operation.
T_{spu} = 1	Speed-up mode always on. **NOTE**: All other test bits must be set to 0 for normal operation.

TYPICAL PERFORMANCE CHARACTERISTICS

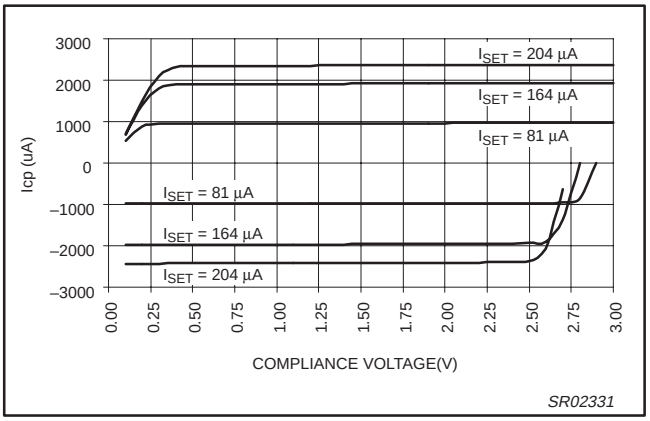


Figure 13. PHI Charge Pump Output vs. I_{SET} (CP = 01_12x; Temp = 25 °C)

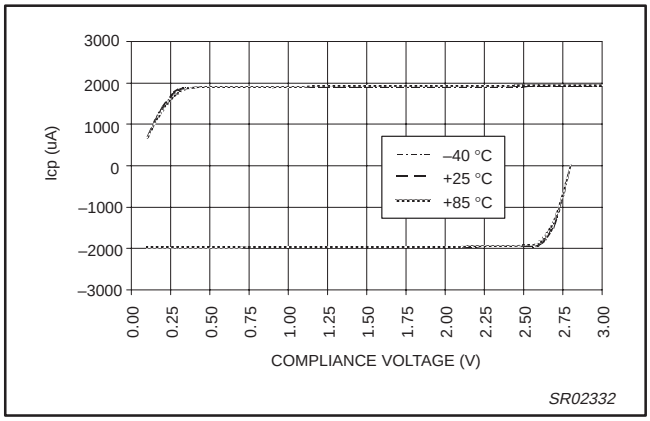


Figure 14. PHI Charge Pump Output vs. Temperature (CP = 01_12x; V_{DD} = 3.0 V; I_{SET} = 164 µA)

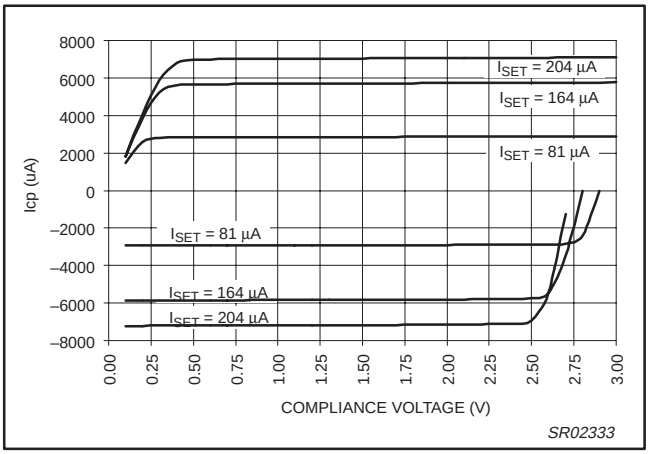


Figure 15. PHI Charge Pump Output vs. I_{SET} (CP = 00_36x; Temp = 25 °C)

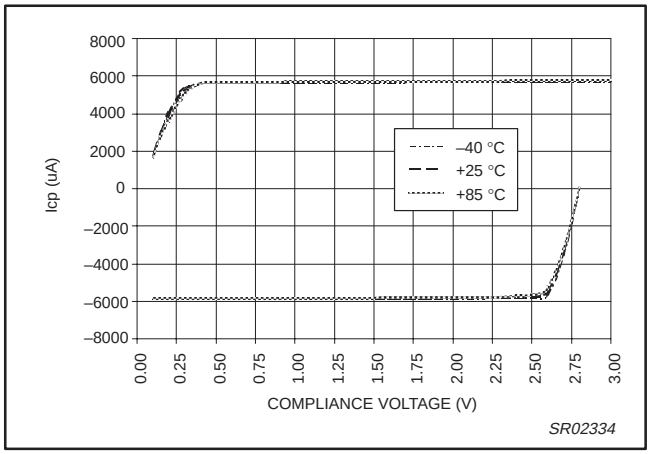


Figure 16. PHI Charge Pump Output vs. Temperature (CP = 00_36x; V_{DD} = 3.0 V; I_{SET} = 164 µA)

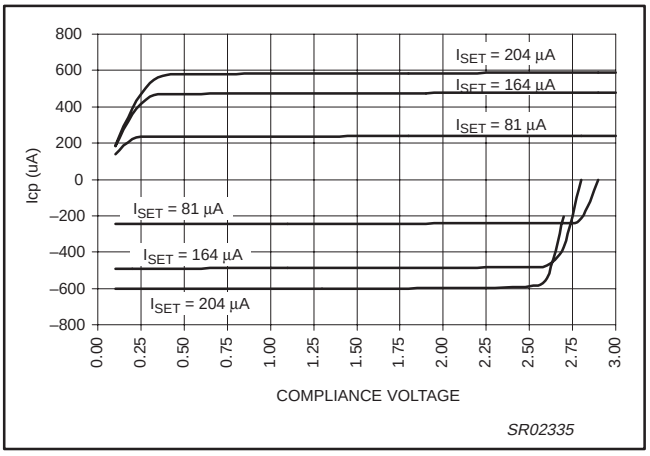


Figure 17. PHP Charge Pump Output vs. I_{SET} (CP = 10_3x; V_{DD} = 3.0 V; Temp = 25°C)

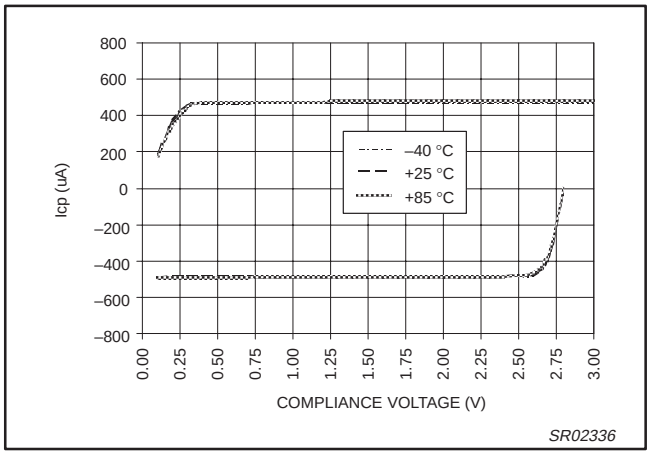


Figure 18. PHP Charge Pump Output vs. Temperature (CP = 10_3x; V_{DD} = 3.0 V; I_{SET} = 164 µA)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

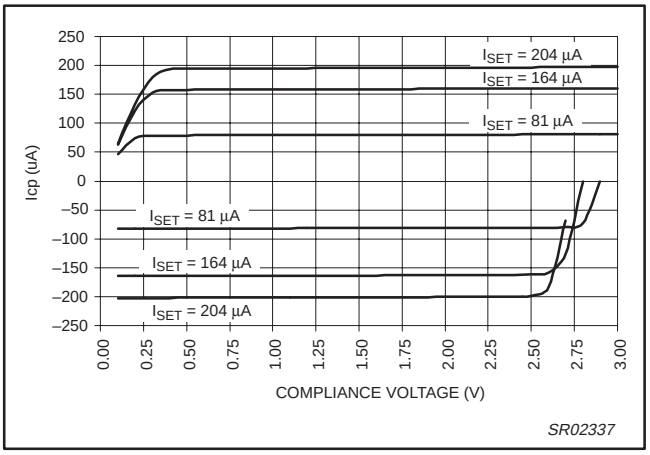


Figure 19. PHP Charge Pump Output vs. I_{SET} (CP = 11_1x; V_{DD} = 3.0 V; Temp = 25 °C)

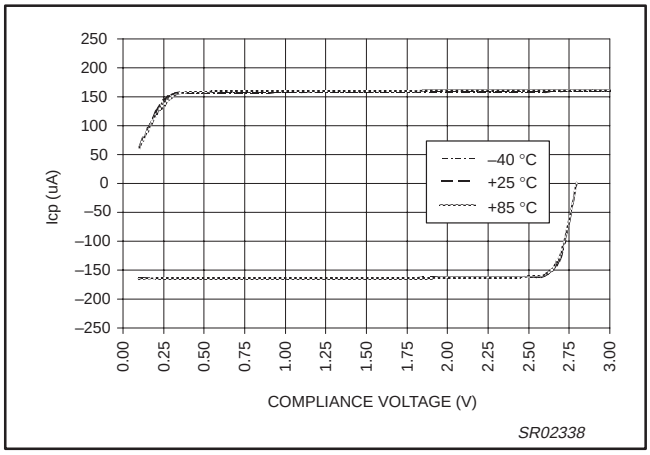


Figure 20. PHP Charge Pump Output vs. Temperature (CP = 11_1x; V_{DD} = 3.0 V; I_{SET} = 164 µA)

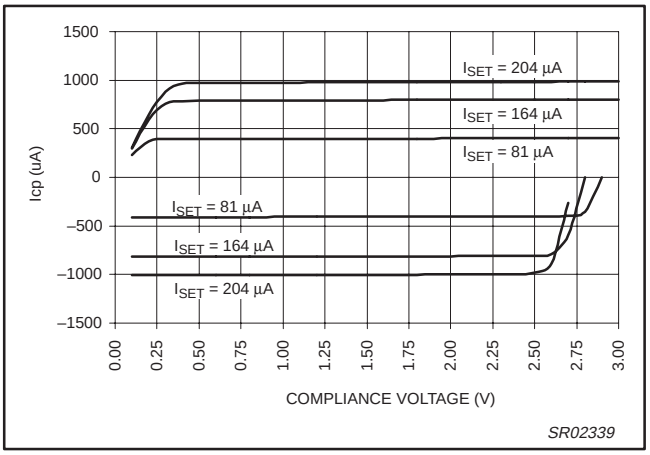


Figure 21. PHP–SU Charge Pump Output vs. I_{SET} (CP = 01_5x; V_{DD} = 3.0 V; Temp = 25 °C)

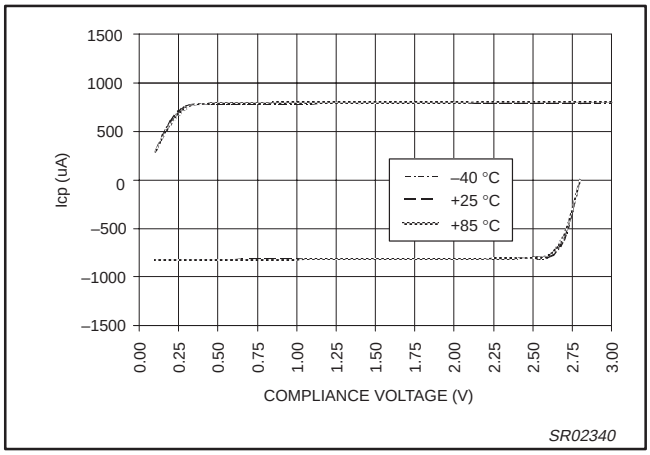


Figure 22. PHP–SU Charge Pump Output vs. Temperature (CP = 01_5x; V_{DD} = 3.0 V; I_{SET} = 164 µA)

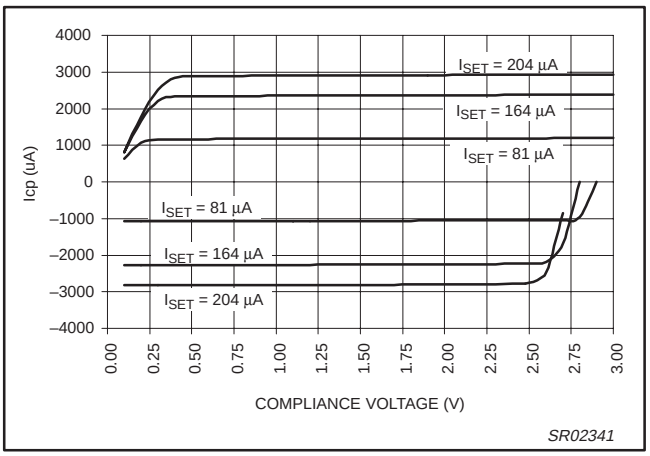


Figure 23. PHP–SU Charge Pump Output vs. I_{SET} (CP = 00_15x; V_{DD} = 3.0 V; Temp = 25 °C)

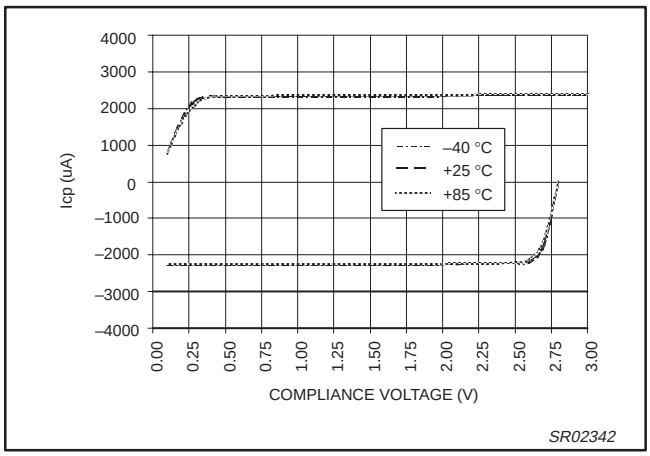


Figure 24. PHP–SU Charge Pump Output vs. Temperature (CP = 00_15x; V_{DD} = 3.0 V; I_{SET} = 164 µA)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

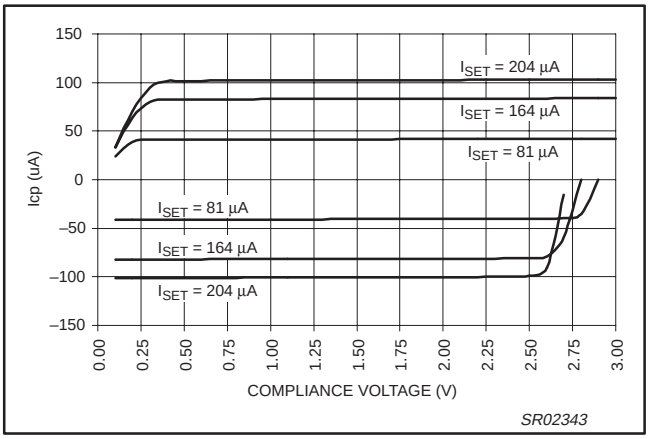


Figure 25. PHA Charge Pump Output vs. I_{SET} (CP = 11_0.5x; Temp = 25 °C)

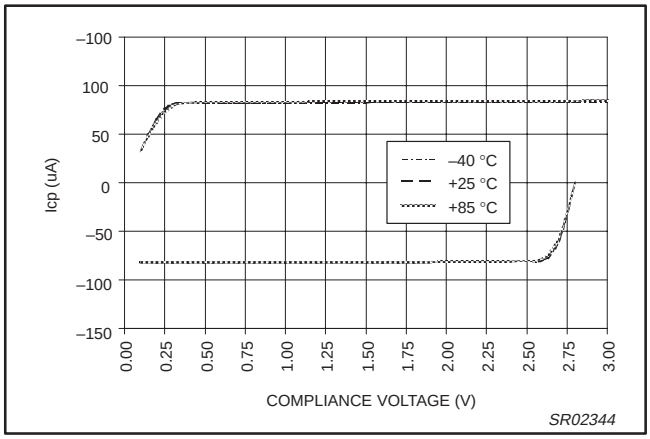


Figure 26. PHA Charge Pump Output vs. Temperature (CP = 11_0.5x; V_{DD} = 3.0 V; I_{SET} = 164 µA)

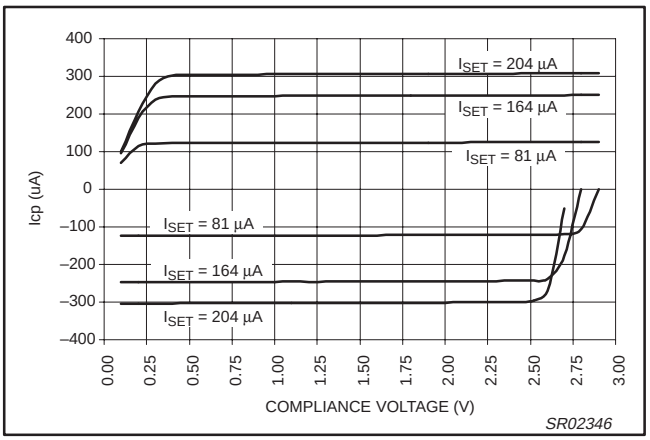


Figure 27. PHA Charge Pump Output vs. I_{SET} (CP = 10_1.5x; V_{DD} = 3.0 V; Temp = 25 °C)

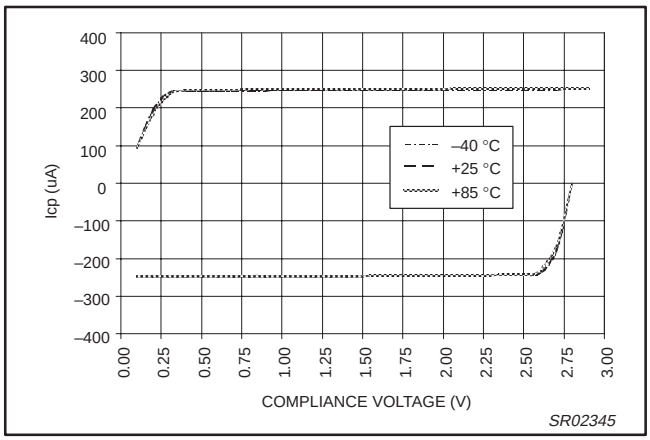


Figure 28. PHA Charge Pump Output vs. Temperature (CP = 10_1.5x; V_{DD} = 3.0 V; I_{SET} = 164 µA)

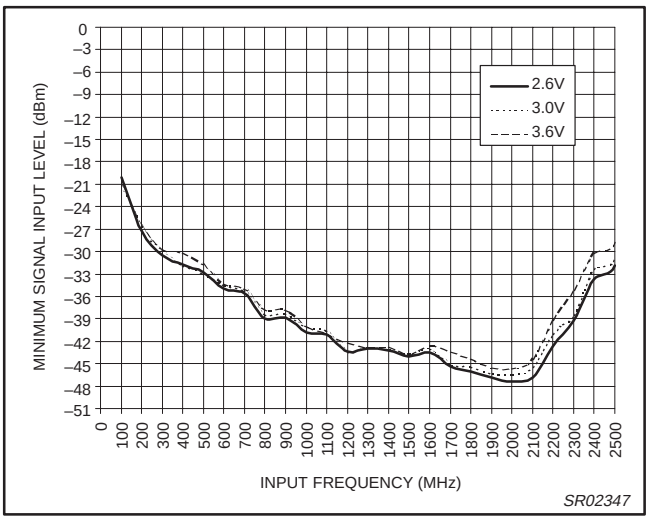


Figure 29. Main Divider Input Sensitivity vs. Frequency and Supply Voltage (Temp = 25 °C; I_{SET} = 164 µA; NF = 0; MOD = 8; N = 853)

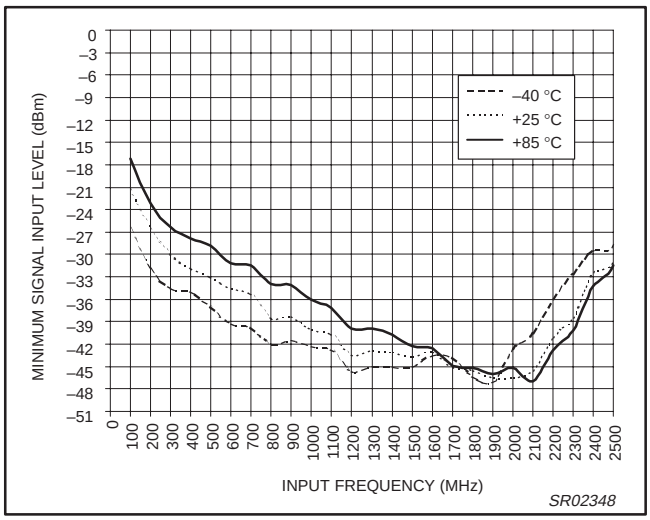


Figure 30. Main Divider Input Sensitivity vs. Frequency and Temperature (I_{SET} = 164 µA; NF = 0; MOD = 8; N = 853; V_{DD} = 3.0 V)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

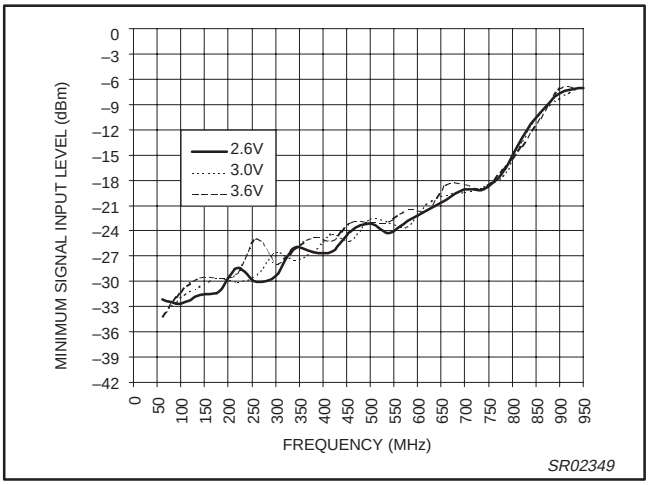


Figure 31. Auxiliary Divider Input Sensitivity vs. Frequency and Supply Voltage (Temp = 25 °C; I_{SET} = 164 μA; Divider Ratio = 213)

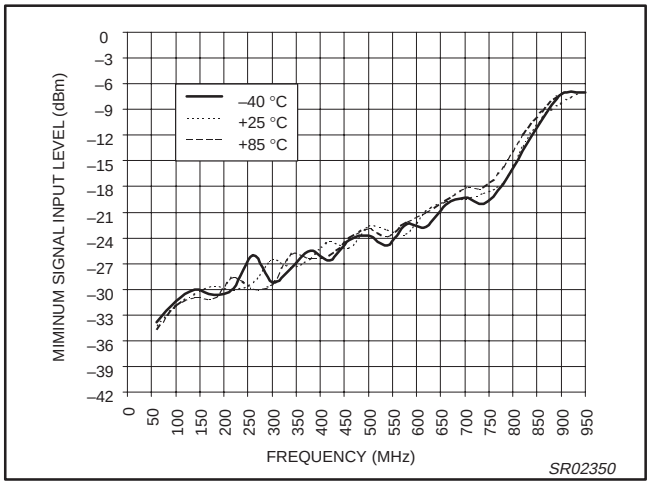


Figure 32. Auxiliary Divider Input Sensitivity vs. Frequency and Temperature (I_{SET} = 164 μA; Divider Ratio = 213; V_{DD} = 3.0 V)

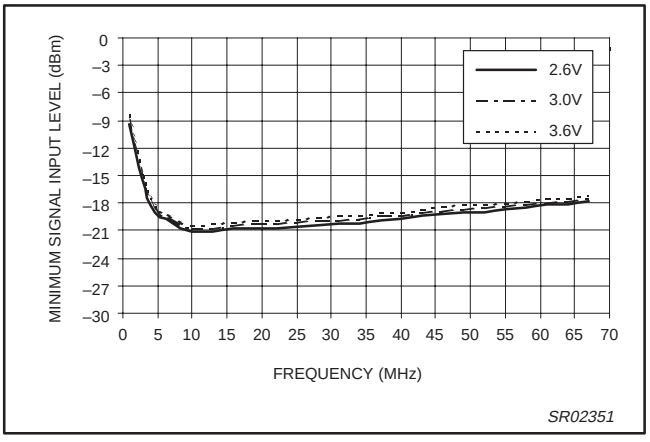


Figure 33. Reference Divider Input Sensitivity vs. Frequency and Supply Voltage (Temp = 25 °C; I_{SET} = 164 μA; Divider Ratio = 682)

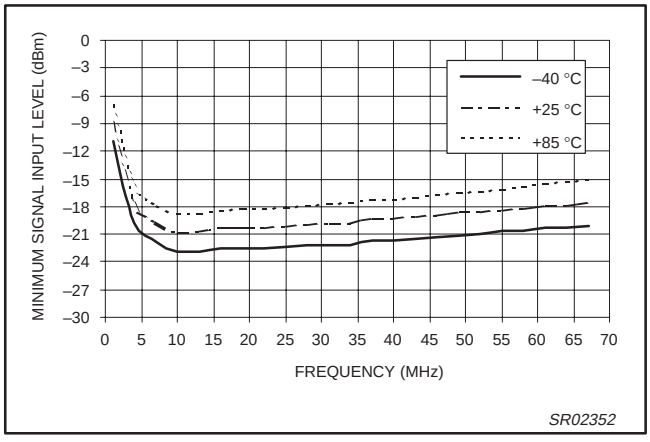


Figure 34. Reference Divider Input Sensitivity vs. Frequency and Temperature (I_{SET} = 164 μA; Divider Ratio = 682; V_{DD} = 3.0 V)

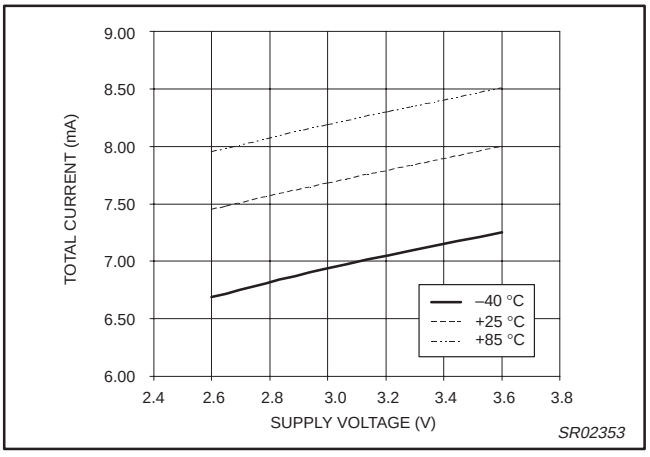
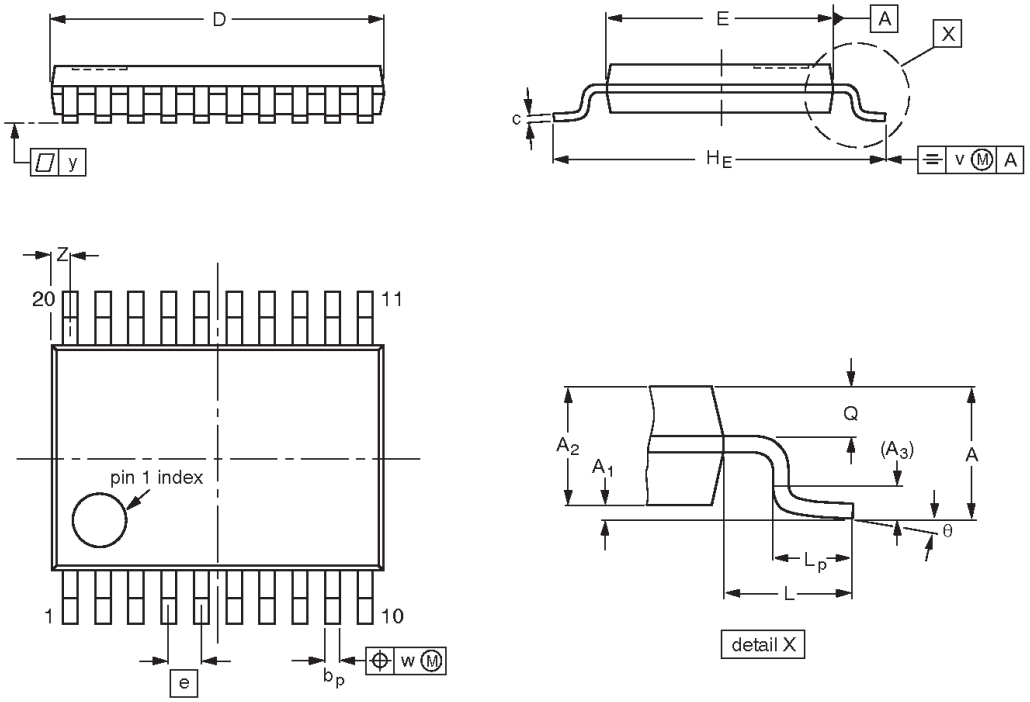
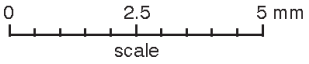


Figure 35. Total Supply Current vs. Temperature (I_{SET} = 164 μA)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm SOT360-1





DIMENSIONS (mm are the original dimensions)

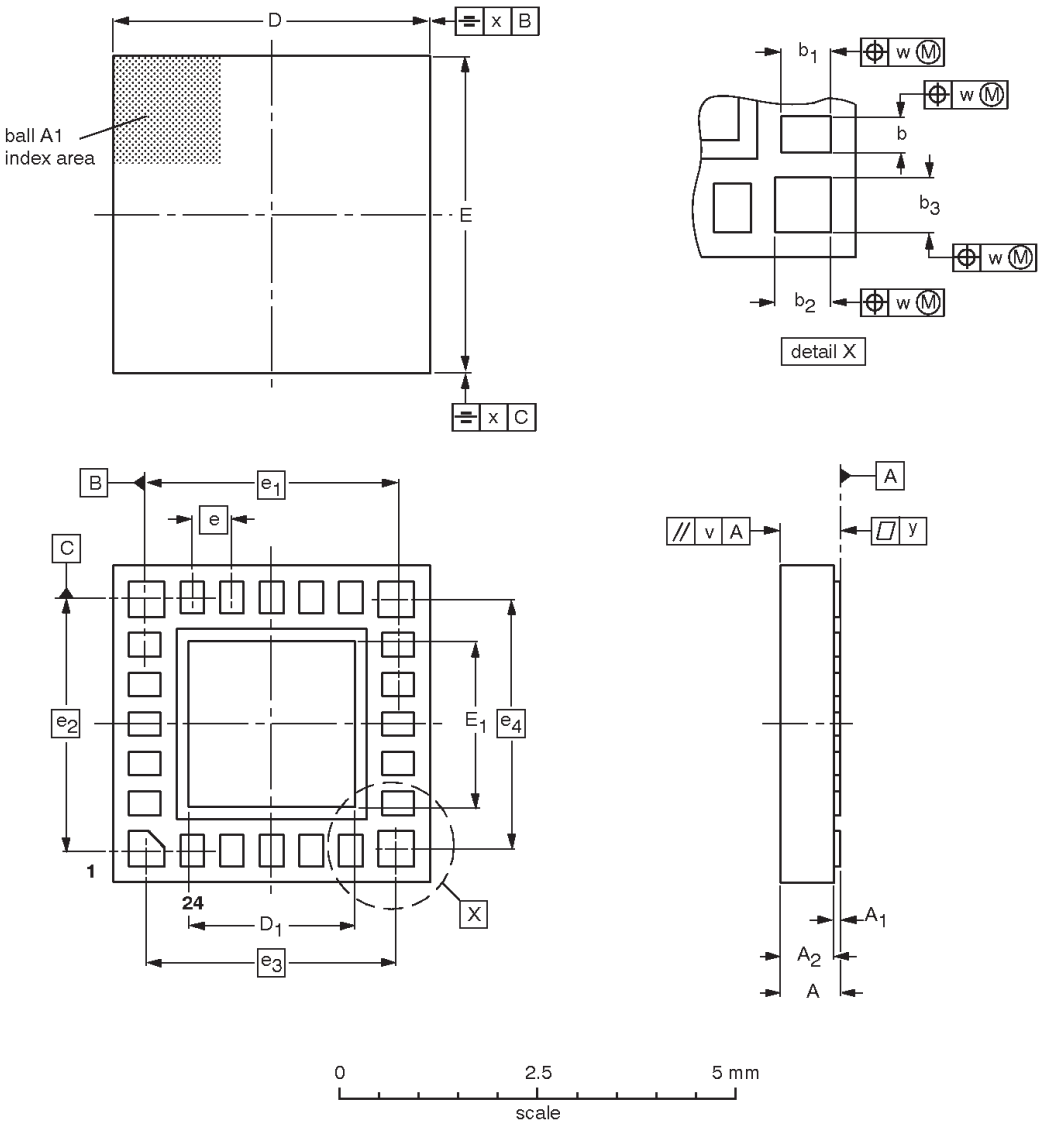
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153				~~95-02-04~~ 99-12-27

HBCC24: plastic, heatsink bottom chip carrier; 24 terminals; body 4 x 4 x 0.65 mm SOT564-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	b_1	b_2	b_3	D	D_1	E	E_1	e	e_1	e_2	e_3	e_4	v	w	x	y
mm	0.80	0.10 0.05	0.70 0.60	0.35 0.20	0.50 0.30	0.50 0.35	0.50 0.35	4.1 3.9	2.2 2.0	4.1 3.9	2.2 2.0	0.5	3.2	3.2	3.15	3.15	0.2	0.15	0.15	0.05

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT564-1		MO-217				~~00-02-01~~ 00-08-28

NOTES

2.5 GHz low voltage, low power RF fractional-N/IF integer frequency synthesizer

SA8027

Data sheet status

Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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