

# CGS700V

## Commercial Low Skew PLL 1 to 9 CMOS Clock Driver

### General Description

CGS700 is an off the shelf clock driver specifically designed for today's high speed processors. It provides low skew outputs which are produced at different frequencies from three fixed input references. The XTALIN input pin is designed to be driven from three distinct crystal oscillators running at 25 MHz, 33 MHz or 40 MHz.

The PLL, using a charge pump and an internal loop filter, multiplies this input frequency to create a maximum output frequency of four times the input.

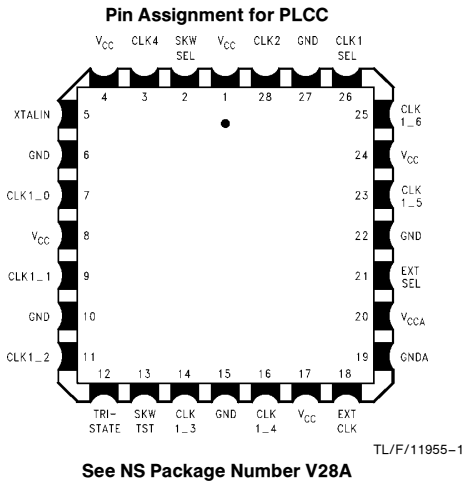
The device includes a TRI-STATE® control pin to disable the outputs while the PLL is still in lock. This function allows for testing the board without having to wait to acquire the lock once the testing is complete. (continued)

### Features

- Guaranteed and tested:
  - 500 ps pin-to-pin skew ( $t_{OSHL}$  and  $t_{OSLH}$ ) on 1X outputs

- Guaranteed:
  - 400 ps pin-to-pin skew ( $t_{OSHL}$  and  $t_{OSLH}$ ) on 1X outputs
- Pentium™ and PowerPC™ compatible
- Output buffer of nine drivers for large fanout
- 25 MHz–160 MHz output frequency range
- Outputs operating at 4X, 2X, 1X of the reference frequency for multi-frequency bus applications
- Selectable output frequency
- TRI-STATE output control with the PLL is in the lock state
- Internal loop filter to reduce noise and jitter
- Separate analog and digital  $V_{CC}$  and Ground pins
- Low frequency test mode by disabling the PLL
- Implemented on National's Core CMOS process
- Symmetric output current drive:
  - +30 mA / -30 mA  $I_{OL}/I_{OH}$
- 28-pin PCC for optimum skew performance
- Guaranteed 2k ESD protection

### Connection Diagram



### Pin Description

#### PLCC Package

Pin	Name	Description
1	$V_{CC}$	Digital $V_{CC}$
2	SKWSEL	Skew Test Selector Pin
3	CLK4	4X Clock Output
4	$V_{CC}$	Digital $V_{CC}$
5	XTALIN	Crystal Oscillator Input
6	GND	Digital Ground
7	CLK1__0	1X Clock Output
8	$V_{CC}$	Digital $V_{CC}$
9	CLK1__1	1X Clock Output
10	GND	Digital Ground
11	CLK1__2	1X Clock Output
12	TRI-STATE	Output TRI-STATE Control
13	SKWTST	Skew Testing Pin
14	CLK1__3	1X Clock Output
15	GND	Digital Ground
16	CLK1__4	1X Clock Output
17	$V_{CC}$	Digital $V_{CC}$
18	EXTCLK	External Test Clock
19	GND	Analog Ground
20	$V_{CCA}$	Analog $V_{CC}$
21	EXTSEL	External Clock Mux Selector
22	GND	Digital Ground
23	CLK1__5	1X Clock Output
24	$V_{CC}$	Digital $V_{CC}$
25	CLK1__6	1X Clock Output
26	CLK1SEL	CLK1 Multiplier Selector
27	GND	Digital Ground
28	CLK2	2X Clock Output

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## General Description (Continued)

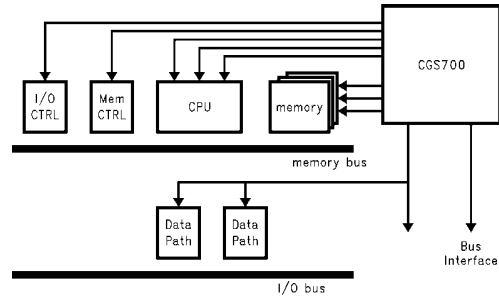
Also included, are two EXTSEL and EXTCLK pins to allow testing the chip via an external source. The EXTSEL pin, once set to high, causes the External-Clock\_Mux to change its input from the output of the VCO and Counter to the external clock signal provided via EXTCLK input pin. CLK1SEL pin changes the output frequency of the CLK1\_\_0, CLK1\_\_6 outputs. During normal operation, when CLK1SEL pin is high, these outputs are at the same frequency as the input crystal oscillator, while CLK2 and CLK4 outputs are at twice and four times the input frequency respectively.

Once CLK1SEL pin is set to a low logic level, the CLK1 outputs will be at twice the input frequency, the same as the CLK2 output, with CLK4 output still being at four times the input frequency.

In addition two other pins are added for increasing the test capability. SKWSEL and SKWTST pins allow testing of the counter's output and skew of the output drivers by bypassing the VCO. In this test mode CLK4 frequency is the same

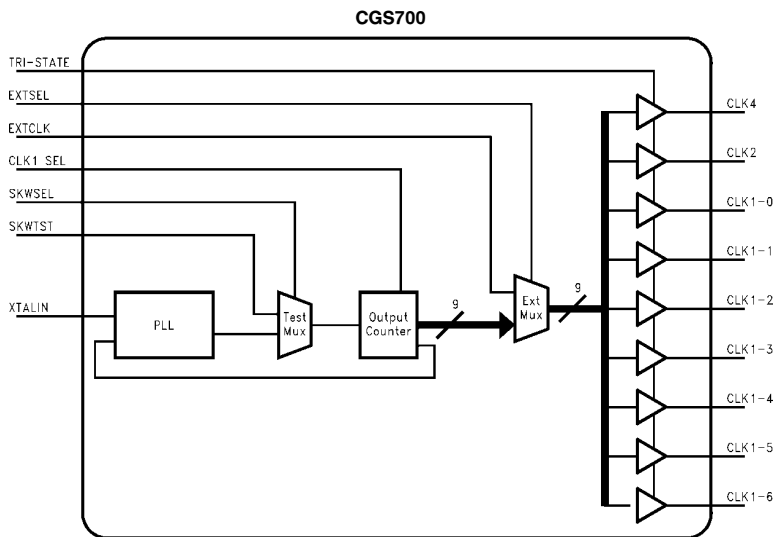
as SKWTST input frequency, while CLK2 is  $\frac{1}{2}$  and CLK1 frequencies are  $\frac{1}{4}$  respectively (refer to the truth table). In addition CLK1SEL functionality is also true under this test condition.

## Typical Application



TL/F/11955-3

## Block Diagram



TL/F/11955-2

## Truth Table

Input						Output		
CLK1 SEL	EXT SEL	EXT CLK	SKW SEL	SKW TST	TRI-STATE	CLK4	CLK2	CLK1
*H	L	X	L	X	H	$4 \times f_{IN}$	$2 \times f_{IN}$	$f_{IN}$
*L	L	X	L	X	H	$4 \times f_{IN}$	$2 \times f_{IN}$	$2 \times f_{IN}$
X	H		X	X	H			
H	L	X	H		H	$1 \times f_{tst}$	$\frac{1}{2} \times f_{tst}$	$\frac{1}{4} \times f_{tst}$
L	L	X	H		H	$1 \times f_{tst}$	$\frac{1}{2} \times f_{tst}$	$\frac{1}{2} \times f_{tst}$
X	X	X	X	X	L	Z	Z	Z

\*Steady State phase, frequency lock.

## CGS700

### Absolute Maximum Ratings (Note A)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage Diode Current ( $I_{IK}$ )	
$V = -0.5V$	-20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_O$ )	
$V = -0.5V$	-20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 60$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 60$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature	150°C
Power Dissipation (Static and Dynamic) (Note B)	1400 mW

**Note A:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

**Note B:** Power dissipation is calculated using  $49^\circ/W$  as the thermal coefficient for the PCC package at 225 LFM airflow. The input frequency is assumed @ 33 MHz with CLK4 at 132 MHz and CLK2 and CLK1's being at 66 MHz. In addition the ambient temperature is assumed with power supply at 5.0V.

### Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Input Crystal Frequency	25 MHz to 40 MHz
Operating Temperature ( $T_A$ )	0°C to +70°C
External Clock Frequency (EXTCLK Pin)	1 MHz to 10 MHz
XTALIN Duty Cycle Range	25/75 (75/25)%
Input Rise and Fall Times (0.8V to 2.0V)	
Crystal Input	5 ns max
All Other Inputs	10 ns max
Typical $\theta_{JA}$	
0 LFM	54 °C/W
225 LFM	45 °C/W
500 LFM	38 °C/W
900 LFM	34 °C/W

### DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$

Symbol	Parameter	Conditions	$V_{CC} = 4.5V-5.5V$ $T_A = 0^\circ C-70^\circ C$			Units
			Min	Typ	Max	
$V_{IH}$	Minimum Input High Level Voltage		2.0			V
$V_{IL}$	Maximum Input Low Level Voltage				0.8	V
$V_{OH}$	Minimum Output High Level Voltage	$I_{OUT} = -50 \mu A$ $I_{OH} = -30 mA$	$V_{CC} - 0.1$			V
$V_{OL}$	Maximum Output Low Level Voltage	$I_{OUT} = 50 \mu A$ $I_{OL} = 30 mA$			0.1 0.6	V
$I_{OHD}$	High Level Output Current	$V_{OH} = V_{CC} - 1.0V$	50	110	170	mA
$I_{OLD}$	Low Level Output Current	$V_{OL} = 1.0V$	50	110	170	mA
$I_{IN}$	Leakage Current	$V_{IN} = 0.4V$ or $4.6V$	-50		50	$\mu A$
$I_{OZL/H}$	Output Leakage Current					
$C_{IN}$	Input Capacitance				10.0	pF
$I_{CC}$	Quiescent Digital + Analog Current (No Load)	$V_{IN} = V_{CC}, GND$		3.0	5.0	mA
$I_{CCT}$	$I_{CC}$ per TTL Input	$V_{IN} = V_{CC} - 2.1, GND$			2.5	

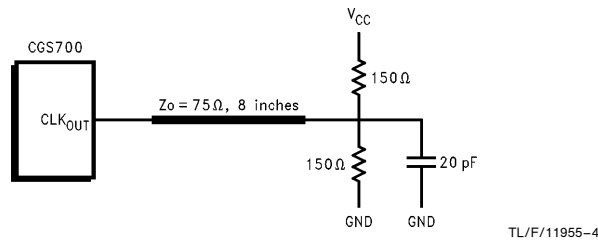
## CGS700 (Continued)

### AC Electrical Characteristics

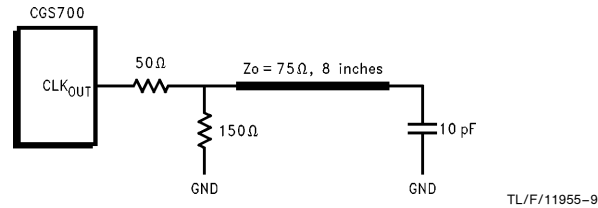
Over recommended operating free air temperature range. All typical values are measured at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$

Symbol	Parameter		$V_{CC} = 4.5V-5.5V$ $F_{IN} = 25\text{ MHz}-40\text{ MHz}$ $T_A = 0^\circ C-70^\circ C$ $C_L = \text{Circuit 1 and 2}$ $R_L = \text{Circuit 1 and 2}$			Units	Notes	
			Min	Typ	Max			
$t_{rise}$	Output Rise	CLK4	0.8V-2.6V			2.0	ns	(Notes 1, 5)
		CLK2	$1.0V - V_{CC} - 1.0V$					
		CLK1	$1.0V - V_{CC} - 1.0V$					
		ALL	0.8V-2.0V			1.5		
$t_{fall}$	Output Fall	CLK4	2.6V-0.8V			2.0	ns	(Notes 1, 5)
		CLK2	$V_{CC} - 1.0V - 1.0V$					
		CLK1	$V_{CC} - 1.0V - 1.0V$					
		ALL	2.0V-0.8V			1.5		
$t_{skew}$	Maximum Edge-to-Edge Output Skew	+ to + Edges	CLK1_CLK1			400	ps	(Notes 2, 5)
		+ to + Edges	CLK1_CLK4			1000		
		+ to + Edges	CLK2_CLK4			1000		
$t_{lock}$	Time to Lock the Output to the Synch Input					100	$\mu s$	
$t_{cycle}$	Output Duty Cycle	CLK1 Outputs		49		51	%	(Notes 3, 5)
		CLK2 Output		49		51		
		CLK4 Output		35		65		
$J_{LT}$	Output Jitter (Long Term)					0.3	ns	(Notes 4, 5)
$F_{MIN}$	Minimum XTALIN Frequency					15	MHz	
$F_{MAX}$	Maximum XTALIN Frequency					43	MHz	

**Circuit 1. Test Circuit for CLK1 and CLK2**



**Circuit 2. Test Circuit for CLK4**



## CGS700 (Continued)

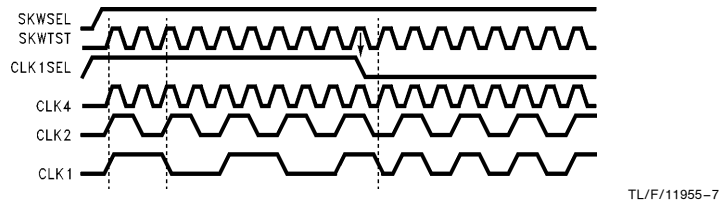
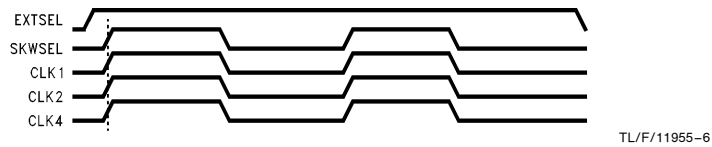
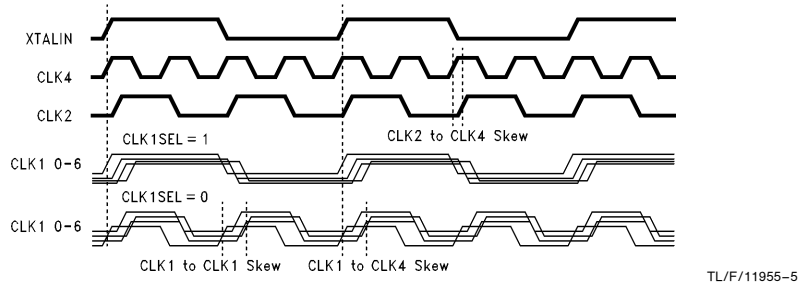
**Note 1:**  $t_{rise}$  and  $t_{fall}$  parameters are measured at the pin of the device.

**Note 2:** Skew is measured at 50% of  $V_{CC}$  for CLK1 and CLK2 while it is measured @ 1.4V for CLK4. Limits are guaranteed by design.

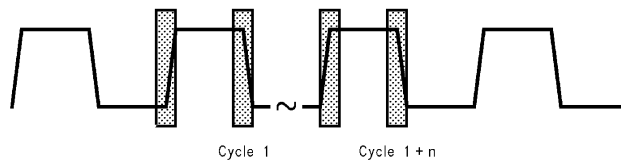
**Note 3:** Output duty cycle is measured at  $V_{DD}/2$  for CLK1 and CLK2 while it is measured @ 1.4V for CLK4. Limits are guaranteed by design.

**Note 4:** Jitter parameter is characterized and is guaranteed by design only. It measures the uncertainty of either the positive or the negative edge over 1000 cycles. It is also measured at output levels of  $V_{CC}/2$ . Refer to *Figure 2* for further explanation.

**Note 5:** The GNDA pins of the 700 must be as free of noise as possible for minimum jitter. Separate analog ground plane is recommended for the PCB. Also the  $V_{CCA}$  pin requires extra filtering to further reduce noise. Ferrite beads for filtering and bypass capacitors are suggested for  $V_{CCA}$  pin.



**FIGURE 1. Waveforms**



Jitter =  $|\text{Period}(1) - \text{Period}(n+1)| = 300 \text{ ps}$  for either the rising or falling edge, where  $n$  is 1 to 1000 cycles.

**FIGURE 2. Jitter**

### Application References and Bibliography

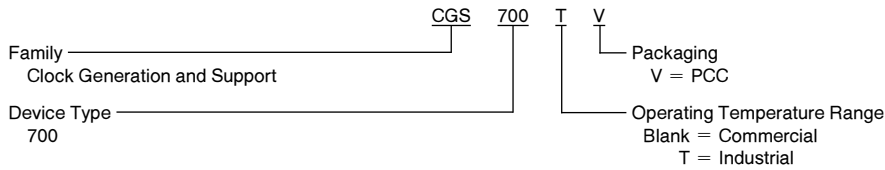
Information relating to EMI as well as general application issues are in the following application notes:

AN-988—EMI App Note

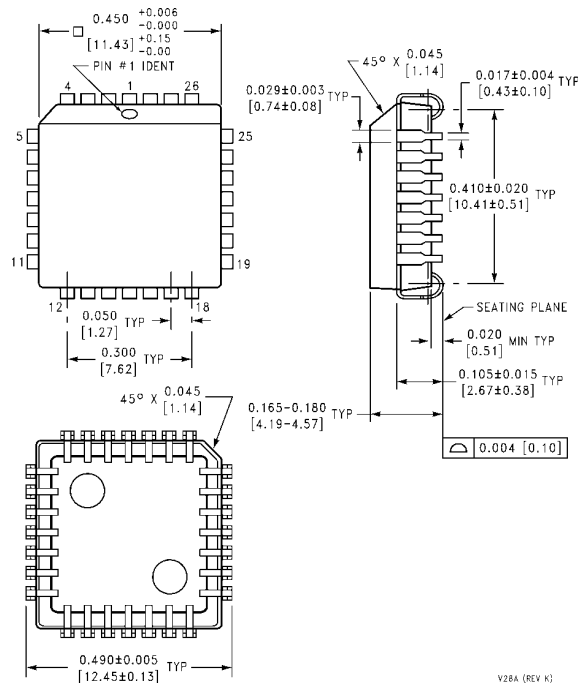
AN-640

AN-991

**Ordering Information** (Contact NSC Marketing for specific date of availability)



**Physical Dimensions** inches (millimeters) unless otherwise noted




**28-Lead Plastic Leaded Chip Carrier  
 NS Package Number V28A**

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