



# TAS2552 4.0-W Class-D Mono Audio Amplifier with Class-G Boost and Speaker Sense

## 1 Features

- Analog or Digital Input Mono Boosted Class-D Amplifier
- 4.0 W into 8  $\Omega$  Load from 4.2 V Supply (1% THD+N)
- Efficiency of 85% at Rated Power
- I2S, Left-Justified, Right-Justified, DSP, PDM, and TDM Input and Output Interface
- Input Sample Rates from 8 kHz to 192 kHz
- High Efficiency Class-G Boost Converter
  - Automatically Adjusts Class-D Supply
- Built-In Speaker Sense
  - Measures Speaker Current and Voltage
  - Measures VBAT and VBOOST Voltages
- Built-In Automatic Gain Control (AGC)
  - Limits Battery Current Consumption
- Adjustable Class-D Switching Edge-Rate Control
- Power Supplies
  - Boost Input: 3.0 V to 5.5 V
  - Analog: 1.65 V to 1.95 V
  - Digital I/O: 1.5 V to 3.6 V
- Thermal and Short-Circuit Protection
- I<sup>2</sup>C Interface for Register Control
- Stereo Configuration Using Two TAS2552s
  - I<sup>2</sup>C Address Select Terminal (ADDR)
- 2.855 mm x 2.575 mm, 0.4 mm Pitch 30-Ball WCSP

## 2 Applications

- Mobile Phones
- PND
- Portable Audio Docks
- Tablets
- Gaming Devices

## 3 Description

The TAS2552 is a high efficiency Class-D audio power amplifier with advanced battery current management and an integrated Class-G boost converter. The device constantly measures the current and voltage across the load and provides a digital stream of this information.

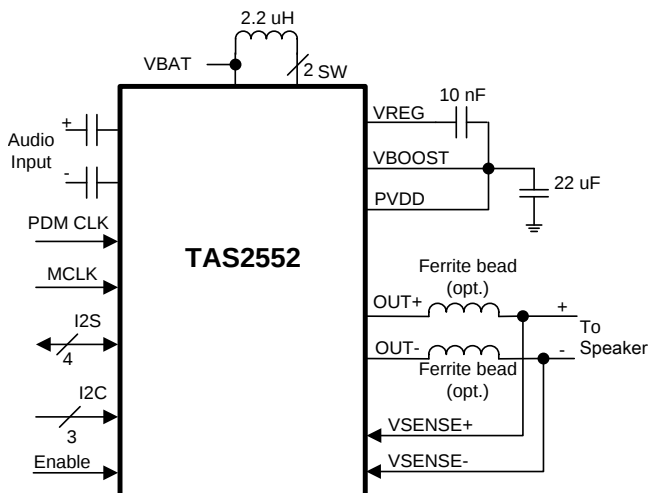
The Class-G boost converter generates the Class-D amplifier supply rail. During low Class-D output power, the boost improves efficiency by deactivating and connecting VBAT directly to the Class-D amplifier supply. When high power audio is required, the boost quickly activates to provide significantly louder audio than a stand-alone amplifier connected directly to the battery.

The AGC automatically adjusts Class-D gain to reduce battery current at end-of-charge voltages, preventing output clipping, distortion and early system shutdown. The fixed gain is adjustable via I<sup>2</sup>C. The gain range is -7 dB to +24 dB in 1 dB steps.

In addition to a differential mono analog input, the TAS2552 has built-in a 16-bit D/A converter used with a digital input. Moving the D/A converter from the digital host processor into the integrated amplifier process provides better dynamic performance at lower system cost. Additionally, since the PCB routing is digital rather than analog, sensitivity to external perturbations such as GSM frame-rate noise is decreased at the system level.

### Device Information

| ORDER NUMBER | PACKAGE   | BODY SIZE           |
|--------------|-----------|---------------------|
| TAS2552YFF   | WCSP (30) | 2.855 mm x 2.575 mm |



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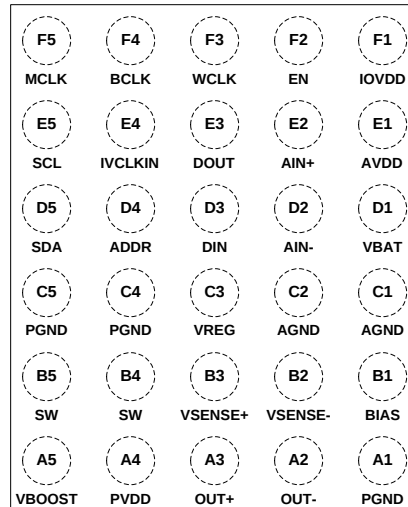
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## 4 Revision History

| Changes from Revision A (February 2014) to Revision B                    | Page      |
|--------------------------------------------------------------------------|-----------|
| • Added clarification on EN Pin Function and Configuration.....          | <b>3</b>  |
| • Changed VBAT MAX = 2.45 V. Added footnote to avoid VBAT reset. ....    | <b>7</b>  |
| • Added clarification on wait time regarding DEV_RESET Register.....     | <b>32</b> |
| • Added clarification on VBAT reset range for normal operation mode..... | <b>49</b> |
| Changes from Original (January 2014) to Revision A                       | Page      |
| • Changed from Product Preview to Production Data .....                  | <b>1</b>  |

## 5 Pin Configuration and Functions

**30-Ball WCSP  
YFF Package  
(Top View)**



**Pin Functions**

| TERMINAL          |           | INPUT/OUTPUT/<br>POWER | DESCRIPTION                                                                                                                      |
|-------------------|-----------|------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| NAME              | BALL WCSP |                        |                                                                                                                                  |
| PGND              | A1        | P                      | Power ground. Connect to high current ground plane.                                                                              |
| OUT–              | A2        | O                      | Inverting Class D output.                                                                                                        |
| OUT+              | A3        | O                      | Non-inverting Class D output.                                                                                                    |
| PVDD              | A4        | P                      | Class-D power supply. Connected internally to VBOOST – do not drive this terminal externally.                                    |
| VBOOST            | A5        | P                      | 8.5 V boost output. Connected internally to PVDD – do not drive this terminal externally.                                        |
| BIAS              | B1        | O                      | Mid-rail reference for Class D channel.                                                                                          |
| VSENSE–           | B2        | I                      | Inverting voltage sense input.                                                                                                   |
| VSENSE+           | B3        | I                      | Non-inverting voltage sense input.                                                                                               |
| SW                | B4,B5     | I/O                    | Boost switch terminal.                                                                                                           |
| AGND              | C1,C2     | P                      | Analog ground. Connect to low noise ground plane.                                                                                |
| VREG              | C3        | O                      | High-side FET gate drive boost converter.                                                                                        |
| PGND              | C4,C5     | P                      | Power ground. Connect to high current ground plane.                                                                              |
| VBAT              | D1        | P                      | Battery power supply. Connect to 3.0 V to 5.5 V battery supply.                                                                  |
| AIN–              | D2        | I                      | Inverting analog input.                                                                                                          |
| DIN               | D3        | I                      | Audio serial data input. Format is I2S, LJF, RJF, or TDM data.                                                                   |
| ADDR              | D4        | I                      | I <sup>2</sup> C address select terminal. Set ADDR = GND for device 7-bit address 0x40; set ADDR = IOVDD for 7-bit address 0x41. |
| SDA               | D5        | I/O                    | I <sup>2</sup> C control bus data.                                                                                               |
| AVDD              | E1        | P                      | Analog low voltage supply terminal. Connect to 1.65 V to 1.95 V supply.                                                          |
| AIN+              | E2        | I                      | Non-inverting analog input.                                                                                                      |
| DOUT              | E3        | O                      | Serial I/V digital output. Format is I2S, LJF, RJF, TDM, or undecimated PDM data.                                                |
| IVCLKIN           | E4        | I                      | Serial clock input for undecimated PDM I/V data.                                                                                 |
| SCL               | E5        | I                      | I <sup>2</sup> C control bus clock.                                                                                              |
| EN <sup>(1)</sup> | F2        | I                      | Device enable (HIGH = Normal Operation, LOW = Standby)                                                                           |

(1) Wait a minimum of 1ms after EN is pulled high or DEV\_RESET is issued before accessing the control interface. EN=low will erase the TAS2552 device configuration. The TAS2552 device must be configured (see [Initialization](#)) after EN=high.

## Pin Functions (continued)

| TERMINAL |           | INPUT/OUTPUT/<br>POWER | DESCRIPTION                                                                  |
|----------|-----------|------------------------|------------------------------------------------------------------------------|
| NAME     | BALL WCSP |                        |                                                                              |
| WCLK     | F3        | I                      | Audio serial word clock.                                                     |
| BCLK     | F4        | I                      | Audio serial bit clock.                                                      |
| MCLK     | F5        | I                      | External master clock.                                                       |
| IOVDD    | F1        | P                      | Supply for digital input and output levels. Voltage range is 1.5 V to 3.6 V. |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

|            |                                           | MIN                                     | MAX         | UNIT |
|------------|-------------------------------------------|-----------------------------------------|-------------|------|
| VBAT       | Battery voltage                           | −0.3                                    | 6.0         | V    |
| AVDD       | Analog supply voltage                     | −0.3                                    | 2.5         | V    |
| IOVDD      | I/O Supply voltage                        | −0.3                                    | 3.9         | V    |
| AIN+, AIN− | Analog input voltage                      | −0.3                                    | AVDD + 0.3  | V    |
|            | Digital input voltage                     | −0.3                                    | IOVDD + 0.3 | V    |
|            | Output continuous total power dissipation | See <a href="#">Thermal Information</a> |             | NA   |

### 6.2 Handling Ratings

| PARAMETER        | DEFINITION                | MIN | MAX  | UNIT             |
|------------------|---------------------------|-----|------|------------------|
| $T_{\text{stg}}$ | Storage temperature range | −65 | 150  | $^\circ\text{C}$ |
| ESD              | HBM                       |     | 3000 | V                |
|                  | CDM                       |     | 1500 |                  |

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|       |                                | MIN  | NOM | MAX  | UNIT             |
|-------|--------------------------------|------|-----|------|------------------|
| VBAT  | Battery voltage                | 3.0  |     | 5.5  | V                |
| AVDD  | Analog supply voltage          | 1.65 | 1.8 | 1.95 | V                |
| IOVDD | I/O supply voltage             | 1.5  | 1.8 | 3.6  | V                |
| $T_A$ | Operating free-air temperature | −40  |     | 85   | $^\circ\text{C}$ |
| $T_J$ | Operating junction temperature | −40  |     | 150  | $^\circ\text{C}$ |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TAS2552            | UNIT               |
|-------------------------------|----------------------------------------------|--------------------|--------------------|
|                               |                                              | YFF (30 TERMINALS) |                    |
| $\theta_{JA}$                 | Junction-to-ambient thermal resistance       | 76.5               | $^\circ\text{C/W}$ |
| $\theta_{J\text{Ctop}}$       | Junction-to-case (top) thermal resistance    | 0.2                |                    |
| $\theta_{JB}$                 | Junction-to-board thermal resistance         | 44.0               |                    |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 1.6                |                    |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 43.4               |                    |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

VBAT = 3.6 V, AVDD = IOVDD = 1.8 V, EN = IOVDD, SWS = 0, Gain = 15 dB, ERC = 14 ns,  $R_L = 8\ \Omega + 33\ \mu\text{H}$ , 48 kHz sample rate for digital input, ILIM = 2.5 A (unless otherwise noted)

| PARAMETER                                                | TEST CONDITIONS                                                                                                    | MIN  | TYP  | MAX | UNIT             |
|----------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|------|------|-----|------------------|
| <b>BOOST CONVERTER</b>                                   |                                                                                                                    |      |      |     |                  |
| Boost Output Voltage                                     | Average voltage (w/o including ripple). Includes load regulation (0-0.6A) and line regulation (VBAT = 3.0 – 4.8V). |      | 8.5  |     | V                |
| Boost Converter Switching Frequency                      |                                                                                                                    |      | 1.8  |     | MHz              |
| <b>CLASS-D CHANNEL</b>                                   |                                                                                                                    |      |      |     |                  |
| Max Analog Input                                         | For THD+N < 1%                                                                                                     |      | 1    |     | V <sub>RMS</sub> |
| Full-Scale DAC Output                                    | All digital interface modes                                                                                        |      | 1    |     | V <sub>RMS</sub> |
| Load Resistance (Load Spec Reistance)                    |                                                                                                                    | 6    | 8    |     | $\Omega$         |
| Class-D Frequency                                        |                                                                                                                    |      | 758  |     | kHz              |
| Class-D + Boost Efficiency                               | VBAT = 5.5, Pout = 1 W (sinewave)                                                                                  |      | 75%  |     |                  |
| Class-D Output Current Limit (Short Circuit Protection)  | VBOOST = 8.5 V, OUT– shorted to VBAT or VBOOST                                                                     |      | 3.6  |     | A                |
| Class-D Output Offset Voltage in Analog Input Mode       | VBAT = 3.6 V, AV = 15 dB, $R_L = 8\ \Omega$ , input shorted to ground through single capacitor                     | -7.4 |      | 4.6 | mV               |
| Class-D Output Offset Voltage in Digital Input Mode      | VBAT = 3.6 V, AV = 15 dB, $R_L = 8\ \Omega$ , 0's data                                                             | -9.8 |      | 5.6 | mV               |
| Programmable Channel Gain Range (PGA + class-D), minimum | Typical value, analog and digital input                                                                            |      | -7   |     | dB               |
| Programmable Channel Gain Range (PGA + class-D), maximum | Typical value, analog and digital input                                                                            |      | 24   |     | dB               |
| Programmable Channel Gain Step (PGA + class-D)           | Typical value, analog and digital input                                                                            |      | 1    |     | dB               |
| Mute Attenuation                                         | Device in shutdown, digital input only                                                                             |      | 110  |     | dB               |
| VBAT Power Supply Rejection Ratio (PSRR)                 | Ripple of 200mVpp @ 217 Hz, Gain = 15 dB, analog and digital input                                                 |      | 73   |     | dB               |
|                                                          | Ripple of 200mVpp @ 1 kHz, Gain = 15 dB, analog and digital input                                                  |      | 72   |     |                  |
|                                                          | Ripple of 200mVpp @ 4 kHz, Gain = 15 dB, analog and digital input                                                  |      | 72   |     |                  |
| AVDD Power Supply Rejection Ratio (PSRR)                 | Ripple of 200mVpp @ 217 Hz, Gain = 15 dB, analog and digital input                                                 |      | 77   |     | dB               |
|                                                          | Ripple of 200mVpp @ 1 kHz, Gain = 15 dB, analog and digital input                                                  |      | 78   |     |                  |
|                                                          | Ripple of 200mVpp @ 4 kHz, Gain = 15 dB, analog and digital input                                                  |      | 84   |     |                  |
| Common Mode Rejection Ratio                              | Ripple of 200mVpp @ 217 Hz, Gain = 15 dB, analog input                                                             |      | 59   |     | dB               |
| THD+N                                                    | 1 kHz, Po = 0.1W, VBAT = 3.6 V, $R_L = 8\ \Omega$                                                                  |      | 0.1% |     |                  |
|                                                          | 1 kHz, Po = 0.5W, VBAT = 3.6 V, $R_L = 8\ \Omega$                                                                  |      | 0.1% |     |                  |
|                                                          | 1 kHz, Po = 1 W, VBAT = 3.6 V, $R_L = 8\ \Omega$                                                                   |      | 0.1% |     |                  |
|                                                          | 1 kHz, Po = 2 W, VBAT = 3.6 V, $R_L = 8\ \Omega$                                                                   |      | 0.1% |     |                  |
| Output Integrated Noise (20Hz-20kHz) - 8 $\Omega$        | A-wt Filter, Gain = 15 dB, DAC modulator switching                                                                 |      | 114% |     | $\mu\text{V}$    |
|                                                          | A-wt Filter, Gain = 15 dB, Analog In, Inputs shorted                                                               |      | 114% |     |                  |

## Electrical Characteristics (continued)

VBAT = 3.6 V, AVDD = IOVDD = 1.8 V, EN = IOVDD, SWS = 0, Gain = 15 dB, ERC = 14 ns,  $R_L = 8\ \Omega + 33\ \mu\text{H}$ , 48 kHz sample rate for digital input, ILIM = 2.5 A (unless otherwise noted)

| PARAMETER                    |                                        | TEST CONDITIONS                                                                       | MIN   | TYP   | MAX   | UNIT              |
|------------------------------|----------------------------------------|---------------------------------------------------------------------------------------|-------|-------|-------|-------------------|
| Max Output Power, 8-Ω Load   |                                        | THD+N = 1%, VBAT = 3.0 V, ILIM = 2.5 A                                                |       | 2.8   |       | W                 |
|                              |                                        | THD+N = 1%, VBAT = 3.6 V, ILIM = 2.5 A                                                |       | 3.3   |       |                   |
|                              |                                        | THD+N = 1%, VBAT = 4.2 V, GAIN = 16 dB, ILIM = 3.0 A                                  |       | 4.0   |       |                   |
| Output Impedance in Shutdown |                                        | EN = 0 V                                                                              |       | 10    |       | kΩ                |
| Startup Time                 |                                        | Analog/digital input measured from time when device is taken out of software shutdown |       | 8     |       | mS                |
| Shutdown Time                |                                        | Measured from time when device is programmed in software shutdown mode                |       | 1     |       | μS                |
| INPUT SECTION                |                                        |                                                                                       |       |       |       |                   |
| Full-scale DAC output        |                                        | All digital interface modes                                                           |       | 1.0   |       | V <sub>RMS</sub>  |
| Maximum analog input voltage |                                        |                                                                                       |       | 1.0   |       | V <sub>RMS</sub>  |
| R <sub>IN</sub>              | Input impedance (terminals AIN+, AIN-) | EN = IOVDD, Amplifier active                                                          |       | 10    |       | kΩ                |
|                              |                                        | EN = 0 V, In shutdown                                                                 |       | 19    |       |                   |
| CURRENT SENSE                |                                        |                                                                                       |       |       |       |                   |
| Current Sense Full Scale     |                                        | Peak current which will give full scale digital output                                |       | 1.4   |       | A <sub>PEAK</sub> |
| Current Sense Accuracy       |                                        | I <sub>OUT</sub> = 354 mA <sub>RMS</sub> (1 W)                                        |       | 1%    |       |                   |
| Current Sense Offset         |                                        | Input referred                                                                        |       | 0.002 |       | mA                |
| Current Sense Gain Error     |                                        |                                                                                       |       | -0.09 |       | dB                |
| THD+N                        | Distortion + Noise                     | Po = 1.0W (Load = 8Ω + 33 μH)                                                         |       | 0.17% |       |                   |
| VOLTAGE SENSE                |                                        |                                                                                       |       |       |       |                   |
| Voltage Sense Full Scale     |                                        | Peak voltage which will give full scale digital output                                |       | 8.5   |       | V <sub>PEAK</sub> |
| Voltage Sense Accuracy       |                                        | V <sub>OUT</sub> = 2.83 Vrms (1W)                                                     |       | 2.2%  |       |                   |
| Voltage Sense Offset         |                                        | Input referred                                                                        |       | 1.45  |       | mV                |
| Voltage Sense Gain Error     |                                        |                                                                                       |       | -0.20 |       | dB                |
| THD+N                        | Distortion + Noise                     | Po = 1.0 W (Load = 8Ω + 33μH)                                                         |       | 0.08% |       |                   |
| INTERFACE                    |                                        |                                                                                       |       |       |       |                   |
| F <sub>MCLK</sub>            | MCLK frequency                         |                                                                                       | 0.512 |       | 49.15 | MHz               |
| F <sub>PDM</sub>             | PDM Clock (IVCLK) Frequency Range      |                                                                                       | 1.636 |       | 3.25  | MHz               |
| PDM <sub>DC</sub>            | PDM Clock (IVCLK) Duty Cycle Range     |                                                                                       | 40%   |       | 60%   |                   |

## Electrical Characteristics (continued)

VBAT = 3.6 V, AVDD = IOVDD = 1.8 V, EN = IOVDD, SWS = 0, Gain = 15 dB, ERC = 14 ns,  $R_L = 8\ \Omega + 33\ \mu\text{H}$ , 48 kHz sample rate for digital input, ILIM = 2.5 A (unless otherwise noted)

| PARAMETER                                                  | TEST CONDITIONS                   | MIN | TYP         | MAX                 | UNIT          |
|------------------------------------------------------------|-----------------------------------|-----|-------------|---------------------|---------------|
| <b>POWER CONSUMPTION</b>                                   |                                   |     |             |                     |               |
| Power Consumption with Analog Input and IV Sense Disabled  | From VBAT, PLL off, no signal     |     | 6.54        |                     | mA            |
|                                                            | From AVDD, PLL off, no signal     |     | 4.01        |                     | mA            |
|                                                            | From IOVDD, PLL off, no signal    |     | 0.04        |                     | mA            |
| Power Consumption with Digital Input and IV Sense Disabled | From VBAT, PLL off, no signal     |     | 6.82        |                     | mA            |
|                                                            | From AVDD, PLL off, no signal     |     | 4.16        |                     | mA            |
|                                                            | From IOVDD, PLL off, no signal    |     | 0.34        |                     | mA            |
| Power Consumption with Analog Input and IV Sense Enabled   | From VBAT, PLL on, no signal      |     | 6.54        |                     | mA            |
|                                                            | From AVDD, PLL on, no signal      |     | 7.26        |                     | mA            |
|                                                            | From IOVDD, PLL on, no signal     |     | 0.05        |                     | mA            |
| Power Consumption with Digital Input and IV Sense Enabled  | From VBAT, PLL on, no signal      |     | 6.59        |                     | mA            |
|                                                            | From AVDD, PLL on, no signal      |     | 8.34        |                     | mA            |
|                                                            | From IOVDD, PLL on, no signal     |     | 0.34        |                     | mA            |
| Power Consumption in Hardware Shutdown                     | From VBAT, EN = 0                 |     | 0.1         |                     | $\mu\text{A}$ |
|                                                            | From AVDD, EN = 0                 |     | 0.2         |                     | $\mu\text{A}$ |
|                                                            | From IOVDD, EN = 0                |     | 0.0         |                     | $\mu\text{A}$ |
| Power Consumption in Software Shutdown                     | From VBAT                         |     | 6.5         |                     | $\mu\text{A}$ |
|                                                            | From AVDD                         |     | 8.6         |                     | $\mu\text{A}$ |
|                                                            | From IOVDD                        |     | 126         |                     | $\mu\text{A}$ |
| <b>DIGITAL INPUT / OUTPUT</b>                              |                                   |     |             |                     |               |
| V <sub>IH</sub>                                            | High-level digital input voltage  |     | 0.7 x IOVDD |                     | V             |
| V <sub>IL</sub>                                            | Low-level digital input voltage   |     |             | 0.3 x IOVDD         | V             |
| V <sub>OH</sub>                                            | High-level digital output voltage |     | 0.9 x IOVDD |                     | V             |
| V <sub>OL</sub>                                            | Low-level digital output voltage  |     |             | 0.1 x IOVDD         | V             |
| <b>MISCELLANEOUS</b>                                       |                                   |     |             |                     |               |
| AVDD Supply Under-voltage Threshold                        | Device is in reset state          |     | 0.9         |                     | V             |
|                                                            | Device comes out of reset state   |     |             | 1.4                 |               |
| VBAT Supply Under-voltage Threshold                        | Device is in reset state          |     | 1.8         |                     | V             |
|                                                            | Device comes out of reset state   |     |             | 2.45 <sup>(1)</sup> |               |

(1) VBAT must be  $\geq 2.45\text{ V}$  to guarantee that the device is not reset.

## 6.6 Timing Requirements/Timing Diagrams

For I<sup>2</sup>C interface signals over recommended operating conditions (unless otherwise noted). **Note:** All timing specifications are measured at characterization but not tested at final test.

| PARAMETER   | TEST CONDITIONS                                | MIN | TYP | MAX | UNIT    |
|-------------|------------------------------------------------|-----|-----|-----|---------|
| $f_{SCL}$   | Frequency, SCL                                 |     |     | 400 | kHz     |
| $t_{W(H)}$  | Pulse duration, SCL high                       | 0.6 |     |     | $\mu$ s |
| $t_{W(L)}$  | Pulse duration, SCL low                        | 1.3 |     |     | $\mu$ s |
| $t_{su1}$   | Setup time, SDA to SCL                         | 100 |     |     | ns      |
| $t_{h1}$    | Hold time, SCL to SDA                          | 10  |     |     | ns      |
| $t_{(buf)}$ | Bus free time between stop and start condition | 1.3 |     |     | $\mu$ s |
| $t_{su2}$   | Setup time, SCL to start condition             | 0.6 |     |     | $\mu$ s |
| $t_{h2}$    | Hold time, start condition to SCL              | 0.6 |     |     | $\mu$ s |
| $t_{su3}$   | Setup time, SCL to stop condition              | 0.6 |     |     | $\mu$ s |

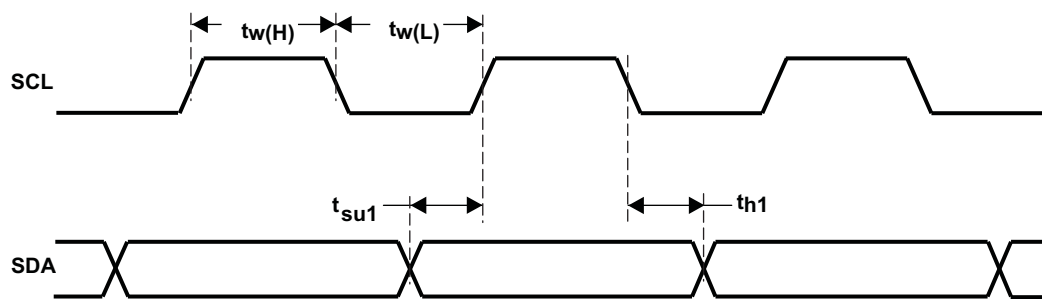


Figure 1. SCL and SDA Timing

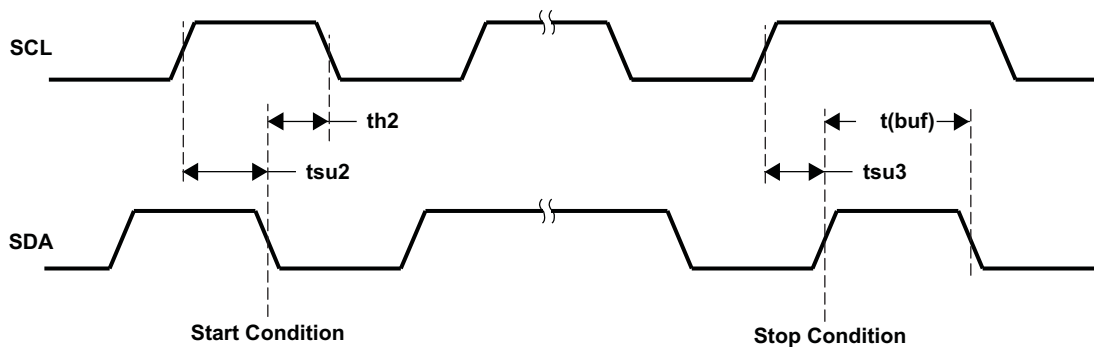
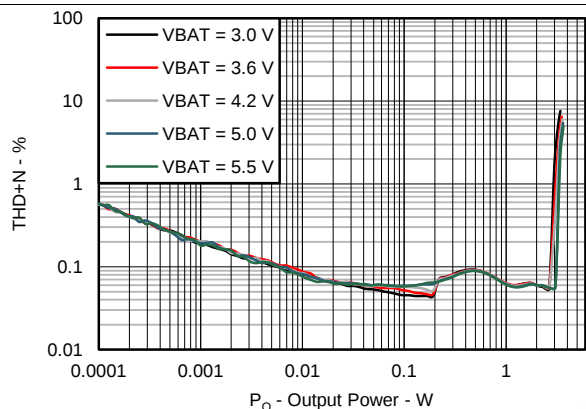


Figure 2. Start and Stop Conditions Timing

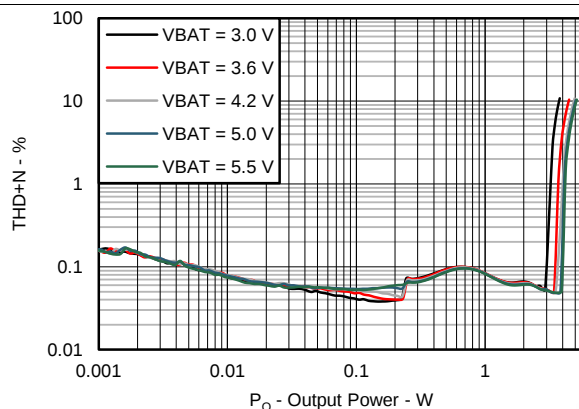
## 6.7 Typical Characteristics

VBAT = 3.6 V, AVDD = IOVDD = 1.8 V, EN = IOVDD, SWS = 0,  $R_L = 8\ \Omega + 33\ \mu\text{H}$  (unless otherwise noted).



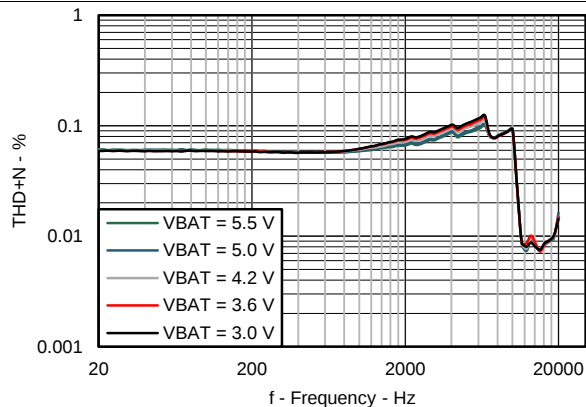
AGC = OFF, Gain = 15 dB

**Figure 3. THD+N vs Output Power (8Ω) for Digital Input**



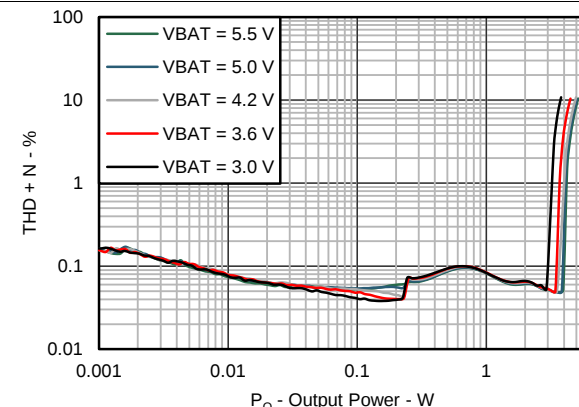
AGC = OFF, Gain = 15 dB

**Figure 4. THD+N vs Output Power (6Ω) for Digital Input**



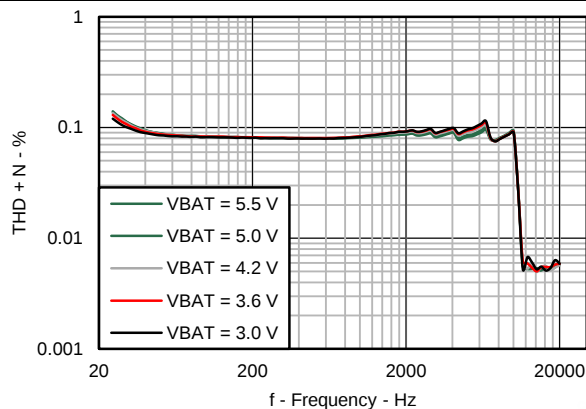
AGC = OFF, Gain = 15 dB,  $P_{out} = 1\ \text{W}$

**Figure 5. THD+N vs Frequency (8Ω) for Digital Input**



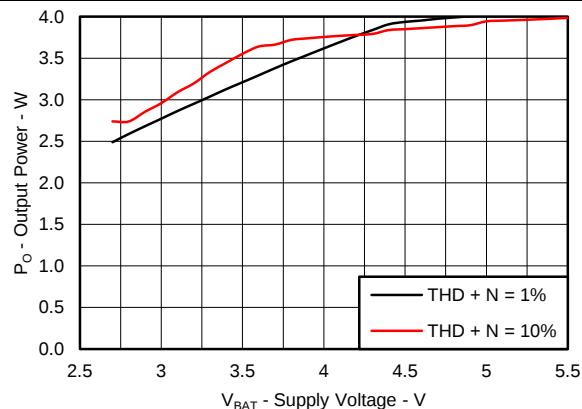
AGC = OFF, Gain = 15 dB,  $f = 1\ \text{kHz}$

**Figure 6. THD+N vs Output Power (8Ω) for Analog Input**



AGC = OFF, Gain = 15 dB

**Figure 7. THD+N vs Frequency (8Ω) for Analog Input**

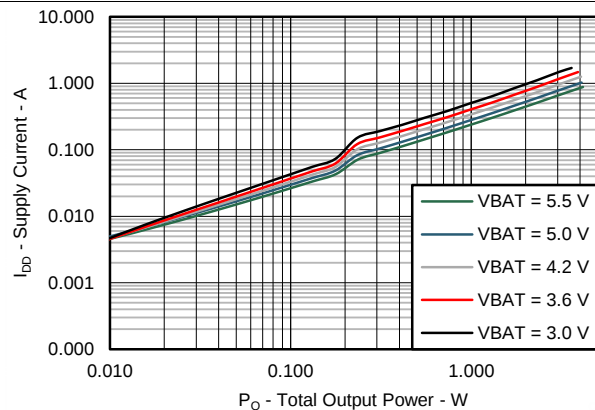


AGC = OFF, Gain = 24 dB,  $f = 1\ \text{kHz}$

**Figure 8. Output Power for 1% and 10% THD+N vs Supply Voltage (8Ω)**

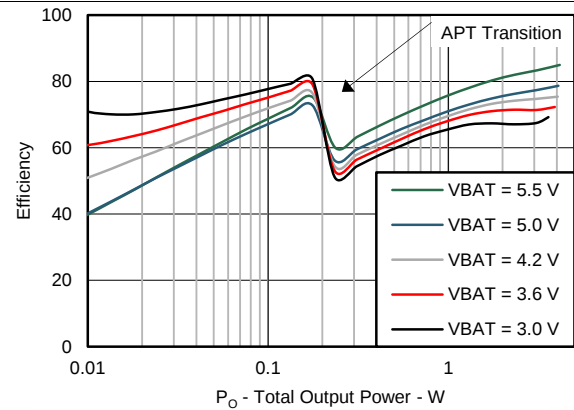
## Typical Characteristics (continued)

VBAT = 3.6 V, AVDD = IOVDD = 1.8 V, EN = IOVDD, SWS = 0,  $R_L = 8\ \Omega + 33\ \mu\text{H}$  (unless otherwise noted).



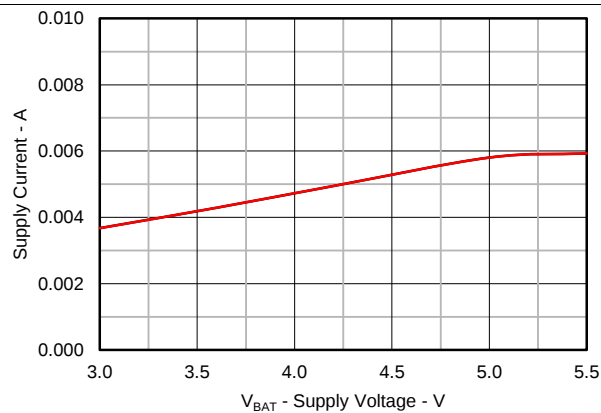
AGC = OFF, Gain = 15 dB,  $f = 1\ \text{kHz}$

**Figure 9. VBAT Average Supply Current vs Class-D Output Power (8Ω)**



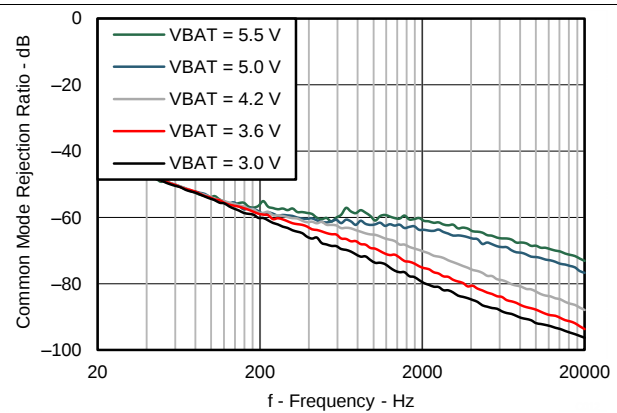
AGC = OFF, Gain = 15 dB,  $f = 1\ \text{kHz}$

**Figure 10. Total Efficiency vs Output Power (8Ω)**



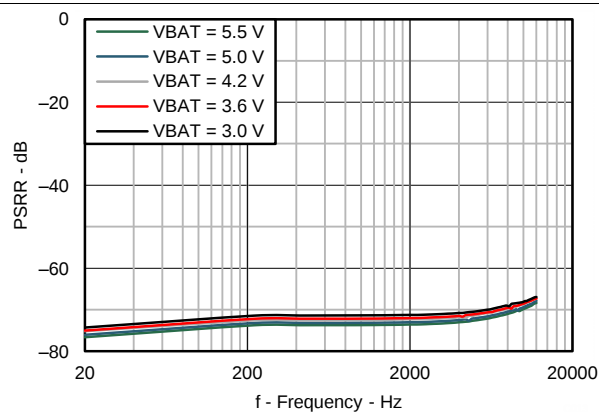
VBAT = 3.0, 3.6, 4.2, 5.0, 5.5 V

**Figure 11. VBAT Quiescent Supply Current vs Supply Voltage**



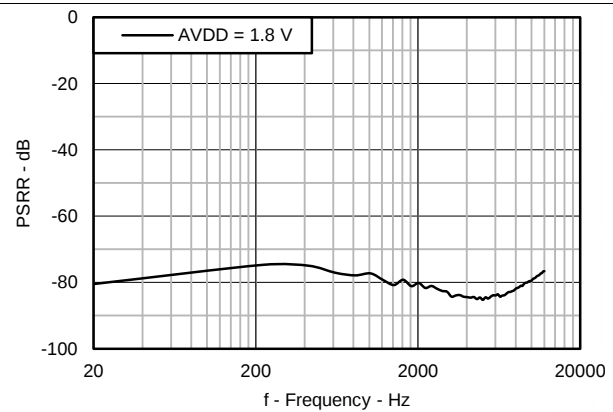
20 Hz to 20 kHz, Analog Input, Gain = 15 dB

**Figure 12. Common Mode Rejection vs Frequency**



20 Hz to 20 kHz, Digital Input, Gain = 15 dB

**Figure 13. VBAT Supply Ripple Rejection vs Frequency**

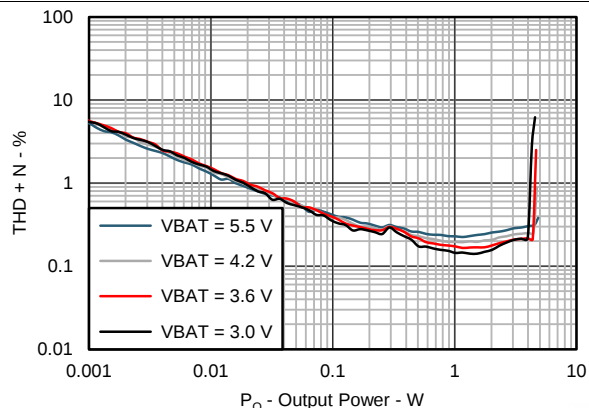


20 Hz to 20 kHz, Digital Input, Gain = 15 dB

**Figure 14. AVDD Supply Ripple Rejection vs Frequency**

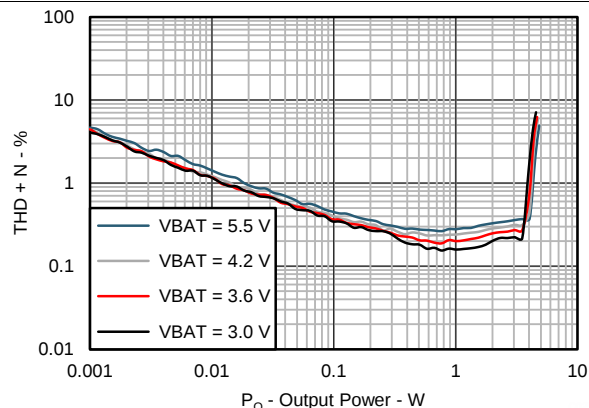
## Typical Characteristics (continued)

$V_{BAT} = 3.6\text{ V}$ ,  $AVDD = IOVDD = 1.8\text{ V}$ ,  $EN = IOVDD$ ,  $SWS = 0$ ,  $R_L = 8\ \Omega + 33\ \mu\text{H}$  (unless otherwise noted).



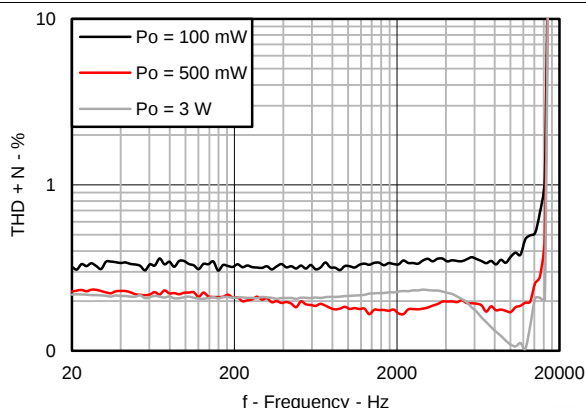
AGC = OFF, Gain = 15 dB

**Figure 15. I-Sense THD+N vs Output Power (8Ω)**



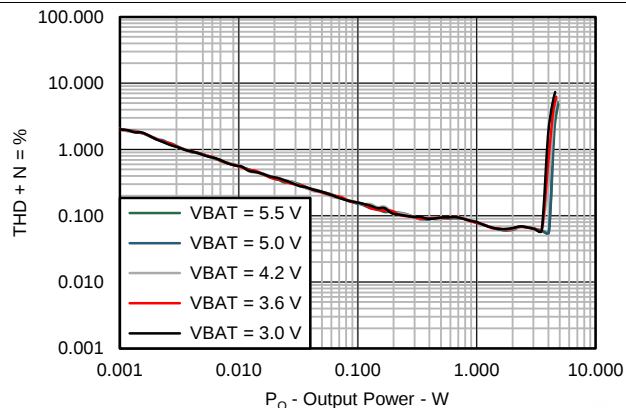
AGC = OFF, Gain = 15 dB

**Figure 16. I-Sense THD+N vs Output Power (6Ω)**



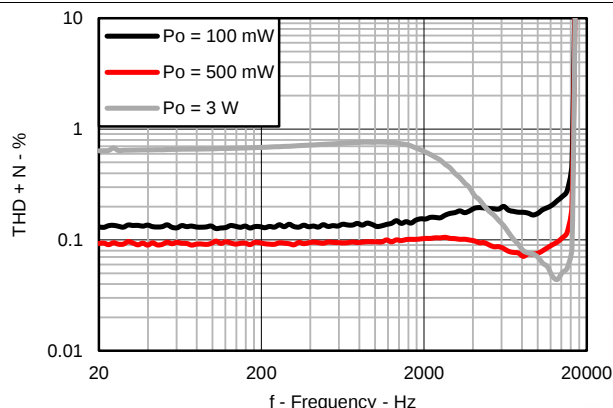
8 Ω Load, AGC = OFF, Gain = 15 dB

**Figure 17. I-Sense THD+N vs Frequency (8Ω)**



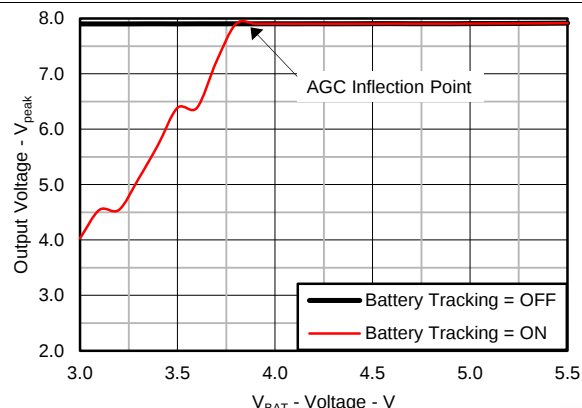
AGC = OFF, Input Level = -20 dBFS, Gain = 15 dB

**Figure 18. V-Sense THD+N vs. Output Power (8Ω)**



8 Ω Load, AGC = OFF, Input Level = -20 dBFS, Gain = 15 dB

**Figure 19. V-Sense THD+N vs Frequency (8Ω)**

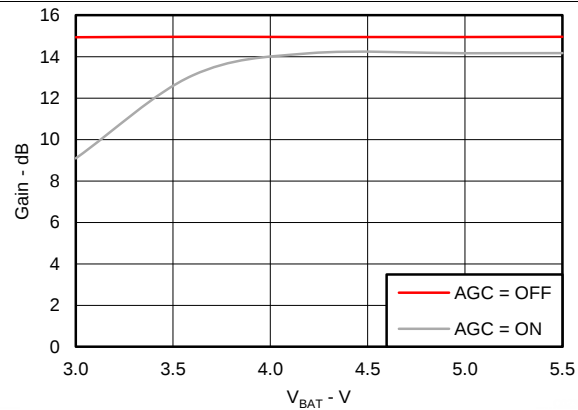


$f = 1\text{ kHz}$ ,  $0\text{ dBFS}$ , Gain = 15 dB,  
Inflection point = 3.6 V, Slope = 4.5 V/V, No Load

**Figure 20. Maximum Peak Output Voltage vs. Supply Voltage (8Ω)**

## Typical Characteristics (continued)

VBAT = 3.6 V, AVDD = IOVDD = 1.8 V, EN = IOVDD, SWS = 0,  $R_L = 8\ \Omega + 33\ \mu\text{H}$  (unless otherwise noted).



AGC = ON, Gain = 15 dB,  $f = 1\ \text{kHz}$ , Inflection point = 3.6 V, Limiter value = 7.87 V, Slope = 4.5 V

**Figure 21. Gain vs Supply Voltage**

## 7 Detailed Description

### 7.1 Overview

The TAS2552 is a high efficiency Class-D audio power amplifier with advanced battery current management and an integrated Class-G boost converter. The TAS2552 provides real-time output current and voltage information to the host processor via the I<sup>2</sup>S, L<sup>2</sup>JF, R<sup>2</sup>JF, TDM, DSP, or PDM interface. This output current and voltage information is useful for speaker protection and sound enhancement algorithms, allowing the host to track the speaker impedance and to enable usage of lower-cost, wider tolerance speakers reliably pushed to their rated output power and beyond.

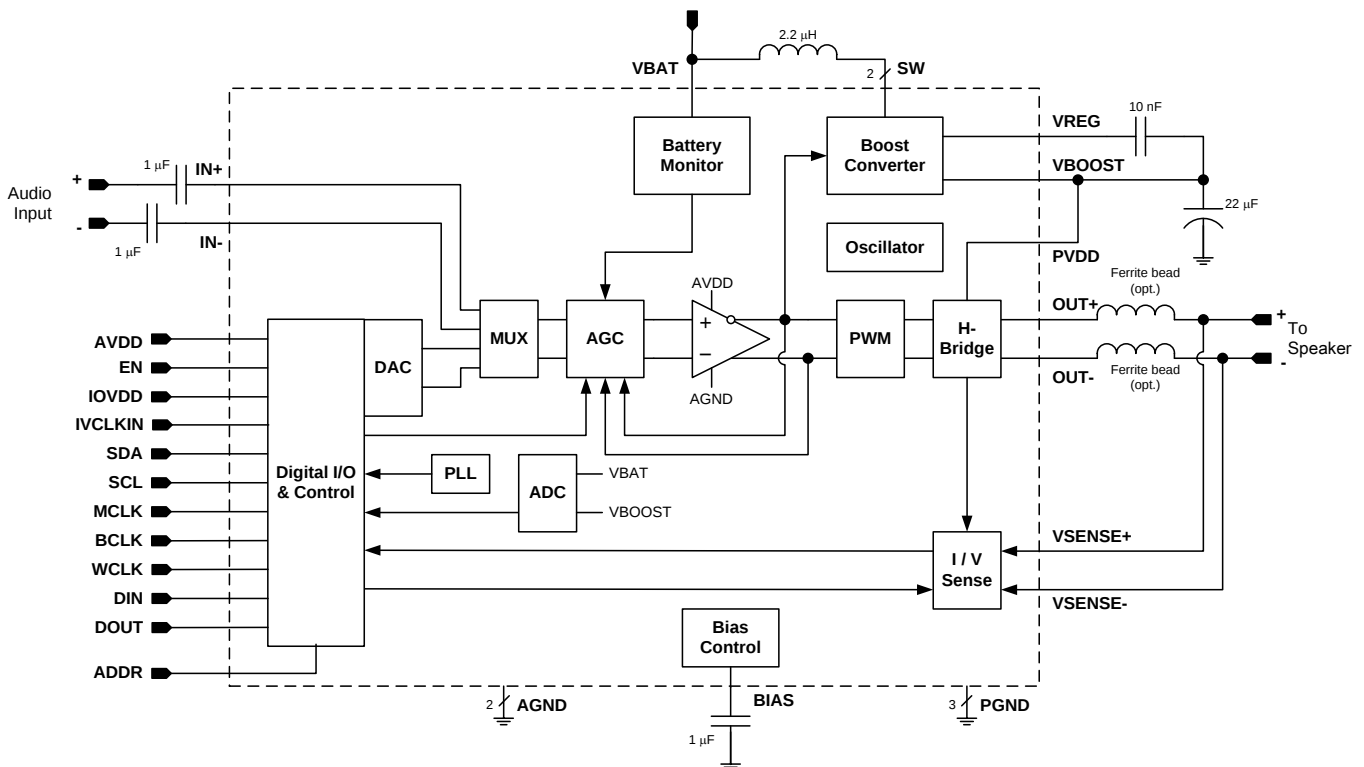
When auto-passthrough mode is enabled, the Class-G boost converter generates the Class-D amplifier supply rail. During low Class-D output power, the boost improves efficiency by deactivating and connecting VBAT directly to the Class-D amplifier supply. When high power audio is required, the boost quickly activates to provide significantly louder audio than a stand-alone amplifier connected directly to the battery.

The battery monitor and AGC work together in the Battery Tracking AGC to automatically adjust the Class-D gain to reduce battery current at end-of-charge voltage levels, preventing output clipping, distortion and early system shutdown. The fixed gain is adjustable via I<sup>2</sup>C. The gain range is -7 dB to +24 dB in 1 dB steps.

In addition to a differential mono analog input, the TAS2552 has built-in a 16-bit D/A converter used with a digital input. The digital audio interface supports I<sup>2</sup>S, Left-Justified, Right-Justified, DSP, PDM and TDM modes. Moving the D/A converter from the digital host processor into the integrated amplifier process provides better dynamic performance at lower system cost. Additionally, since the PCB routing is digital rather than analog, sensitivity to external perturbations such as GSM frame-rate noise is decreased at the system level.

Stereo configuration can be achieved with two TAS2552s by using the ADDR terminal to address each TAS2552 separately. Set ADDR to ground to configure the device for I<sup>2</sup>C address 0x40 (7-bit). Set ADDR to IOVDD for I<sup>2</sup>C address 0x41 (7-bit). Refer to the General I<sup>2</sup>C Operation section for more details.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 General I<sup>2</sup>C Operation

The TAS2552 operates as an I<sup>2</sup>C slave over the IOVDD voltage range. It is adjustable to one of two I<sup>2</sup>C addresses. This allows two TAS2552 devices in a system to connect to the same I<sup>2</sup>C bus.

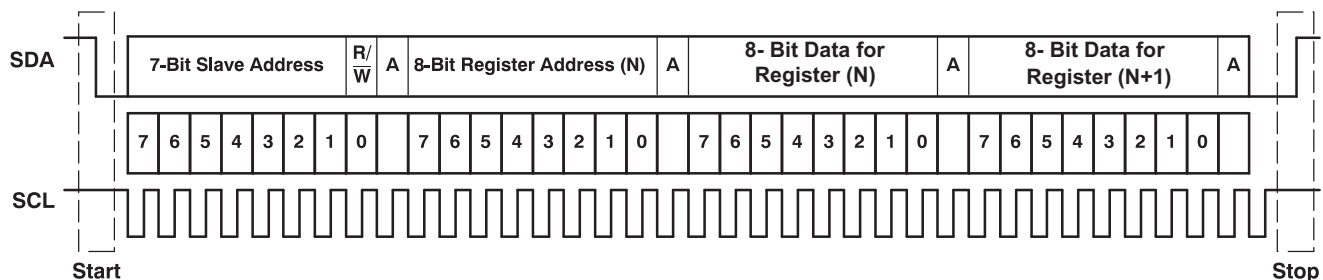
Set the ADDR terminal to ground to assign the device I<sup>2</sup>C address to 0x40 (7-bit). This is equivalent to 0x80 (8-bit) for writing and 0x81 (8-bit) for reading.

Set ADDR to IOVDD for I<sup>2</sup>C address 0x41 (7-bit). This is equivalent to 0x82 (8-bit) for writing and 0x83 (8-bit) for reading.

The I<sup>2</sup>C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The bus transfers data serially, one bit at a time. The address and data 8-bit bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. [Figure 22](#) shows a typical sequence.

The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The TAS2552 holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bi-directional bus using a wired-AND connection.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus. Use pull-up resistors between 660  $\Omega$  and 4.7 k $\Omega$ . Do not allow the SDA and SCL voltages to exceed the TAS2552 supply voltage, IOVDD.



**Figure 22. Typical I<sup>2</sup>C Sequence**

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. [Figure 22](#) shows a generic data transfer sequence.

### 7.3.2 Single-Byte and Multiple-Byte Transfers

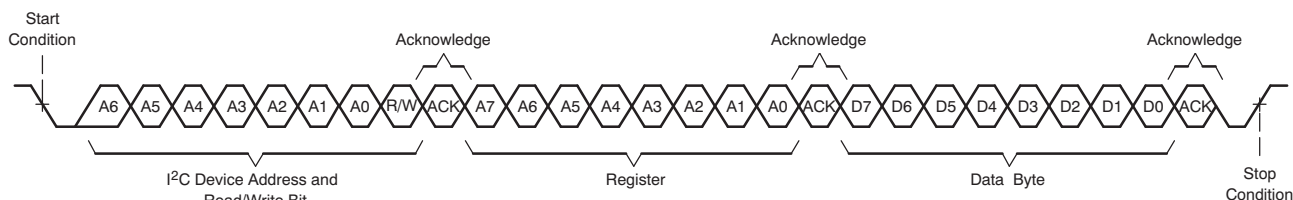
The serial control interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the TAS2552 responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges.

The TAS2552 supports sequential I<sup>2</sup>C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I<sup>2</sup>C write transaction has taken place. For I<sup>2</sup>C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines to how many registers are written.

## Feature Description (continued)

### 7.3.3 Single-Byte Write

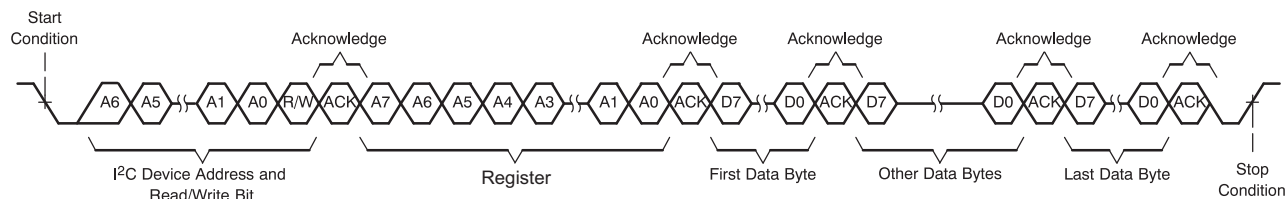
As shown in Figure 23, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I<sup>2</sup>C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I<sup>2</sup>C device address and the read/write bit, the TAS2552 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the TAS2552 internal memory address being accessed. After receiving the register byte, the TAS2552 again responds with an acknowledge bit. Finally, the master device transmits a data byte. After receiving the data byte, the TAS2552 responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.



**Figure 23. Single-Byte Write Transfer**

### 7.3.4 Multiple-Byte Write and Incremental Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the TAS2552 as shown in Figure 24. After receiving each data byte, the TAS2552 responds with an acknowledge bit.



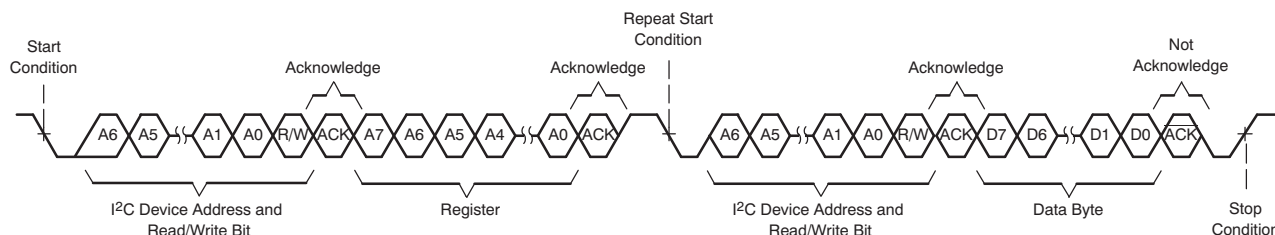
**Figure 24. Multiple-Byte Write Transfer**

### 7.3.5 Single-Byte Read

As shown in Figure 25, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I<sup>2</sup>C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0.

After receiving the TAS2552 address and the read/write bit, the TAS2552 responds with an acknowledge bit. The master then sends the internal memory address byte, after which the TAS2552 issues an acknowledge bit. The master device transmits another start condition followed by the TAS2552 address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the TAS2552 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer.

The device address is 0x40 (7-bit). This is equivalent to 0x81 (8-bit) for reading.

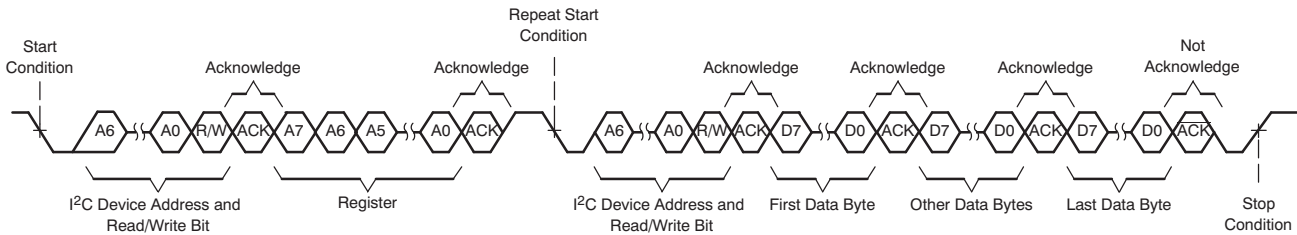


**Figure 25. Single-Byte Read Transfer**

## Feature Description (continued)

### 7.3.6 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the TAS2552 to the master device as shown in Figure 26. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.



**Figure 26. Multiple-Byte Read Transfer**

### 7.3.7 PLL

The TAS2552 has an on-chip PLL to generate the clock frequency for the audio DAC and I-V sensing ADCs. The programmability of the PLL allows operation from a wide variety of clocks that may be available in the system.

The PLL input supports clocks varying from 512 kHz to 24.576 MHz and is register programmable to enable generation of required sampling rates with fine resolution. Set Register 0x02, D(3) = 1 to activate the PLL. When the PLL is enabled, the PLL output clock PLL\_CLK is:

$$\text{PLL\_CLK} = \frac{0.5 \times \text{PLL\_CLKIN} \times \text{JD}}{2^P} \quad (1)$$

J = 4, 5, 6, ... 96

D = 0, 1, 2, ... 9999

P = 0, 1

Choose J, D, P such that PLL\_CLK = 22.5792 MHz (44.1ksps sampling rate) or 24.5760 MHz (48ksps sampling rate). Program variable J in Register 0x08, D(6:0). Program variable D in Register 0x09, D(5:0) and Register 0x0A, D(7:0). The default value for D is 0. Program variable P in Register 0x08, D(7). The default value for P is 0.

Register 0x01, D(5:4) sets the PLL\_CLKIN input to MCLK, BCLK, or IVCLKIN. Set Register 0x01, D(5:4) = 00 to use MCLK, 01 to use BCLK, and 10 to use IVCLKIN.

There is also an option to use a 1.8 MHz internal oscillator for PLL\_CLKIN. This is useful for systems using the analog inputs and the I-V sense data returning to a host processor via PDM mode interface. Set Register 0x01, D(5:4) = 11 to use the 1.8 MHz internal oscillator.

To bypass the PLL, set Register 0x09, D(7) = 1. Deactivate the PLL by setting Register 0x02, D(3) = 0.

When the PLL is enabled, the following conditions must be satisfied:

- If D = 0, the PLL clock input (PLL\_CLKIN) must satisfy:

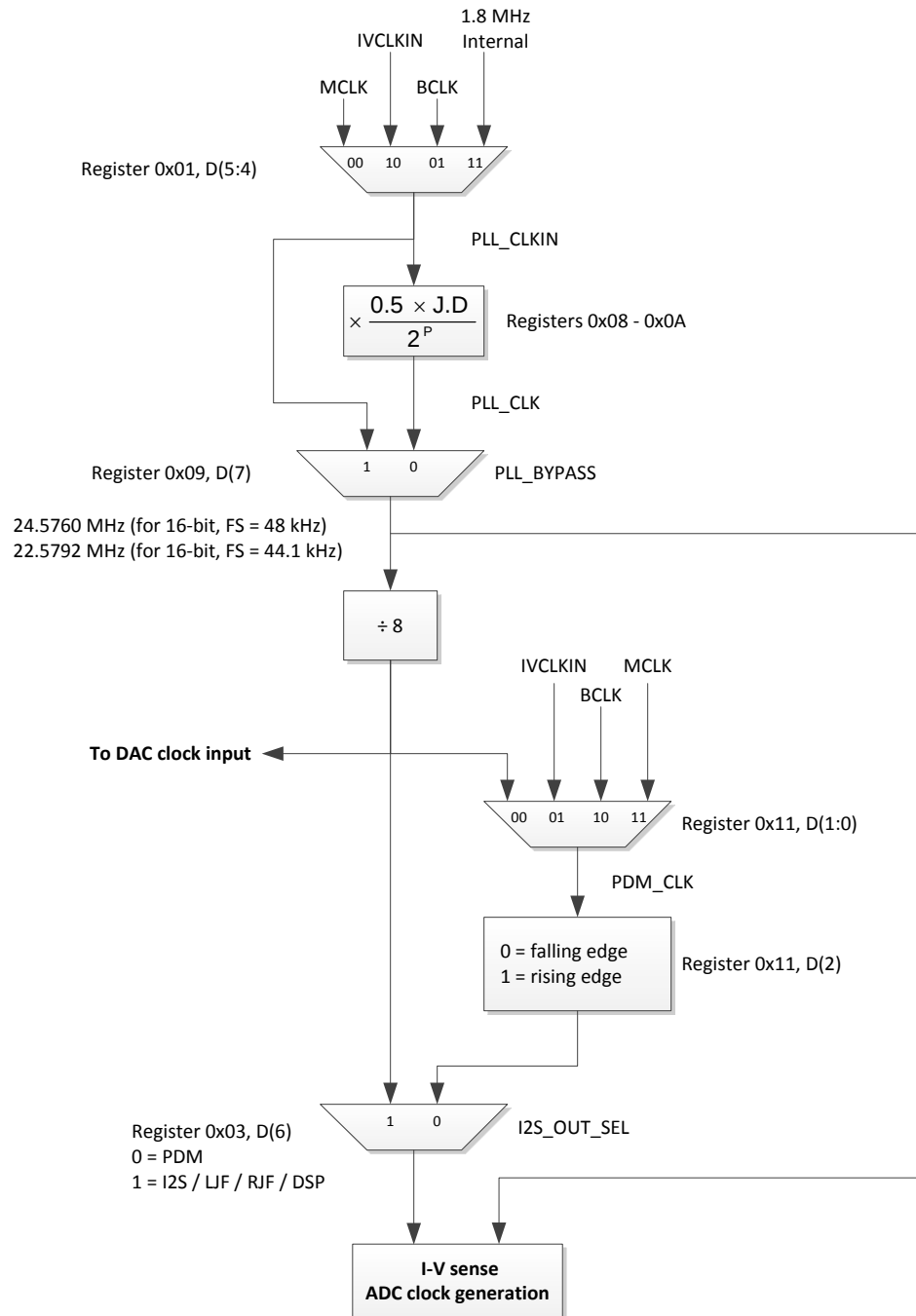
$$512 \text{ kHz} \leq \frac{\text{PLL\_CLKIN}}{2^P} \leq 12.288 \text{ MHz}$$

- If D ≠ 0, the PLL clock input (PLL\_CLKIN) must satisfy:

$$1.1 \text{ MHz} \leq \frac{\text{PLL\_CLKIN}}{2^P} \leq 9.2 \text{ MHz}$$

Figure 27 shows the clock distribution tree and the registers required to set the audio input DAC and the I-V sense ADC.

### Feature Description (continued)



### Figure 27. Clock Distribution Tree

### 7.3.8 Gain Settings

The TAS2552 has one gain register for both analog input and digital input (DAC output) gain. A mux selects only one of these inputs for the Class-D speaker amplifier. The analog and digital inputs cannot be mixed together.

The full-scale DAC output voltage is the same as the maximum analog input voltage (for less than 1% THD): 1  $V_{RMS}$ , or 1.4  $V_{PEAK}$ .

**Table 1. TAS2552 Gain Table**

| GAIN BYTE:<br>GAIN[4:0] | NOMINAL GAIN | GAIN BYTE:<br>GAIN[4:0] | NOMINAL GAIN |
|-------------------------|--------------|-------------------------|--------------|
| 00000                   | –7 dB        | 10000                   | 9 dB         |
| 00001                   | –6 dB        | 10001                   | 10 dB        |
| 00010                   | –5 dB        | 10010                   | 11 dB        |
| 00011                   | –4 dB        | 10011                   | 12 dB        |
| 00100                   | –3 dB        | 10100                   | 13 dB        |
| 00101                   | –2 dB        | 10101                   | 14 dB        |
| 00110                   | –1 dB        | 10110                   | 15 dB        |
| 00111                   | 0 dB         | 10111                   | 16 dB        |
| 01000                   | 1 dB         | 11000                   | 17 dB        |
| 01001                   | 2 dB         | 11001                   | 18 dB        |
| 01010                   | 3 dB         | 11010                   | 19 dB        |
| 01011                   | 4 dB         | 11011                   | 20 dB        |
| 01100                   | 5 dB         | 11100                   | 21 dB        |
| 01101                   | 6 dB         | 11101                   | 22 dB        |
| 01110                   | 7 dB         | 11110                   | 23 dB        |
| 01111                   | 8 dB         | 11111                   | 24 dB        |

### 7.3.9 Class-D Edge Rate Control

The edge rate of the Class-D output is controllable via an I<sup>2</sup>C register. This allows users the ability to adjust the switching edge rate of the Class-D amplifier, trading off some efficiency for lower EMI. [Table 2](#) lists the typical edge rates.

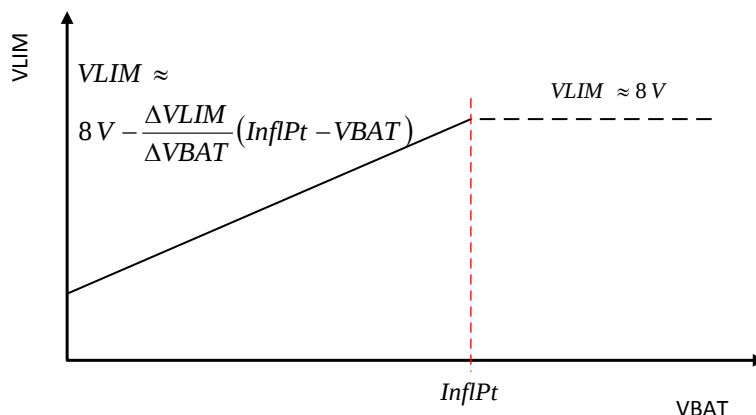
**Table 2. Class-D Edge Rate Control**

| ERC BYTE:<br>EDGE[2:0] | T <sub>R</sub> AND T <sub>F</sub><br>(TYPICAL) |
|------------------------|------------------------------------------------|
| 000                    | 50 ns                                          |
| 001                    | 40 ns                                          |
| 010                    | 30 ns                                          |
| 011                    | 25 ns                                          |
| 100                    | 14 ns                                          |
| 101                    | 13 ns                                          |
| 110                    | 12 ns                                          |
| 111                    | 11 ns                                          |

### 7.3.10 Battery Tracking AGC

The TAS2552 monitors battery voltage and the audio signal to automatically decrease gain when the battery voltage is low and audio output power is high. This finds the optimal gain to maximize loudness and minimize battery current, providing louder audio and preventing early shutdown at end-of-charge battery voltage levels.

This does not mean the battery tracking AGC automatically decreases amplifier gain when VBAT is below the inflection point. Rather, gain is decreased only when the Class-D output voltage exceeds the limiter level.



**Figure 28. VLIM versus Supply Voltage (VBAT)**

When VBAT is greater than the inflection point, VLIM - the peak allowed output voltage - is set by the boost voltage. The inflection point is set in Register 0x0B, Bits 7-0. The inflection point range is 3.0 V to 5.5 V, adjustable in 17.33 mV steps.

When VBAT is less than the inflection point, the peak output voltage is controlled by the slope. Set the VLIM vs. VBAT slope in Register 0x0C, Bits 7-0. This  $\Delta VLIM / \Delta VBAT$  range is 1.2 V/V to 10.75 V/V and is adjustable in 37.3 mV/V steps.

If the audio signal is higher than VLIM, then the gain decreases until the audio signal is just below VLIM. The gain decrease rate (attack time) is set via the I<sup>2</sup>C interface. If the audio signal is below VLIM and the gain is below the fixed gain, the gain will increase. The gain increase rate (release time) is set via the I<sup>2</sup>C interface. The attack and release times are selected via I<sup>2</sup>C interface. Eight attack times are available in 350  $\mu$ s / dB steps. Sixteen release times are in 105 ms / dB steps. ATK\_TIME[2:0] is Register 0x0E, Bits 0-2. REL\_TIM[3:0] is Register 0x0F, Bits 3-0.

**Table 3. Attack Time Selection**

| ATTACK TIME REGISTER<br>BYTE: ATK_TIME[2:0] | ATTACK TIME<br>( $\mu$ S / STEP) |
|---------------------------------------------|----------------------------------|
| 000                                         | 20                               |
| 001                                         | 370                              |
| 010                                         | 720                              |
| 011                                         | 1070                             |
| 100                                         | 1420                             |
| 101                                         | 1770                             |
| 110                                         | 2120                             |
| 111                                         | 2470                             |

**Table 4. Release Time Selection**

| RELEASE TIME REGISTER<br>BYTE: REL_TIME[3:0] | RELEASE TIME<br>(MS / STEP) | RELEASE TIME REGISTER<br>BYTE: REL_TIME[4:0] | RELEASE TIME<br>(MS / STEP) |
|----------------------------------------------|-----------------------------|----------------------------------------------|-----------------------------|
| 0000                                         | 50                          | 1000                                         | 890                         |
| 0001                                         | 155                         | 1001                                         | 995                         |

**Table 4. Release Time Selection (continued)**

| RELEASE TIME REGISTER<br>BYTE: REL_TIME[3:0] | RELEASE TIME<br>( MS / STEP) | RELEASE TIME REGISTER<br>BYTE: REL_TIME[4:0] | RELEASE TIME<br>(MS / STEP) |
|----------------------------------------------|------------------------------|----------------------------------------------|-----------------------------|
| 0010                                         | 260                          | 1010                                         | 1100                        |
| 0011                                         | 365                          | 1011                                         | 1205                        |
| 0100                                         | 470                          | 1100                                         | 1310                        |
| 0101                                         | 575                          | 1101                                         | 1415                        |
| 0110                                         | 680                          | 1110                                         | 1520                        |
| 0111                                         | 785                          | 1111                                         | 1625                        |

### 7.3.11 Configurable Boost Current Limit (ILIM)

The TAS2552 has a configurable boost current limit (ILIM).

**Table 5. Current Limit Settings**

| CURRENT LIMIT REGISTER<br>Bit [7:6] | BOOST CURRENT LIMIT (ILIM)<br>(A) |
|-------------------------------------|-----------------------------------|
| 00                                  | 1.5                               |
| 01                                  | 2.0                               |
| 10                                  | 2.5 (default)                     |
| 11                                  | 3.0                               |

Because changes to the current limit may require changes to the passive components connected to the boost, a special I<sup>2</sup>C sequence is required to change the current limit values. To program the current limit of the TAS2552, follow this I<sup>2</sup>C write sequence.

1. w 80 21 02
2. w 80 21 01
3. w 80 21 04
4. w 80 21 07
5. r 80 32 01 and save the value of register 0x32
6. w 80 32 0bYYXXXXXX where YY are the two bits from [Table 5](#). RETAIN the values in the other bits read in the step above.
7. w 80 21 07

## 7.4 Device Functional Modes

### 7.4.1 Audio Digital I/O Interface

Audio data is transferred between the host processor and the TAS2552 via the digital audio data serial interface, or audio bus. The audio bus on this device is very flexible, including left or right-justified data options, support for I<sup>2</sup>S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master/slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The audio bus of the TAS2552 can be configured for left or right-justified, I<sup>2</sup>S, DSP, or TDM modes of operation, where communication with standard telephony PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits by configuring Register 0x05, D(1:0). In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies.

The bit clock is used to clock in and clock out the digital audio data across the serial bus. This signal can be programmed to generate variable clock pulses by controlling the bit-clock multiply-divide factor in Registers 0x08 through 0x10. The number of bit-clock pulses in a frame may need adjustment to accommodate various word-lengths as well as to support the case when multiple TAS2552 devices may share the same audio bus.

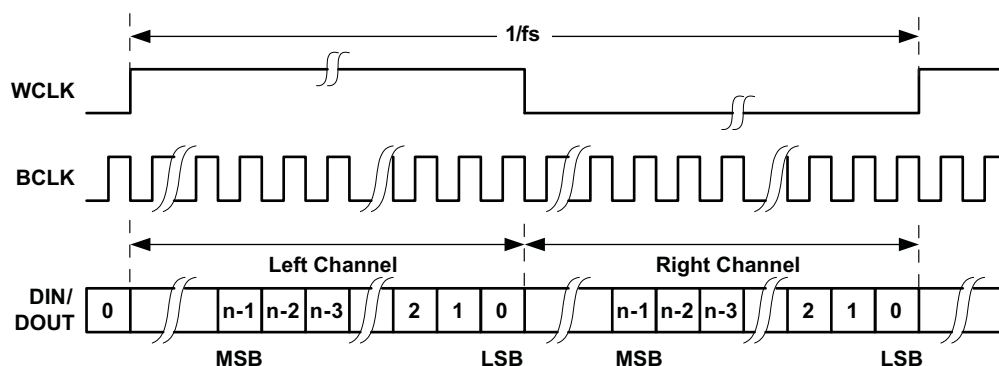
## Device Functional Modes (continued)

The TAS2552 also includes a feature to offset the position of start of data transfer with respect to the word-clock. This offset is in number of bit-clocks and is programmed in Register 0x06.

To place the DOUT line into a Hi-Z (3-state) condition during all bit clocks when valid data is not being sent, set Register 0x04, D(2) = 1. By combining this capability with the ability to program what bit clock in a frame the audio data begins, time-division multiplexing (TDM) can be accomplished. This enables the use of multiple devices on a single audio serial data bus. When the audio serial data bus is powered down while configured in master mode, the terminals associated with the interface are put into a Hi-Z output state.

### 7.4.1.1 Right-Justified Mode

Set Register 0x03, D(6) = 0 and Register 0x05, D(3:2) = 10 to place the TAS2552 audio interface into right-justified mode. In right-justified mode, the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

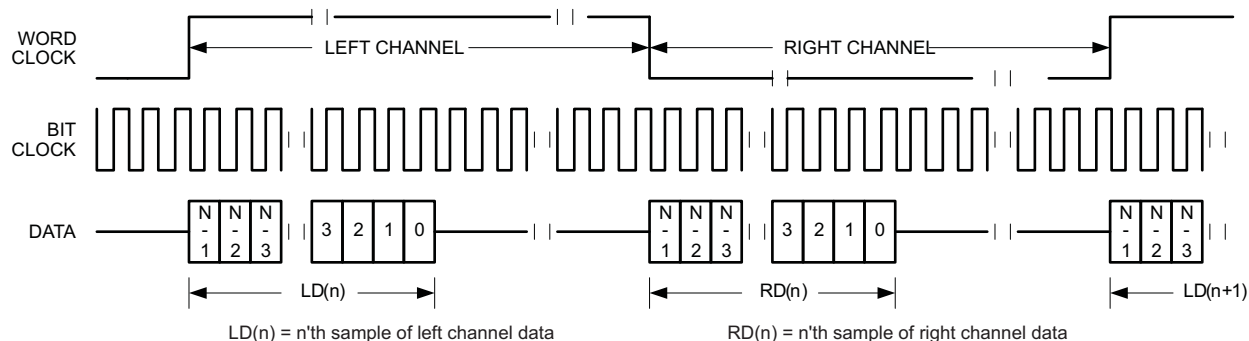


**Figure 29. Timing Diagram for Right-Justified Mode**

For right-justified mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data.

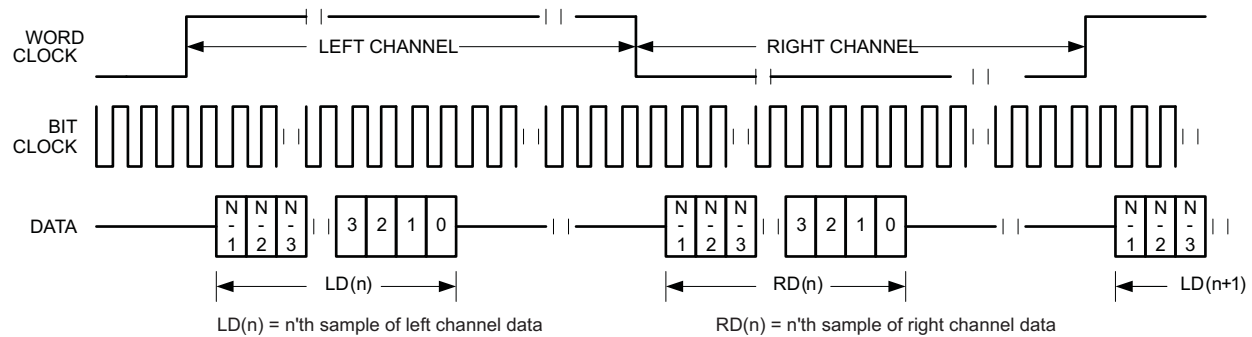
### 7.4.1.2 Left-Justified Mode

Set Register 0x03, D(7:6) = 01 and Register 0x05, D(3:2) = 11 to place the TAS2552 audio interface into left-justified mode. In left-justified mode, the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. Similarly the MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

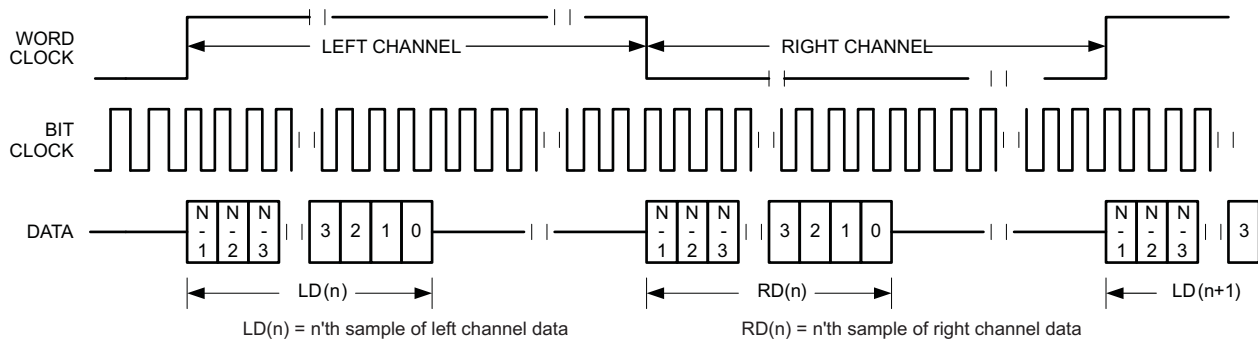


**Figure 30. Timing Diagram for Left-Justified Mode**

## Device Functional Modes (continued)



**Figure 31. Timing Diagram for Light-Left Mode with Offset=1**

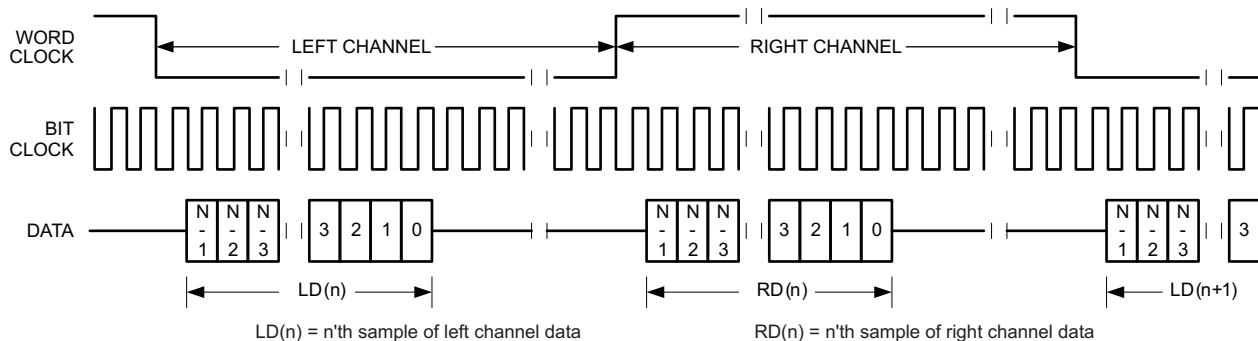


**Figure 32. Timing Diagram for Left-Justified Mode with Offset=0 and Inverted Bit Clock**

For left-justified mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data. Also, the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

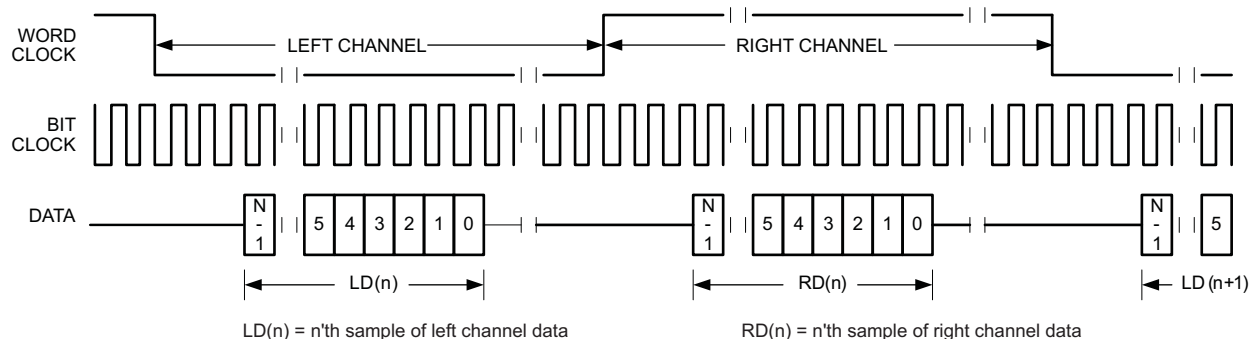
### 7.4.1.3 I<sup>2</sup>S Mode

Set Register 0x03, D(7:6) = 01 and Register 0x05, D(3:2) = 00 to place the TAS2552 audio interface into I<sup>2</sup>S mode. In I<sup>2</sup>S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

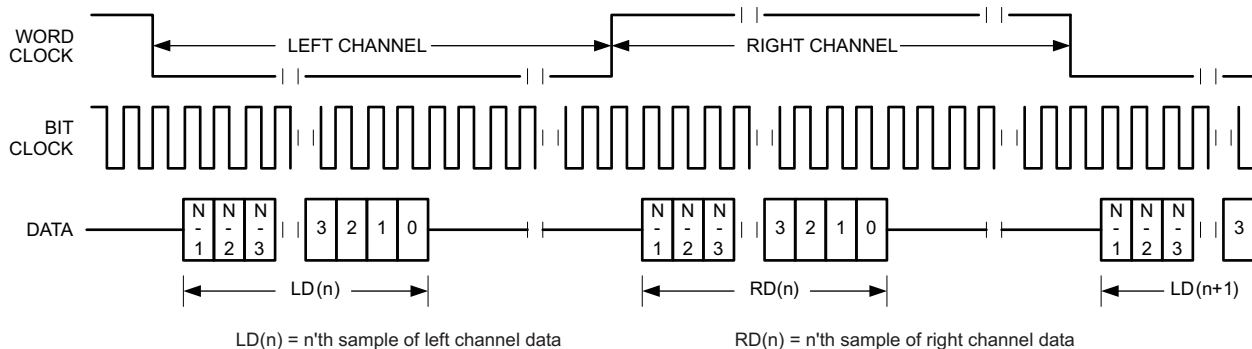


**Figure 33. Timing Diagram for I<sup>2</sup>S Mode**

## Device Functional Modes (continued)



**Figure 34. Timing Diagram for I²S Mode with Offset=2**



**Figure 35. Timing Diagram for I²S Mode with Offset=0 and Inverted Bit Clock**

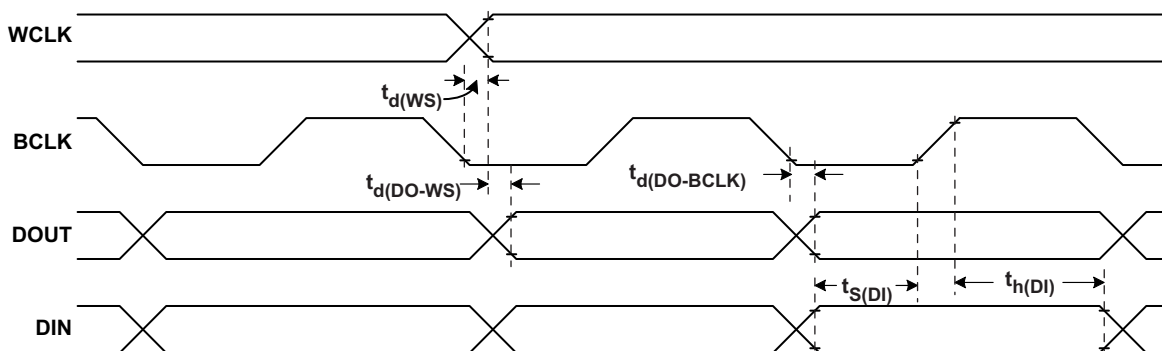
For I²S mode, the number of bit-clcks per channel should be greater than or equal to the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clcks per frame by at least the programmed word-length of the data.

### 7.4.1.4 Audio Data Serial Interface Timing (I²S, Left-Justified, Right-Justified Modes)

All specifications at 25°C, IOVDD = 1.8 V

#### NOTE

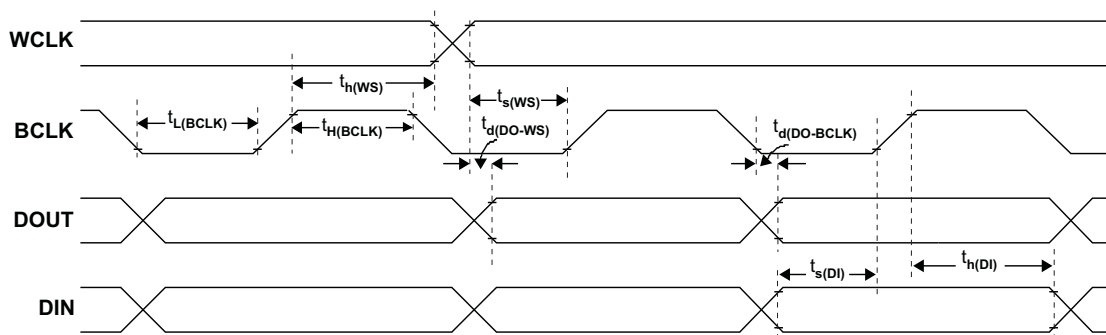
All timing specifications are measured at characterization but not tested at final test.



**Figure 36. I²S/LJF/RJF Timing in Master Mode**

**Device Functional Modes (continued)**
**Table 6. I<sup>2</sup>S/LJF/RJF Timing in Master Mode (see Figure 36)**

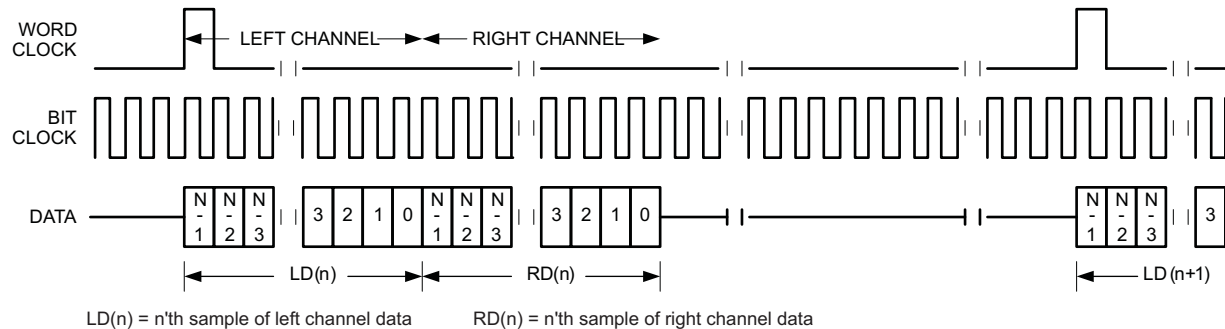
| PARAMETER             |                                        | IOVDD=1.8V |     | IOVDD=3.3V |     | UNIT |
|-----------------------|----------------------------------------|------------|-----|------------|-----|------|
|                       |                                        | MIN        | MAX | MIN        | MAX |      |
| $t_d(\text{WS})$      | WCLK delay                             |            | 30  | 20         |     | ns   |
| $t_d(\text{DO-WS})$   | WCLK to DOUT delay (For LJF Mode only) |            | 50  | 25         |     | ns   |
| $t_d(\text{DO-BCLK})$ | BCLK to DOUT delay                     |            | 50  | 25         |     | ns   |
| $t_s(\text{DI})$      | DIN setup                              | 8          |     | 8          |     | ns   |
| $t_h(\text{DI})$      | DIN hold                               | 8          |     | 8          |     | ns   |
| $t_r$                 | Rise time                              |            | 24  | 12         |     | ns   |
| $t_f$                 | Fall time                              |            | 24  | 15         |     | ns   |


**Figure 37. I<sup>2</sup>S/LJF/RJF Timing in Slave Mode**
**Table 7. I<sup>2</sup>S/LJF/RJF Timing in Slave Mode (see Figure 37)**

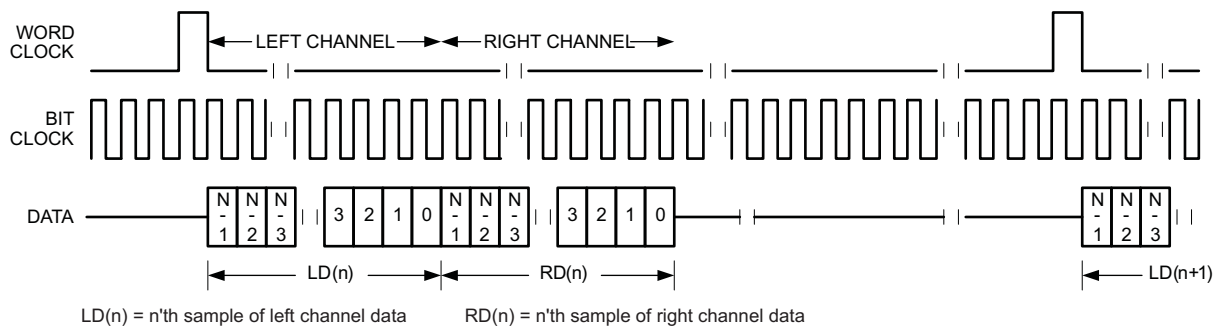
| PARAMETER             |                                        | IOVDD=1.8V |     | IOVDD=3.3V |     | UNIT |
|-----------------------|----------------------------------------|------------|-----|------------|-----|------|
|                       |                                        | MIN        | MAX | MIN        | MAX |      |
| $t_H(\text{BCLK})$    | BCLK high period                       | 35         |     | 35         |     | ns   |
| $t_L(\text{BCLK})$    | BCLK low period                        | 35         |     | 35         |     | ns   |
| $t_s(\text{WS})$      | (WS)                                   | 8          |     | 8          |     | ns   |
| $t_h(\text{WS})$      | WCLK hold                              | 8          |     | 8          |     | ns   |
| $t_d(\text{DO-WS})$   | WCLK to DOUT delay (For LJF Mode only) |            | 50  |            | 25  | ns   |
| $t_d(\text{DO-BCLK})$ | BCLK to DOUT delay                     |            | 50  |            | 25  | ns   |
| $t_s(\text{DI})$      | DIN setup                              | 8          |     | 8          |     | ns   |
| $t_h(\text{DI})$      | DIN hold                               | 8          |     | 8          |     | ns   |
| $t_r$                 | Rise time                              |            | 4   |            | 4   | ns   |
| $t_f$                 | Fall time                              |            | 4   |            | 4   | ns   |

### 7.4.1.5 DSP Mode

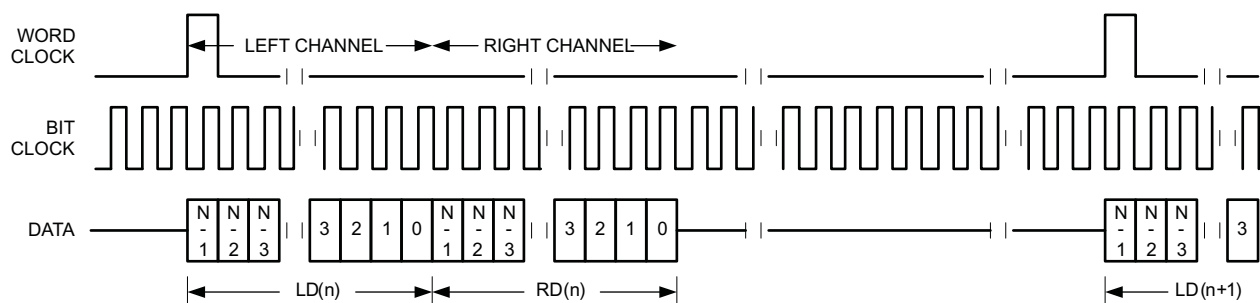
Set Register 0x03, D(7:6) = 01 and Register 0x05, D(3:2) = 01 to place the TAS2552 audio interface into DSP mode. In DSP mode, the rising edge of the word clock starts the data transfer with the left channel data first and immediately followed by the right channel data. Each data bit is valid on the falling edge of the bit clock.



**Figure 38. Timing Diagram for DSP Mode**



**Figure 39. Timing Diagram for DSP Mode with Offset=1**



**Figure 40. Timing Diagram for DSP Mode with Offset=0 and Inverted Bit Clock**

For DSP mode, the number of bit-clcks per frame should be greater than twice the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clcks per frame by at least the programmed word-length of the data.

### 7.4.1.6 DSP Timing

All specifications at 25°C, IOVDD = 1.8 V

#### NOTE

All timing specifications are measured at characterization but not tested at final test.

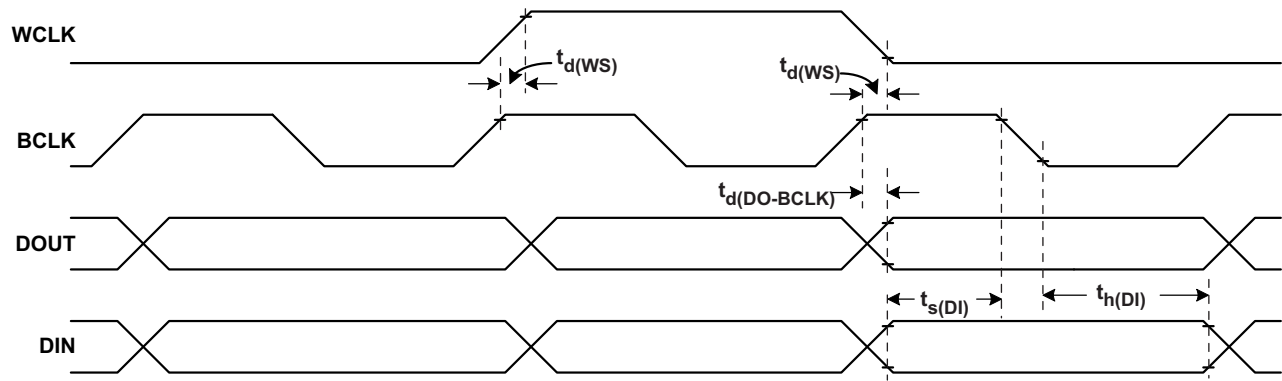


Figure 41. DSP Timing in Master Mode

Table 8. DSP Timing in Master Mode (see Figure 41)

| PARAMETER             |                    | IOVDD=1.8V |     | IOVDD=3.3V |     | UNIT |
|-----------------------|--------------------|------------|-----|------------|-----|------|
|                       |                    | MIN        | MAX | MIN        | MAX |      |
| $t_d(\text{WS})$      | WCLK delay         |            | 30  |            | 20  | ns   |
| $t_d(\text{DO-BCLK})$ | BCLK to DOUT delay |            | 40  |            | 20  | ns   |
| $t_s(\text{DI})$      | DIN setup          | 8          |     | 8          |     | ns   |
| $t_h(\text{DI})$      | DIN hold           | 8          |     | 8          |     | ns   |
| $t_r$                 | Rise time          |            | 4   |            | 4   | ns   |
| $t_f$                 | Fall time          |            | 4   |            | 4   | ns   |

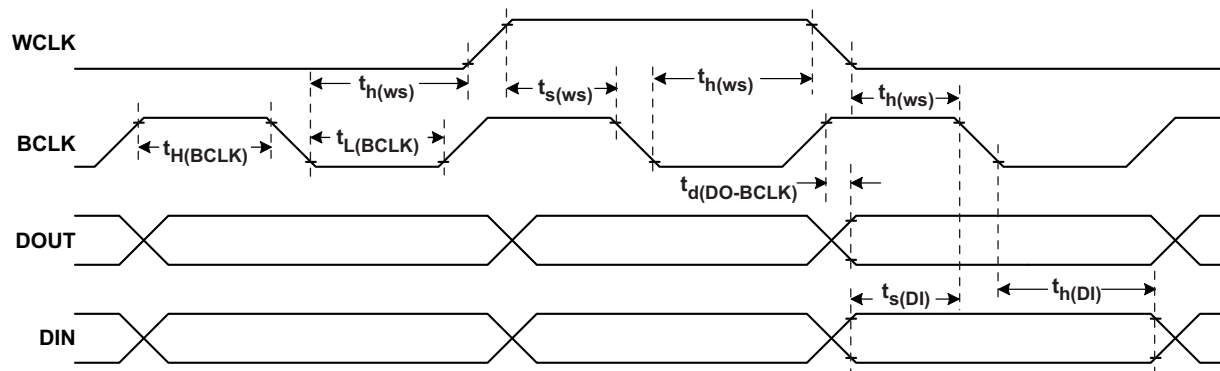


Figure 42. DSP Timing in Slave Mode

**Table 9. DSP Timing in Slave Mode (see Figure 42)**

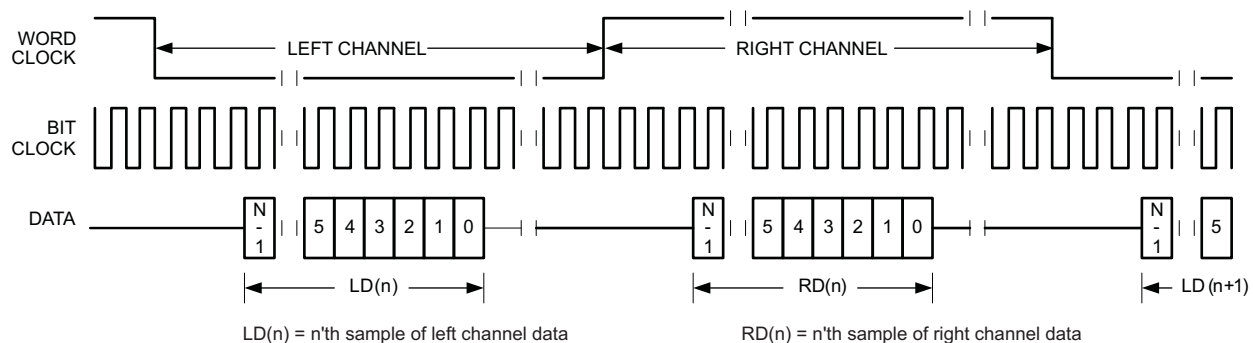
| PARAMETER     |                                        | IOVDD=1.8V |     | IOVDD=3.3V |     | UNIT |
|---------------|----------------------------------------|------------|-----|------------|-----|------|
|               |                                        | MIN        | MAX | MIN        | MAX |      |
| $t_{H(BCLK)}$ | BCLK high period                       | 35         |     | 35         |     | ns   |
| $t_{L(BCLK)}$ | BCLK low period                        | 35         |     | 35         |     | ns   |
| $t_s(WS)$     | (WS)                                   | 8          |     | 8          |     | ns   |
| $t_h(WS)$     | WCLK hold                              | 8          |     | 8          |     | ns   |
| $t_d(DO-WS)$  | WCLK to DOUT delay (For LJF Mode only) |            | 40  |            | 22  | ns   |
| $t_s(DI)$     | DIN setup                              | 8          |     | 8          |     | ns   |
| $t_h(DI)$     | DIN hold                               | 8          |     | 8          |     | ns   |
| $t_r$         | Rise time                              |            | 4   |            | 4   | ns   |
| $t_f$         | Fall time                              |            | 4   |            | 4   | ns   |

### 7.4.2 TDM Mode

Time-division multiplexing (TDM) allows two or more devices to share a common DIN connection and a common DOUT connection. Using TDM mode, all devices transmit their DOUT data in user-specified sub-frames within one WCLK period. When one device transmits its DOUT information, the other devices place their DOUT terminals in a high impedance tri-state mode.

TDM mode is useable with I<sup>2</sup>S, LJF, RJF, and DSP interface modes. Refer to the respective sections for a description of how to set the TAS2552 into those modes. TDM cannot be used with PDM mode. This is because the PDM requires a continuous stream of samples from one data source.

Use Register 0x06 to set the clock cycle offset from WCLK to the MSB. Each data bit is valid on the falling edge of the bit clock. Set Register 0x04, D(2) = 1 to force DOUT into tri-state when it is not transmitting data. This allows DOUT terminals from multiple TAS2552 devices to share a common wire to the host.



**Figure 43. Timing Diagram for I<sup>2</sup>S in TDM Mode with Offset=2**

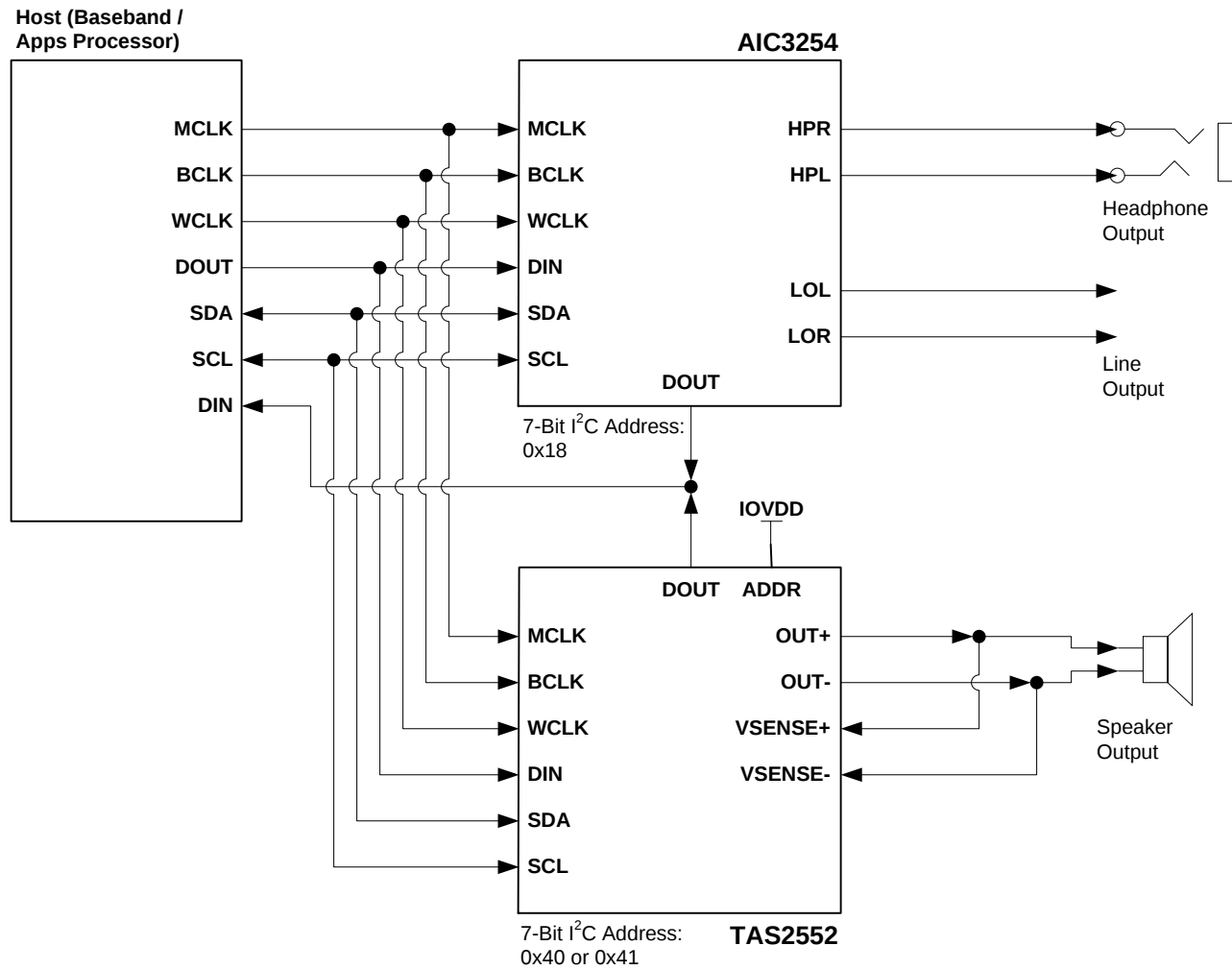
For TDM mode, the number of bit-clocks per frame should be less than the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

Figure 44 shows how to configure the TAS2552 with the TI codec, AIC3254, with both devices sharing DIN and DOUT

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**Figure 44. Configuration with TAS2552 and AIC3254 Muxed in TDM Mode**

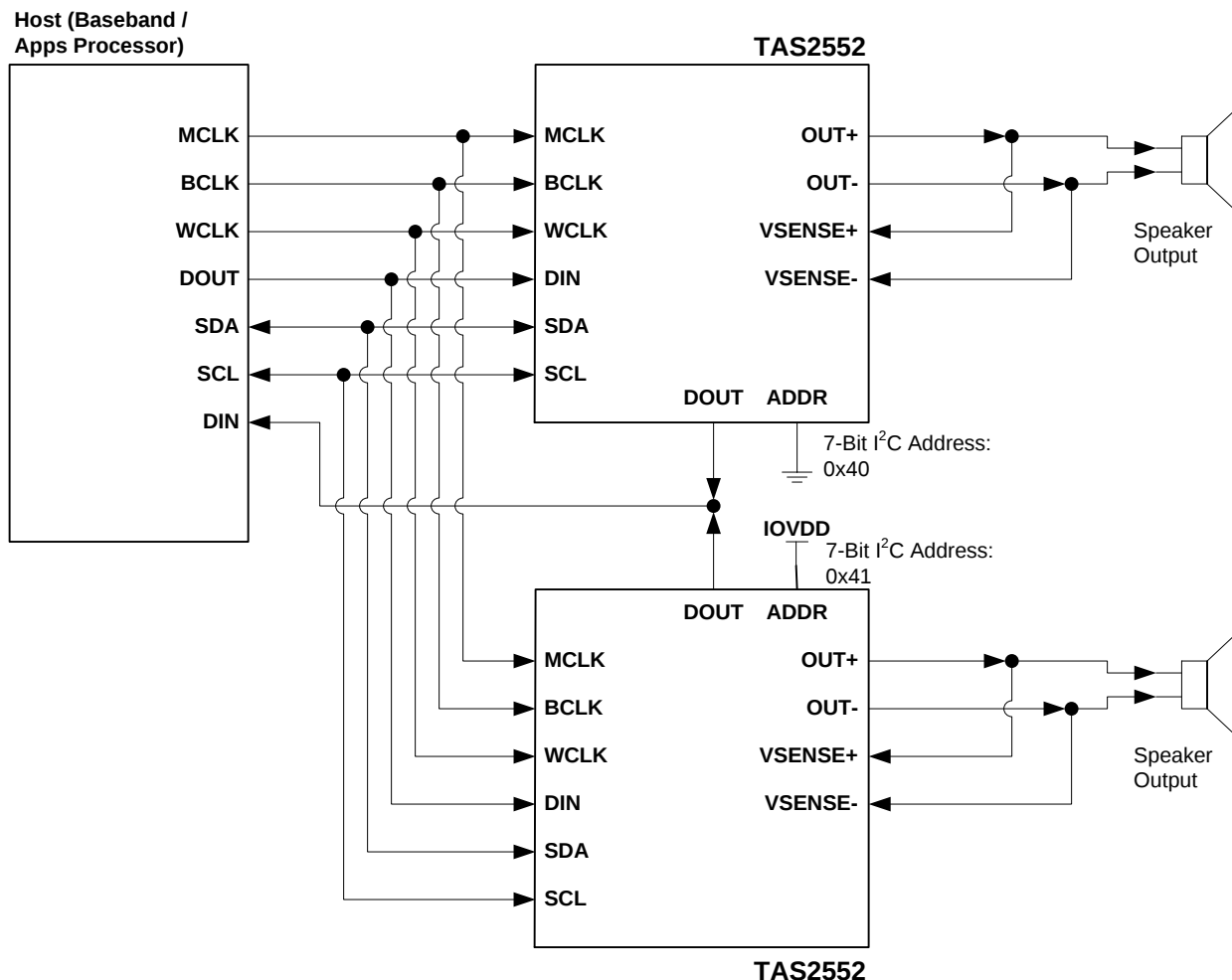


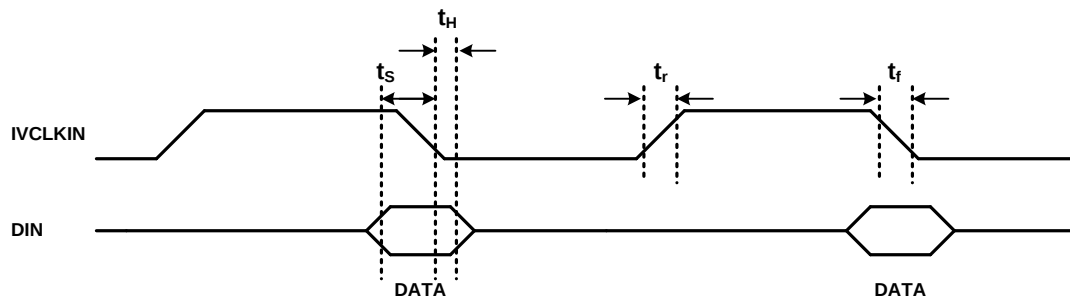
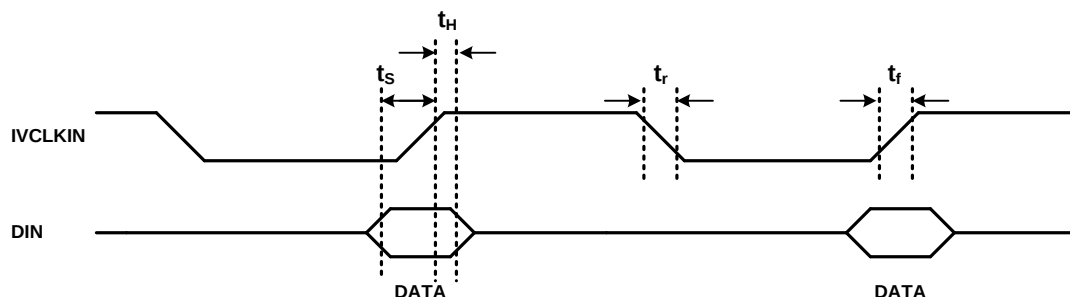
Figure 45. Stereo Configuration with Two TAS2552 DOUT Muxed in TDM Mode

### 7.4.3 PDM Mode

Set Register 0x03, D(7:6) = 00 to place the TAS2552 audio interface into PDM mode. In PDM mode, the data stream is a continuous stream of undecimated pulse-modulated data that is 64x the sample rate. Because it is a continuous stream, frame synchronization is not required and WCLK is not used. Specifying clocks-per-frame is not required for PDM mode. The PDM input bit clock is IVCLKIN as set in Register 0x11, D(1:0).

The TAS2552 can be configured for I²S input mode and PDM output mode. Figure 46 shows the timing diagram for PDM input mode. Timing specifications are listed in Table 10 and Table 11.

The TAS2552 clocks PDM input data on either the rising edge or falling edge of IVCLKIN as set in Register 0x11, D(2). The device does not read concurrent data on both edges. Set the I²C register to read either rising clock edge or falling clock edge data.


**Figure 46. DIN Timing Diagram in PDM Mode, Register 0x11, D(2) = 0**

**Figure 47. DIN Timing Diagram in PDM Mode, Register 0x11, D(2) = 1**
**Table 10. PDM Input Timing<sup>(1)</sup>**

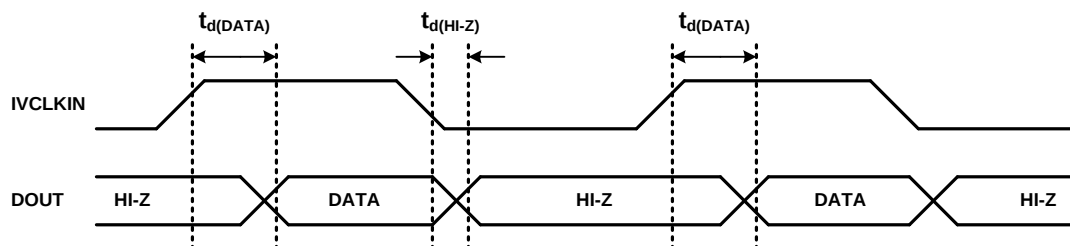
| PARAMETER      |           | IOVDD=1.8V <sup>(2)</sup> |     | IOVDD=3.3V |     | UNIT |
|----------------|-----------|---------------------------|-----|------------|-----|------|
|                |           | MIN                       | MAX | MIN        | MAX |      |
| t <sub>s</sub> | DIN setup | 20                        |     | 20         |     | ns   |
| t <sub>h</sub> | DIN hold  | 3                         |     | 3          |     | ns   |
| t <sub>r</sub> | Rise time |                           | 4   |            | 4   | ns   |
| t <sub>f</sub> | Fall time |                           | 4   |            | 4   | ns   |

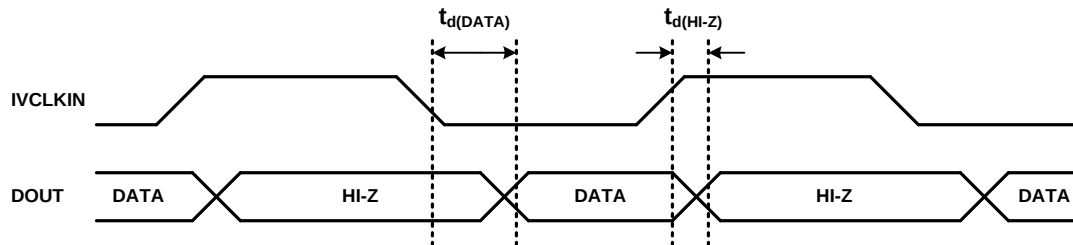
(1) All timing specifications are measured at characterization but not tested at final test.

(2) All specifications at 25°C, IOVDD = 1.8 V

#### 7.4.3.1 DOUT Timing – PDM Output Mode

Set Register 0x03, D(6) = 0 to transmit PDM data on the DOUT terminal. Register 0x07, D(7:6) selects either I Data, V Data, or both for PDM transmission. Register 0x07, D(5) selects whether the data transmits on either the rising edge or the falling edge of IVCLKIN. The DOUT terminal becomes high-impedance on the opposing clock cycle.


**Figure 48. DOUT Timing in PDM Mode (Data on IVCLKIN High)**


**Figure 49. DOUT Timing in PDM Mode (Data on IVCLKIN Low)**
**Table 11. DOUT Timing in PDM Mode<sup>(1)</sup>**

| PARAMETER          |                                       | IOVDD=1.8V <sup>(2)</sup> |     | IOVDD=3.3V |     | UNIT |
|--------------------|---------------------------------------|---------------------------|-----|------------|-----|------|
|                    |                                       | MIN                       | MAX | MIN        | MAX |      |
| $t_d(\text{DATA})$ | IVCLKIN to DOUT delay                 |                           | 30  |            | 30  | ns   |
| $t_d(\text{HI-Z})$ | IVCLKIN to high impedance state delay |                           | 6   |            | 6   | ns   |

(1) All timing specifications are measured at characterization but not tested at final test.

(2) All specifications at 25°C, IOVDD = 1.8 V

## 7.5 Register Map

The TAS2552 I<sup>2</sup>C address is 0x40 (7-bit) when ADDR = 0 and 0x41 (7-bit) when ADDR = 1. See the General I<sup>2</sup>C Operation section for more details.

### 7.5.1 Register Map Summary

| REGISTER |      | READ/WRITE | DEFAULT | FUNCTION                                   |
|----------|------|------------|---------|--------------------------------------------|
| DEC      | HEX  |            |         |                                            |
| 0        | 0x00 | R/W        | 0x00    | Device Status Register                     |
| 1        | 0x01 | R/W        | 0x22    | Configuration Register 1                   |
| 2        | 0x02 | R/W        | 0xFF    | Configuration Register 2                   |
| 3        | 0x03 | R/W        | 0x80    | Configuration Register 3                   |
| 4        | 0x04 | R/W        | 0x00    | DOUT Tristate Mode                         |
| 5        | 0x05 | R/W        | 0x00    | Serial Interface Control Register 1        |
| 6        | 0x06 | R/W        | 0x00    | Serial Interface Control Register 2        |
| 7        | 0x07 | R/W        | 0xC0    | Output Data Register                       |
| 8        | 0x08 | R/W        | 0x10    | PLL Control Register 1                     |
| 9        | 0x09 | R/W        | 0x00    | PLL Control Register 2                     |
| 10       | 0x0A | R/W        | 0x00    | PLL Control Register 3                     |
| 11       | 0x0B | R/W        | 0x8F    | Battery Tracking Inflection Point Register |
| 12       | 0x0C | R/W        | 0x80    | Battery Tracking Slope Control Register    |
| 13       | 0x0D | R/W        | 0xBE    | Limiter Level Control Register             |
| 14       | 0x0E | R/W        | 0x08    | Limiter Attack Rate and Hysteresis Time    |
| 15       | 0x0F | R/W        | 0x05    | Limiter Release Rate                       |
| 16       | 0x10 | R/W        | 0x00    | Limiter Integration Count Control          |
| 17       | 0x11 | R/W        | 0x01    | PDM Configuration Register                 |
| 18       | 0x12 | R/W        | 0x00    | PGA Gain Register                          |
| 19       | 0x13 | R/W        | 0x40    | Class-D Edge Rate Control Register         |
| 20       | 0x14 | R/W        | 0x00    | Boost Auto-Pass Through Control Register   |
| 21       | 0x15 | R/W        | 0x00    | Reserved                                   |
| 22       | 0x16 | R          | 0x00    | Version Number                             |
| 23       | 0x17 | R/W        | 0x00    | Reserved                                   |

## Register Map (continued)

| REGISTER |      | READ/WRITE | DEFAULT | FUNCTION           |
|----------|------|------------|---------|--------------------|
| DEC      | HEX  |            |         |                    |
| 24       | 0x18 | R          | 0x00    | Reserved           |
| 25       | 0x19 | R          | 0x00    | VBAT Data Register |

### 7.5.2 Register 0x00: Device Status Register

This register uses latched faults. The fault bits are clear on write. Read-only commands retain the latched value of the fault bit.

| BIT | NAME            | READ/WRITE | DEFAULT | DESCRIPTION                                                                                        |
|-----|-----------------|------------|---------|----------------------------------------------------------------------------------------------------|
| 7-6 |                 | R/W        | 00      | Reserved. Write only default values.                                                               |
| 5   | PLL_OUT_OF_LOCK | R/W        | 0       | PLL lock<br>0 = PLL is locked<br>1 = PLL is not locked                                             |
| 4-2 |                 | R/W        | 0       | Reserved. Write only default values.                                                               |
| 1   | CLASSD_ILIM     | R/W        | 0       | Class-D over-current<br>0 = Normal operation<br>1 = Class-D output current limit has been exceeded |
| 0   | THERMAL         | R/W        | 0       | Thermal limit<br>0 = Normal operation<br>1 = Limit exceeded                                        |

### 7.5.3 Register 0x01: Configuration Register 1

| BIT | NAME                     | READ/WRITE | DEFAULT | DESCRIPTION                                                                                                                                                         |
|-----|--------------------------|------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 |                          | R/W        | 00      | Reserved. Write only default values.                                                                                                                                |
| 5-4 | PLL_SRC                  | R/W        | 10      | PLL Input<br>00 = MCLK<br>01 = BCLK<br>10 = IVCLKIN<br>11 = 1.8 MHz fixed internal oscillator                                                                       |
| 3   |                          | R/W        | 0       | Reserved. Write only default values.                                                                                                                                |
| 2   | MUTE                     | R/W        | 0       | Triggers mute of Class-D channel controller.<br>0 = Not muted<br>1 = Muted                                                                                          |
| 1   | SWS                      | R/W        | 1       | Software shutdown. When high shuts down all blocks and places part in low power mode. THIS BIT MUST BE SET TO ZERO ONLY AFTER THE DEVICE CONFIGURATION IS COMPLETE. |
| 0   | DEV_RESET <sup>(1)</sup> | R/W        | 0       | Synchronous reset of all digital registers & control circuitry.                                                                                                     |

(1) Wait a minimum of 1ms after EN is pulled high or DEV\_RESET is issued before accessing the control interface.

### 7.5.4 Register 0x02: Configuration Register 2

| BIT | NAME       | READ/WRITE | DEFAULT | DESCRIPTION                          |
|-----|------------|------------|---------|--------------------------------------|
| 7   | CLASSD_EN  | R/W        | 1       | Class D Enable                       |
| 6   | BOOST_EN   | R/W        | 1       | Boost Enable                         |
| 5   | APT_EN     | R/W        | 1       | Auto Pass-Thru Enable                |
| 4   | RESERVED   | R/W        | 0       | Reserved. Write only default values. |
| 3   | PLL_EN     | R/W        | 1       | PLL Enable                           |
| 2   | LIM_EN     | R/W        | 1       | Battery Tracking AGC Enable          |
| 1   | IVSENSE_EN | R/W        | 1       | I/V Sense Enable                     |

| BIT | NAME     | READ/WRITE | DEFAULT          | DESCRIPTION                                                                                                  |
|-----|----------|------------|------------------|--------------------------------------------------------------------------------------------------------------|
| 0   | RESERVED | R/W        | 1 <sup>(1)</sup> | Reserved. MUST BE WRITTEN TO ZERO DURING CONFIGURATION SEQUENCE as shown in <a href="#">Initialization</a> . |

(1) Register 0x02, Bit 0 defaults to 1, but must be written to 0 during initialization.

### 7.5.5 Register 0x03: Configuration Register 3

| BIT | NAME           | READ / WRITE | DEFAULT | DESCRIPTION                                                                                                                                                                                               |
|-----|----------------|--------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | ANALOG_IN_SEL  | R/W          | 1       | Selects analog in path for data to class-D. When set to zero (digital in), no signal should be present on the analog terminals.<br>0 = Digital Audio Input<br>1 = Analog Audio Input                      |
| 6   | I2S_OUT_SEL    | R/W          | 0       | Selects between PDM and I2S for I/V Sense output data format.<br>0 = PDM<br>1 = I2S                                                                                                                       |
| 5   | PDM_IN_SEL     | R/W          | 0       | Selects PDM as input to modulator<br>0 = PDM is not selected<br>1 = PDM is selected only if Digital Audio Input is selected (Reg 0x03 D[7] = 0)                                                           |
| 4-3 | DIN_SOURCE_SEL | R/W          | 00      | DIN Source Select<br>00 = Modulator input muted<br>01 = Use left stream for modulator<br>10 = Use right stream for modulator<br>11 = Use average of left and right streams for modulator                  |
| 2-0 | WCLK_FREQ      | R/W          | 000     | WCLK Frequency<br>000 = 8 kHz<br>001 = 11.025 kHz / 12 kHz<br>010 = 16 kHz<br>011 = 22.05 kHz / 24 kHz<br>100 = 32 kHz<br>101 = 44.1 kHz / 48 kHz<br>110 = 88.2 kHz / 96 kHz<br>111 = 176.4 kHz / 192 kHz |

### 7.5.6 Register 0x04: DOUT Tristate Mode

For systems with multiple devices sharing a common DOUT line with a TDM interface mode, set Bit 2 to 1 to ensure DOUT stays in high-impedance tri-state mode when it is not transmitting data.

| BIT | NAME           | READ / WRITE | DEFAULT | DESCRIPTION                                                                                                                                                             |
|-----|----------------|--------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-3 |                | R/W          | 0000 0  | Reserved. Write only default values.                                                                                                                                    |
| 2   | SDOUT_TRISTATE | R/W          | 0       | DOUT Tri-state Mode (for I2S mode only, see Reg 0x03, bit 7)<br>0 = DOUT set to logic low when not transmitting data<br>1 = DOUT in tristate when not transmitting data |
| 1-0 |                | R/W          | 00      | Reserved. Write only default values.                                                                                                                                    |

### 7.5.7 Register 0x05: Serial Interface Control Register 1

| BIT | NAME         | READ/WRITE | DEFAULT | DESCRIPTION                                                                                                                      |
|-----|--------------|------------|---------|----------------------------------------------------------------------------------------------------------------------------------|
| 7   | WCLKDIR      | R/W        | 0       | WCLK Direction<br>0 = WCLK is an input terminal<br>1 = WCLK is an output terminal                                                |
| 6   | BCLKDIR      | R/W        | 0       | BCLK Direction<br>0 = BCLK is an input terminal<br>1 = BCLK is an output terminal                                                |
| 5-4 | CLKSPERFRAME | R/W        | 00      | Clocks per Frame<br>00 = 32 clocks<br>01 = 64 clocks<br>10 = 128 clocks<br>11 = 256 clocks                                       |
| 3-2 | DATAFORMAT   | R/W        | 00      | Data Format<br>00 = I2S format<br>01 = DSP (PCM format)<br>10 = Right justified format (RJF)<br>11 = Left justified format (LJF) |
| 1-0 | WORDLENGTH   | R/W        | 00      | Word Length<br>00 = 16 bits<br>01 = 20 bits<br>10 = 24 bits<br>11 = 32 bits                                                      |

### 7.5.8 Register 0x06: Serial Interface Control Register 2

This register sets the clock cycle offset between the WCLK edge to the MSB of serial interface patterns. This is useful for TDM mode where multiple devices share DIN or DOUT lines.

| BIT | NAME          | READ / WRITE | DEFAULT   | DESCRIPTION                                                                                                                                         |
|-----|---------------|--------------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | I2S_SHIFT_REG | R/W          | 0000 0000 | Offset from WCLK to MSB in serial interface patterns.<br>0000 0000 = 0 bit offset<br>0000 0001 = 1 bit offset<br>....<br>1111 1111 = 255 bit offset |

### 7.5.9 Register 0x07: Output Data Register

This register sets the output data for DOUT. Most systems will simply set L\_DATA\_OUT to transmit output current data and R\_DATA\_OUT to transmit voltage data. Other data is available, like VBAT voltage, VBOOST voltage, and PGA gain.

Bit 5 is a dual-purpose bit. If I2S\_OUT\_SEL = 0 (Register 0x03, Bit 6) and the PDM\_DATA\_SEL bits are set to transmit only I-Data or V-Data, then Bit 5 dictates if that data is transmitted on the clock rising edge or falling edge. This allows two TAS2552 devices in PDM mode to tie their DOUT lines together and connect to the host digital mic input. In this configuration, each device broadcasts its output current or output voltage information – one on the rising edge of the clock, the other on the falling edge. This is a simple interface technique that does not require programming the host for TDM-interface mode.

| BIT | NAME         | READ / WRITE | DEFAULT | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----|--------------|--------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 | PDM_DATA_SEL | R/W          | 11      | <p>PDM Data Select</p> <p>These bits are operative only if I2S_OUT_SEL = 0 for PDM mode (see Register 0x03, Bit 6).</p> <p>00 - I Data Only - Select Ch1 or Ch2 with bit[5]</p> <p>01 - V Data Only - Select Ch1 or Ch2 with bit[5]</p> <p>10 - I/V Data (Ch1/2)</p> <p>11 - V/I Data (Ch1/2)</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 5-3 | R_DATA_OUT   | R/W          | 000     | <p>Serial Interface Data, Right Channel</p> <p>Bit 5 is a dual-purpose bit, depending on the state of I2S_OUT_SEL (Register 0x03, Bit 6).</p> <p>If I2S_OUT_SEL = 0 and PDM_DATA_SEL = 00 or 01 (for single-channel PDM output mode), then Bit 5 will select whether data is transmitted on the rising or falling edge of the clock.</p> <p>0xx = Falling Edge (Ch 1)</p> <p>1xx = Rising Edge (Ch 2)</p> <p>If I2S_OUT_SEL = 1, then Bits 5-3 have the same function as L_DATA_OUT. Read the description in L_DATA_OUT for requirements on BCLK and WORD_LENGTH.</p> <p>000 = I Data (16'b)</p> <p>001 = V Data (16'b)</p> <p>010 = VBAT Data (8'b)</p> <p>011 = VBOOST Data (8'b)</p> <p>100 = PGA Gain (5'b)</p> <p>101 = I Data, V Data (32'b)</p> <p>110 = VBAT, VBOOST, PGA Gain (21'b)</p> <p>111 = Disabled (Hi-Z)</p> <p>NOTE: For VBAT and VBOOST, the device must be in a mode that uses this information, such as Battery Tracking AGC.</p> |
| 2-0 | L_DATA_OUT   | R/W          | 000     | <p>Serial Interface Data, Left Channel</p> <p>Users must provide enough BCLK cycles per WCLK frame to shift all the data out. If there are additional BCLK cycles per WCLK frame beyond the WORD_LENGTH setting, the data line will be HI-Z if SDOUT_TRISTATE (Register 0x04, Bit 3) is set to 1; otherwise the data line will be held low for the extra BCLK cycles.</p> <p>Users must also program a sufficient WORD_LENGTH setting. If selected data contains fewer bits than WORD_LENGTH setting, the extra bits will be 0's.</p> <p>000 = I Data (16'b)</p> <p>001 = V Data (16'b)</p> <p>010 = VBAT Data (8'b)</p> <p>011 = VBOOST Data (8'b)</p> <p>100 = PGA Gain (5'b)</p> <p>101 = I Data, V Data (32'b)</p> <p>110 = VBAT, VBOOST, PGA Gain (21'b)</p> <p>111 = Disabled (Hi-Z)</p> <p>NOTE: For VBAT and VBOOST, the device must be in a mode that uses this information, such as Battery Tracking AGC.</p>                                 |

### 7.5.10 Register 0x08: PLL Control Register 1

The equation for the PLL frequency is:

$$PLL\_CLK = \frac{0.5 \times PLL\_CLKIN \times J \cdot D}{2^P} \quad (2)$$

J = 4, 5, 6, ... 96

D = 0, 1, 2, ... 9999

P = 0,1

Registers 0x08 – 0x0A will only update when the PLL is disabled. To update the J, D, and P coefficients, set PLL\_EN = 0 (Register 0x02, Bit 3) to disable the PLL, update Registers 0x08 – 0x0A, then set PLL\_EN = 1 to activate the PLL.

| BIT | NAME             | READ / WRITE | DEFAULT  | DESCRIPTION                                                                                                                                                                                          |
|-----|------------------|--------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | PLL_PRESCALE_SEL | R/W          | 0        | PLL P Pre-Scale Select<br>1: P = 1<br>0: P = 0                                                                                                                                                       |
| 6-0 | PLL_J            | R/W          | 001 0000 | PLL J Characteristic Multiplier Value<br>000 0000 ... 000 0011: Do not use<br>000 0100: J=4<br>...<br>001 0000: J=16<br>...<br>101 1111: J=95<br>110 0000: J=96<br>110 0001 ... 111 1111: Do not use |

### 7.5.11 Register 0x09: PLL Control Register 2

| BIT | NAME        | READ / WRITE | DEFAULT | DESCRIPTION                                                                                                                                                                                                                                                                                                       |
|-----|-------------|--------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | PLL_BYPASS  | R/W          | 0       | 1: Bypasses PLL by setting PLL_CLK = PLL_CLKIN<br>0: Sets PLL_CLK according to <a href="#">Equation 2</a>                                                                                                                                                                                                         |
| 6   |             |              | 0       | Reserved                                                                                                                                                                                                                                                                                                          |
| 5-0 | PLL_D[13:8] | R/W          | 00 0000 | PLL D Mantissa Multiplier Value (LSB)<br>The complete PLL D value comprises PLL_D[13:8] (MSB) concatenated with PLLD[7:0] (LSB)<br>00 0000 0000 0000: D=0000<br>00 0000 0000 0001: D=0001<br>...<br>10 0111 0000 1110: D=9998<br>10 0111 0000 1111: D=9999<br>10 0111 0001 0000 ... 11 1111 1111 1111: Do not use |

### 7.5.12 Register 0x0A: PLL Control Register 3

| BIT | NAME       | READ / WRITE | DEFAULT   | DESCRIPTION                                                                                                                                                                                                                                                                                                       |
|-----|------------|--------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | PLL_D[7:0] | R/W          | 0000 0000 | PLL D Mantissa Multiplier Value (LSB)<br>The complete PLL D value comprises PLL_D[13:8] (MSB) concatenated with PLLD[7:0] (LSB)<br>00 0000 0000 0000: D=0000<br>00 0000 0000 0001: D=0001<br>...<br>10 0111 0000 1110: D=9998<br>10 0111 0000 1111: D=9999<br>10 0111 0001 0000 ... 11 1111 1111 1111: Do not use |

### 7.5.13 Register 0x0B: Battery Tracking Inflection Point Register

| BIT | NAME       | READ / WRITE | DEFAULT   | DESCRIPTION                                                                                                                                                                                                  |
|-----|------------|--------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | INFLECTION | R/W          | 1000 1111 | Battery Inflection Point Value<br>0.01733 V per step<br>0000 0000 = RESERVED<br>...<br>0110 1100 = RESERVED<br>0110 1101 = 3.00 V<br>...<br>1111 1101 = 5.49 V<br>1111 1110 = 5.50 V<br>1111 1111 = RESERVED |

### 7.5.14 Register 0x0C: Battery Tracking Slope Control Register

| BIT | NAME  | READ / WRITE | DEFAULT   | DESCRIPTION                                                                                                                                                                                                                   |
|-----|-------|--------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | SLOPE | R/W          | 1000 0000 | Battery Tracking Slope Value ( $\Delta V_{LIM} / \Delta V_{BAT}$ )<br>0.0373 V/V per step<br>0000 0000 = 1.2 V/V<br>0000 0001 = 1.237 V/V<br>...<br>1111 1101 = 10.675 V/V<br>1111 1110 = 10.713 V/V<br>1111 1111 = 10.75 V/V |

### 7.5.15 Register 0x0D: Reserved Register

| BIT | NAME | READ / WRITE | DEFAULT   | DESCRIPTION                                                               |
|-----|------|--------------|-----------|---------------------------------------------------------------------------|
| 7-0 |      | R/W          | 1011 1110 | Write to 0xC0 during initialization. See <a href="#">Initialization</a> . |

### 7.5.16 Register 0x0E: Battery Tracking Limiter Attack Rate and Hysteresis Time

| BIT | NAME            | READ / WRITE | DEFAULT | DESCRIPTION                                                                                                                                                                 |
|-----|-----------------|--------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 | HYSTERESIS      | R/W          | 00      | Hysteresis before re-arming release time<br>00 = No hysteresis<br>01 = 4.36 mV hysteresis<br>10 = 13.08 mV hysteresis<br>11 = 30.52 mV hysteresis                           |
| 5   |                 | R/W          | 0       | Write to 1 during initialization. See <a href="#">Initialization</a> .                                                                                                      |
| 4-3 | APT_DIS_VOLTAGE | R/W          | 01      | VBAT threshold below which Boost APT is disabled and the boost remains active regardless of Class-D output voltage.<br>00 = 2.5 V<br>01 = 2.7 V<br>10 = 2.9 V<br>11 = 3.1 V |
| 2-0 | ATTACK_TIME     | R/W          | 000     | Attack Time<br>350 $\mu$ s / dB per step<br>000 = 20 $\mu$ s / dB<br>001 = 370 $\mu$ s / dB<br>...<br>110 = 2120 $\mu$ s / dB<br>111 = 2470 $\mu$ s / dB                    |

### 7.5.17 Register 0x0F: Battery Tracking Limiter Release Rate

| BIT | NAME     | READ / WRITE | DEFAULT | DESCRIPTION                                                                                                                          |
|-----|----------|--------------|---------|--------------------------------------------------------------------------------------------------------------------------------------|
| 7-4 |          | R/W          | 00      | Reserved. Write only default values.                                                                                                 |
| 3-0 | REL_TIME | R/W          | 0100    | Release Time<br>105 ms / dB per step<br>0000 = 50 ms / dB<br>0001 = 155 ms / dB<br>...<br>1110 = 1520 ms / dB<br>1111 = 1625 ms / dB |

### 7.5.18 Register 0x10: Battery Tracking Limiter Integration Count Control

Limiter integration affects how the AGC state machine interprets the AGC output voltage trigger threshold. Increasing the integration count requires more AGC output peaks to exceed the limiter threshold before the limiter changes its gain.

| BIT | NAME         | READ / WRITE | DEFAULT | DESCRIPTION                                                                                                                                                                                                                                                                              |
|-----|--------------|--------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 | UP_DWN_RATIO | R/W          | 00      | Control Integration Count Up/Down Ratio<br>The UP_DWN_RATIO sets the ratio of the addition to and the subtraction from the integration count, meaning that the input has to be below the limit threshold for $4^{\text{UP\_DWN\_RATIO}}$ counts before the integration count is reduced. |
| 5-0 | INT_CNT      | R/W          | 00 0000 | Integration Count Control Register<br>Larger values increase filtering before the attack and decay time are triggered.                                                                                                                                                                   |

### 7.5.19 Register 0x11: PDM Configuration Register

Sets the PDM clock source and whether channel 1 data is transmitted on the rising or falling edge of the clock. Channel 2 transmits on the opposite edge.

| BIT | NAME        | READ / WRITE | DEFAULT | DESCRIPTION                                                                |
|-----|-------------|--------------|---------|----------------------------------------------------------------------------|
| 7-3 |             | R/W          | 0 0000  | Reserved. Write only default values.                                       |
| 2   | PDM_DATA_ES | R/W          | 0       | PDM Data Edge Select<br>0 = falling edge<br>1 = rising edge                |
| 1-0 | PDM_CLK_SEL | R/W          | 01      | PDM Clock Select<br>00 = PLL / 8<br>01 = IVCLKIN<br>10 = BCLK<br>11 = MCLK |

### 7.5.20 Register 0x12: PGA Gain Register

| BIT | NAME     | READ / WRITE | DEFAULT | DESCRIPTION                                                                                 |
|-----|----------|--------------|---------|---------------------------------------------------------------------------------------------|
| 7-5 |          | R/W          | 000     | Reserved. Write only default values.                                                        |
| 4-0 | PGA_GAIN | R/W          | 0 0000  | PGA Gain Value<br>00000 = -7 dB<br>00001 = -6 dB<br>...<br>11110 = +23 dB<br>11111 = +24 dB |

### 7.5.21 Register 0x13: Class-D Edge Rate Control Register

| BIT | NAME        | READ / WRITE | DEFAULT | DESCRIPTION                                                                                                                                                                                                                                                                           |
|-----|-------------|--------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | GAINCOMP_EN | R/W          | 0       | I-V Sense Gain Compensation Control<br>Enables AGC compensation for current sense feedback. AGC compensation increases the gain of the current sense data by the same gain the AGC instantaneously attenuates.<br>0 = No I-V sense gain compensation<br>1 = Gain compensation enabled |
| 6-4 | ERC_SEL     | R/W          | 100     | Class-D Output Edge Rate Control<br>000 = 50 ns<br>001 = 40 ns<br>010 = 29 ns<br>011 = 25 ns<br>100 = 14 ns (default)<br>101 = 13 ns<br>110 = 12 ns<br>111 = 11 ns                                                                                                                    |
| 3-0 |             | R/W          | 0000    | Reserved. Write only default values.                                                                                                                                                                                                                                                  |

### 7.5.22 Register 0x14: Boost Auto-Pass Through Control Register

Auto-Pass Through deactivates the boost converter when the battery voltage is sufficient for the required Class-D output voltage. This register sets the threshold for activating the boost converter and the delay time between the Class-D output voltage dropping below the threshold before the boost converter deactivates.

| BIT | NAME          | READ / WRITE | DEFAULT | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|---------------|--------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-4 |               | R/W          | 0000    | Reserved. Write only default values.                                                                                                                                                                                                                                                                                                                                                                        |
| 3-2 | APT_THRESHOLD | R/W          | 00      | Analog Input – Auto-Pass Through Threshold<br>The boost converter activates when the Class-D output voltage exceeds this threshold voltage.<br>00 = 0.5 V<br>01 = 1.0 V<br>10 = 1.4 V<br>11 = 2.0 V<br>Digital Input – Auto-Pass Through Threshold<br>The boost converter activates when the Class-D output voltage exceeds this threshold voltage.<br>00 = 0.2 V<br>01 = 0.7 V<br>10 = 1.1 V<br>11 = 1.7 V |
| 1-0 | APT_DELAY_SEL | R/W          | 00      | Auto-Pass Thru Delay<br>The delay between the Class-D output voltage dropping below the auto-pass thru threshold voltage and the boost converter deactivating.<br>00 = 50 ms<br>01 = 75 ms<br>10 = 125 ms<br>11 = 200 ms                                                                                                                                                                                    |

### 7.5.23 Register 0x15: Reserved Register

| BIT | NAME | READ / WRITE | DEFAULT   | DESCRIPTION |
|-----|------|--------------|-----------|-------------|
| 7-0 |      | R            | 0000 0000 | Reserved    |

### 7.5.24 Register 0x16: Version Number

| BIT | NAME        | READ / WRITE | DEFAULT | DESCRIPTION                     |
|-----|-------------|--------------|---------|---------------------------------|
| 7-4 |             | R            | 0000    | Reserved                        |
| 3-0 | SILICON_VER | R            | 1000    | Silicon version identifier bits |

### 7.5.25 Register 0x17: Reserved Register

| BIT | NAME | READ / WRITE | DEFAULT   | DESCRIPTION |
|-----|------|--------------|-----------|-------------|
| 7-0 |      | R            | 0000 0000 | Reserved    |

### 7.5.26 Register 0x18: Reserved Register

| BIT | NAME | READ / WRITE | DEFAULT   | DESCRIPTION |
|-----|------|--------------|-----------|-------------|
| 7-0 |      | R            | 0000 0000 | Reserved    |

### 7.5.27 Register 0x19: VBAT Data Register

| BIT | NAME | READ /<br>WRITE | DEFAULT   | DESCRIPTION                                                                                                                                                                                                                                                                                                                           |
|-----|------|-----------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | VBAT | R               | 0000 0000 | <p>Battery Voltage Data</p> <p>VBAT data is only available when the device is in a mode that uses the VBAT measurement, such as Battery Tracking AGC.</p> <p>1 LSB <math>\approx</math> 17.33 mV</p> <p>0000 0000 = RESERVED</p> <p>...</p> <p>0100 1001 = RESERVED</p> <p>0101 0000 = 2.5 V</p> <p>...</p> <p>1111 1111 = 5.55 V</p> |

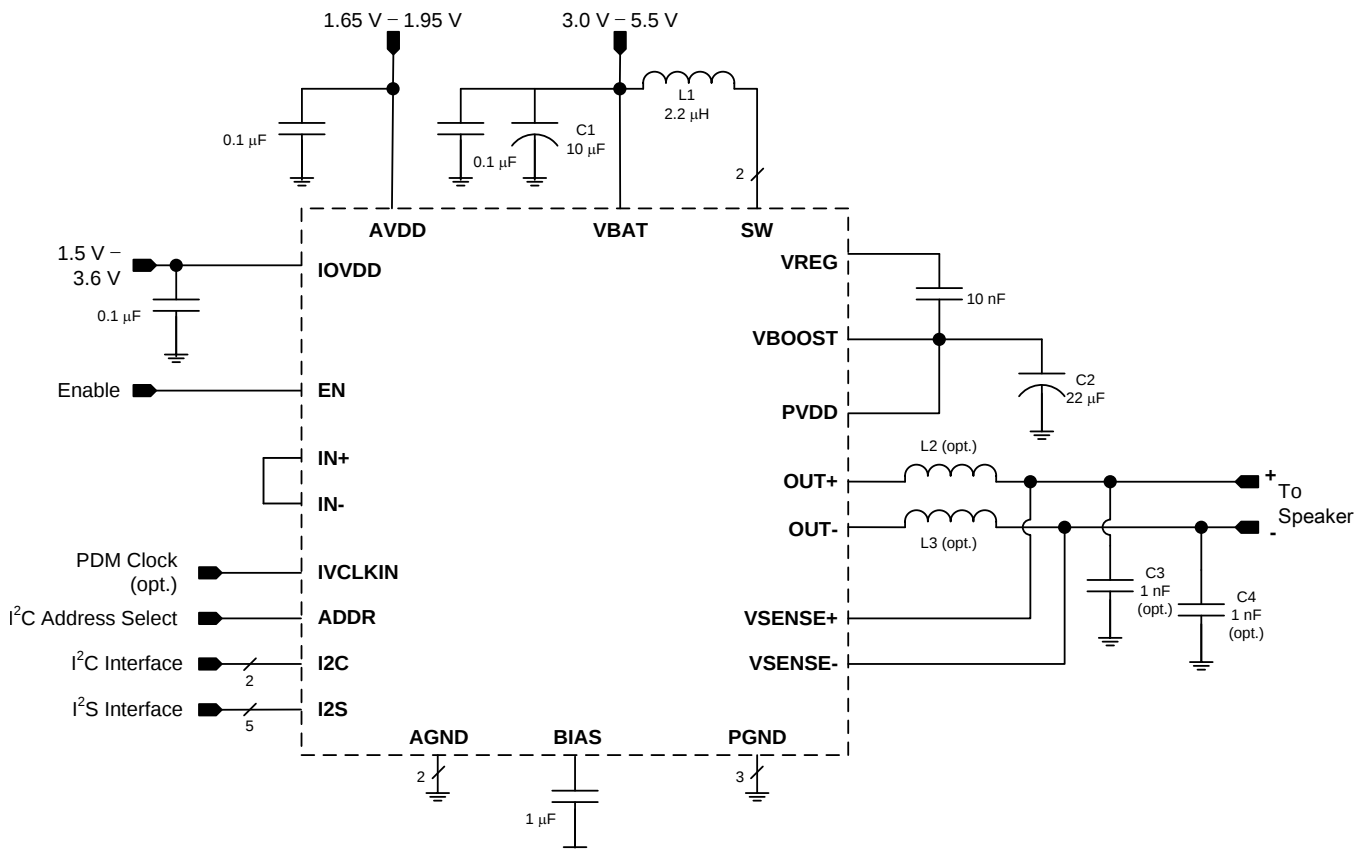
## 8 Applications and Implementation

### 8.1 Application Information

The TAS2552 is a digital or analog input high efficiency Class-D audio power amplifier with advanced battery current management and an integrated Class-G boost converter. In auto passthrough mode, the Class-G boost converter generates the Class-D amplifier supply rail. During low Class-D output power, the boost improves efficiency by deactivating and connecting VBAT directly to the Class-D amplifier supply. When high power audio is required, the boost quickly activates to provide louder audio than a stand-alone amplifier connected directly to the battery. To enable load monitoring, the TAS2552 constantly measures the current and voltage across the load and provides a digital stream of this information back to a processor.

### 8.2 Typical Applications

#### 8.2.1 Typical Application - Digital Audio Input



**Figure 50. Typical Application Schematic**

**Table 12. Recommended External Components**

| COMPONENT | DESCRIPTION                     | SPECIFICATION              | MIN | TYP  | MAX   | UNIT |
|-----------|---------------------------------|----------------------------|-----|------|-------|------|
| L1        | Boost Converter Inductor        | Inductance, 20% Tolerance  |     | 2.2  |       | μH   |
|           |                                 | Saturation Current         |     | 2.6  |       | A    |
| L2, L3    | EMI Filter Inductors (optional) | Impedance at 100MHz        |     | 120  |       | Ω    |
|           |                                 | DC Resistance              |     |      | 0.095 | Ω    |
|           |                                 | DC Current                 |     |      | 1.5   | A    |
|           |                                 | Size                       |     | 0402 |       | EIA  |
|           |                                 |                            |     |      |       |      |
| C1        | Boost Converter Input Capacitor | Capacitance, 20% Tolerance | 10  |      |       | μF   |

## Typical Applications (continued)

**Table 12. Recommended External Components (continued)**

| COMPONENT | DESCRIPTION                                                      | SPECIFICATION                 | MIN | TYP | MAX | UNIT |
|-----------|------------------------------------------------------------------|-------------------------------|-----|-----|-----|------|
| C2        | Boost Converter Output Capacitor                                 | Type                          | X5R |     |     |      |
|           |                                                                  | Capacitance, 20% Tolerance    | 22  |     | 47  | μF   |
|           |                                                                  | Rated Voltage                 | 16  |     |     | V    |
|           |                                                                  | Capacitance at 8.5 V derating | 7   |     |     | μF   |
| C3, C4    | EMI Filter Capacitors (optional, must use L2, L3 if C3, C4 used) | Capacitance                   |     | 1   |     | nF   |

### 8.2.1.1 Design Requirements

**Table 13. Design Parameters**

| DESIGN PARAMETER                | EXAMPLE VALUE                   |
|---------------------------------|---------------------------------|
| Audio Input                     | Digital Audio, I <sup>2</sup> S |
| Current and Voltage Data Stream | Digital Audio, I <sup>2</sup> S |
| Mono or Stereo Configuration    | Mono                            |
| Max Output Power at 1% THD+N    | 3.3                             |

### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 Audio Input/Output

The choice of digital or analog audio input is driven by system specific considerations. However, since a digital audio interface will typically be used to send current and voltage data from the TAS2552 to a system processor, using a bidirectional I<sup>2</sup>S interface is likely to be the best choice.

If a digital audio input is used, the analog inputs, IN+ and IN-, should be shorted together, and not tied to ground.

#### 8.2.1.2.2 Mono/Stereo Configuration

In this application, the device is assumed to be operating in mono mode. See [General I<sup>2</sup>C Operation](#) for information on changing the I<sup>2</sup>C address of the TAS2552 to support stereo operation. Mono or stereo configuration does not impact the device performance.

#### 8.2.1.2.3 Boost Converter Passive Devices

The boost converter requires three passive devices that are labeled L1, C1 and C2 in [Figure 50](#) and whose specifications are provided in [Table 12](#). These specifications are based on the design of TAS2552 and are necessary to meet the performance targets of the device. In particular, L1 should not be allowed to enter in the current saturation region.

Specifically, the product of L1 and C2 (derated value at 8.5 V) has to be greater than 10e-12 for boost stability after accounting worst case variation of L1 and C2. To satisfy sufficient energy transfer, L1 needs to be > 2 μH at the boost switching frequency (~1.75 MHz). Minimum C2 (derated value at 8.5 V) should be > 4 μF for Class-D power delivery specification. The saturation current for L1 should be > ILIM to deliver Class-D peak power.

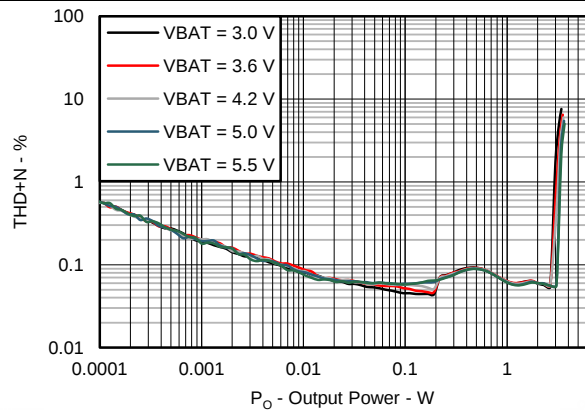
#### 8.2.1.2.4 EMI Passive Devices

The TAS2552 supports edge-rate control to minimize EMI, but the system designer may want to include passive devices on the Class-D output devices. These passive devices that are labeled L2, L3, C3 and C4 in [Figure 50](#) and their recommended specifications are provided in [Table 12](#). If C3 and C4 are used, they must be placed after L2 and L3 respectively to maintain the stability of the output stage.

#### 8.2.1.2.5 Miscellaneous Passive Devices

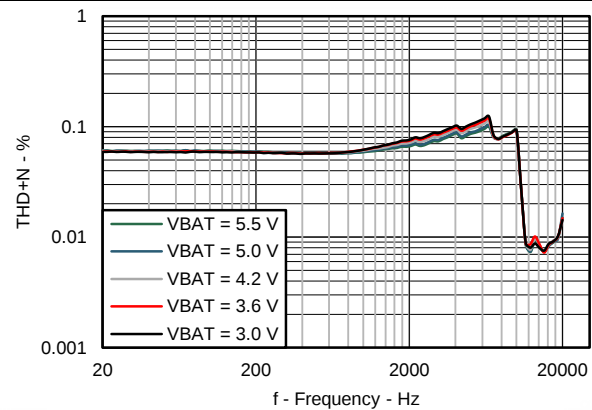
- VREG Capacitor: Needs to be 10 nF to meet boost and class-D power delivery and efficiency specs.
- BIAS Capacitor: Needs to be 1 μF to meet PSSR and noise performance.

### 8.2.1.3 Application Performance Plots



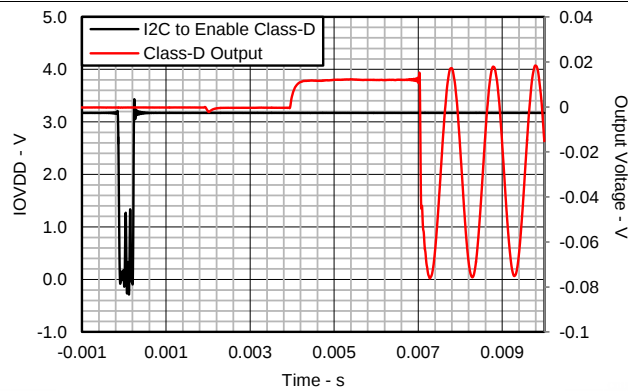
AGC=OFF, Gain = 15 dB

Figure 51. THD+N vs Output Power (8Ω) for Digital Input



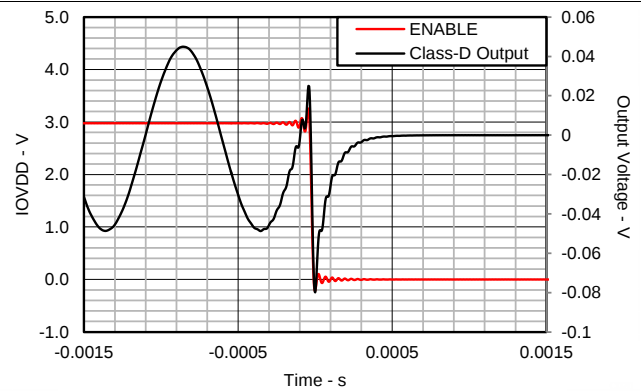
AGC=OFF, Gain = 15 dB,  $P_{out} = 1\text{ W}$

Figure 52. THD+N vs Frequency (8Ω) for Digital Input



Use start-up sequence in [Initialization](#)

Figure 53. Startup Timing

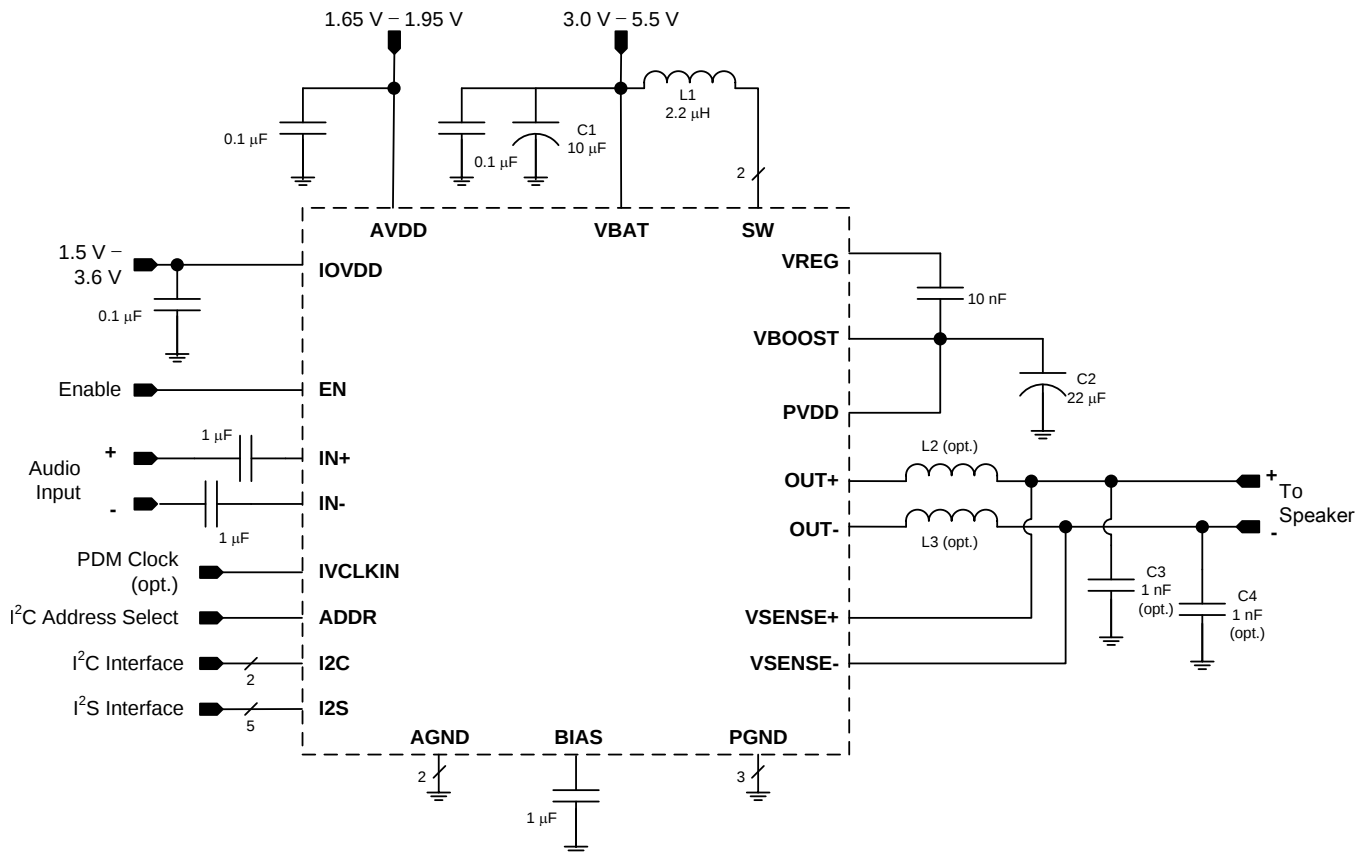


Class D output and EN pulled low

Figure 54. Shutdown Timing

## 8.2.2 Typical Application - Analog Audio Input

Using the analog audio input is very similar to the digital audio input case in [Typical Application - Digital Audio Input](#), and this section will only discuss the differences from the digital input configuration.



**Figure 55. Typical Application Schematic**

### 8.2.2.1 Design Requirements

**Table 14. Design Parameters**

| DESIGN PARAMETER                | EXAMPLE VALUE                   |
|---------------------------------|---------------------------------|
| Audio Input                     | Analog                          |
| Current and Voltage Data Stream | Digital Audio, I <sup>2</sup> S |
| Mono or Stereo Configuration    | Mono                            |
| Max Output Power at 1% THD+N    | 3.3                             |

### 8.2.2.2 Detailed Design Procedure

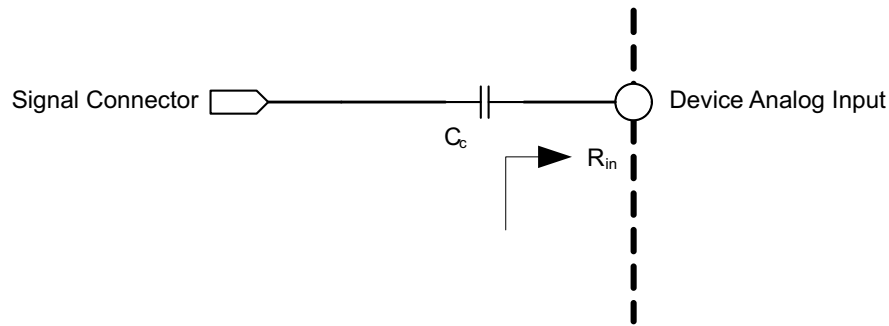
#### 8.2.2.2.1 Audio Input/Output

In this application, system considerations require the use of an analog audio input. Note that a digital audio interface, such as I<sup>2</sup>S, still needs to be connected to send current and voltage data from the TAS2552 to a system processor.

The analog inputs to TAS2552 should be ac-coupled to the device terminals to allow decoupling of signal source's common mode voltage with that of TAS2552's common mode voltage. The input coupling capacitor in combination with the selected input impedance of TAS2552 forms a high-pass filter.

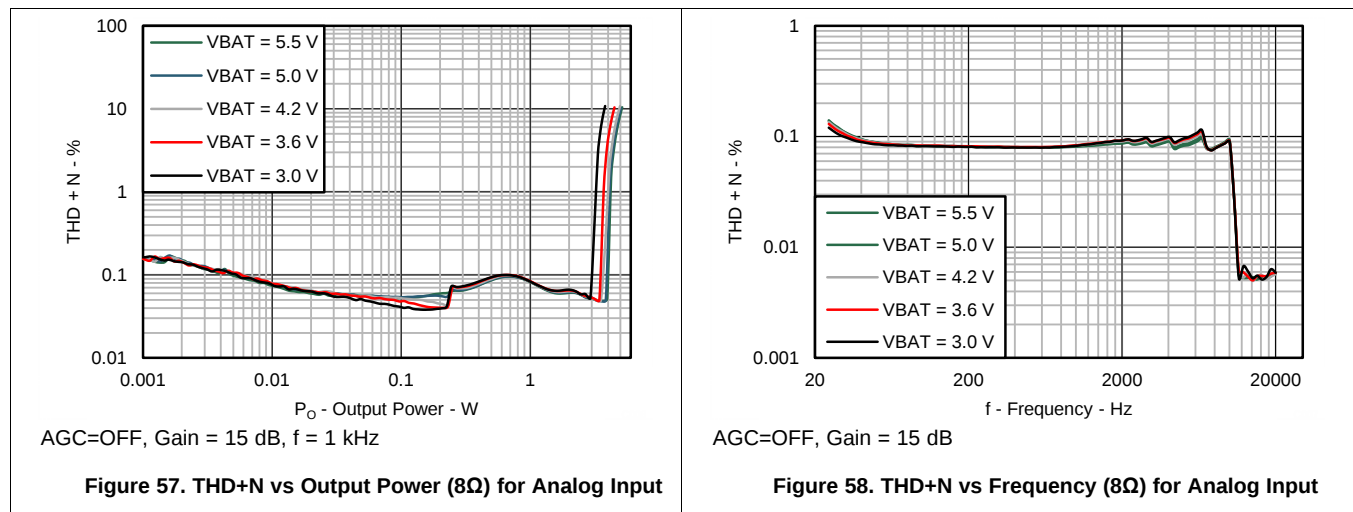
$$F_c = 1/(2\pi R_{in} C_c) \quad (3)$$

$$C_c = 1/(2\pi R_{in} F_c) \quad (4)$$


**Figure 56. Analog Input Connection**

For high fidelity audio playback, it is desirable to keep the cutoff frequency of the high pass filter below the minimum reproducible frequency of the speaker. For example, a 1  $\mu\text{F}$  capacitor connected to the differential analog inputs with input resistance 10 k $\Omega$  results in a cutoff frequency of 16 Hz.

### 8.2.2.3 Application Performance Plots



### 8.2.3 Typical Application - Maximum Output Power, Analog Audio Input

This application is the same as [Typical Application - Analog Audio Input](#), except that in this case the boost current limit is set to the maximum value of 3.1 A and the boost inductor needs to be chosen appropriately. See [Configurable Boost Current Limit \(ILIM\)](#) for instructions on setting the boost current limit. The same boost current limit and resulting capacitor change can be used for digital audio input as well.

For schematic, see [Figure 55](#).

**Table 15. Recommended External Components**

| COMPONENT | DESCRIPTION                                                      | SPECIFICATION                 | MIN | TYP  | MAX   | UNIT |
|-----------|------------------------------------------------------------------|-------------------------------|-----|------|-------|------|
| L1        | Boost Converter Inductor                                         | Inductance, 20% Tolerance     |     | 2.2  |       | μH   |
|           |                                                                  | Saturation Current            |     | 3.1  |       | A    |
| L2, L3    | EMI Filter Inductors (optional)                                  | Impedance at 100MHz           |     | 120  |       | Ω    |
|           |                                                                  | DC Resistance                 |     |      | 0.095 | Ω    |
|           |                                                                  | DC Current                    |     |      | 1.5   | A    |
|           |                                                                  | Size                          |     | 0402 |       | EIA  |
| C1        | Boost Converter Input Capacitor                                  | Capacitance, 20% Tolerance    | 10  |      |       | μF   |
| C2        | Boost Converter Output Capacitor                                 | Type                          | X5R |      |       |      |
|           |                                                                  | Capacitance, 20% Tolerance    | 22  |      | 47    | μF   |
|           |                                                                  | Rated Voltage                 | 16  |      |       | V    |
|           |                                                                  | Capacitance at 8.5 V derating | 7   |      |       | μF   |
| C3, C4    | EMI Filter Capacitors (optional, must use L2, L3 if C3, C4 used) | Capacitance                   |     | 1    |       | nF   |

#### 8.2.3.1 Design Requirements

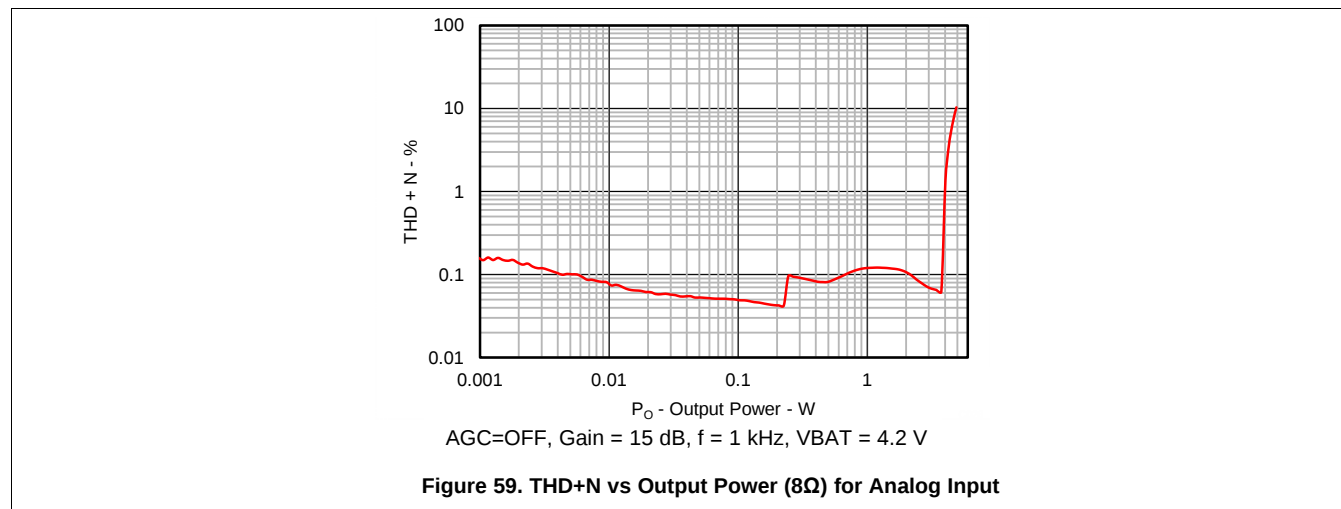
**Table 16. Design Parameters**

| DESIGN PARAMETER                | EXAMPLE VALUE                   |
|---------------------------------|---------------------------------|
| Audio Input                     | Analog                          |
| Current and Voltage Data Stream | Digital Audio, I <sup>2</sup> S |
| Mono or Stereo Configuration    | Mono                            |
| Max Output Power at 1% THD+N    | 4.0                             |

### 8.2.3.2 Detailed Design Procedure

The Design Procedure is the same as in [Detailed Design Procedure](#).

### 8.2.3.3 Application Performance Plots



## 8.3 Initialization

To configure the TAS2552, follow these steps.

1. Bring-up the power supplies as in [Power Supply Sequencing](#).
2. Set the EN terminal to HIGH.
3. Configure the registers in the sequence below. Do not set the bits in the final two steps to zero anytime before the end of the sequence.
  - Configure device register
  - ...
  - ...
  - ...
  - Configure device register
  - Set Register 0x0D D[7:0] = 0xC0
  - Set Register 0x0E D[5] = 1
  - Set Register 0x02 D[0] = 0
  - Set Register 0x01 D[1] = 0

## 9 Power Supply Recommendations

### 9.1 Power Supplies

The TAS2552 requires three power supplies:

- Boost Input (terminal: VBAT)
  - Voltage: 3.0 V to 5.5 V
  - Max Current: 2.6 A for ILIM = 2.5 A (default), 3.1 A for ILIM = 3.0 A
- Analog Supply (terminal: AVDD)
  - Voltage: 1.65 V to 1.95 V
  - Max Current: 30 mA
- Digital I/O Supply (terminal: IOVDD)
  - Voltage: 1.5 V to 3.6 V
  - Max Current: 5 mA

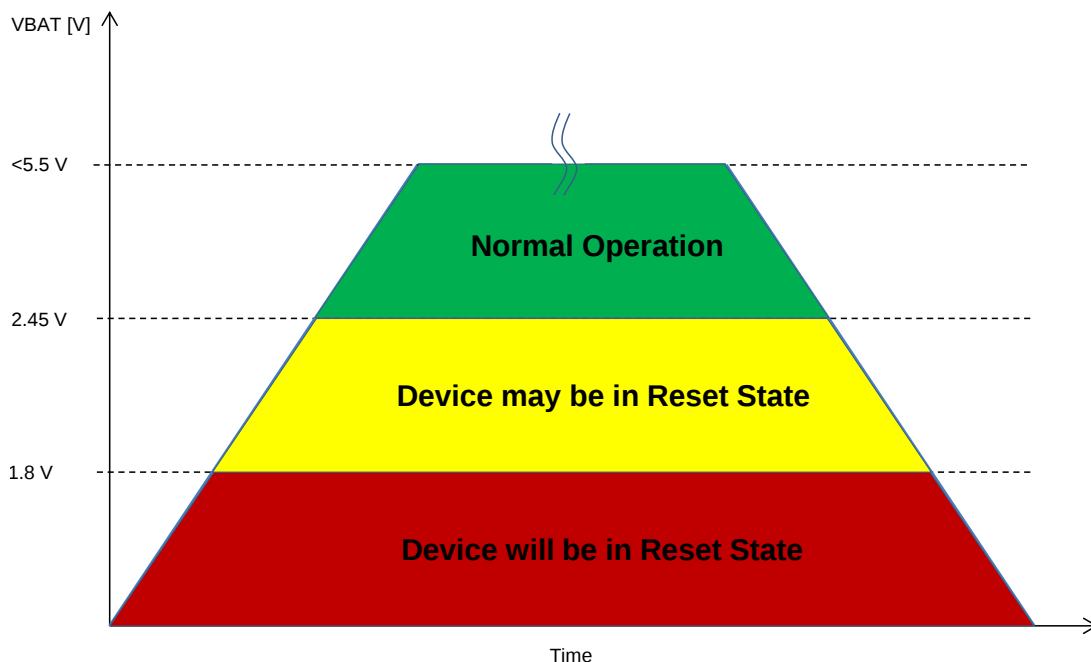
The decoupling capacitors for the power supplies should be placed close to the device terminals. For VBAT, IOVDD and AVDD, a small decoupling capacitor of 0.1  $\mu$ F should be placed close to the device terminals. Refer to [Figure 55](#) for the schematic.

### 9.2 Power Supply Sequencing

The power supplies should be started in the following order:

1. VBAT,
2. IOVDD,
3. AVDD.

The TAS2552 device has integrated reset circuitry, which requires that VBAT is above 2.45 V for the device to enter normal operation mode. [Figure 60](#) shows the internal thresholds and reset states. Normal operation mode is within the green area of [Figure 60](#).



**Figure 60. VBAT Reset Range**

When the supplies have settled, wait at least 1 ms after EN is set HIGH to operate the device. The above sequence should be completed before any I<sup>2</sup>C operation.

### 9.3 Boost Supply Details

The boost supply (VBAT) and associated passives need to be able to support the current requirements of the device. By default, the peak current limit of the boost is set to 2.5 A. Please see [Configurable Boost Current Limit \(ILIM\)](#) for information on changing the current limit. A minimum of a 10  $\mu$ F capacitor is recommended on the boost supply to quickly support changes in required current. Refer to [Figure 55](#) for the schematic.

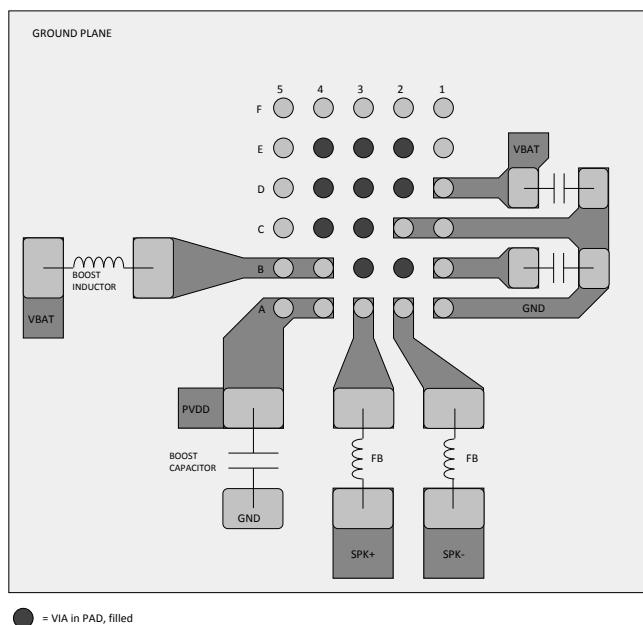
The current requirements can also be reduced by lowering the gain of the amplifier, or in response to decreasing battery through the use of the battery-tracking AGC feature of the TAS2552 described in [Battery Tracking AGC](#).

## 10 Layout

### 10.1 Layout Guidelines

- Place the boost inductor between VBAT and SW close to device terminals with no VIAS between the device terminals and the inductor.
- Place the capacitor between VREG and VBOOST close to device terminals with no VIAS between the device terminals and capacitor.
- Place the capacitor between VBOOST/PVDD and GND close to device terminals with no VIAS between the device terminals and capacitor.
- Do not use VIAS for traces that carry high current. These include the traces for VBOOST, SW, PVDD and the speaker OUT+, OUT-.
- Use epoxy filled vias for the interior pads.
- Connect VSENSE+, VSENSE- as close as possible to the speaker.
  - VSENSE+, VSENSE- should be connected between the EMI ferrite and the speaker if EMI ferrites are used on OUT+, OUT-.
  - VSENSE+, VSENSE- should be connected between the EMI ferrite and the EMI capacitor if EMI capacitors are used. EMI ferrites must be used if EMI capacitors are used on OUT+, OUT-.
- If the analog inputs, IN+ and IN-, are:
  - used, analog input traces should be routed symmetrically for true differential performance.
  - used, do not run analog input traces parallel to digital lines.
  - used, they should be ac coupled.
  - not used, they should be shorted together.
- Use a ground plane with multiple vias for each terminal to create a low-impedance connection to GND for minimum ground noise.
- Use supply decoupling capacitors as shown in [Figure 50](#) and [Figure 55](#) and described in [Power Supply Recommendations](#).
- Place EMI ferrites, if used, close to the device.

### 10.2 Layout Example



**Figure 61. TAS2552 Board Layout**

### 10.3 Package Dimensions

The TAS2552 uses a 30-ball, 0.4 mm pitch WCSP package. The die length (D) and width (E) correspond to the package mechanical drawing at the end of the datasheet.

| DIMENSION | D                  | E                  |
|-----------|--------------------|--------------------|
| Max       | 2885 $\mu\text{m}$ | 2605 $\mu\text{m}$ |
| Typ       | 2855 $\mu\text{m}$ | 2575 $\mu\text{m}$ |
| Min       | 2825 $\mu\text{m}$ | 2545 $\mu\text{m}$ |

## 11 Device and Documentation Support

### 11.1 Trademarks

All trademarks are the property of their respective owners.

### 11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TAS2552YFFR      | ACTIVE        | DSBGA        | YFF                | 30   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | TAS2552                 | <a href="#">Samples</a> |
| TAS2552YFFT      | ACTIVE        | DSBGA        | YFF                | 30   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | TAS2552                 | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TAS2552YFFR | DSBGA        | YFF             | 30   | 3000 | 180.0              | 8.4                | 2.76    | 3.02    | 0.83    | 4.0     | 8.0    | Q1            |
| TAS2552YFFT | DSBGA        | YFF             | 30   | 250  | 180.0              | 8.4                | 2.76    | 3.02    | 0.83    | 4.0     | 8.0    | Q1            |

## TAPE AND REEL BOX DIMENSIONS

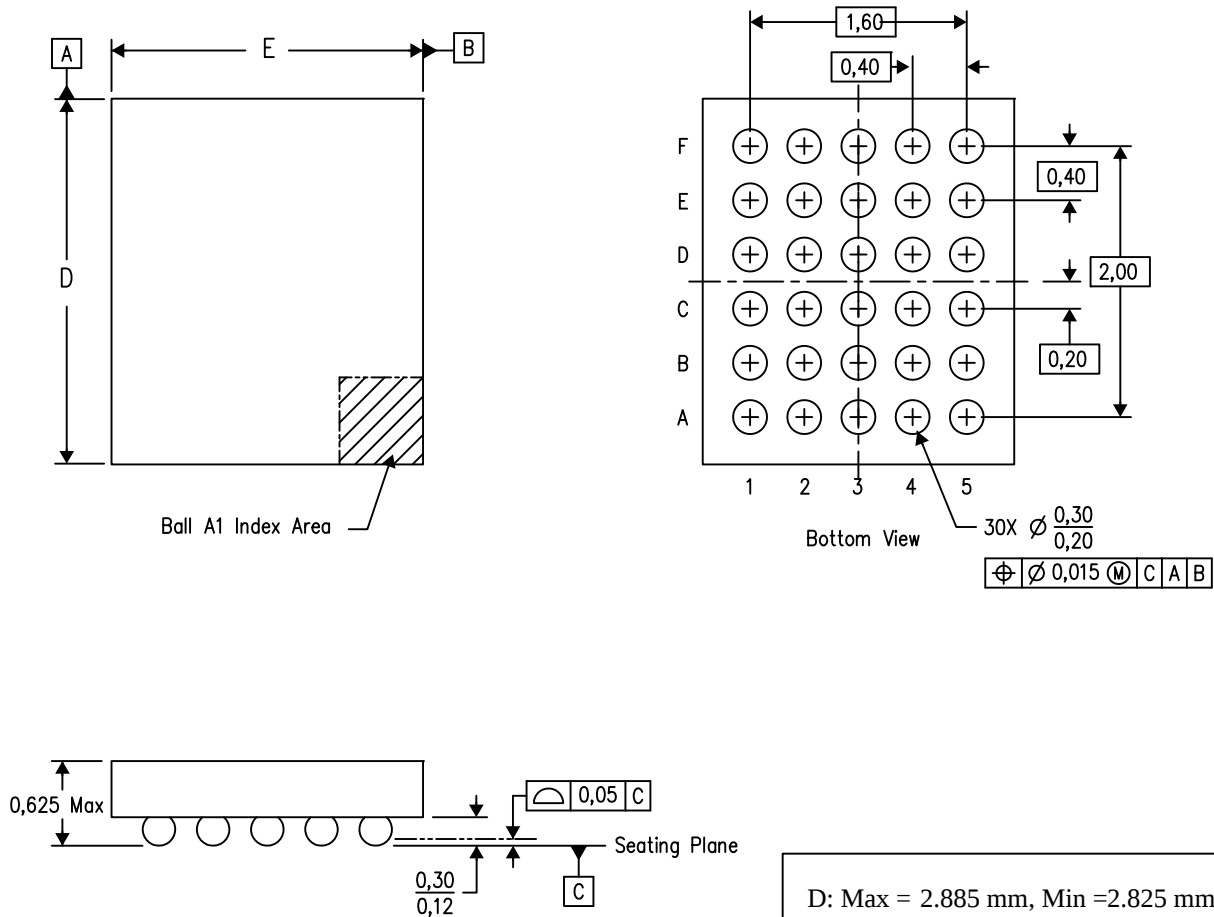


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TAS2552YFFR | DSBGA        | YFF             | 30   | 3000 | 182.0       | 182.0      | 20.0        |
| TAS2552YFFT | DSBGA        | YFF             | 30   | 250  | 182.0       | 182.0      | 20.0        |

YFF (R-XBGA-N30)

DIE-SIZE BALL GRID ARRAY



D: Max = 2.885 mm, Min = 2.825 mm

E: Max = 2.605 mm, Min = 2.545 mm

4207625-13/A0 12/13

## NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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| DLP® Products                | <a href="http://www.dlp.com">www.dlp.com</a>                                         |
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