JPEG Still Color Image Data Compression/Decompression LSI

KL5A71006

KAWASAKI LSI

PRODUCT FEATURE

1. INTRODUCTION

KL5A71006 is a single VLSI chip which can compress and decompress still color images based on JPEG (Joint Photographic Experts Group) standard baseline.

2. FEATURE

1) Fully compatible with JPEG standard baseline.
2) Automatic decodes and generation of some JPEG header data such as marker code.
3) Both Pixel and Host Buses with DMA interface.
4) Small plastic package.
5) Low operating power.
6) High cost performance.
7) Power save mode.
8) JPEG ASIC Core is available integrated with customer logic as KSC ASIC.

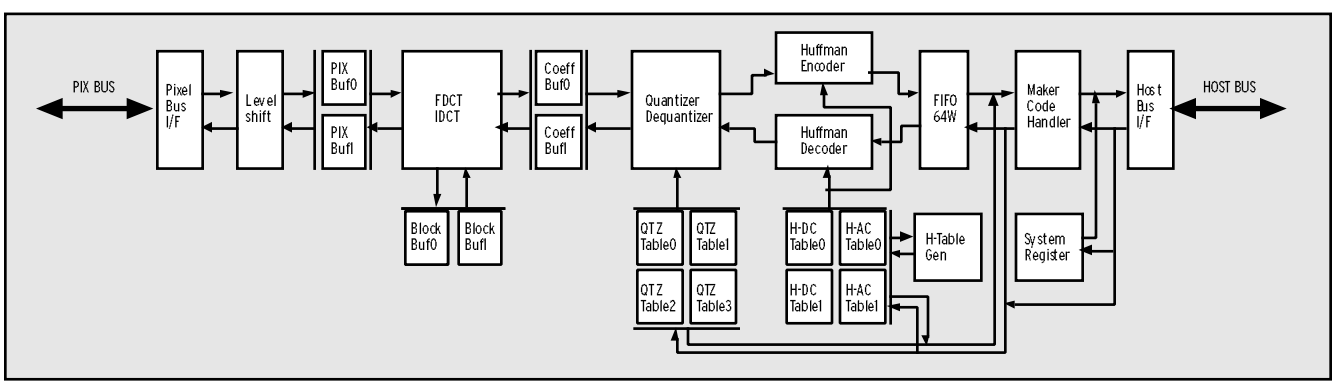
3. APPLICATION

Digital Still Camera, TV-conference, Scanner, Printer and other Multimedia Image Processing.

4. FUNCTIONALITY

1) JPEG baseline
   Compression/decompression processing.
   DCT compression, sequential coding.
   Huffman encode (available for 4 on-chip RAM for 2AC and 2DC table store).
   Support up to 4 color components.
   Quantize dequantize (available for 4 on-chip RAMs for 4 color components).
   Block interleave scanning input.
2) Pixel Bus (PB) 8/16 bits up to 4Mbyte/sec
3) Host Bus (HB) 8/16 bits up to 4Mbyte/sec
   Register access mode / DMA slave mode.
4) Internal FIFO 64 Words
5) Initial preparation
   System register setting.
   Load table data from CPU or coded data.
6) Error reporting function
7) Count up compressed data volume automatically, and stop data out when reached preset max value.
8) Header data processing
   Generate and decode code - SOI, DHT, DQT, SOF, SOS, EOI
   Decode only - DNL, DRI, APP0, COM, RST

BLOCK DIAGRAM



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PRODUCT SPECIFICATION

1. ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage V_{DD}	-0.3 ~ +4.6 V
Input Voltage V_{IN}	-0.3 ~ +7.3 V
Output Current I_{OUT}	30 mA
Storage Temperature T_{STG}	-55 ~ +125°C

2. RECOMMENDED OPERATING CONDITION

DC Supply Voltage V_{DD}	3.0 ~ 3.6 V
Ambient Temperature T_A	0 ~ +70°C
Maximum Clock rate	32 MHz
AC Power (Max)	0.36W

3. IMPLEMENTATION

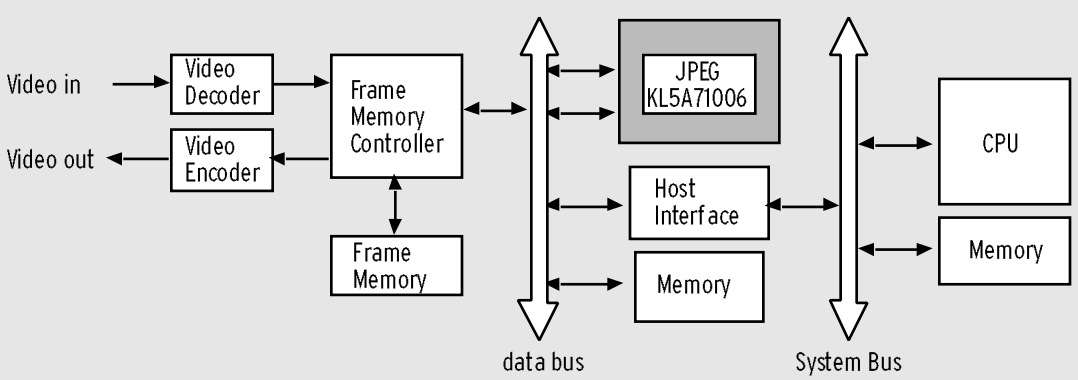
1) 0.5 µm CMOS double metal layer process.
2) Low power oriented ASIC library cell.
3) Top down design methodology of RTL coding with logic compilation CAD tool.
4) Extremely low stand-by power up to 500 µA.

4. PACKAGING

1) Plastic LQFP80
2) Size
   lead pitch 0.5 mm
   mold size 14 mm x 14 mm, thickness 1.7 mm
3) Pin assignment
   signal pin 55, test pin 9
   power/ground 16

SYSTEM APPLICATION

Example: PC board application



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