TOSHIBA POWER MOS FET MODULE SILICON N CHANNEL MOS TYPE (L^2-π-MOS III 4 IN 1)

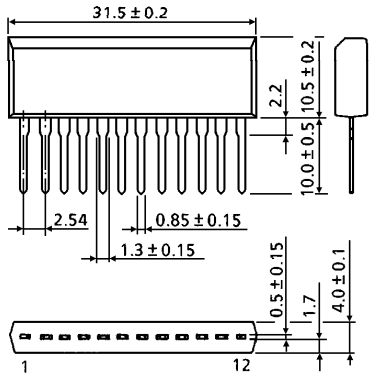
MP4401

HIGH POWER, HIGH SPEED SWITCHING APPLICATIONS.

HAMMER DRIVE, PULSE MOTOR DRIVE AND INDUCTIVE LOAD SWITCHING.

INDUSTRIAL APPLICATIONS

Unit in mm



MOS FET		DIODE	
1, 5, 8, 12	GATE	2, 4, 9, 11	ANODE
2, 4, 9, 11	DRAIN	3, 10	CATHODE
6, 7	SOURCE		

JEDEC	—
EIAJ	—
TOSHIBA	2-32C1D

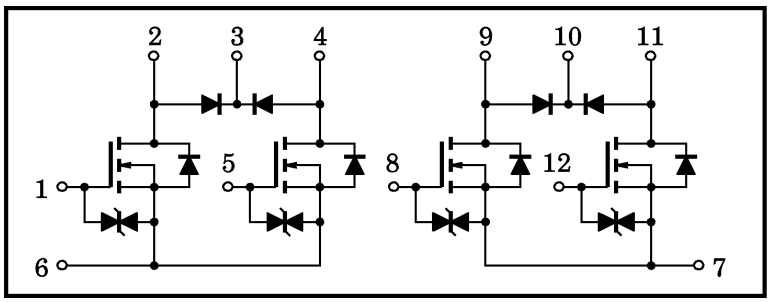
Weight : 3.9g

- 4-Volt Gate Drive Available
- Small Package by Full Molding (SIP 12 Pin)
- High Drain Power Dissipation (4 Devices Operation)
  : $P_T = 28W$ (Tc = 25°C)
- Low Drain-Source ON Resistance : $R_{DS\,(ON)} = 0.33\Omega$ (Typ.)
- Low Leakage Current : $I_{GSS} = \pm 10\mu A$ (Max.) ($V_{GS} = \pm 16V$)
  $I_{DSS} = 100\mu A$ (Max.) ($V_{DS} = 120V$)
- Enhancement-Mode : $V_{th} = 0.8 \sim 2.0V$ ($I_D = 1mA$)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Drain-Source Voltage		V_{DSS}	120	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current		I_D	3	A
Peak Drain Current		I_{DP}	12	A
Drain Power Dissipation (1 Device Operation)		P_D	2.2	W
Drain Power Dissipation (4 Devices Operation)	Ta = 25°C	P_T	4.4	W
	Tc = 25°C		28	
Channel Temperature		T_{ch}	150	°C
Storage Temperature Range		T_{stg}	−55~150	°C

ARRAY CONFIGURATION

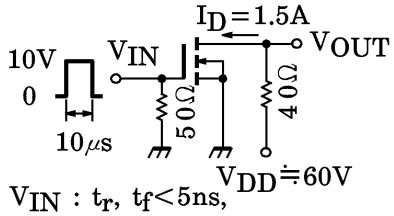


THERMAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MAX.	UNIT
Thermal Resistance of Channel to Ambient (4 Devices Operation, Ta = 25°C)	$\Sigma R_{th\,(ch\text{-}a)}$	28.4	°C / W
Thermal Resistance of Channel to Case (4 Devices Operation, Tc = 25°C)	$\Sigma R_{th\,(ch\text{-}c)}$	4.46	°C / W
Maximum Lead Temperature for Soldering Purposes (3.2mm from Case for 10s)	T_L	260	°C

This Transistor is an Electrostatic Sensitive Device. Please Handle with Caution.

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GSS}	$V_{GS} = \pm 16V$, $V_{DS} = 0$	—	—	±10	μA
Drain Cut-off Current		I_{DSS}	$V_{DS} = 120V$, $V_{GS} = 0$	—	—	100	μA
Drain-Source Breakdown Voltage		$V_{(BR)\,DSS}$	$I_D = 10mA$, $V_{GS} = 0$	120	—	—	V
Gate Threshold Voltage		V_{th}	$V_{DS} = 10V$, $I_D = 1mA$	0.8	—	2.0	V
Forward Transfer Admittance		$\|Y_{fs}\|$	$V_{DS} = 10V$, $I_D = 1.5A$	1.5	3.2	—	S
Drain-Source ON Resistance		$R_{DS\,(ON)}$	$I_D = 1.5A$, $V_{GS} = 4V$	—	0.42	0.74	Ω
		$R_{DS\,(ON)}$	$I_D = 1.5A$, $V_{GS} = 10V$	—	0.33	0.45	
Input Capacitance		C_{iss}	$V_{DS} = 10V$, $V_{GS} = 0$, f = 1MHz	—	350	—	pF
Reverse Transfer Capacitance		C_{rss}	$V_{DS} = 10V$, $V_{GS} = 0$, f = 1MHz	—	35	—	pF
Output Capacitance		C_{oss}	$V_{DS} = 10V$, $V_{GS} = 0$, f = 1MHz	—	155	—	pF
Switching Time	Rise Time	t_r	 V_{IN} : t_r, $t_f < 5ns$, Du. ≦ 1% ($Z_{OUT} = 50\Omega$)	—	6	—	ns
	Turn-on Time	t_{on}		—	12	—	
	Fall Time	t_f		—	40	—	
	Turn-off Time	t_{off}		—	100	—	
Total Gate Charge (Gate-Source Plus Gate-Drain)		Q_g	$I_D = 3A$, $V_{GS} = 10V$, $V_{DD} = 96V$	—	11	—	nC
Gate-Source Charge		Q_{gs}		—	7	—	
Gate-Drain ("Miller") Charge		Q_{gd}		—	4	—	

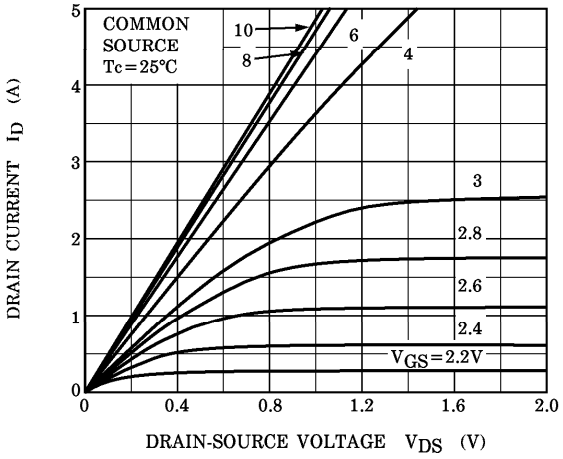
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Drain Reverse Current	I_{DR}	—	—	—	3	A
Peak Drain Reverse Current	I_{DRP}	—	—	—	12	A
Diode Forward Voltage	V_{DSF}	$I_{DR}=3A$, $V_{GS}=0$	—	−0.9	−1.5	V
Reverse Recovery Time	t_{rr}	$I_{DR}=3A$, $V_{GS}=0$, $dI_{DR}/dt=-20A/\mu s$	—	130	—	ns
Reverse Recovery Charge	Q_{rr}		—	0.14	—	μC

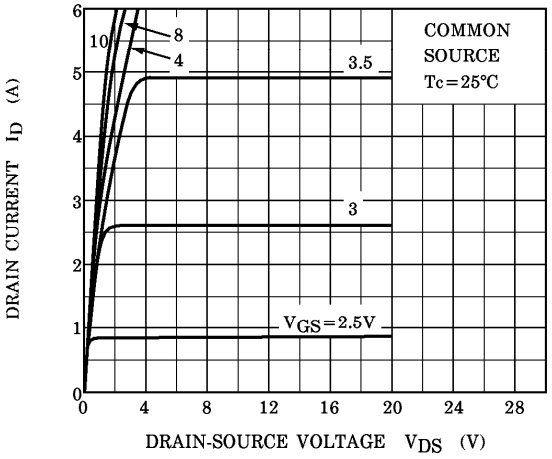
FLYBACK-DIODE RATINGS AND CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum Forward Current	I_{FM}	—	—	—	3	A
Reverse Current	I_R	$V_R=120V$	—	—	0.4	μA
Reverse Voltage	V_R	$I_R=100\mu A$	120	—	—	V
Forward Voltage	V_F	$I_F=0.5A$	—	—	1.8	V

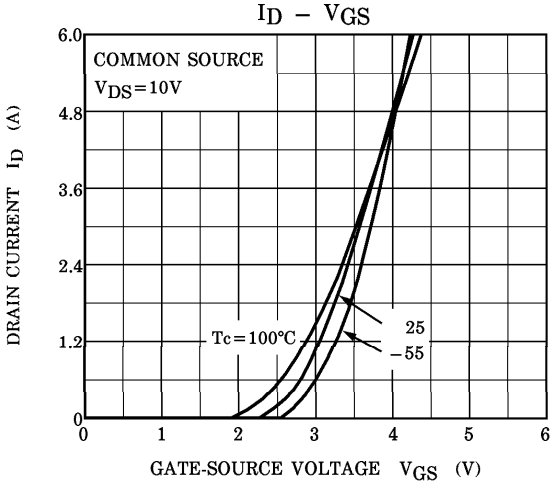
$I_D - V_{DS}$



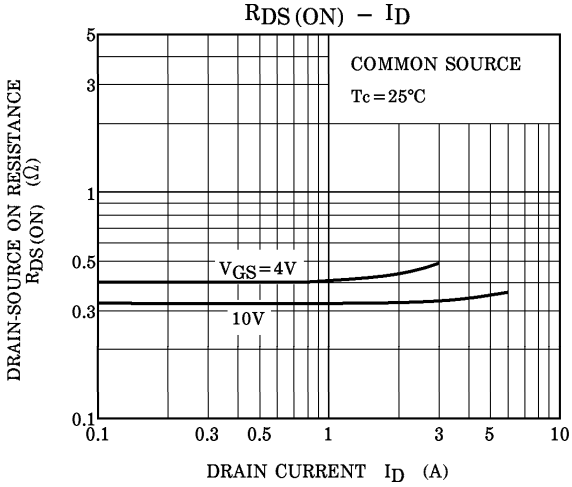
$I_D - V_{DS}$



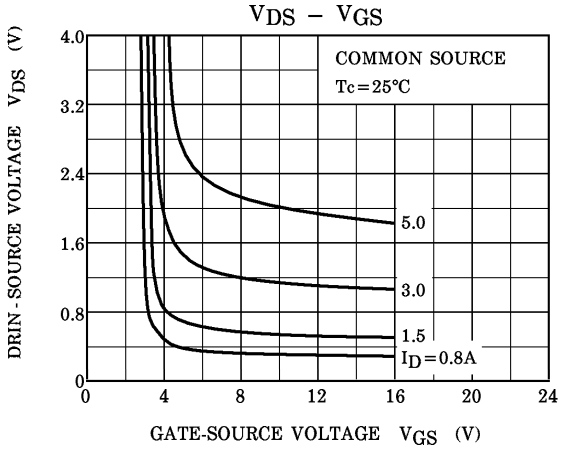
$I_D - V_{GS}$



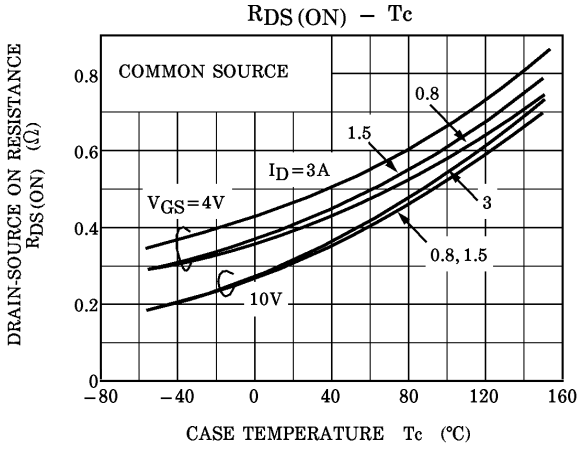
$R_{DS(ON)} - I_D$



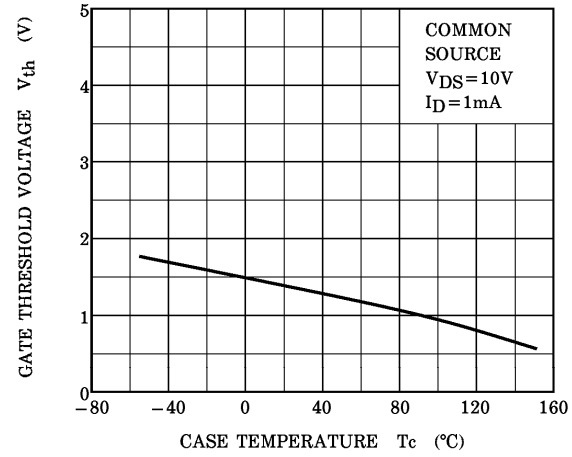
$V_{DS} - V_{GS}$



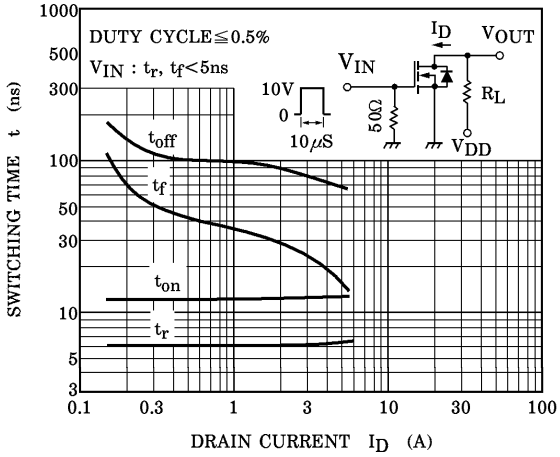
$R_{DS(ON)} - Tc$



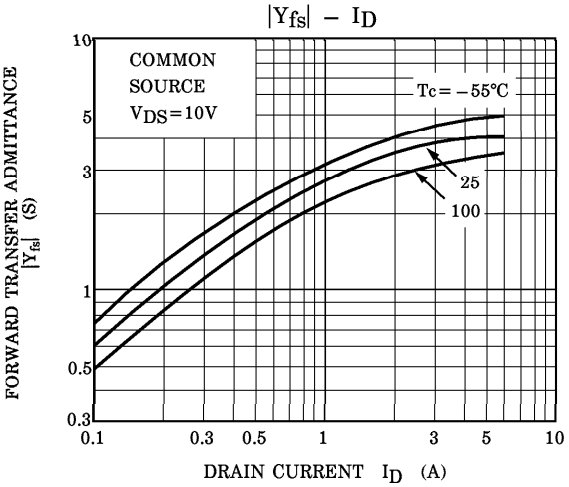
V_{th} – Tc



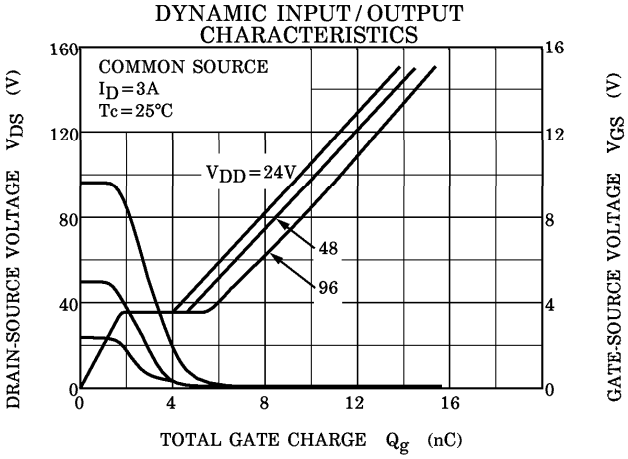
SWITCHING TIME – I_D



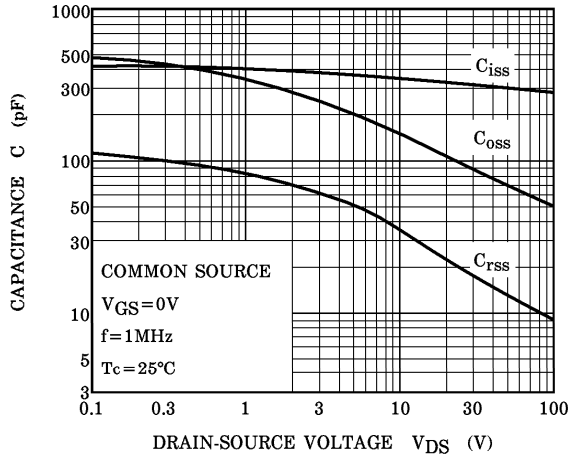
$|Y_{fs}|$ – I_D



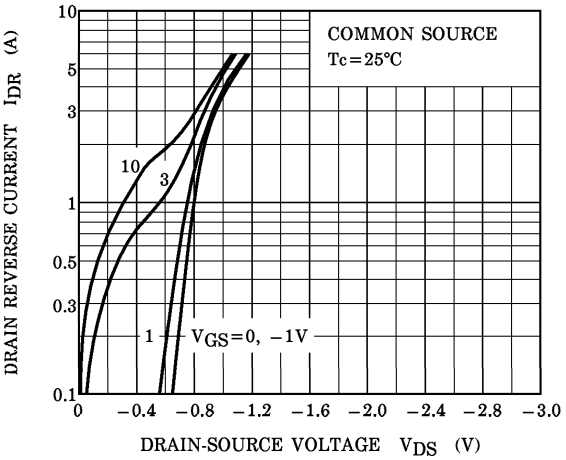
DYNAMIC INPUT / OUTPUT CHARACTERISTICS



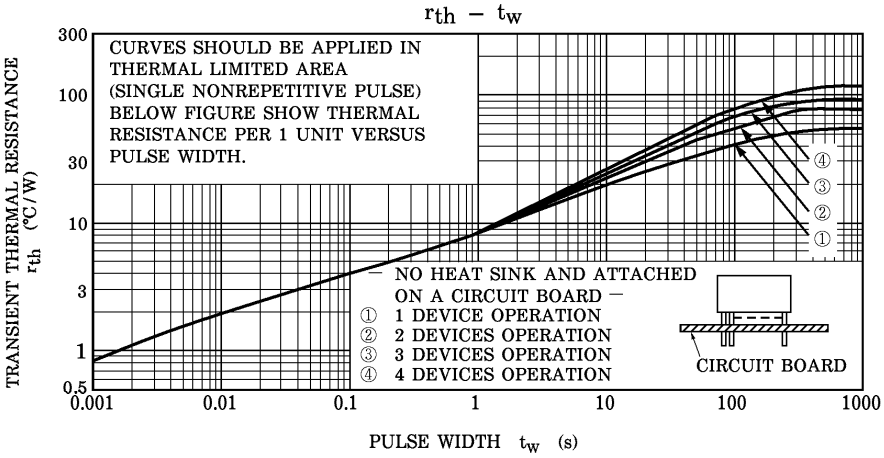
CAPACITANCE – V_{DS}



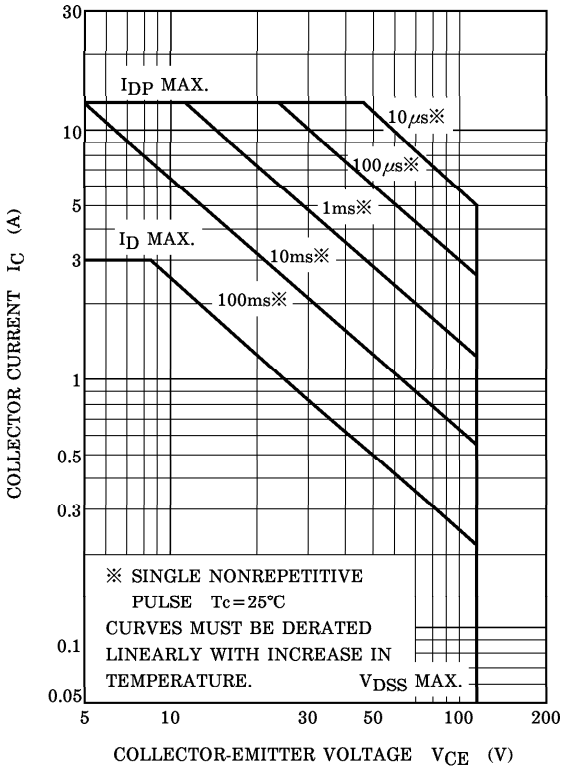
I_{DR} – V_{DS}



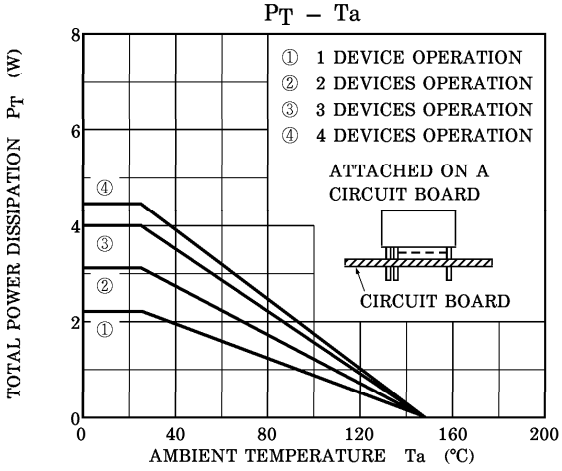
r_{th} – t_w



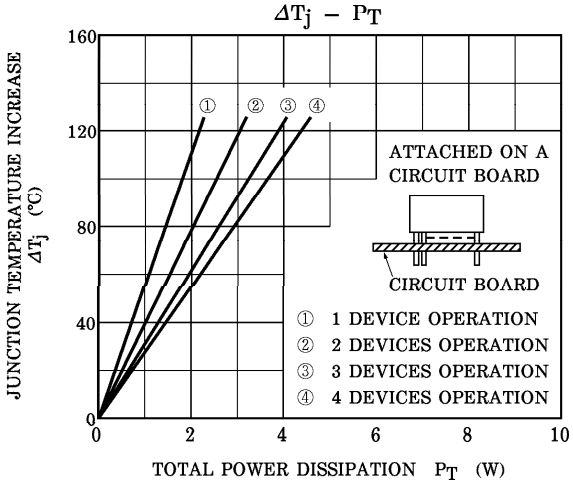
SAFE OPERATING AREA



P_T – Ta



ΔT_j – P_T



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