MAS6503

Piezoresistive Sensor Signal Interface IC

- **Optimized for Piezoresistive Pressure Sensors**
- **Very Low Power Consumption**
- **1.8V operation**
- **VDD Level Monitoring**
- **Ratiometric 24 Bit ΔΣ ADC**
- **SPI or I2C Bus with programmable I2C address**
- **EEPROM Calibration Memory**

DESCRIPTION

MAS6503 is a 24 bit Analog-to-Digital Converter (ADC), which employs a delta-sigma (ΔΣ) conversion technique. The resolution for a signal range of 373 mV is 17.4 bits.

MAS6503 is designed especially to meet the requirement for low power consumption, thus making it an ideal choice for battery powered systems. Overall current consumption values of 18.3 µA (one conversion in a second at maximum resolution) or less can be achieved. The minimum supply voltage is as low as 1.8V.

MAS6503 has an on-chip decimator filter that processes the output of the third order ΔΣ – modulator, giving a high resolution conversion result. The ADC also has four selectable input signal ranges with eight optional offset levels.

A 4-wire SPI or 2-wire I2C bus compatible serial bus is used for configuring conversion parameters, starting a conversion and reading out the A/D conversion result. The I2C address is programmable to allow several sensors to be connected to the same bus.

MAS6503 has one input channel suitable for a piezoresistive pressure sensor. In addition to pressure measurement the device can be configured for temperature measurement. The VDD level monitoring feature is also useful especially in battery operated systems.

The 256-bit EEPROM memory is available for storing trimming and calibration data on chip. An application optimized compensation algorithm can be used by the host system for optimal performance.

FEATURES

- Low Standby Current Consumption: 10 nA Typ
- Very Low Supply Current: 0.9 µA…18.3 µA Typ
- Supply Voltage: 1.8 V…3.6 V
- Ratiometric ΔΣ Conversion
- Selectable Input Signal Ranges (VDD=2.7V):
  - 373, 253, 172 and 115 mV_{PP}
- Selectable Offset Options (VDD=2.7V):
  - ±126, ±86, ±57 and ±40 mV
- Selectable Sensor Resistance Values
  - 2, 2.5, 3, 3.5, 4, 4.5, 5 and 10 kΩ
- Over Sampling Ratio: 4096, 2048, 1024, 512, 256
- Internal System Clock Signal 250 kHz
- Conversion Times 1.41 ms…16.77 ms Typ
- 2-Wire Serial Data Interface (I2C Bus) with programmable I2C address
- 256 Bit EEPROM Memory

APPLICATIONS

- Calibrated Piezoresistive Pressure Modules
- Temperature measurement
- Battery Powered Systems
- Low Frequency Measurement Applications
- Current/Power Consumption Critical Systems
- Navigation systems.
- Industrial and Process Control Applications in Noisy Environments

BLOCK DIAGRAM

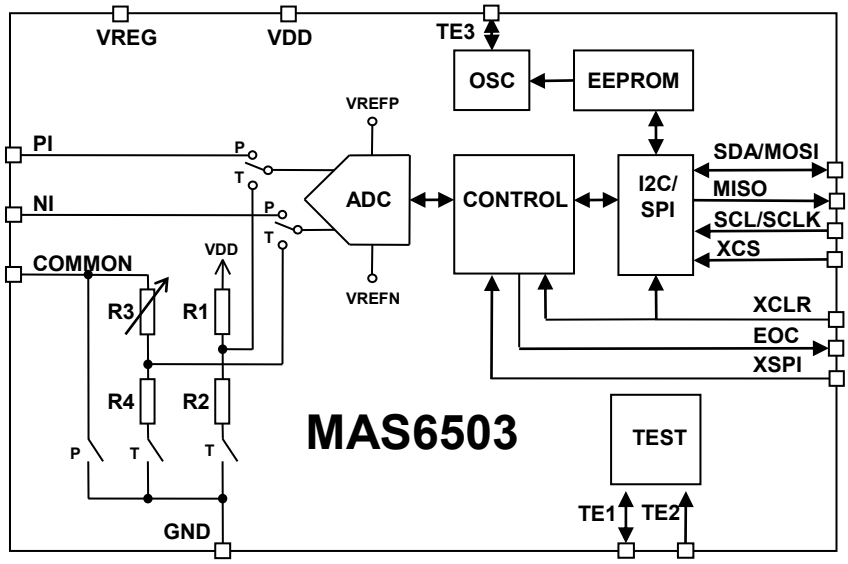


Figure 1. MAS6503 block diagram

FUNCTIONAL DESCRIPTION

MAS6503 has one input channel suitable for a piezoresistive pressure sensor. There are four input signal conversion ranges and eight offset values selectable to meet various sensor signal ranges.

In addition the device can be configured for temperature measurement. The temperature is typically needed for temperature compensation and indication purposes. The device supports eight different sensor bridge resistance values from 2.0kΩ up to 10kΩ.

MAS6503 also features VDD level monitoring which is useful especially in battery operated systems. The VDD level information could be used for battery energy capacity indication, switching between different power modes in the system and also for VDD dependency compensation purposes. In the VDD level monitoring mode the on-chip regulator need to be disabled.

The AD-converter is ratiometric offering possibility to run measurements at varying supply voltage conditions. However the device has also an optional voltage regulator with four selectable output voltage options 1.8V, 2.2V, 2.6V and 2.9V. The on-chip voltage regulator offers additional regulation against supply noise and variations. Note that in the VDD level monitoring mode the on-chip voltage regulator needs to be disabled.

The AD-converter resolution is selected by the over sampling ratio (OSR) setting. Higher OSR corresponds to higher resolution but also longer conversion time.

MAS6503 has an internal clock oscillator making an external clock unnecessary. To save power the clock oscillator and the optional voltage regulator are turned on only when a conversion is running. The oscillator frequency is factory trimmed to 500 kHz using a 6-bit register. The converter runs from a system clock which is half of the oscillator frequency. In a specific test mode an external clock signal can be also used when connected to the OSC pin.

Communication with MAS6503 is handled by the serial interface compatible with either a bi-directional 2-wire I2C bus or a 4-wire SPI bus. The XSPI pin is for selecting which bus type is used.

In addition to a fixed I2C device address the MAS6503 has also a programmable device address. It has been factory programmed to same value as the fixed device address of MAS6503. When unique device address is needed it can be programmed to EEPROM address ($DE/5E_{HEX}$)..

Note: The 2-wire I2C bus of MAS6503 supports only basic I2C bus communication protocol but not for example 10-bit addressing, arbitration and clock stretching features of the I2C bus specification.

The 256-bit EEPROM memory is available for storing trimming and calibration data on chip. Two of the EEPROM bytes are reserved for dedicated function. One is for internal clock oscillator trimming value and the another one for programmable I2C address value but the remaining 240 bits are free for storing calibration and other information.

FUNCTIONAL DESCRIPTION

The calibrated measurement value calculations need to be done outside in the host system by utilizing the stored calibration coefficient data.

To avoid modification of the EEPROM by mistake there is an EEPROM write enable bit (EWE) in the EEPROM Control Register ($E6/66_{HEX}$) which needs to be set high (1) before any changes can be done to the EEPROM.

The XCLR pin can be used to hard reset the device including the serial communication. However device reset is possible also via serial bus using the reset register. Despite of on chip power on reset (POR) circuit it is recommended to reset the device manually after every power up to guarantee proper register settings after any VDD rise conditions.

The EOC pin indicates if a conversion has finished and the result is ready to be read from the memory via the serial interface. Using the EOC signal is not necessary since it is alternatively possible to wait at least maximum conversion time period before reading out the result.

ABSOLUTE MAXIMUM RATINGS

All Voltages with Respect to Ground

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	5.0	V
Voltage Range for All Pins			-0.3	V_{IN} + 0.3	V
Latchup Current Limit	I_{LUT}	For all pins, test according to JESD78A.	-100	+100	mA
Junction Temperature	T_{Jmax}			+ 150	°C
Storage Temperature	T_S	Note 1	- 55	+125	°C

Note 1: See EEPROM memory data retention at hot temperature. Storage or bake at hot temperatures will reduce the wafer level trimming and calibration data retention time.
Note: The absolute maximum rating values are stress ratings only. Functional operation of the device at conditions between maximum operating conditions and absolute maximum ratings is not implied and EEPROM contents may be corrupted. Exposure to these conditions for extended periods may affect device reliability (e.g. hot carrier degradation, oxide breakdown). Applying conditions above absolute maximum ratings may be destructive to the devices.
Note: This is a CMOS device and therefore it should be handled carefully to avoid any damage by static voltages (ESD).

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	Without internal regulator With internal regulator	1.8 V_{REG}+0.1V	2.7	3.6 3.6	V
Operating Temperature	T_A		-40	+25	+85	°C
EEPROM Write Temperature	T_A	Note 1	+10	+25	+40	°C

Note 1: EEPROM write operation is recommended to be done at room temperature

ELECTRICAL CHARACTERISTICS

T_A = -40ºC to +85ºC, VDD = 2.7V, Typ T_A = 27ºC, Typ VDD = 2.7 V, R_{SENSOR} = 4.5kΩ unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Regulator Output Voltage	V_{REG}	VDD=V_{REG}+0.1V V_{REG}=1.8V V_{REG} =2.2V V_{REG} =2.6V V_{REG} =2.9V	 -3.5% -3.5% -3.5% -3.5%	 1.8 2.2 2.6 2.9	 +3.5% +3.5% +3.5% +3.5%	V
Standby current	I_{STBY}	All inputs at VDD, no load. Note 1.		0.01	0.1	µA
Conversion Current Consumption	I_{DD_CONV}	Pressure mode, Reg ON (V_{REG} =1.8V) Temperature mode, Reg ON (V_{REG} =1.8V) Pressure mode, Reg OFF Temperature mode, Reg OFF VDD monitor mode, Reg OFF		760 600 710 560 760	1200 1000 1100 900 1200	µA
Peak Supply Current During Pressure Measurement	I_{PEAK_P}	VDD = 2.7 V, R_{SENSOR} = 4.5 kΩ		1.39		mA
Peak Supply Current During Temperature Measurement	I_{PEAK_T}	VDD = 2.7 V, R_{SENSOR} = 4.5 kΩ		0.75		mA

Note 1. Leakage current may increase if digital input voltages are not close to VDD (logic level high) or GND (logic level low). Also setting XCS low activates the EEPROM memory regardless of the XSPI setting and the device consumes 20µA …30µA current. To minimize current consumption XCS should be set low only during time periods when the device is used during SPI communication.

ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C, VDD = 2.7V, Typ T_A = 27°C, Typ VDD = 2.7 V, R_{SENSOR} = 4.5kΩ unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Oscillator Frequency	OSC		460	500	540	kHz
Internal System Clock Frequency	MCLK	Normal clock (DIV=0, ENDIV=0) DIV=0, ENDIV=1 DIV=1, ENDIV=0 DIV=1, ENDIV=1	230 115 57.5 28.7	250 125 62.5 31.25	270 135 67.5 33.8	kHz
Average ADC Current in Pressure Measurement (incl. sensor current)	I_{AVG_P}	1 conversion/s, Reg ON (V_{REG} =1.8V) Normal clock (DIV=0, ENDIV=0) T_A = 27°C OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256		 17.8 9.1 4.8 2.6 1.5	 25.2 12.9 6.7 3.7 2.1	µA
Average ADC Current in Temperature Measurement (incl. sensor current	I_{AVG_T}	1 conversion/s, Reg ON (V_{REG} =1.8V) Normal clock (DIV=0, ENDIV=0) T_A = 27°C OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256		 11.1 6.8 3.4 1.8 0.9	 17.8 10.4 5.3 2.7 1.4	µA
Average ADC Current in VDD Level Monitoring Measurement	I_{AVG_VDD}	1 conversion/s, Reg OFF Normal clock (DIV=0, ENDIV=0) T_A = 27°C OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256		 12.7 6.5 3.4 1.9 1.1	 20.1 10.3 5.4 2.9 1.7	µA
Conversion Time	t_{CONV}	Normal clock (DIV=0, ENDIV=0) T_A = 27°C OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256		 16.77 8.58 4.48 2.43 1.41	 18.23 9.32 4.87 2.64 1.53	ms
VDD Rise Time for Proper Power On Reset (POR)	t_{VDD_RISE}	Note 1.			1	ms

Note 1. It is also recommended to reset the device manually either by XCLR pin or using reset register after every power up (VDD rise). In case the VDD rise time is longer than specified here the device has to be kept in a reset during power up by the XCLR pin (XCLR=low). Violating this may risk EEPROM memory integrity. See APPLICATION INFORMATION for examples of external POR circuits.

ELECTRICAL CHARACTERISTICS

T_A = -40ºC to +85ºC, VDD = 2.7V, Typ T_A = 27ºC, Typ VDD = 2.7 V, R_{SENSOR} = 4.5kΩ unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution	V_N	Pressure mode, ISR=373mV, V_{IN}=0V Reg OFF OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256 Note 1.		 2.25 (17.4) 3.02 (16.9) 4.28 (16.4) 5.63 (16.0) 9.16 (15.3)		 μV_{RMS} (bit)
Linearity	INL_{BIT}	ISRLIN = 298 mV Reg OFF OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256 Note 2.		 15.1 15.1 14.9 14.7 14.3		 Bit
VDD Sensitivity in Pressure Mode	VDD_{SENSP}	Pressure mode, V_{REG} =1.8V VDD step 1.9V ⇒ 3.6V OSR=4096 Note 3.		 0.00017		 %FS/V
VDD Sensitivity in Temperature Mode	VDD_{SENST}	Temperature mode, V_{REG} =1.8V VDD step 1.9V ⇒ 3.6V OSR=4096 Note 3.		 0.077		 %FS/V

Note 1. Resolution in bits is calculated as follows: V_{N_BIT}=log(ISR / V_N)/log(2) when V_N is the RMS noise voltage.

Note 2. Linearity in bits is calculated as follows: INL_{BIT}=log(CODELIN / INL)/log(2) when integral nonlinearity (INL) is calculated from best fit line to linear input signal range containing 21 pcs analysis points.

Note 3. VDD sensitivity in %FS/V calculated as follows: VDD_{SENS} =100%*((CODE @ VDD_{MAX}) – (CODE @ VDD_{MIN}))/CODEFS/(VDD_{MAX} - VDD_{MIN}) where VDD_{MAX}=3.6V and VDD_{MIN}=1.9V when the regulator is enabled (ENREG=1). and set to V_{REG}=1.8V (REGEB=00).

ELECTRICAL CHARACTERISTICS

T_A = -40ºC to +85ºC, VDD = 2.7V, Typ T_A = 27ºC, Typ VDD = 2.7 V, R_{SENSOR} = 4.5kΩ unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Signal Range	ISR	VDD=2.7V		373 253 172 115		mV
Linear Input Signal Range	ISRLIN	VDD=2.7V 10%...90% (80%) of ISR		298 202 138 92		mV
Input Signal Offset	OFFSET	VDD=2.7V		±126 ±86 ±57 ±40 0		mV
Full Scale Output Code Range Values	CODEFS	OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256	0 0 0 0 0		14671872 14663680 14647296 1826816 227328	
Linear Range Output Code Values (10%...90% of Full Scale Code Range)	CODELIN	OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256	1467187 1466368 1464730 182682 22733		13204685 13197312 13182566 1644134 204595	
Temperature Measurement Resistors	R_1 R_2 R_4		-30%	13900 30600 30600	+30%	Ω
	R_3	R_{SENSOR} = 2 kΩ R_{SENSOR} = 2.5 kΩ R_{SENSOR} = 3 kΩ R_{SENSOR} = 3.5 kΩ R_{SENSOR} = 4 kΩ R_{SENSOR} = 4.5 kΩ R_{SENSOR} = 5 kΩ R_{SENSOR} = 10 kΩ	-30%	11900 11400 10900 10400 9900 9400 8900 3900	+30%	Ω
Temperature Coefficient of Temperature Measurement Resistors	TC_R			-180		ppm/°C
EEPROM size		Note 1.		256		bit
EEPROM data write time		Note 2.			16	ms
EEPROM data retention		T_A = +85 °C T_A = +125 °C Note 3	10	24 1		years

Note 1. 16 bits out of 256 bits are reserved for internal oscillator trimming and programmable I2C device address. The remaining 240 bits can be freely used for storing calibration coefficients and other data.
Note 2. There should be at least a 16ms delay after each EEPROM write since EEPROM programming can take up to 16ms.
Note 3. Data retention values apply when extended EEPROM tests are done. Please contact Micro Analog Systems Oy if the data retention values here need to be guaranteed by comprehensive EEPROM testing.

Digital inputs

T_A = -40°C to +85°C, VDD = 2.7V, Typ T_A = 27°C, R_P = 4.7kΩ (I2C bus pull up) unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH}		80% VDD		100% VDD	V
Input Low Voltage	V_{IL}		0% VDD		20% VDD	V
Serial Bus Clock Frequency	f_{SCL}	I2C bus SPI bus			400 2	kHz MHz
XCLR Reset Pulse Length	t_{XCLR}	XCLR low pulse	200			ns
Wait time after reset	t_{RESET_WAIT}	Note 1.	20			µs
XCLR Pin Pull Up Current	I_{PULL_UP}	XCLR=0V		-8		µA

Note 1. This is the necessary wait time after reset to allow MAS6503 reading the programmable I2C device address from the EEPROM

Digital outputs

T_A = -40°C to +85°C, VDD = 2.7V, Typ T_A = 27°C, R_P = 4.7kΩ (I2C bus pull up) unless otherwise noted

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output high voltage	V_{OH}	I_{Source}=0.6mA	80% VDD		100% VDD	V
Output low voltage	V_{OL}	I_{Sink}=0.6mA	0% VDD		20% VDD	V
Signal rise time (from 10% to 90%)	t_r	EOC pin, C_L=50pF SDA pin, C_B=50pF		14 550		ns
Signal fall time (from 90% to 10%)	t_f	EOC pin, C_L=50pF SDA pin, C_B=50pF		11 11		ns

OPERATING MODES

After connecting the power supply the device is reset by on-chip power on reset (POR) circuit and then set to standby mode. The POR circuit works only for supply voltage rise rates faster than max 1ms rise time. To provide reset in all supply rise conditions it is recommended to reset the device manually after every power up (VDD rise) either via the XCLR pin or via the serial bus using the reset register.

MAS6503 has three operating modes, pressure, temperature and VDD level monitoring mode. In the pressure mode the pressure dependent sensor bridge voltage is connected to the ADC input. In the temperature measurement mode the resistive sensor bridge is connected into a Wheatstone bridge configuration together with four internal resistors (see Temperature Measurement Configuration in the Application Information chapter). The formed Wheatstone bridge output voltage is connected to the ADC input. It is proportional to absolute temperature. In the VDD level monitoring mode an internal bandgap voltage is connected to the ADC input but the ratiometric ADC references are allowed to follow supply voltage by disabling the internal regulator. The supply voltage monitoring can be useful feature especially in battery operated systems.

Switching between pressure, temperature and VDD level monitoring modes is done via the single ADC control register. The measurement configuration includes selection of over sampling ratio, input signal range, offset and sensor resistance. By writing two 8-bit configuration data to two ADC control registers a new A/D conversion is started. MAS6503 includes a 256-bit EEPROM memory for storing trimming and calibration data on chip. 16-bits of EEPROM are reserved for internal oscillator trimming and programmable I2C device address but the remaining 240-bits are free for calibration and other data.

The stored calibration data should comprise of calibration and temperature compensation coefficients which can be used to calculate accurate calibrated pressure and temperature measurement results from the non-calibrated measurement results. All calculations need to be done in the external micro controller unit (MCU).

A calibrated MAS6503 sensor system is operated as illustrated in figure 2. The calibration and compensation coefficients need to be read to the MCU memory only once. From each pair of pressure and temperature measurements results the accurate pressure and temperature values are then calculated by using the external MCU.

All communication with MAS6503 is done using a 4-wire SPI bus or a 2-wire I2C bus. Starting an A/D conversion, reading out the conversion result and reading and writing data from and to the EEPROM memory are all accomplished via serial bus communication.

In addition to the serial bus the digital interface includes also end-of-conversion (EOC) and master reset (XCLR) pins. See Serial interface in the following Serial Data Interface Control chapter.

OPERATING MODES

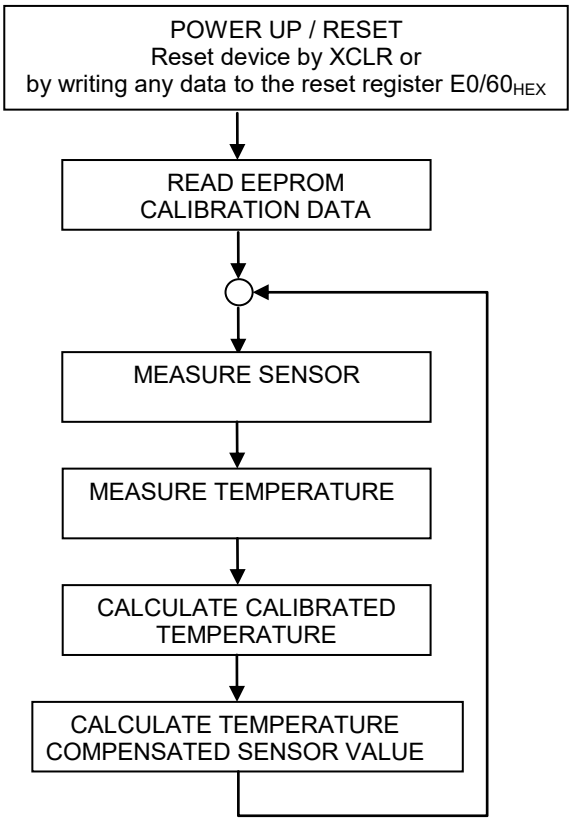


Figure 2. Flow chart for a calibrated MAS6503 sensor system

REGISTER AND EEPROM DATA ADDRESSES

Table 1. Register and EEPROM data addresses

A7	A6	A5	A4	A3	A2	A1	A0	I2C BUS (HEX)	SPI BUS (HEX) W=write R=read	Description	Note
A7	1	0	0 … 1	0 … 1	0 … 1	0 … 0	0 … 1	C0 … DD	W: 40…5D R: C0…DD	EEPROM; free for any data	E
A7	1	0	1	1	1	1	0	DE	W: 5E R: DE	Programmable I2C Device Address	E
A7	1	0	1	1	1	1	1	DF	W: 5F R: DF	EEPROM; Oscillator frequency trim data	E+T
A7	1	1	0	0	0	0	0	E0	W: 60 R: E0	Reset register; no data, only addressed for reset	R
A7	1	1	0	0	0	0	1	E1	W: 61 R: E1	Test register	R
A7	1	1	0	0	0	1	0	E2	W: 62 R: E2	Measurement control register 1	R
A7	1	1	0	0	0	1	1	E3	W: 63 R: E3	Measurement control register 2	R
A7	1	1	0	0	1	0	0	E4	W: 64 R: E4	Oscillator frequency control register	R+T
A7	1	1	0	0	1	0	1	E5	W: 65 R: E5	EEPROM data input register	R
A7	1	1	0	0	1	1	0	E6	W: 66 R: E6	EEPROM write enable register	R
A7	1	1	0	0	1	1	1	E7	W: 67 R: E7	1st (MSB) byte of the conversion result	R
A7	1	1	0	1	0	0	0	E8	W: 68 R: E8	2nd (ISB) byte of the conversion result	R
A7	1	1	0	1	0	0	1	E9	W: 69 R: E9	3rd (LSB) byte of the conversion result	R
A7	1	1	0	1	0	1	0	EA	W: 6A R: EA	Status register for EEPROM	R
A7	1	1	0	1	0	1	1	EB	W: 6B R: EB	Regulator output voltage control register	R

E = EEPROM, R= Register, T = Trim data

Note: When using the SPI serial interface the register address bit A7 is also used for selecting write (A7= 0) or read (A7=1) operation. For the I2C interface address bit A7 = 1.

Note: The programmable I2C device address register (DE_{HEX}) has been factory programmed to value EA_{HEX} (%11101010) which is the same as the hard wired device address of MAS6503. When unique device address is needed it can be programmed to this register.

REGISTER AND EEPROM DATA ADDRESSES

MAS6503 includes a 32 bytes (256 bits) EEPROM data memory and twelve registers. Two bytes (16 bits) of EEPROM are reserved for internal 500 kHz oscillator frequency trim and programmable I2C device address data but the remaining 30 bytes (240 bits) are free for storing sensor calibration and other data. See table 1 on the previous page for register and EEPROM data addresses.

In the SPI serial bus the address bit A7 selects between write (A7=0) and read (A7=1) operation. In the I2C serial bus A7 is always high (A7=1) and selection between write and read operation is done with the LSB bit of the I2C device address. See table 9 in chapter SERIAL DATA INTERFACE CONTROL. The MAS6503 has both hard wired and programmable I2C device addresses. The programmable device address is factory programmed to value EA_{HEX} (%11101010) which is the same as the hard wired device address of MAS6503. When unique device address is needed it can be programmed to the Programmable I2C Device Address register ($DE_{HEX}/5E_{HEX}$). The MAS6503 will respond to both hard wired and programmed I2C device addresses.

MAS6503 has one trim register: Oscillator frequency control register ($E4/64_{HEX}$). This is marked with “R+T” in table 1. In the EEPROM there is specific Oscillator frequency trim data address ($DF/5F_{HEX}$) reserved for permanent storage of the trim value. This is marked with “E+T” in table 1. The internal 500 kHz oscillator frequency trim value is automatically read from EEPROM in the beginning of each conversion when this feature is enabled in the Test register ($E1/61_{HEX}$). When disabled it is possible to test different trim data in the trim registers before trimming value is found and stored into the EEPROM. Note that Oscillator frequency trim value has been factory calibrated and stored into the EEPROM.

Reset register ($E0/60_{HEX}$) does not contain any data. Any dummy data written to this register forces a reset. A reset initializes all control registers (addresses $E1_{HEX}$…EB_{HEX}) to a zero value.

Test register ($E1/61_{HEX}$) is mainly used for testing and trimming purposes. It defines whether the internal oscillator frequency trim data is taken from the EEPROM (default setting) or from the registers. However if an external clock signal is used the test register is needed for selecting the external clock signal. See the Test register description for details.

There are two Measurement control registers, first ($E2/62_{HEX}$) and second ($E3/63_{HEX}$) which are used for configuring and starting an A/D conversion.

The Oscillator frequency control register ($E4/64_{HEX}$) is used only during internal clock oscillator trimming. During trimming there is searched register value which gives closest to the nominal 500 kHz oscillator frequency. However the internal clock oscillator frequency is trimmed by MAS during wafer level testing and the trimming value is stored into the Oscillator frequency trim data EEPROM address ($DF/5F_{HEX}$). Thus there is no need to adjust the factory stored clock oscillator trimming value. In normal operation the trim value is automatically read from the EEPROM memory in the beginning of each conversion.

EEPROM write enable register ($E6/66_{HEX}$) is used for enabling EEPROM write (EWE bit = 1) since by default the EEPROM is write protected (EWE bit = 0).

The 24-bit A/D conversion result (sensor, temperature or VDD level) is stored into three registers $E8_{HEX}$ (MSB, most significant byte), $E9_{HEX}$ (ISB, intermediate significant byte), EA_{HEX} (LSB, least significant byte).

EEPROM status register ($EA/6A_{HEX}$) reflects the EEPROM error correction status. This register can be used to verify that the EEPROM operation has finished without errors.

Regulator output voltage control register ($EB/6B_{HEX}$) defines regulator output voltage when the internal regulator is enabled.

PROGRAMMABLE I2C DEVICE ADDRESS (DE/5E$_{HEX}$)

The MAS6503 has both hard wired and programmable I2C device addresses. The programmable I2C device address is factory programmed to value EA $_{HEX}$ (%11101010) which is the same as the hard wired device address of MAS6503. When unique device address is needed it can be programmed to the Programmable I2C Device Address register (DE$_{HEX}$/5E$_{HEX}$). However note that the hard wired address cannot be changed and that the MAS6503 will respond to both hard wired and programmed I2C device addresses.

RESET REGISTER (E0/60$_{HEX}$)

This register is used to reset all control registers (addresses E1$_H$…EB$_H$) to a zero value. There are no data bits in this register. However it is necessary to write dummy data to this register to make a reset.

The reset will take place immediately after any data has been written to the address E0/60$_{HEX}$ via the I2C or SPI interface.

TEST REGISTER (E1/61$_{HEX}$)

The Test register is mainly for a testing purpose. In normal operation the Test register default value is 00$_{HEX}$ and the internal clock oscillator frequency 500 kHz. The system runs from system clock frequency MCLK which is normally half from the oscillator frequency i.e. 250 kHz. However Test register ENDIV bit and Measurement control register 1 (E2/62$_{HEX}$) DIV bit can select additional clock divisions of 2 and 4 respectively. See Internal System Clock Frequency MCLK selections on Electrical Characteristics page 5 as function of DIV and ENDIV bit selections.

FOSC can be used to force the internal oscillator to be on all the time. This is for internal oscillator trimming purpose only. Normally (FOSC=0) the internal oscillator is turned on only during the measurements to save power and the OSC pin output is at logic low. To get the internal 500 kHz clock signal out from OSC pin it is necessary to set FOSC=1.

ENDIV bit can be used to enable an extra system clock divider. By default it is disabled (ENDIV=0).

The STEST bits are used for connecting different internal signals to the TEST1 and TEST2 pins that are necessary in the testing. In STEST=000…100 selections the TEST1 and TEST2 pins act as outputs and in STEST=101 selection they act as inputs.

SEL_EXTCLK bit selects between internal clock oscillator (OSC pin as digital output) which is the default setting and external clock signal (OSC pin as digital input). Note that if SEL_EXTCLK=1 is selected the internal oscillator is disabled and OSC pin acts as digital input despite of FOSC selection. Note also that the frequency division selections DIV or ENDIV do not apply to OSC pin clock signals. The internal 500 kHz clock signal from OSC pin and the external clock signal applied to OSC pin are not affected by the DIV and ENDIV selections.

Table 2. MAS6503 test register ($E1/61_{HEX}$) description

Bit Number	Bit Name	Description	Value	Function
7	-	Not used	X	-
6	TRIM	Selects source of oscillator trimming bits	0 1	Osc trimming values from EEPROM Osc trimming values from control registers
5	SEL_EXTCLK	Selects external clock	0 1	Internal clock (default) External clock (OSC input) can be connected to OSC and the internal clock oscillator is disabled
4-2	STEST	TEST1 and TEST2 signal selection	000…100 101…111	Reserved for internal testing purpose (TEST1 and TEST2 are outputs) No function
1	ENDIV	Enable for extra system clock divider	0 1	MCLK not divided (default) MCLK divided by 2 Note: DIV bit of measurement control register 1 choose extra MCLK division by 4
0	FOSC	Forces the oscillator on without conversion	0 1	OSC is on only during conversion (default) OSC is forced on

X = Don't care

MEASUREMENT CONTROL REGISTER 1 (E2/62$_{HEX}$)

Measurement control register 1 (E2/62$_{HEX}$) is for configuring the first half of the measurement settings. The second half of measurement settings is configured by Measurement control register 2 (E3/63$_{HEX}$) which is also used for starting a conversion.

DIV bit selects between normal clock (DIV=0) and divided by 4 clock (DIV=1). By default DIV=0 selection is used. Note also that the MCLK clock frequency can be further divided by 2 using the Test register (E1/61$_{HEX}$) ENDIV bit. See Electrical Characteristics page 5 for MCLK options as function of DIV and ENDIV bits.

ISCR bits select full scale input signal range from four options. The table 3 input signal range voltage values correspond to values at supply voltage VDD=2.7V. At other supply voltage the ISCR values scale directly with VDD due to ratiometric A/D converter principle. The linear input signal range is 80% (10%...90%) of the full scale input range. See also Input Signal Range Definitions in the Application Information section.

ENOFS bit is for enabling offset voltage to the input signal conversion range (ENOFS=0 disabled, ENOFS=1 enabled).

SGNOFS bit is for selecting sign of the input signal conversion range offset (SGNOFS=0 positive, SGNOFS=1 negative).

OFS bits select input signal conversion range offset from four options.

ENREG is for enabling internal voltage regulator (ENREG=0 disabled, ENREG=1 enabled). When enabled the regulator is turned on during conversions and automatically turned off after each conversion to save power. However note that if in the Test register FOSC=1 and if ENREG=1 the regulator is forced on all the time even when measurement is not running. In the VDD level monitoring mode it is necessary to disable the internal regulator (ENREG=0).

See also Regulator output voltage control register (EB/6B$_{HEX}$) for internal voltage regulator output voltage selections.

Table 3. Measurement control register 1 (E2/62$_{HEX}$) description

Bit Number	Bit Name	Description	Value	Function
7	DIV	Clock Divider by 4	0 1	Normal clock Divided by 4 clock
6-5	ISCR	Input Signal Conversion Range (full scale)	00 01 10 11	373mV 253mV 172mV 115mV at VDD=2.7V
4	ENOFS	Offset Enable	0 1	Offset disabled Offset enabled
3	SGNOFS	Offset Sign	0 1	Positive offset Negative offset
2-1	OFS	Offset value	00 01 10 11	40mV 57mV 86mV 126mV at VDD=2.7V
0	ENREG	Regulator Enable	0 1	Voltage regulator disabled Voltage regulator enabled

MEASUREMENT CONTROL REGISTER 2 (E3/63HEX)

Measurement control register 2 (E3/63HEX) configures second half of the measurement settings and also starts the measurement. See table 4.

OSRS bits select over sampling ratio (OSR) setting from five options. The OSR selection affects both measurement resolution and conversion time. The best resolution is achieved at highest OSR setting 4096 but the conversion time is longest. The fastest conversion is achieved at lowest OSR setting 256 but the achieved resolution is lowest. Typically highest OSR setting is used only in the most precise measurement such as pressure measurement. Medium or lowest OSR setting is typically sufficient in the temperature measurement. The lowest OSR setting can be used in the least precision VDD level monitoring measurement.

RSENSOR bits select sensor resistance from eight options from 2.0kΩ up to 10 kΩ. Selecting proper RSENSOR according to sensor resistance is important only for the temperature measurement mode. See also Temperature Measurement Configuration in the Application Information section.

PTS bits select between three measurement modes; pressure, temperature and VDD level monitoring modes.

The conversion starts right after writing data byte to the Measurement control register 2. Thus to start new conversion the measurement configuration data has to be written first to Measurement control register 1 and after that to the Measurement control register 2. To avoid disturbing the running measurement the serial communication with MAS6503 should be kept idle during conversions. The EOC pin goes low when the conversion starts and it returns back high when the conversion is ready.

Table 4. Measurement control register 2 (E3/63HEX) description

Bit Number	Bit Name	Description	Value	Function
7-5	OSRS	Over Sampling Ratio (OSR) Selection	000 001 010 011 100	OSR = 256 OSR = 512 OSR = 1024 OSR = 2048 OSR = 4096
4-2	RSENSOR	Sensor Resistance	000 001 010 011 100 101 110 111	2.0kΩ 2.5kΩ 3.0kΩ 3.5kΩ 4.0kΩ 4.5kΩ 5.0kΩ 10.0kΩ
1-0	PTS	Pressure/ Temperature/ VDD Level Monitoring Mode Selection	00 01 10 11	Temperature mode VDD level monitoring mode Pressure mode -

OSCILLATOR FREQUENCY CONTROL REGISTER (E4/64$_{HEX}$)

Note that the internal clock oscillator frequency has been factory trimmed and the trim value has been stored in the EEPROM (DF/5F$_{HEX}$). It is recommended not to change the factory programmed value!

The oscillator frequency control register (E4/64$_{HEX}$) is for trimming the internal clock oscillator to 500 kHz frequency. When settings FOSC=1 in the Test register (E1/61$_{HEX}$) the 500 kHz clock signal can be measured at the OSC pin.

The six LSB bits adjust the oscillator signal period in 65ns steps. The signal period decreases and frequency increases when the trim value increases. The six bit register value is considered as a 2's complement number. Typically a mid value 00$_{HEX}$ corresponds to the nominal 500 kHz clock oscillator frequency.

After finding a suitable trim value it can be stored to the EEPROM (DF/5F$_{HEX}$).

Table 5. Oscillator frequency control register (E6/66$_{HEX}$)

Bit Number	Bit Name	Description	Value (bin)	Value (2's complement)	Value (dec)	Function
7-6	-	Not used	X	X	X	-
5-0	OSCF	Oscillator frequency control	011111	31	31	Max frequency
			011110	30	30	…
			…….	…	…	…
			000001	1	1	…
			000000	0	0	Nominal 500 kHz
			111111	-1	63	…
			111110	-2	62	…
			…….	…	…	…
			100001	-31	33	…
			100000	-32	32	Min frequency

X = Don't care

EEPROM DATA INPUT REGISTER (E5/65$_{HEX}$)

This register can be ignored by user. It is related to internal EEPROM operations and updated automatically during every EEPROM write operation.

EEPROM WRITE ENABLE REGISTER (E6/66$_{HEX}$)

The EEPROM is normally write protected. To enable write the EEPROM write enable register should be set to %00000100 (04$_{HEX}$). To disable write the register should be set to %00000000 (00$_{HEX}$) which is the register default value after power-on-reset or manual reset by XCLR or by reset register. Note: don't use any other EEPROM write enable register values than these two since other register bits are reserved for internal testing purpose only.

Table 6. EEPROM write enable register (E9/69$_{HEX}$)

Bit Number	Bit Name	Description	Value	Function
7-3			00000	Reserved. Keep these bits always 0.
2	EWE	EEPROM write enable	0 1	EEPROM write disabled EEPROM write enabled
1-0			00	Reserved. Keep these bits always 0.

CONVERSION RESULT REGISTERS (E7…E9$_{HEX}$)

After measuring external sensor, temperature or VDD level the 24-bit conversion result is stored into three Conversion result register addresses E7…E9$_{HEX}$. The MSB (most significant byte) is at E7$_{HEX}$, ISB (intermediate significant byte) at E8$_{HEX}$ and LSB (least significant byte) at E9$_{HEX}$.

EEPROM STATUS REGISTER (EA/6A$_{HEX}$)

The EEPROM status register (EA/6A$_{HEX}$) indicates if the stored EEPROM byte is corrupted. The register is updated after each EEPROM data byte read command. See table 7 below. The ERROR bit tells if a data error has been detected (ERROR=1). The DED bit tells if two or more bit errors have been detected (DED=1). The EEPROM can correct internally only single bit errors i.e. when ERROR=1 and DED=0. The read EEPROM data byte is corrupted if ERROR=DED=1. The six lowest bits have value 0.

Table 7. MAS6503 EEPROM status register (EA/6A$_{HEX}$). Only bits (7:6) are used.

Bit Number	Bit Name	Description	Value	Function
7	ERROR	EEPROM error detection	0 1	No errors Error detected
6	DED	EEPROM double error detection	0 1	No errors 2 (or more) data errors
5-0			000000	-

REGULATOR OUTPUT VOLTAGE CONTROL REGISTERS (EB/6B$_{HEX}$)

When enabled the internal voltage regulator output voltage is defined by the Regulator output voltage control register (EB/6B$_{HEX}$). In the register only two most significant bits are in use. See table 8.

Table 8. Regulator output voltage control register (EB/6B$_{HEX}$)

Bit Number	Bit Name	Description	Value	Function
7-6	REGEB<7:6>	Regulator output voltage selectors	00 01 10 11	Regulator output 1.8V Regulator output 2.2V Regulator output 2.6V Regulator output 2.9V
5-0	-	Not used	XXXXXX	-

X = Don't care

EEPROM WRITE PROCEDURE

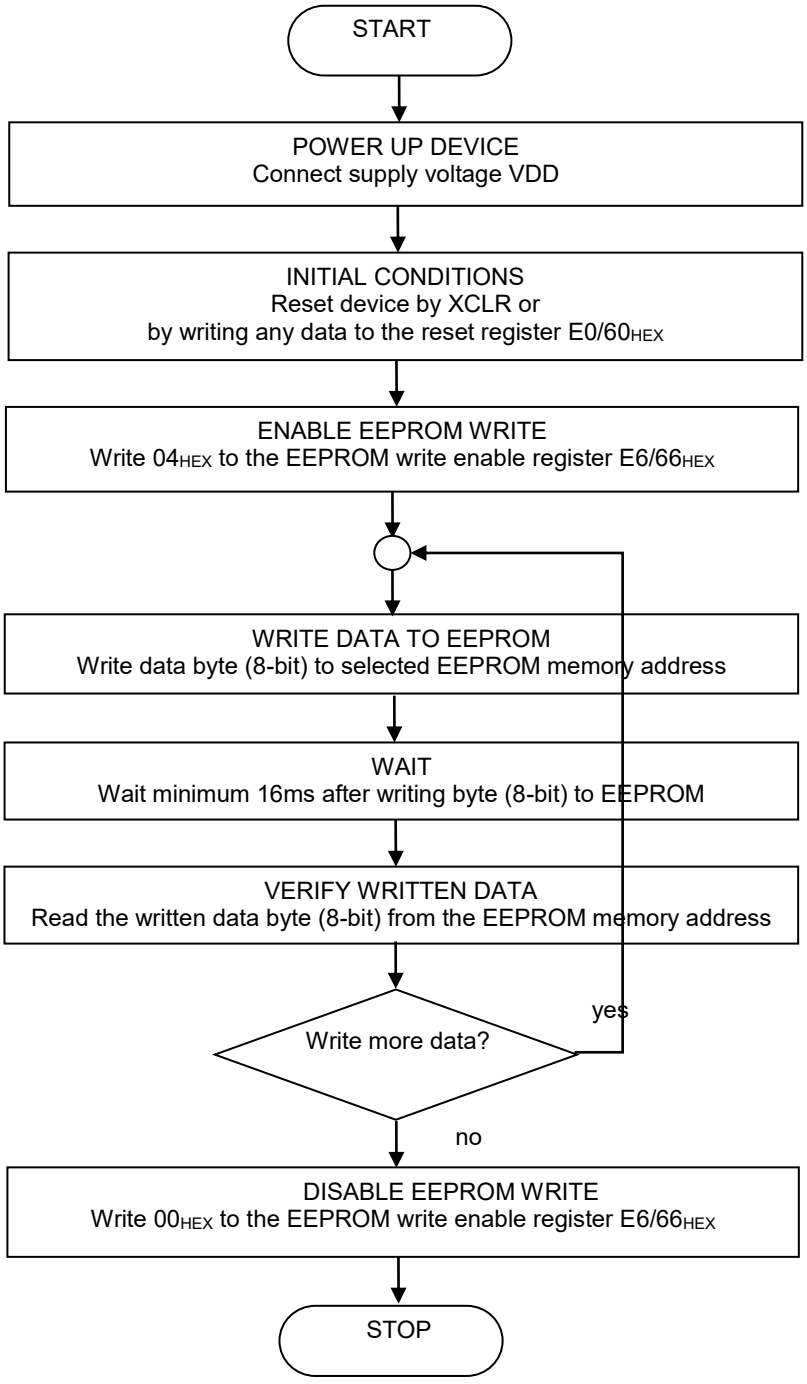


Figure 3. Flow chart for MAS6503 EEPROM write

Important note: Before EEPROM programming make sure that in the Test register (E1/61$_{HEX}$) the ENVIV=0 and in the Measurement control register 1 (E2/62$_{HEX}$) the DIV=0 are selected. These select 250 kHz system clock frequency which is required for the proper EEPROM programming pulses. This condition is guaranteed by making device reset either using the reset register (E0/60$_{HEX}$) or the XCLR pin.
Note: In the “VERIFY WRITTEN DATA” step it could be also additionally checked that the EEPROM status register (EA/6A$_{HEX}$) does not indicate read errors.

EEPROM WRITE PROCEDURE

This chapter gives instructions for writing data to the EEPROM memory.

The MAS6503 24 bit Analog-to-Digital Converter (ADC) has a 256 bit (32 bytes) EEPROM memory. 8 bits (1 byte) has been reserved for storing internal clock oscillator trimming data and other 8 bits (1 byte) for the programmable I2C device address. The remaining 240 bits (30 bytes) are free for storing sensor calibration data and other use.

See figure 3 on previous page showing the EEPROM write procedure.

Make sure in the beginning of the EEPROM write procedure that the MAS6503 initial conditions are met. Connecting VDD triggers power-on-reset (POR) but to make sure the device is reset an additional reset should be given using the XCLR pin or writing any data on the reset register $E0/60_{HEX}$ via the serial bus. The device reset will guarantee that in the Test register ($E1/61_{HEX}$) the ENDIV=0 and in the Measurement control register 1 ($E2/62_{HEX}$) the DIV=0 are selected. These select 250 kHz system clock which is required in the EEPROM programming.

EEPROM write is enabled by writing value 04_{HEX} to the EEPROM write enable register ($E6/66_{HEX}$). The default register value after power on is 00_{HEX}.

Next the data can be written to the EEPROM memory one byte (8-bit) at a time. It is necessary to have a delay of minimum 16ms after programming each byte (8-bit). The success of each write can be verified by reading back the data (8-bit) and comparing it to the original byte (8-bit). Additionally it is also possible to check the EEPROM status register ($EA/6A_{HEX}$) value after each read back. The EEPROM status register value should be 00_{HEX} when the read EEPROM data byte is free of errors.

After all data bytes are written the EEPROM memory can be protected from write by writing 00_{HEX} to the EEPROM write enable register ($E9/69_{HEX}$).

See table 1 showing the MAS6503 register and EEPROM data addresses.

SERIAL DATA INTERFACE CONTROL

Serial Interface

MAS6503 can be operated either via 2-wire serial I2C bus or via 4-wire serial SPI bus. Selection between I2C and SPI communication is done by XSPI pin. XSPI=high selects I2C and XSPI=low selects SPI communication.

2-wire serial I2C bus type interface comprises of serial clock input (SCL) and bi-directional serial data (SDA) input/output. I2C bus is used to write configuration data to sensor interface IC and read the measurement result when A/D conversion has been finished. The interface is also used for reading the calibration EEPROM memory.

Note: The 2-wire I2C bus of MAS6503 supports only basic I2C bus communication protocol but not for example 10-bit addressing, arbitration and clock stretching features of the I2C bus specification.

The alternative 4-wire serial SPI bus type interface comprises of serial clock input (SCLK), serial data input (MOSI), serial data output (MISO) and chip select input (XCS).

Digital interface includes also end of conversion (EOC) and master reset (XCLR) pins. Rising edge in the EOC pin indicates that the conversion is ready and the result can be read out through serial interface.

XCLR is used to reset the MAS6503. A reset initializes registers (set to value 00_{HEX}), counters and the serial communication bus. Alternatively device can be reset via serial bus by writing any data to Reset register (address $E0/60_{HEX}$). The Reset register bits don't have any function. Reading from the reset register is not possible.

After connecting the supply voltage to MAS6503, and before starting operating the device via the serial bus, it is required to reset the device if the supply voltage rise time has been longer than 1ms. However it is recommended to reset the device manually after every power up to guarantee proper register settings after any VDD rise conditions

I2C Bus Communication

In MAS6503 the I2C bus communication is selected by setting XSPI pin high.

The I2C bus standard makes it possible to connect several devices on same bus. The devices are distinguished from each other by unique device addresses. In MAS6503 there is both a hard wired and programmable device address. Both hard wired and programmable addresses can be used to address MAS6503. The MAS6503 hard wired device address is shown in the following table. The LSB bit of the device address defines whether the bus is configured to Read (1) or Write (0) operation. See figure 11 in Application Information chapter showing MAS6503 configured for I2C bus communication.

The programmable device address is located in the EEPROM register $DE_{HEX}/5E_{HEX}$ which has been factory programmed to value EA_{HEX} (%11101010) which is the same as the fixed device address of MAS6503. When unique device address is needed it can be programmed to this register. The programmable I2C device address is read from EEPROM memory only during power on reset or manual reset situations. To guarantee that the programmable address is read from EEPROM the device can be reset manually by using XCLR pin or Reset register ($E0/60_{HEX}$).

Table 9. MAS6503 I2C bus hard wired device address (EA/EB_{HEX})

A7	A6	A5	A4	A3	A2	A1	W/R
1	1	1	0	1	0	1	0/1

I2C Bus Protocol Definitions

Data transfer is initiated with a Start bit (S) when SDA is pulled low while SCL stays high. Then, SDA sets the transferred bit while SCL is low and the data is sampled (received) when SCL rises. When the transfer is complete, a Stop bit (P) is sent by releasing the data line to allow it to be pulled up while SCL is constantly high.

Figure 4 on next page shows the start (S) and stop (P) bits and a data bit. Data must be held stable at the SDA pin when SCL is high. Data at the SDA pin can change value only when SCL is low.

Each SDA line byte transfer must contain 8-bits where the most significant bit (MSB) always comes first. Each byte has to be followed by an acknowledge bit (see further below). The number of bytes transmitted per transfer is unrestricted.

2-WIRE SERIAL DATA INTERFACE (I2C BUS)

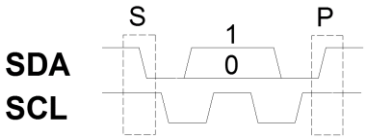


Figure 4. I2C bus protocol definitions

Bus communication includes Acknowledge (A) and not Acknowledge (N) messages. To send an acknowledge the receiver device pulls the SDA low for one SCL clock cycle. For not acknowledge (N) the receiver device leaves the SDA high for one SCL clock cycle in which case the master can then generate either a Stop (P) bit to abort the transfer, or a repeated Start (Sr) bit to start a new transfer.

Abbreviations:
A= Acknowledge by Receiver
N = Not Acknowledge by Receiver
S = Start
Sr = Repeated Start
P = Stop
= from Master (MCU) to Slave (MAS6503)
= from Slave (MAS6503) to Master (MCU)

Conversion Starting – Write Sequence

Conversion is started by writing configuration bits into the Measurement control registers 1 and 2 (addresses $E2_{HEX}$ and $E3_{HEX}$). The write sequence is illustrated in Table 10.

Table 10. MAS6503 I2C bus write sequence of two consecutive Measurement control registers 1 and 2

S	AW	A	MC1	A	DC1	A	DC2	A	P

Abbreviations:
AW = Device Write Address EA_{HEX} (%1110 1010)
AR = Device Read Address EB_{HEX} (%1110 1011)
MC1 = Meas. control reg.1 62_{HEX} (%0110 0010)
Ax = Conversion Result Registers' Addresses; MSB (x=M, 67_{HEX} %0110 0111), ISB (x=I, 68_{HEX} %0110 1000) or LSB (x=L, 69_{HEX} %0110 1001)
DC1 = Measurement Control Register 1 Data
DC2 = Measurement Control Register 2 Data
Dx = Conversion Result Register Data; MSB (x=M), ISB (x=I) or LSB (x=L)

Each serial bus operation, like write, starts with the start (S) bit (see figure 4). After start (S) the MAS6503 device address with write bit (AW, see table 9) is sent followed by an Acknowledge (A). After this the Measurement control register 1 address (see table 1) is sent and followed by an Acknowledge (A). Next the Measurement control register 1 data (DC1, see table 3) is written and followed by an Acknowledge (A). Due to register address auto increment to the next register address the Measurement control register 2 data (DC2, see table 4) can follow right after first data byte. After acknowledge of second data byte the serial bus operation is ended with stop (P) command (see figure 4). A new A/D conversion starts right after Measurement control register 2 bits are received.

A/D Conversion

After power on reset or external reset (XCLR) the EOC output is high. After an A/D conversion is started the EOC output is set low until the conversion is finished and the EOC goes back high, indicating that the conversion is done and data is ready for reading. The EOC is set low only by starting a new conversion. To save power the internal oscillator runs only during conversion.
During an A/D conversion the input signal is sampled continuously leading to an output conversion result that is a weighted average of the samples taken.

2-WIRE SERIAL DATA INTERFACE (I2C BUS)

Conversion Result – Read Sequence

Table 11 presents a general control sequence for a single register data (Dx) read from register address (Ax).

Table 11. MAS6503 I2C bus single register (address Ax) read sequence bits

S	AW	A	Ax	A	Sr	AR	A	Dx	N	P

Table 12 shows the control sequence for reading the 24-bit A/D conversion result from the Conversion result registers. The ISB (DI) and LSB (DL) register data read can follow right after the MSB register data (DM) read since if the read sequence is continued (not ended by a Stop bit P) since the register address is automatically incremented to point to the next register.

Table 12. MAS6503 I2C bus MSB (first), ISB (second) and LSB (third) A/D conversion result read sequence

S	AW	A	AM	A	Sr	AR	A	DM	A	DI	A	DL	N	P

4-WIRE SERIAL DATA INTERFACE (SPI BUS)

SPI bus communication is selected by setting XSPI pin low.

SPI communication differs from I2C bus in the following way. It requires four wires for bi-directional communication since each line operates in one direction only. Device selection is done by using separate chip select XCS control lines instead of using device address. Each SPI bus device has its own XCS control line and a device is selected by pulling its XCS line low (see figure 5 below). The fourth wire in the SPI bus is the serial clock line, SCLK. Data is transferred at rising edges of the serial clock during which the data line should be stable.

The selection between write or read access is done by register address MSB bit A7 (see table 1 "*Register and EEPROM data addresses*"). In write access bit A7 cleared (0) and in read access it is set (1).

Figure 5 illustrates write access communication. MAS6503 has an auto increment function which means that if there are more than one data byte transferred the additional data bytes are delivered to following register addresses. In write communication the MISO line is high impedance.

In SPI bus communication it is good to note that setting XCS low activates the EEPROM memory regardless of the XSPI setting and the device consumes 20μA …30μA current. To minimize current consumption XCS should be set low only during time periods when the device is used during SPI communication.

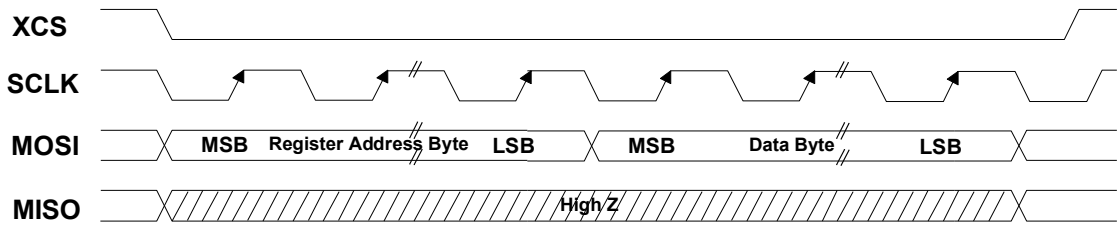


Figure 5. *SPI Protocol – Write Access (register address MSB bit A7=0)*

4-WIRE SERIAL DATA INTERFACE (SPI BUS)

Figure 6 illustrates read access communication. The auto increment function can be utilized also in read access and if there are more than one data byte read the additional data bytes are delivered from following register addresses.

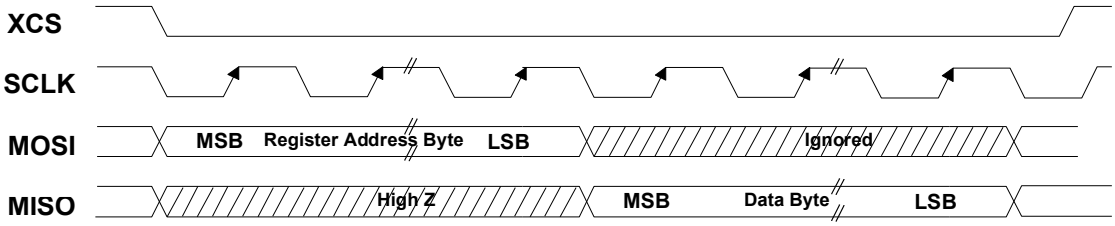


Figure 6. *SPI Protocol – Read Access (register address MSB bit A7=1)*

APPLICATION INFORMATION

Input Signal Range Definitions

The input signal voltage polarity is from positive input PI to the negative input NI. MAS6503 has input signal range (ISR) and offset (OFFSET) selection options that determines the input signal range of the A/D converter. The minimum and maximum input signal values in the linear input signal range (ISRLIN) are calculated as follows. Due to ratiometric principle the input signal range is directly proportional to VDD.

$$V_{IN_MIN} = \frac{VDD}{2.7V} \cdot \left(OFFSET - \frac{ISRLIN}{2} \right)$$ Equation 1.

$$V_{IN_MAX} = \frac{VDD}{2.7V} \cdot \left(OFFSET + \frac{ISRLIN}{2} \right)$$ Equation 2.

Table 13 shows minimum and maximum input signal values in the linear input signal range at different input signal range and offset selection combinations.

Table 13. Examples of minimum and maximum input signal values in the linear input signal range (Vdd=2.7V)

OFFSET [mV]	ISR [mV]	ISRLIN [mV]	VIN_MIN [mV]	VIN_MAX [mV]
0	373	298	-149	149
126	373	298	-23	275
0	253	202	-101	101
86	253	202	-15	187
0	172	138	-69	69
57	172	138	-12	126
0	115	92	-46	46
40	115	92	-6	86

The digital A/D conversion result, CODE, depends on the input signal as follows.

$$CODE = CODEFS \cdot \left[0.5 + \frac{V_{IN} - OFFSET}{ISR} \cdot \right]$$ Equation 3.

CODE = digital A/D-conversion output code
CODEFS = A/D-converter maximum code (minimum code is zero)

See page 4 Electrical Characteristics for CODEFS values at different over sampling ratio (OSR) selections.

Pressure Measurement Configuration

A piezoresistive absolute pressure sensor can be modeled roughly with the following signal voltage characteristic when including only first order pressure and temperature characteristics.

$$V_{IN}(p,T) = \frac{VDD}{VDD_{REF}} \cdot \left[\frac{FS \cdot (1 + TC_{FS} \cdot (T - T_{REF}))}{p_{FS}} \cdot p + OS \cdot (1 + TC_{OS} \cdot (T - T_{REF})) \right]$$ Equation 4.

VDD = supply voltage
VDD_{REF} = reference supply voltage at which the sensor parameters (FS, OS) have been specified (often 5V)
p = pressure [bar]
p_{FS} = full-scale pressure range [bar]
FS = full-scale span [V]
OS = zero pressure offset [V]
TC_{FS} = full-scale span temperature coefficient [ppm/°C]
TC_{OS} = offset temperature coefficient [ppm/°C]
T_{REF} = reference temperature for resistor values [°C]
T = actual temperature to be measured [°C]

The above linear approximation includes sensor full-scale span and offset signal temperature dependencies.

APPLICATION INFORMATION

Temperature Measurement Configuration

In the temperature measurement configuration the piezoresistive sensor R_S is connected into a Wheatstone resistor bridge configuration together with four internal resistors R1, R2, R3 and R4. See figure 7.

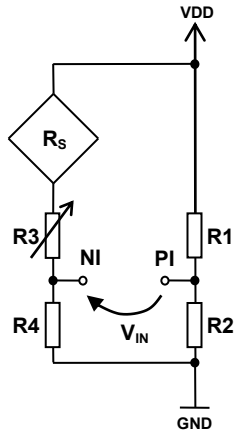


Figure 7. Temperature Measurement Configuration

In the temperature measurement configuration the A/D converter input signal has the following characteristics.

$$V_{IN}(T) = VDD \cdot \left[\frac{1}{\frac{R_1}{R_2}+1} - \frac{1}{\frac{R_S \cdot \left[1+TC_S \cdot (T-T_{REF})\right]}{R_4 \cdot \left[1+TC_R \cdot (T-T_{REF})\right]} + \frac{R_3}{R_4}+1} \right]$$

Equation 5.

VDD = supply voltage
R_S = sensor bridge resistance [Ω]
$R_{1, 2, 3, 4}$ = internal resistors [Ω]
TC_S = sensor resistance temperature coefficient [ppm/°C]
TC_R = internal resistor temperature coefficient [ppm/°C]
T_{REF} = reference temperature for resistor values [°C]
T = actual temperature to be measured [°C]

From equation 5 we get that the temperature signal has a rising temperature dependency vs. temperature when the sensor resistance has a positive temperature coefficient $TC_S>0$. With negative sensor resistance temperature coefficient $TC_S<0$ the signal has a falling temperature dependency vs. temperature. See the signal illustration in figure 8.

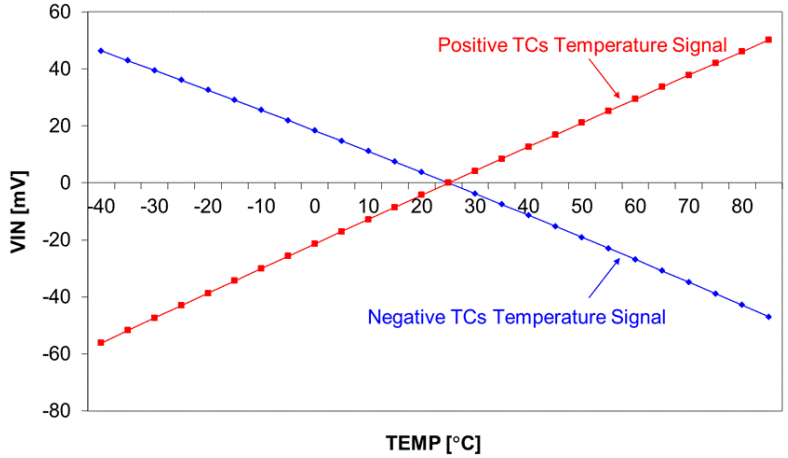


Figure 8. Temperature signal dependency of sensor resistance temperature coefficient

APPLICATION INFORMATION

VDD Level Monitoring Configuration

The MAS6503 has VDD level monitoring feature to measure supply voltage level which is useful especially in battery operated systems. In systems in which VDD can vary the VDD level monitoring could be also used to compensate VDD dependency.

The VDD level monitoring measurement is started by writing configuration data to the measurement control registers 1 (E2/62$_{HEX}$) and 2 (E3/63$_{HEX}$).

In the proper configuration it is necessary to disable both regulator (ENREG=0) and offset (ENOFS=0) and select the widest input signal conversion range 373mV (ISCR=00) and the VDD level monitoring measurement (PTS=01).

Typically the smallest over sampling ratio (OSR) selection 256 offers sufficient resolution for the VDD level monitoring.

VDD level monitoring model

The VDD level monitoring model for output code is following.

$$CODE = CODEFS \cdot \left(a - \frac{b}{VDD} \right)$$

The output has inverse relationship to supply voltage VDD. The OSR selects full scale output code range value CODEFS. See Electrical Characteristics for CODEFS at different OSR values.

The typical VDD level monitoring model parameter values a and b are as follows.
a=1.7064
b=2.9123
Note that these parameter values are subject to about two percent variations.

The supply voltage VDD can be solved from the output result as follows.

$$VDD = \frac{b}{a - \frac{CODE}{CODEFS}}$$

Figure 9 presents typical output code as function of supply voltage at OSR=256 (CODEFS=227328).
Figure 10 present supply voltage as function of output code at OSR=256 (CODEFS =227328).

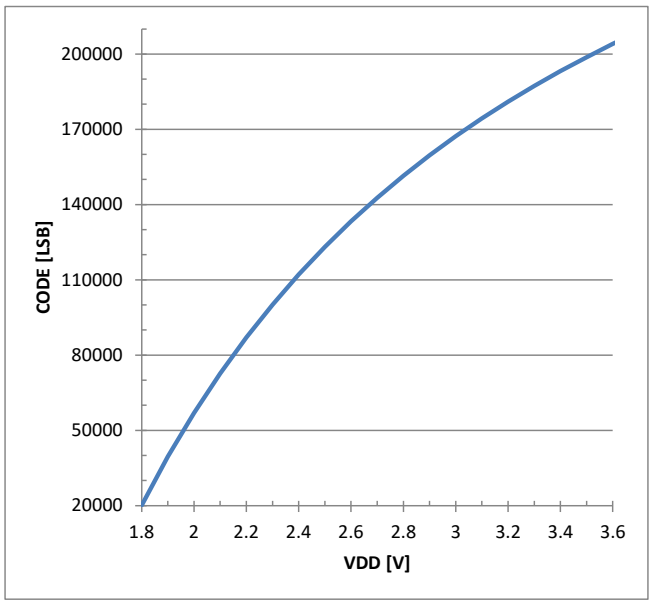


Figure 9. CODE(VDD) at VDD level monitoring

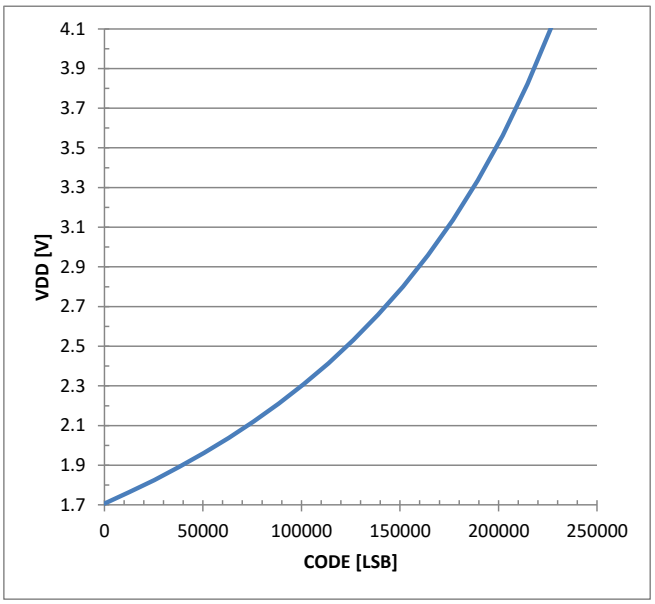
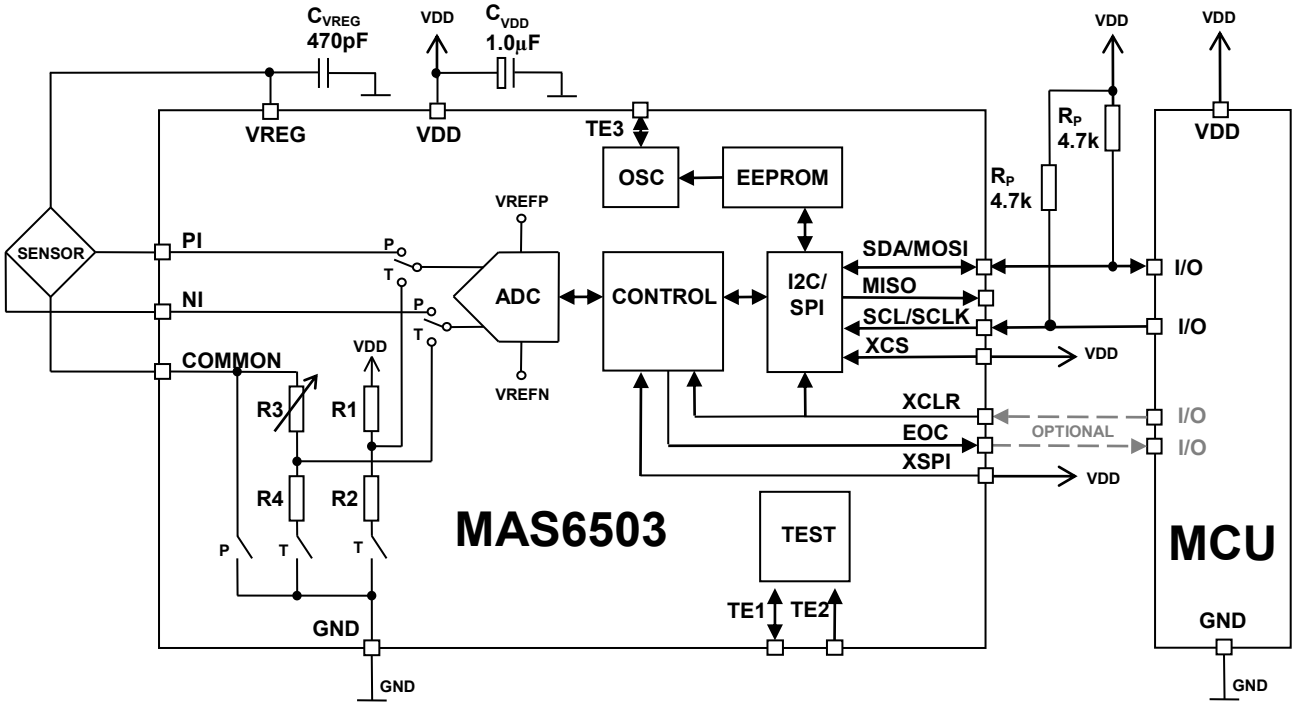


Figure 10. VDD(CODE) at VDD level monitoring

APPLICATION INFORMATION

VDD rise time < 1ms



NOTE: It is recommended to use the XCLR reset feature to solve unexpected error state conditions. In case VDD rise time can exceed 1ms the device has to be kept in a reset during power up by using the XCLR pin. Violating this may risk EEPROM integrity. If not used the XCLR pin can be left unconnected since it has internal pull up to VDD.

Figure 11. Typical application circuit configured for I2C bus communication

Figure 11 presents MAS6503 application circuit using I2C bus and when VDD rise time is guaranteed to be always below internal POR circuit delay of 1ms. In case the VDD rise time can exceed 1ms see the next page application information.

Together with a resistive pressure sensor, MAS6503 can be used in pressure measurement applications. An external micro-controller can control the MAS6503 via an I2C or a SPI serial interface. Note that the I2C serial interface requires suitable pull-up resistors connected to the SDA and SCL pins (see figure 11). If there is only a single master device connected to the serial bus the master's SCL output can be of push-pull type making the SCL pull-up resistor unnecessary.

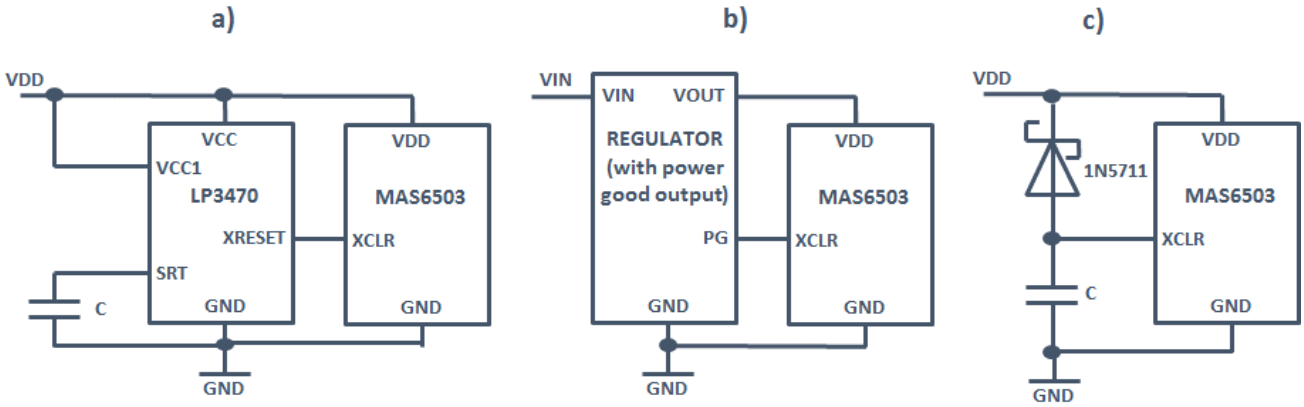
The sensor is connected between voltage regulator output (VREG) and grounding switch (COMMON) of MAS6503. The sensor output is read as a differential signal through PI (positive input) and NI (negative input) to the ΔΣ converter in MAS6503.

When using the internal regulator a 470pF capacitor should be connected between the regulator output VREG and GND and a decoupling capacitor of minimum 1µF should be used for the supply voltage VDD (see figure 11). If the internal regulator is disabled a supply voltage decoupling capacitor of 4.7 µF or more should be placed between VDD and GND to guarantee conversion accuracy.

APPLICATION INFORMATION

VDD rise time > 1ms

If the VDD rise time can exeed 1ms it is necessary to keep the MAS6503 in reset during power up using the XCLR reset pin. Violating this may risk EEPROM memory integrity. Figures 12 a-c present examples of external POR circuits providing reset via the XCLR pin in case the VDD rise time can exceed 1ms.



Figures 12 a, b, c. External XCLR reset circuit examples for VDD rise time >1ms

The XCLR pin has internal pull up with 8µA current which makes the pull up resistor unnecessary. In the figure 12c the external POR circuit delay can be calculated as follows.

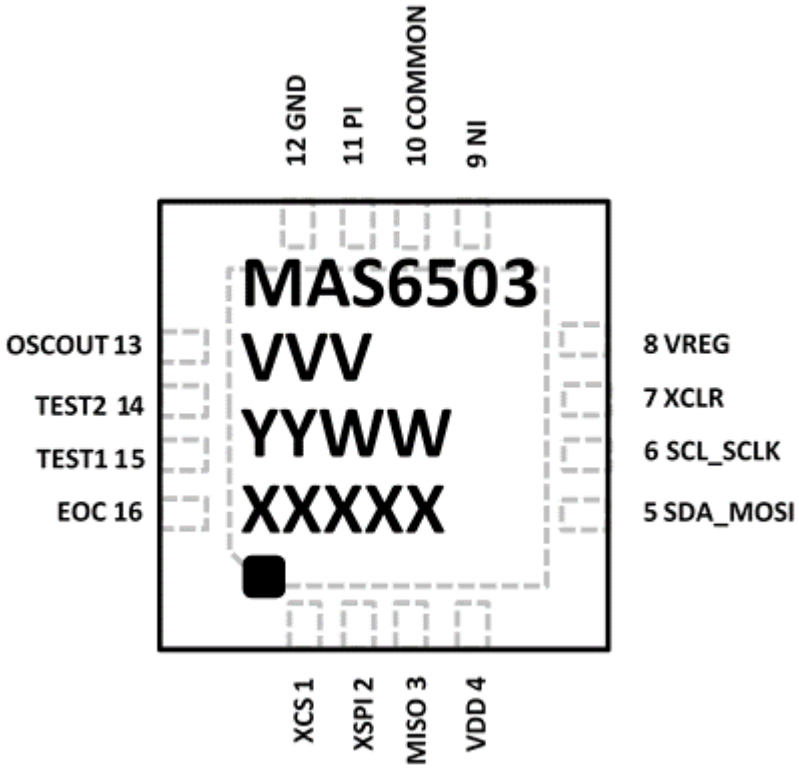
$$t_{POR} = \frac{C}{8\mu A} \cdot VDD$$

The POR delay should be made larger than the maximum VDD rise time. For example if the longest possible VDD rise time is 50ms and VDD=2.7V then we could choose capacitor value which gives at least 100ms POR delay; C=8µA*t_{POR}/VDD=8µA*100ms/2.7V=296nF which is rounded up to 330nF.

Resolution Improvement – Averaging

An averaging technique can be used to remove conversion errors caused by noise and thus improve measurement resolution. By doing several A/D conversions and calculating the average result it's possible to average out noise. Theoretically the noise is reduced by a factor $\sqrt{N}$ where N is the number of averaged samples. A/D converter nonlinearities cannot be removed by averaging.

MAS6503CA1 IN QFN-16 4x4x0.75 PACKAGE



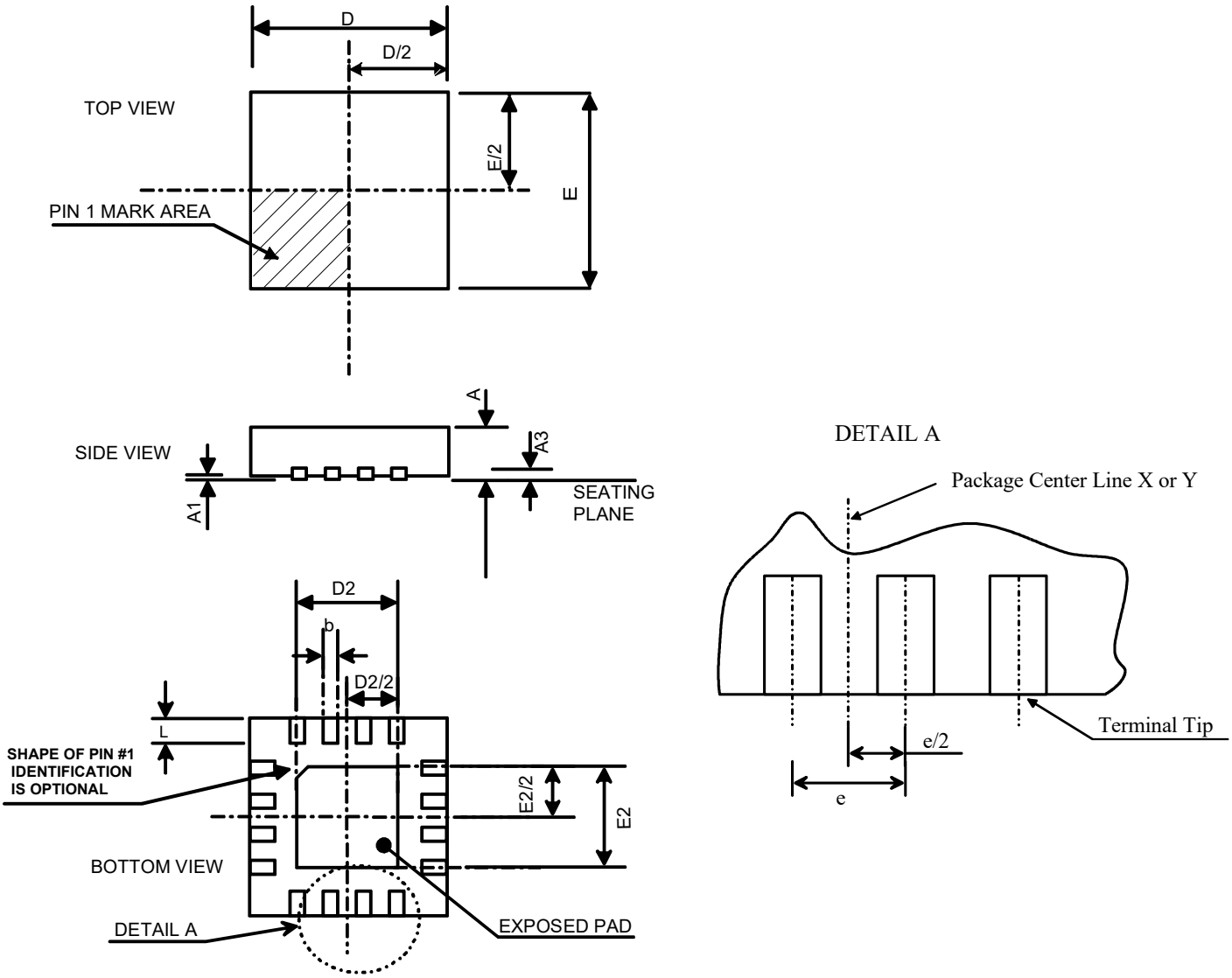
Top Marking Information:
MAS6503 = Product Number,
VVV = Version Number
YYWW = Year Week
XXXXX = Lot Number

QFN-16 4x4x0.75 PIN DESCRIPTION

Pin Name	Pin	Type	Function	Notes
XCS	1	DI	Chip select for SPI mode	
XSPI	2	DI	Selection between I2C (1) and SPI (0)	
MISO	3	DO	Data output pin in SPI mode	
VDD	4	P	Power supply	
SDA_MOSI	5	DIO	Data in/out in I2C and data in SPI mode	
SCL_SCLK	6	DI	Serial bus clock input in both I2C and SPI	
XCLR	7	DI	Master reset with pull-up resistance 245kΩ at VDD=2.7V	2
VREG	8	AO	Regulator output voltage	
NI	9	AI	Negative input for sensor	
COMMON	10	AI	Common input for sensor	
PI	11	AI	Positive input for sensor	
GND	12	G	Supply ground	
OSCOUT	13	DIO	Oscillator output / external clock input	
TEST2	14	AIO	2. test input /output	1
TEST1	15	AIO	1. test input /output	1
EOC	16	DO	End of conversion indication output	

NC = Not Connected, P = Power, G = Ground, DO = Digital Output, DI = Digital Input, AO = Analog Output, AI = Analog Input
Note 1: Test pins TE1, TE2 and TE3 must be left floating.
Note 2: XCLR pin can be left unconnected when not used. It has internal pull up to VDD.
Note: On PCB the exposed pad is recommended to be connected to GND. It could be also left floating but it cannot be connected to any other potential than GND.

PACKAGE (QFN-16 4X4x0.75) OUTLINE



Symbol	Min	Nom	Max	Unit
PACKAGE DIMENSIONS				
A	0.700	0.750	0.800	mm
A1	0.000	0.020	0.050	mm
A3		0.203 REF		mm
b	0.250	---	0.350	mm
D	3.950	4.000	4.050	mm
D2 (Exposed.pad)	2.700	---	2.900	mm
E	3.950	4.000	4.050	mm
E2 (Exposed.pad)	2.700	---	2.900	mm
e		0.650 BSC		mm
L	0.350	---	0.450	mm

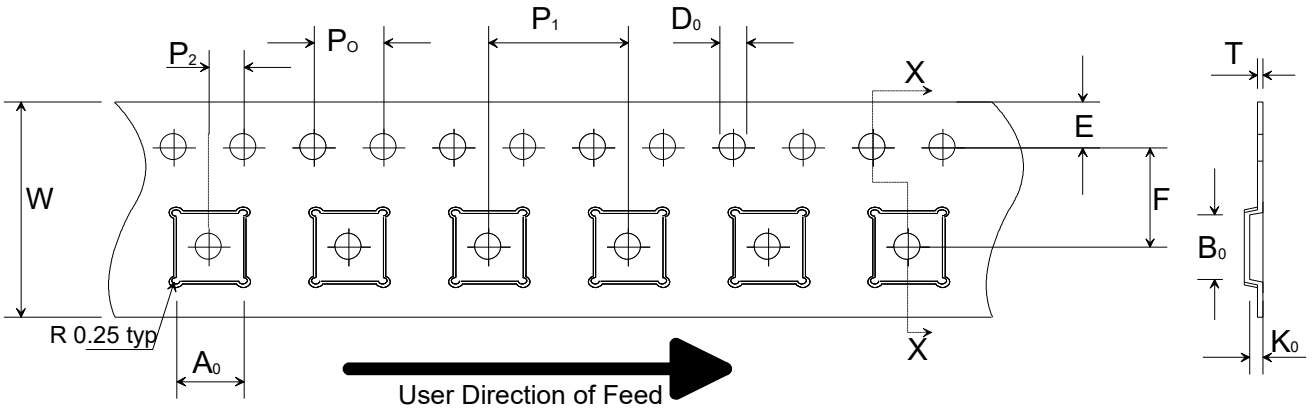
Dimensions do not include mold or interlead flash, protrusions or gate burrs.

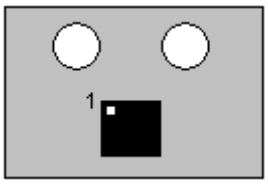
SOLDERING INFORMATION

◆ **For Lead-Free / Green QFN 4mm x 4mm**

Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. http://www.jedec.org
Lead Finish	Solder plate 7.62 - 25.4 µm, material Matte Tin

EMBOSSED TAPE SPECIFICATIONS



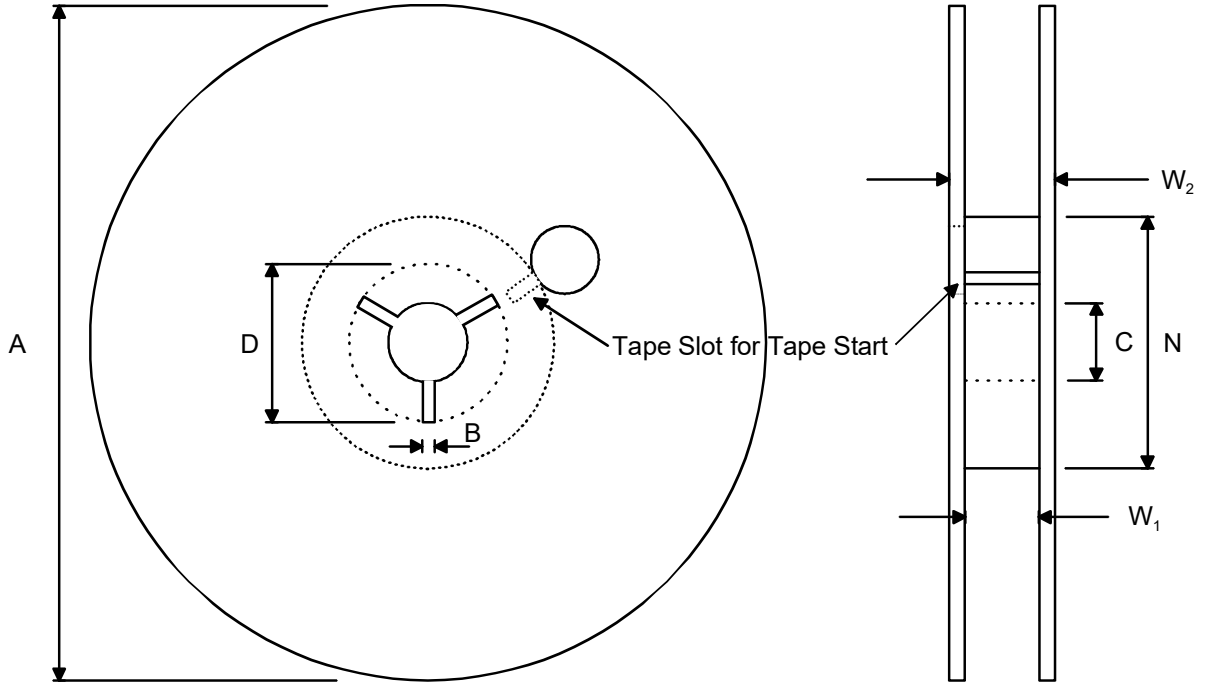


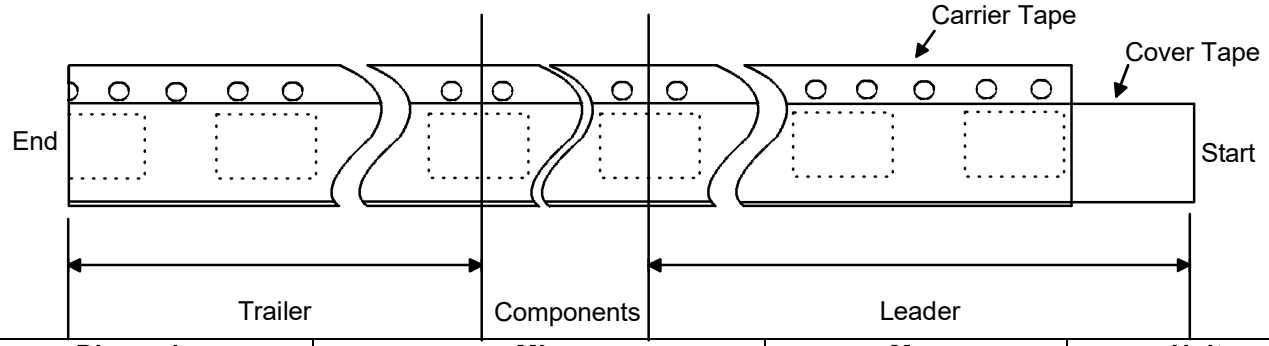
Orientation on tape

Dimension	Min/Max	Unit
A_o	4.30 ±0.10	mm
B_o	4.30 ±0.10	mm
D_o	1.50 +0.1/-0.0	mm
E	1.75	mm
F	5.50 ±0.05	mm
K_o	1.10 ±0.10	mm
P_o	4.0	mm
P_1	8.0 ±0.10	mm
P_2	2.0 ±0.05	mm
T	0.3 ±0.05	mm
W	12.00 ±0.3	mm

All dimensions in millimeters

REEL SPECIFICATIONS





Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	100		mm
W_1 (measured at hub)	12.4	14.4	mm
W_2 (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm

Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative

ORDERING INFORMATION

Product Code	Product	Description
MAS6503CA1WAD00	Piezoresistive Sensor Signal Interface IC	EWS-tested wafer, thickness 370 µm.
MAS6503CA1WAB05	Piezoresistive Sensor Signal Interface IC	Dies on waffle pack, thickness 180 µm
MAS6503CA1Q1706	Piezoresistive Sensor Signal Interface IC	QFN-16 4x4x0.75, Pb-free, RoHS compliant, Tape & Reel, 1000/3000 pcs components on reel

Contact Micro Analog Systems Oy for other wafer and die thickness options.

LOCAL DISTRIBUTOR

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