

## Features

- 4 PIN diodes in a SOT-25 Plastic Package
- Externally Selectable Bias and RF Matching Network
- 10 – 4,000 MHz Useable Frequency Band
- + 43 dBm IP3 @ 1000 MHz (50  $\Omega$ )
- 1.0 dB Loss @ 1000 MHz (50  $\Omega$ )
- 30 dB Attenuation @ 1000 MHz (50  $\Omega$ )
- Lead-Free SOT-25 Package
- 100% Matte Tin Plating over Copper
- Halogen-Free “Green” Mold Compound
- 260°C Reflow Compatible
- RoHS\* Compliant Version of MA4P274-1225

## Description

M/A-COM’s MA4P7455-1225 is a wideband, lower insertion loss, high IP3, Quad PIN Diode  $\pi$  Attenuator in a low-cost, lead free surface mount SOT-25 package. Four PIN Diodes in one package reduce design parasitics and improve circuit density.

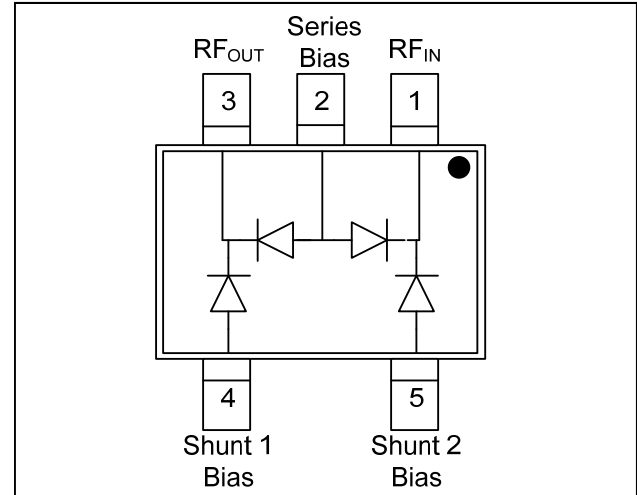
These PIN Diode Attenuators perform well where RF Signal Amplitude Control is required in 50  $\Omega$  Hand-set Circuits and 75  $\Omega$  Broadband CATV Systems. Exceptional Insertion Loss, Attenuation Range, and IP3 at <10 mA bias make these devices suitable for better power level control in RF Amplifiers.

## Ordering Information<sup>1</sup>

Model No.	Package
MA4P7455-1225T	Tape and Reel
MADP-007455-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.

## Functional Schematic



## Pin Configuration

Pin No.	Function	Pin No.	Function
1	RF IN	4	Shunt 1 Bias
2	Series Bias	5	Shunt 2 Bias
3	RF OUT		

## Absolute Maximum Ratings<sup>2,3</sup>

Parameter	Absolute Maximum
Operating Temperature	-65 °C to +125 °C
Storage Temperature No Dissipated Power	-65 °C to +150 °C
DC Voltage at Temperature Extremes	- 100 V
DC Current	75 mA

2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. M/A-COM does not recommend sustained operation near these survivability limits.

\* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

## Typical 50 $\Omega$ Performance<sup>4</sup> @ 25°C using Wideband RF Circuit Design

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	+3 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias 1000 MHz	dB	—	-2.0	—
Insertion Loss	+6.5 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias 1000 MHz	dB	—	-1.0	—
Return Loss	+6.5 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias 1000 MHz	dB	—	-10	—
Attenuation	0 mA - Series Diode Bias / 0.75 V - Shunt 1 and 2 Bias 1000 MHz	dB	—	-29	—
Input IP3	0 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias +6.5 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias F1 = 1000 MHz, F2 = 1100 MHz	dBm	—	43	—
		dBm	—	43	—
Input IP3	0 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias +6.5 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias F1 = 100 MHz, F2 = 110 MHz	dBm	—	43	—
		dBm	—	33	—
Settling Time	Within 1 dB of Final Attenuation Value 1000 MHz	$\mu$ S	—	3	—
RF C.W. Incident Power	0 - 20 V Series Diode Bias / 0.75 V Shunt 1 and 2 Bias	dBm	—	+20	—

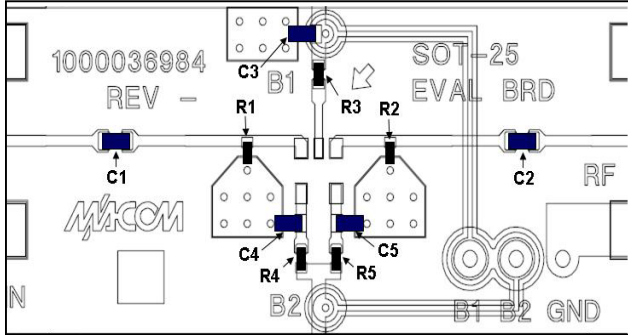
4. Values shown include through loss calibrated out of RF test circuit.

## Typical 75 $\Omega$ Performance<sup>5</sup> @ +25°C using Wideband RF Circuit Design

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	+2 mA Series Diode Bias / 1.0 V Shunt 1 and 2 Bias +4.5 mA Series Diode Bias / 1.0 V Shunt 1 and 2 Bias 1000 MHz	dB	—	-1.1	—
		dB	—	-0.6	—
Attenuation	0 mA / Series Diode and 1.0 V Shunt 1 and 2 Bias 1000 MHz	dB	—	-27	—
Return Loss	+4.5 mA / Series Diode and 1.0 V Shunt 1 and 2 Bias 1000 MHz	dB	—	-10	—

5. Values shown include through loss calibrated out of RF test circuit.

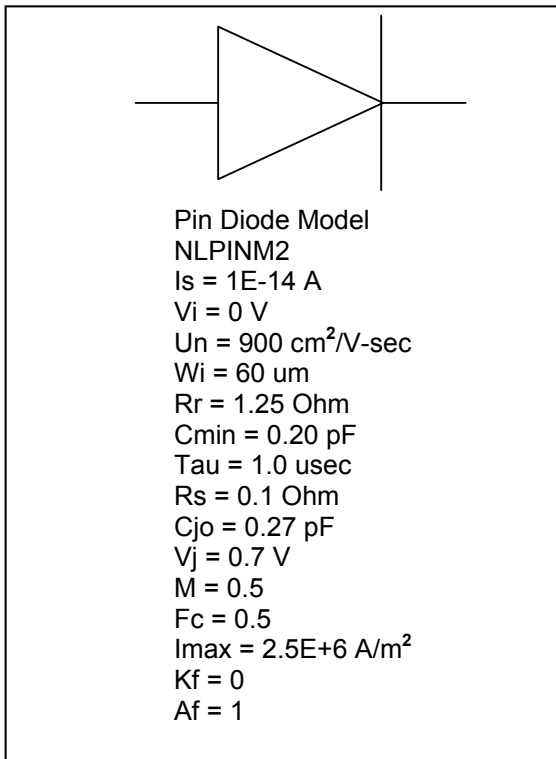
## Recommended PCB Layout



## Parts List

Part	Value	Case Style	Manufacturer
C1, C2, C3, C4, C5	100 pF	0603	Murata
R1, R2, R3, R4, R5	1000 $\Omega$	0402	Panasonic

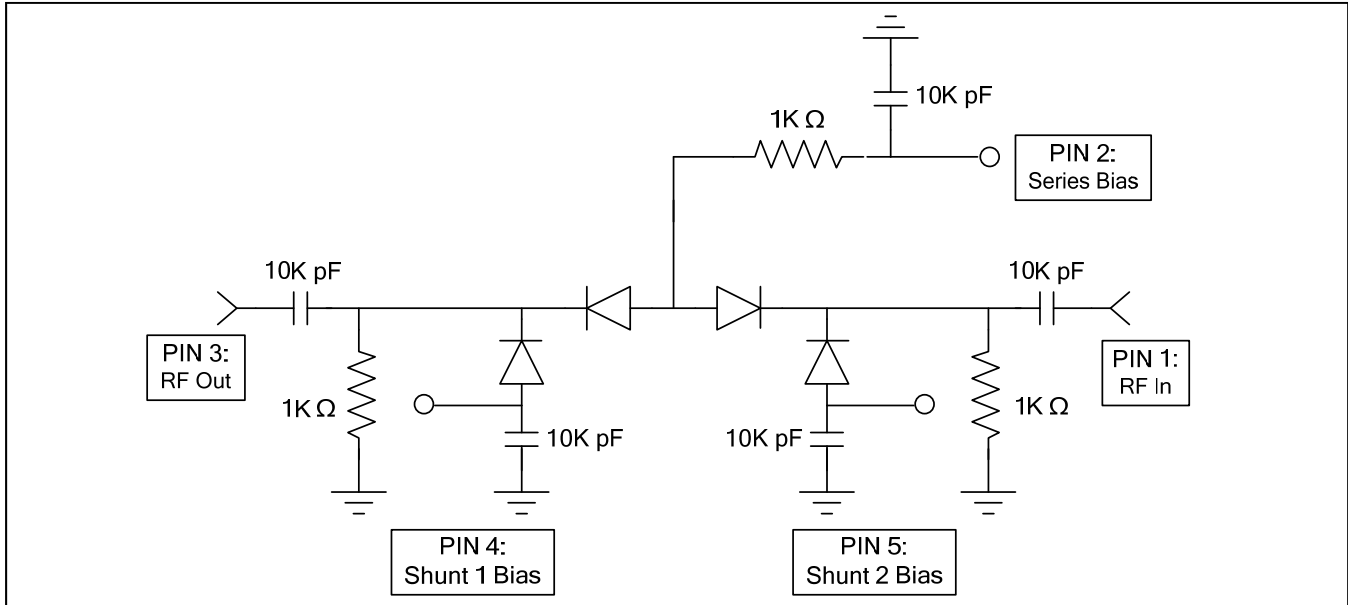
## MA4P7455-1225T Spice Model



## Series and Shunt Diode Bias Currents as a Function of Vseries and Vshunt Voltage (Values shown are PER DIODE)

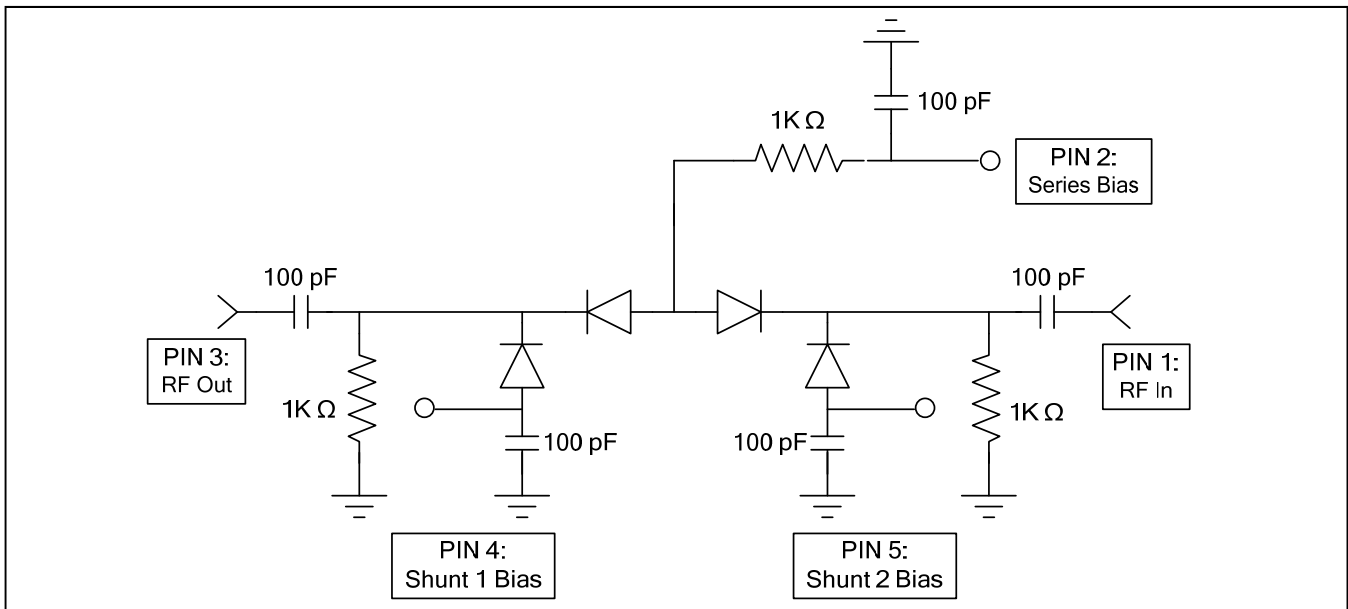
Vshunt Bias (V)	Vseries Bias (V)	Iseries Diode (mA)	Ishunt Diode (mA)
0.75	0	0.000	0.192
0.75	1	0.106	0.120
0.75	2	0.443	0.048
0.75	3	0.773	0
0.75	4	1.099	0
0.75	5	1.426	0
0.75	6	1.750	0
0.75	7	2.092	0
0.75	8	2.424	0
0.75	9	2.756	0
0.75	10	3.088	0
0.75	11	3.421	0
0.75	12	3.754	0
0.75	13	4.087	0
0.75	14	4.410	0
0.75	15	4.743	0
0.75	16	5.081	0
0.75	17	5.406	0
0.75	18	5.750	0
0.75	19	6.079	0
0.75	20	6.413	0

## Schematic 10 - 1000 MHz, 50 $\Omega$ , RF Circuit <sup>9</sup>



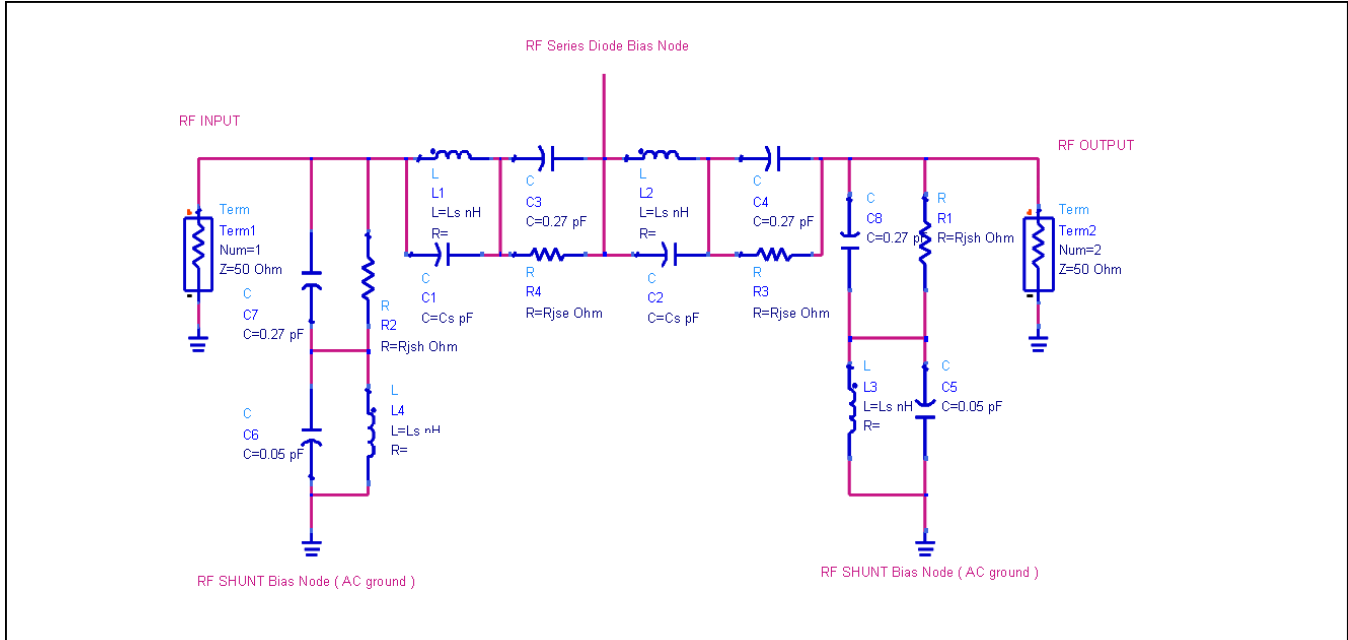
9. Keeping PIN 4 & PIN 5 as Separate Bias Points (Same V) reduces RF leakage (increases attenuation) through an otherwise connected Common Anode Bias Note.

## Schematic 1 - 4 GHz, 50 $\Omega$ , RF Circuit <sup>10</sup>

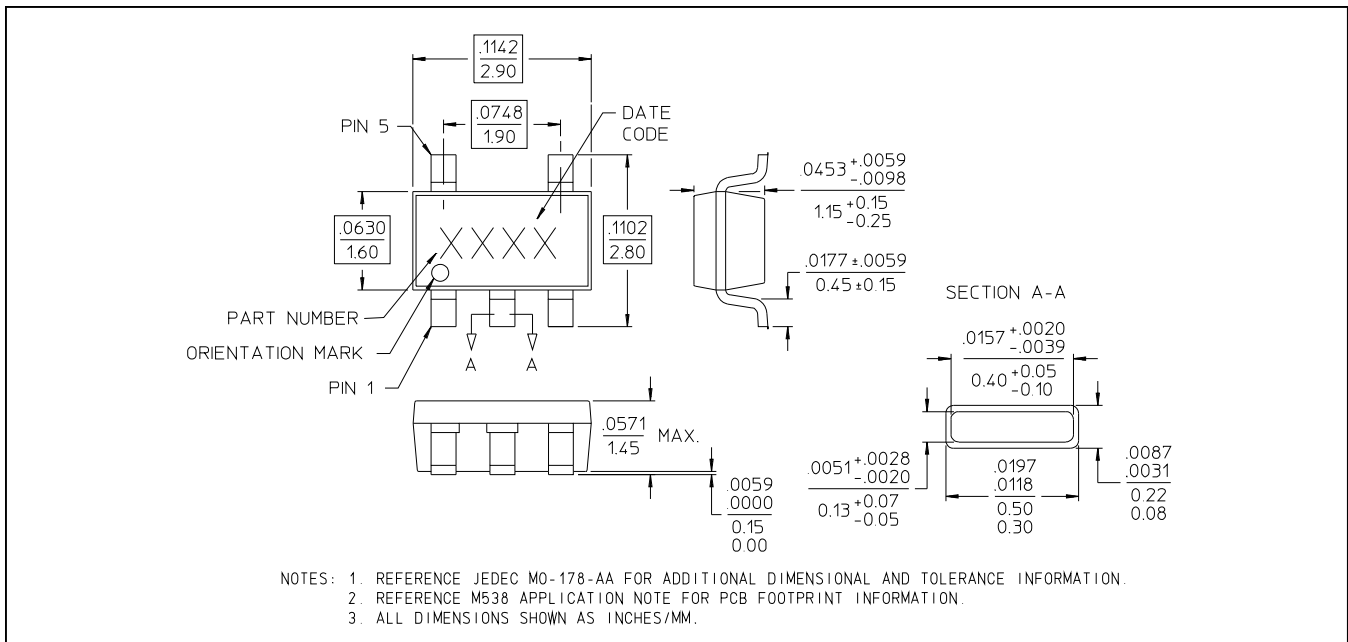


10. Keeping PIN 4 & PIN 5 as Separate Bias Points (Same V) reduces RF leakage through an otherwise connected Common Anode Bias Node.

## Lumped Element Model for MA4P7455-1225 PIN Diode $\pi$ Attenuator in SOT-25



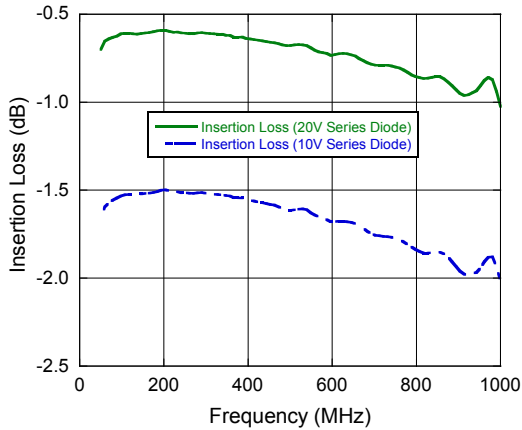
### Lead Free SOT-25 †



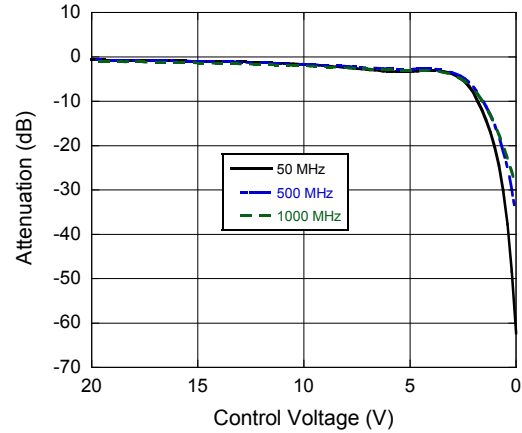
† Reference Application Note M538 for lead-free solder reflow recommendations.  
Meets JEDEC moisture sensitivity level 1 requirements.

Typical Performance Curves @ +25°C, 50 - 1000 MHz, Shunt Bias = 0.75 Volts

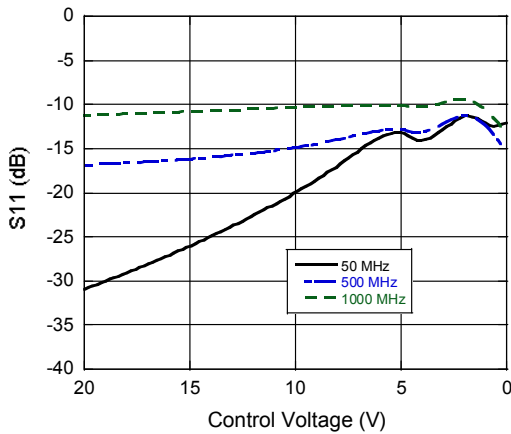
Insertion Loss vs. Frequency



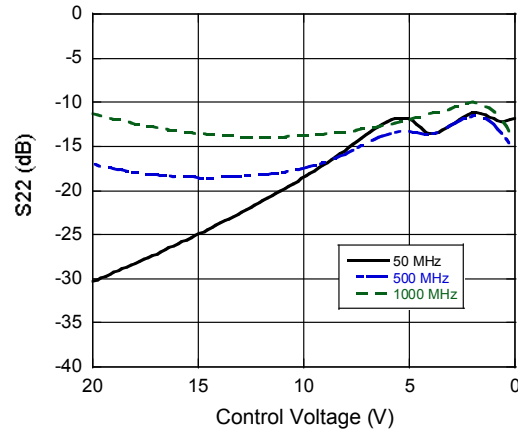
Attenuation vs. Control Voltage



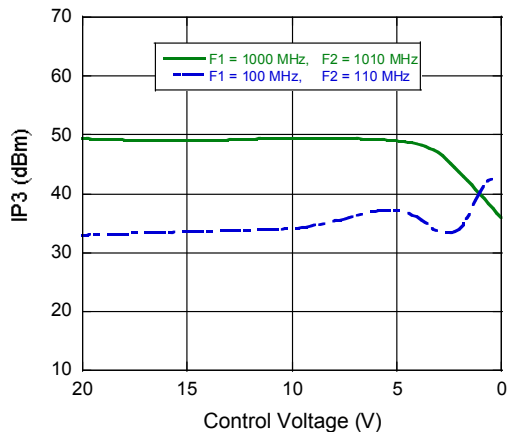
Input Return Loss vs. Control Voltage



Output Return Loss vs. Control Voltage



IP3 vs. Control Voltage



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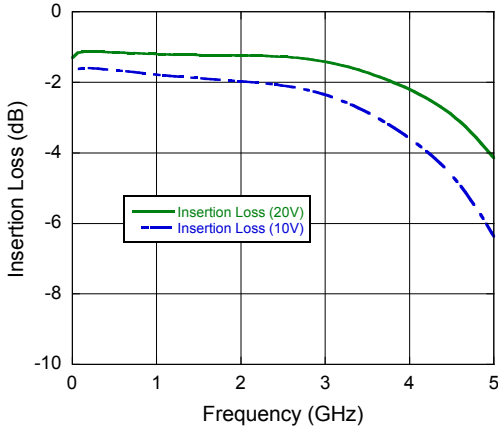
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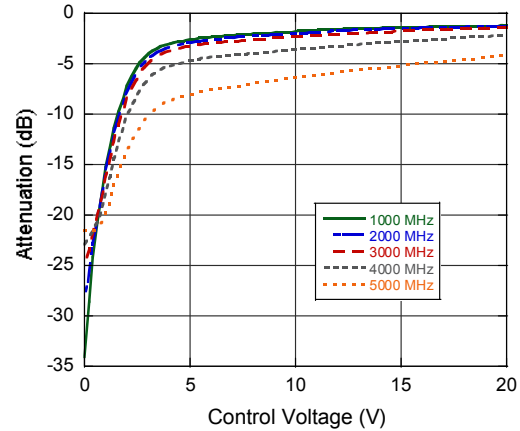
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### Typical Performance Curves @ +25°C, 1000 - 5000 MHz, Shunt Bias = 0.75 Volts

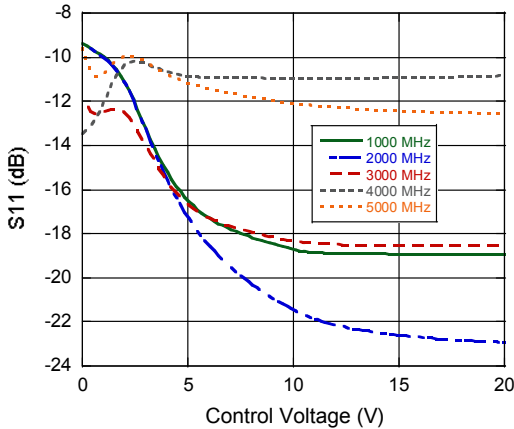
**Insertion Loss vs. Frequency**



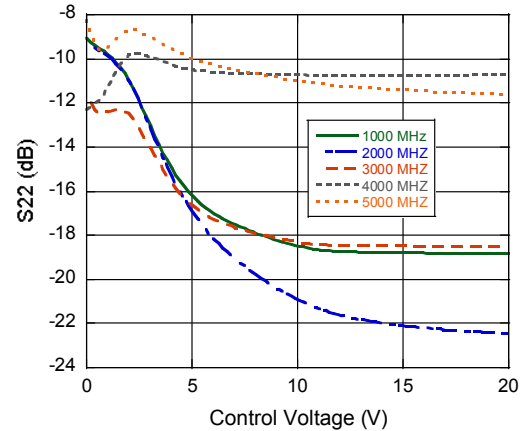
**Attenuation vs. Control Voltage**



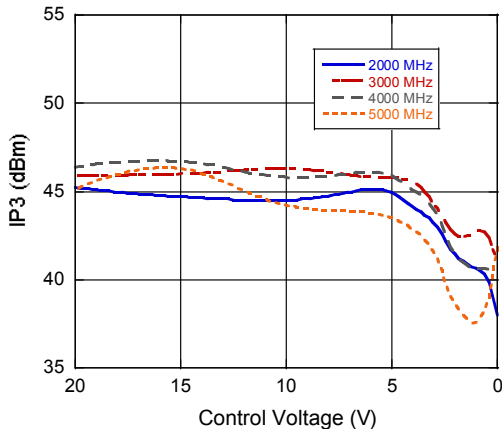
**Input Return Loss vs. Control Voltage**



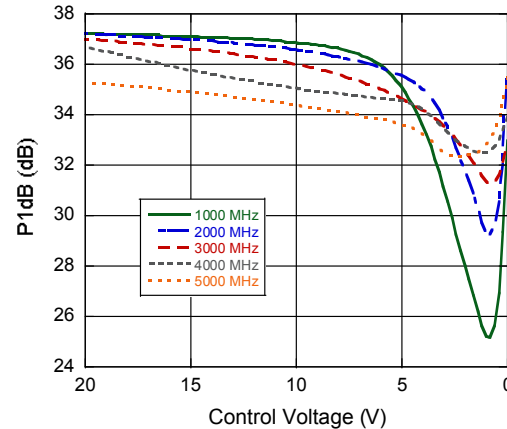
**Output Return Loss vs. Control Voltage**



**IP3 vs. Control Voltage (10 MHz Spacing)**



**P1dB vs. Control Voltage**



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