HMC948LP3E

54 dB, LOGARITHMIC DETECTOR, 1 - 23 GHz

Typical Applications

The HMC948LP3E is ideal for:

- Point-to-Point Microwave Radio
- VSAT
- Wideband Power Monitoring
- Receiver Signal Strength Indication (RSSI)
- Test & Measurement

Features

Wide Input Bandwidth: 1 to 23 GHz

Wide Dynamic Range: 54 dB up to 23 GHz

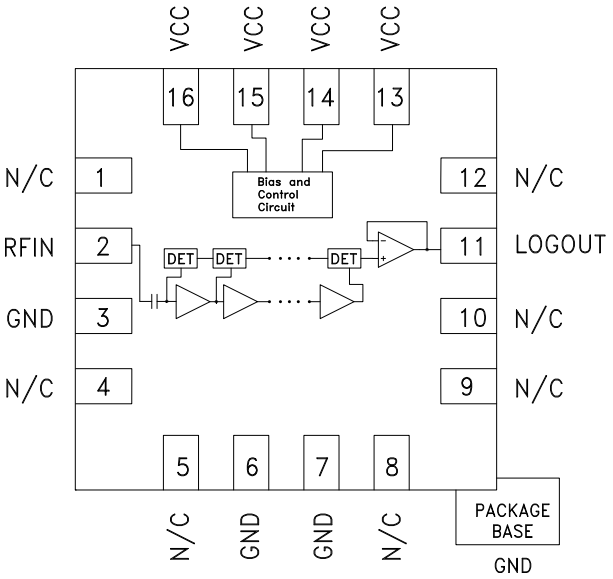
Single Positive Supply: +3.3V

Excellent Stability Over Temperature

Fast Rise / Fall Time: 5 / 7 ns

16 Lead 3x3 mm SMT Package: 9 mm²

Functional Diagram



General Description

The HMC948LP3E Logarithmic Detector converts RF signals at its input, to a proportional DC voltage at its output. The HMC948LP3E employs successive compression topology which delivers high dynamic range over a wide input frequency range. As the input power is increased, successive amplifiers move into saturation one by one creating an approximation of the logarithm function. The output of a series of square law detectors is summed, converted into the voltage domain and buffered to drive the LOG OUT output. The HMC948LP3E provides a nominal logarithmic slope of +14.2 mV/dB and an intercept of -111 dBm at 23 GHz. Ideal as a log detector for high volume microwave radio and VSAT applications, the HMC948LP3E is housed in a compact 3x3 mm RoHS compliant SMT plastic package.

Electrical Specifications, T_A = +25 C Vcc = +3.3V

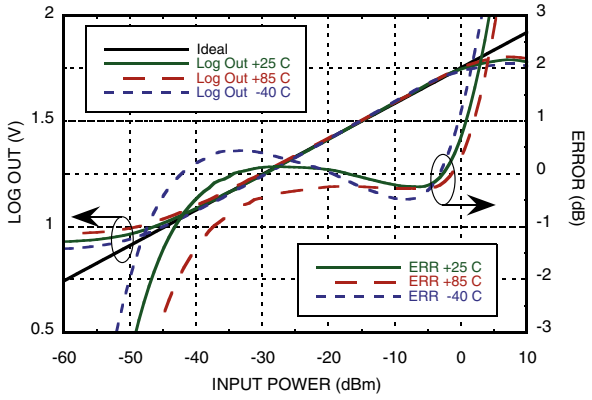
Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Input Frequency	1	5	10	14	18	20	23	GHz
±3 dB Dynamic Range	53	54	54	55	55	55	55	dB
±3 dB Dynamic Range Center	-23	-25	-24	-22	-20	-15	-15	dBm
Log Error Over Temperature (-40 to +85)	±1	±1	±1	±1.5	±1.5	±1.5	±1.5	dB
Output Intercept	-104	-107	-109	-112	-113	-108	-111	dBm
Output Slope	16.8	16.7	15.9	15.2	14.6	14.4	14.2	mV/dB

Electrical Specifications, (continued)

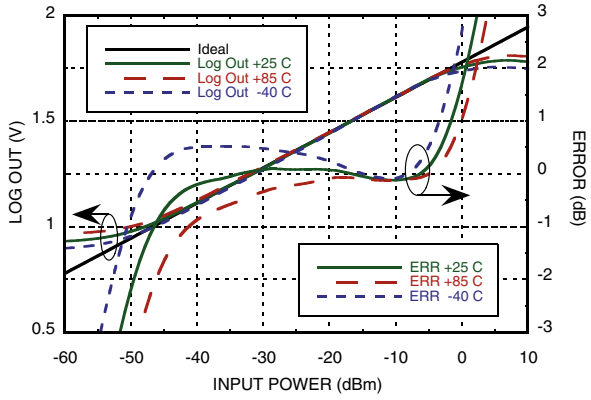
Parameter	Conditions	Min.	Typ.	Max.	Units
LOGOUT Interface					
Output Voltage Range		0.9		1.8	V
Output Rise Time [1] / Fall Time [2]	f = 10 GHz		5 / 7		ns
Power Supply (Vcc)					
Operating Voltage Range		3.15	3.3	3.45	V
Supply Current in Normal Mode			91		mA

[1] 0 dBm Input Pulsed; measured from 10% to 90%
[2] 0 dBm Input Pulsed; measured from 90% to 10%

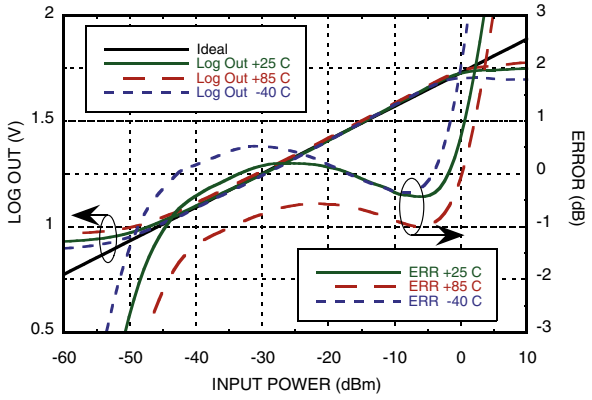
LOG OUT & Error vs. Input Power, Fin = 1 GHz



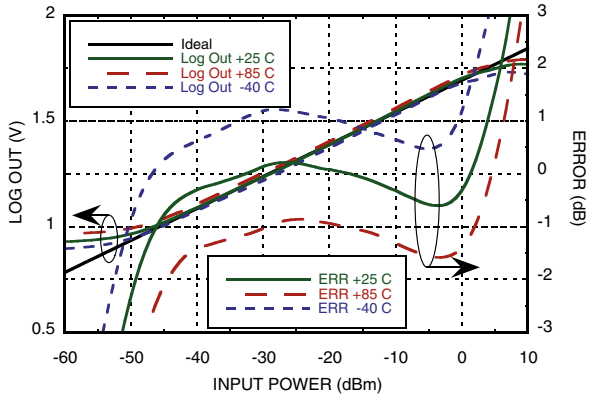
LOG OUT & Error vs. Input Power, Fin = 5 GHz



LOG OUT & Error vs. Input Power, Fin = 10 GHz

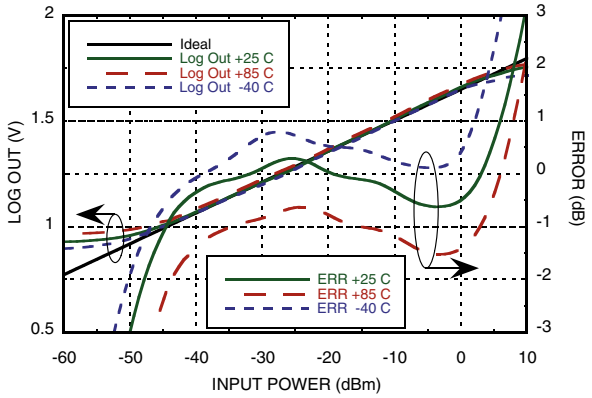


LOG OUT & Error vs. Input Power, Fin = 14 GHz

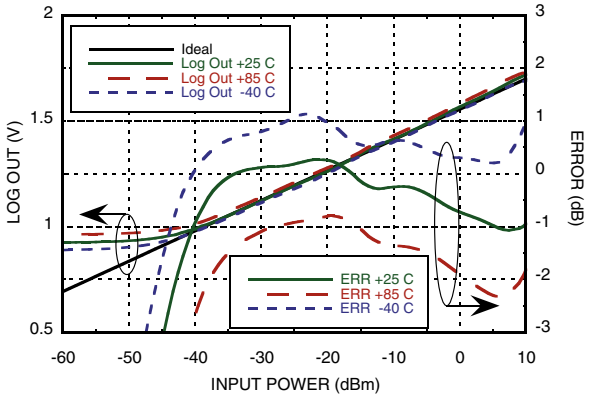


Unless otherwise noted: Vcc = +3.3V, T_A = +25 °C

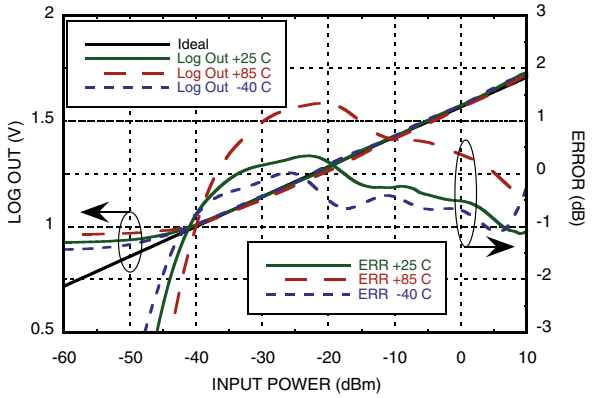
LOG OUT & Error vs. Input Power, Fin = 18 GHz



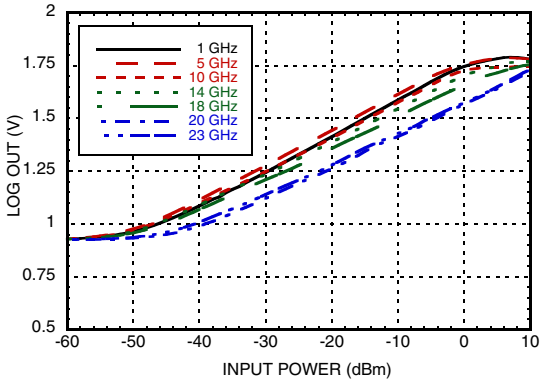
LOG OUT & Error vs. Input Power, Fin = 20 GHz



LOG OUT & Error vs. Input Power, Fin = 23 GHz

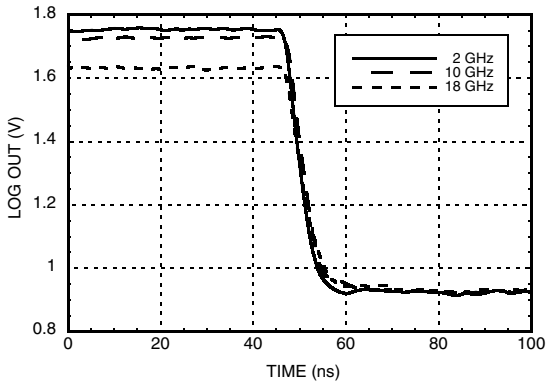


LOG OUT vs. Frequency

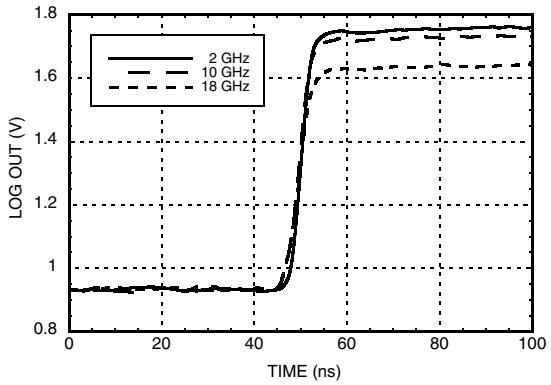


Unless otherwise noted: Vcc = +3.3V, T_A = +25 °C

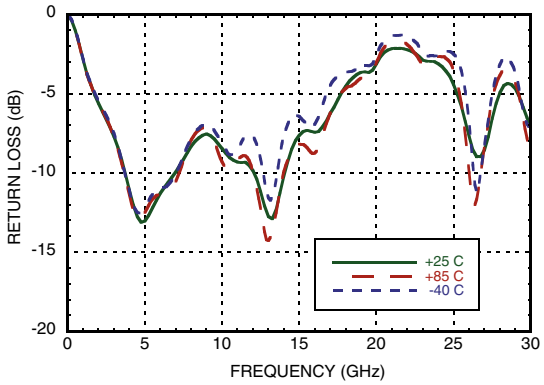
Fall Time for Various Frequencies @ 0 dBm



Rise Time for Various Frequencies @ 0 dBm



Input Return Loss



Unless otherwise noted: Vcc = +3.3V, T_A = +25 °C

HMC948LP3E

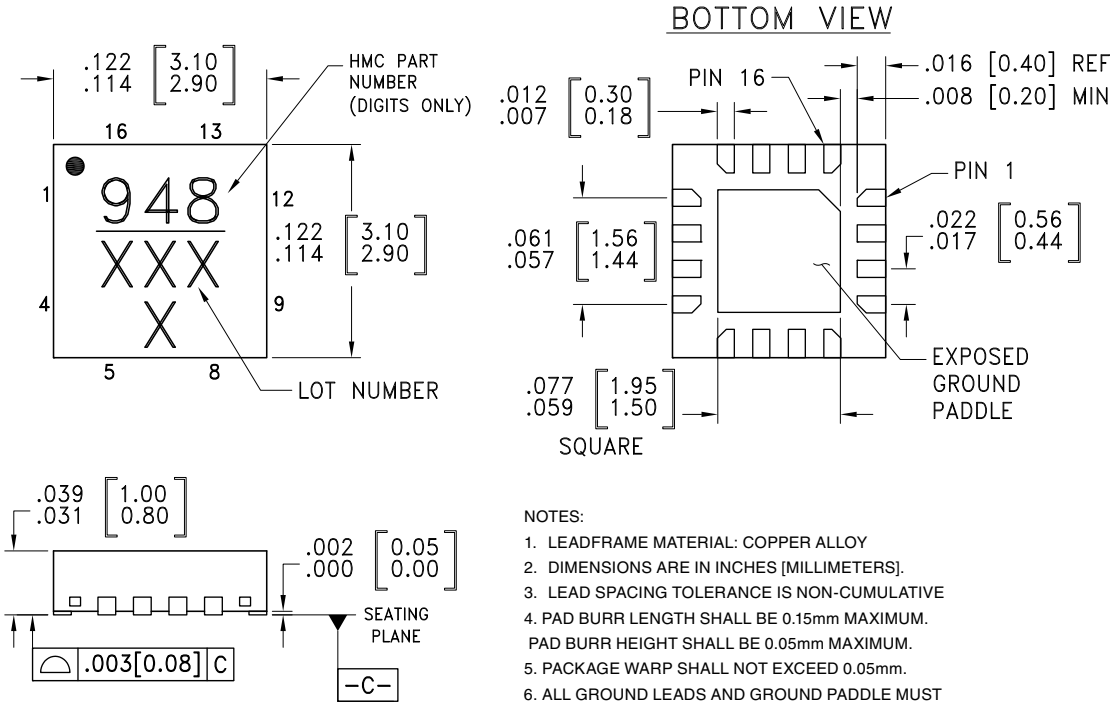
54 dB, LOGARITHMIC DETECTOR, 1 - 23 GHz

Absolute Maximum Ratings

Vcc	+3.6V
RF Input Power	+15 dBm
Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (Derate 11.62 mW/°C above 85°C)	0.46W
Thermal Resistance (R_{th}) (junction to ground paddle)	86.09 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

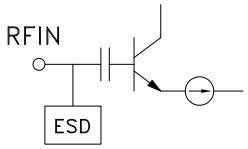
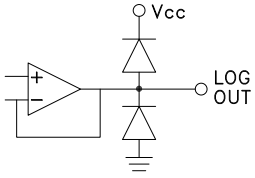
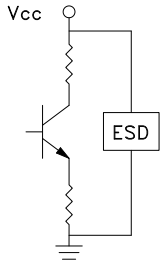
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HMC APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

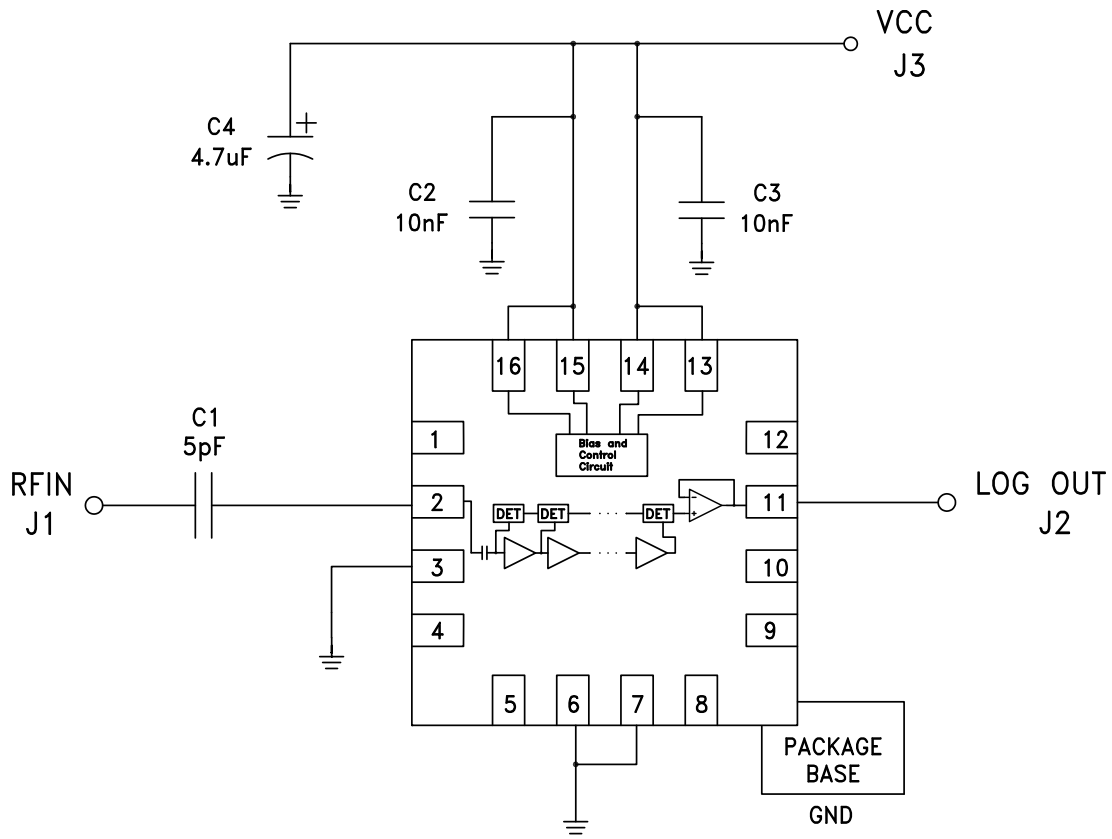
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC948LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	948 XXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

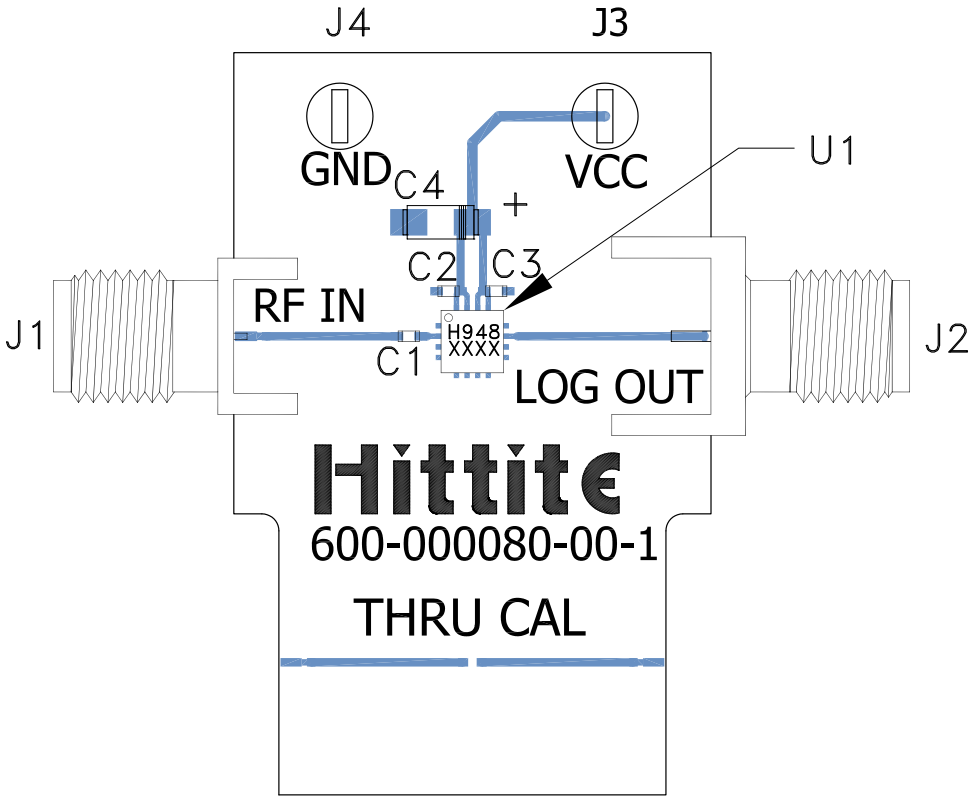
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 10, 12	N/C	No connection necessary. These pins may be connected to RF/DC ground without affecting performance.	
2	RFIN	RF input pin.	
3, 6, 7	GND	These pins and the exposed package bottom must be connected to a high quality RF/DC ground.	
11	LOG OUT	Log out. These pins should be connected to each other through a 0 ohm resistor. See application circuit.	
13 - 16	Vcc	Bias Supply. Connect supply voltage to these pins with appropriate filtering.	

Application & Evaluation PCB Schematic



Evaluation PCB



List of Materials for Evaluation PCB 132032 [1]

Item	Description
J1	K-Type Connector
J2	SMA Connector
J3, J4	DC Pin
C1	5 pF Capacitor, 0402 Pkg.
C2, C3	10 nF Capacitor, 0402 Pkg.
C4	4.7 µF Tantalum Capacitor, CASE A Pkg.
U1	HMC948LP3E Log Detector
PCB [2]	600-00008-00 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25 FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the pckage ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.