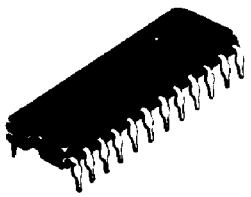
ACIA (Asynchronous Communications Interface Adapter)

The HD6350/HD6850 Asynchronous Communications Interface Adapter provides the data formating and control to interface serial asynchronous data communications information to bus organized systems such as the HMCS6800 Microprocessing Unit.

The bus interface of the HD6350/HD6850 includes select, enable, read/writer, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface with proper formating and error checking.

The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modern operation three control lines are provided.

HD6350P, HD6850P



(DP-24)

FEATURES

- Serial/Parallel Conversion of Data
- Seven and Eight-bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Peripheral/Modem Control Functions (Clear to Send $\overline{CTS}$, Request to Send $\overline{RTS}$, Data Carrier Detect $\overline{DCD}$)
- Optional ÷ 1, ÷ 16, and ÷ 64 Clock Modes
- One-or Two-Stop Bit Operation
- Double Buffered

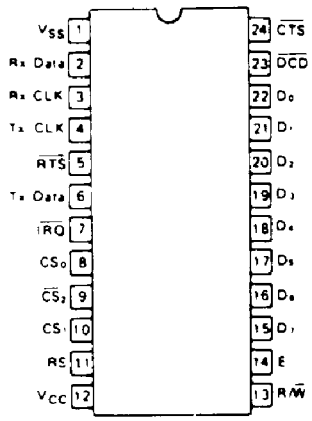
– HD6350 –

- Low-Power, High-Speed, High-Density CMOS
- Compatible with NMOS ACIA (HD6850)
- Wide Range Operating Voltage (V_{CC} = 5V ± 10%)
- Up to 1Mbps Transmission

– HD6850 –

- Compatible with MC6850 and MC68A50
- Up to 500Kbps Transmission

■ PIN ARRANGEMENT



(Top View)

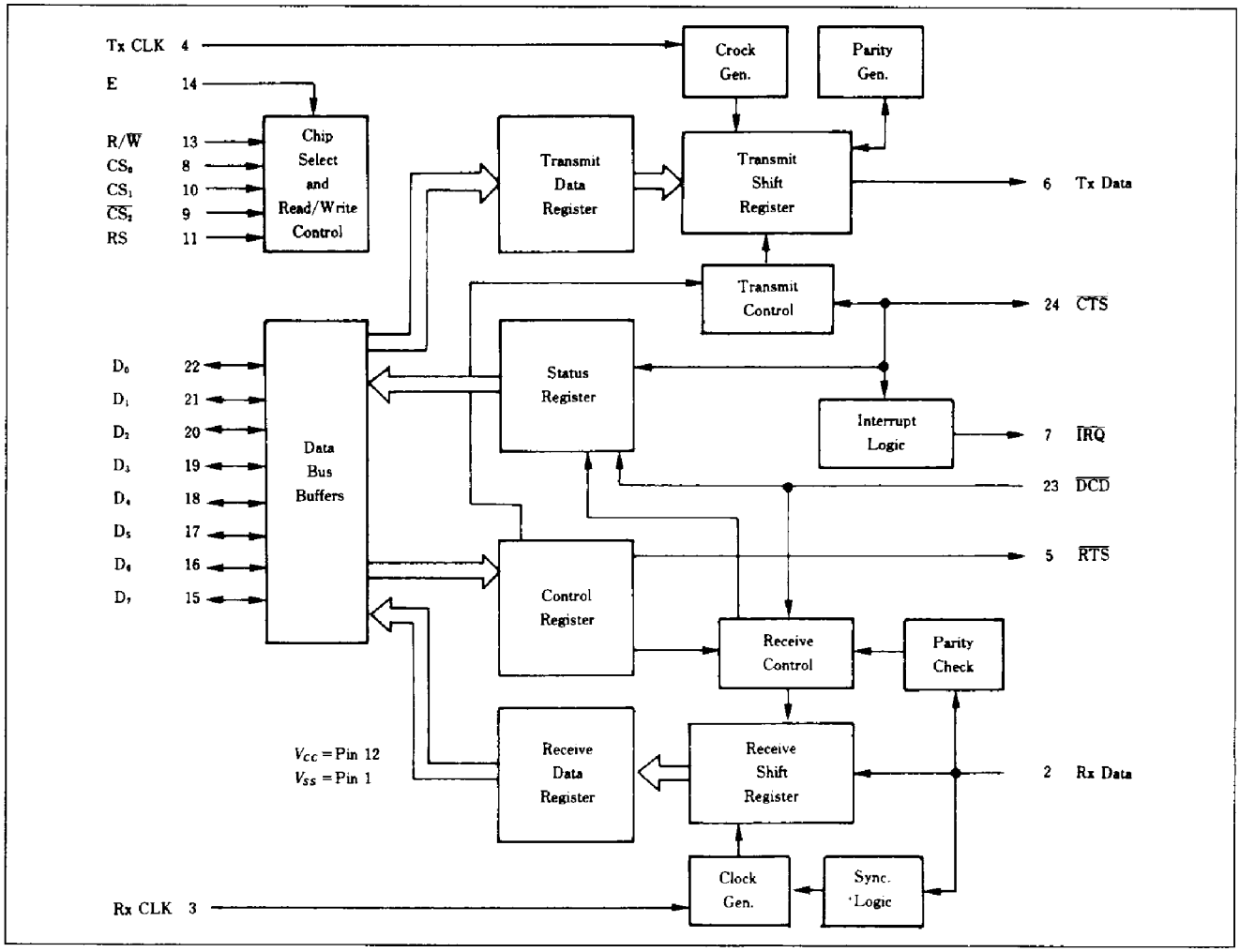
■ TYPE OF PRODUCTS

Type	Process	Clock Frequency	Package
HD6350P	CMOS	1.0MHz	DP-24
HD63A50P		1.5MHz	
HD63B50P		2.0MHz	
HD6350FP	CMOS	1.0MHz	FP-24D
HD63A50FP		1.5MHz	
HD63A50FP		2.0MHz	
HD6850	NMOS	1.0MHz	DC-24
HD68A50		1.5MHz	
HD6850P	NMOS	1.0MHz	DP-24
HD68A50P		1.5MHz	

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■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM PATINGS

Item	Symbol	Value		Unit
		HD6350	HD6850	
Supply Voltage	V_{cc}*	−0.3 ~+7,0	−0.3 ~+7.0	V
Input Voltage	V_{in}*	−0.3 ~+7.0	−0.3 ~+7.0	V
Maximum Output Current**	$\|I_O\|$**	10		mA
Operating Temperature	T_{opr}	−20 ~+75	−20 ~+75	°C
Storage Temperature	T_{stg}	−55 ~+150	−55 ~+150	°C

* With respect to V_{SS} (SYSTEM GND)

** Maximum output current is the maximum current which can flow out from one output terminal or I/O common terminal ($D_0 \sim D_7$, RTS. Tx Data, IRQ).

(NOTE) Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

■ RECOMMENDED OPERATING CONDITIONS

Item		Symbol	HD6350			HD6850			Unit
			min	typ	max	min	typ	max	
Supply Voltage		V_{cc}*	4.5	5.0	5.5	4.75	5.0	5.25	V
Input "Low" Voltage		V_{IL}*	0	–	0.8	−0.3	–	0.8	V
Input "High" Voltage	$D_0 \sim D_7$, RS, Tx CLK, $\overline{DCD}$, $\overline{CTS}$ Rx Data	V_{IH}*	2.0	–	V_{cc}	2.0	–	V_{cc}	V
	CS_0, $\overline{CS_2}$, CS_1, R/$\overline{W}$, E, Rx CLK		2.2	–	V_{cc}				
Operating Temperature		T_{opr}	−20	25	75	−20	25	75	°C

* With respect to V_{SS} (SYSTEM GND)

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■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (HD6350; V_{CC} = 5V ±10%, HD6850; V_{CC} = 5V ±5%, V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)

Item		Symbol	HD6350				HD6850				Unit
			Test Condition	min	typ*	max	Test Condition	min	typ*	max	
Input "High" Voltage	D_0 ~ D_7, RS, Tx CLK, $\overline{DCD}$, $\overline{CTS}$, Rx Data	V_{IH}		2.0	–	V_{CC}		2.0	–	V_{CC}	V
	CS_0, $\overline{CS_2}$, CS_1, R/$\overline{W}$, E Rx CLK			2.2	–	V_{CC}					
Input "Low" Voltate	All Inputs	V_{IL}		−0.3	–	0.8		−0.3	–	0.8	V
Input Leakage Current	R/$\overline{W}$, CS_0, CS_1, CS_2, E	I_{in}	V_{in} = 0 ~ V_{CC}	−2.5	–	2.5	V_{in} = 0 ~ 5.25V	−2.5	–	2.5	μA
Three-State (Off State) Input Current	D_0 ~ D_7	I_{TSI}	V_{in} = 0.4 ~ V_{CC}	−10	–	10	V_{in} = 0.4 ~ 2.4V	−10	–	10	μA
Output "High" Voltage	D_0 ~ D_7	V_{OH}	I_{OH} = −400μA	4.1	–	–	I_{OH} = −205μA, Enable Pulse Width ≦ 25μs	2.4	–	–	V
			I_{OH} ≦ −10μA	V_{CC}−0.1	–	–					
	Tx Data, $\overline{RTS}$		I_{OH} = −400μA	4.1	–	–	I_{OH} = −100μA, Enable Pulse Width ≦ 25μs	2.4	–	–	V
			I_{OH} ≦ −10μA	V_{CC}−0.1	–	–					
Output "Low" Voltage	All Outputs	V_{OL}	I_{OH} = 1.6mA	–	–	0.4	I_{OL} = −1.6mA Enable Pulse Width ≦ 25μs	–	–	0.4	V
Output Leakage Current (Off State)	$\overline{IRQ}$	I_{LOH}	V_{OH} = V_{CC}	–	–	10	V_{OH} = 2.4V	–	–	10	μA
Input Capacitance	D_0 ~ D_7	C_{in}	V_{in} = 0V, T_a = 25°C, f = 1.0 MHz	–	–	12.5	V_{in} = 0V, T_a = 25°C, f = 1.0 MHz	–	–	12.5	pF
	E, Tx CLK, Rx CLK, R/W, RS, RX Data, CS_0, CS_1, $\overline{CS_2}$, $\overline{CTS}$, $\overline{DCD}$			–	–	7.5		–	–	7.5	
Output Capacitance	$\overline{RTS}$, Tx Data	C_{out}	V_{in} = 0V, T_a = 25°C, f = 1.0 MHz	–	–	10	V_{in} = 0V, T_a = 25°C f = 1.0 MHz	–	–	10	pF
	$\overline{IRQ}$			–	–	5.0		–	–	5.0	
Supply Current	• Under transmitting and Receiving operation • 500 kbps • Data bus in R/W operation		E = 1.0 MHz	–	–	3					mA
			E = 1.5 MHz	–	–	4					
			E = 2.0 MHz	–	–	5					
	• Chip is not selected. • 500 kbps • Under non transmitting and receiving operation • Input level (Except E) V_{IH} min = V_{CC}−0.8V V_{IL} max = 0.8V.		E = 1.0 MHz	–	–	200					
			E = 1.5 MHz	–	–	250					
			E = 2.0 MHz	–	–	300					
Power Dissipation		P_D						–	300	525	mW

* T_a = 25°C, V_{CC} = 5.0V

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- **AC CHARACTERISTICS (HD6350; V_{CC} = 5.0V ±10%, HD6850; V_{CC} = 5V ±5%, V_{SS} = 0V, T_a = −20~+75°C, unless otherwise noted.)**

1. TIMING OF DATA TRANSMISSION

Item		Symbol	Test Condition	HD6350		HD63A50		HD63B50		HD6850 /HD68A50		Unit
				min	max	min	max	min	max	min	max	
Minimum Clock Pulse Width	+1 Mode	PW_{CL}	Fig. 1	900	–	650	–	500	–	900	–	ns
	+16, +64 Modes			600	–	450	–	280	–	600	–	ns
	+1 Mode	PW_{CH}	Fig. 2	900	–	650	–	500	–	900	–	ns
	+16, +64 Modes			600	–	450	–	280	–	600	–	ns
Clock Frequency	+1 Mode	f_C		–	500	–	750	–	1000	–	500	kHz
	+16, +64 Modes			–	800	–	1000	–	1500	–	800	
Clock-to-Data Delay for Transmitter		t_{TDD}	Fig. 3	–	600	–	540	–	460	–	1000	ns
Receive Data Setup Time	+1 Mode	t_{RDSU}	Fig. 4	250	–	100	–	30	–	500	–	ns
Receive Data Hold Time	+1 Mode	t_{RDH}	Fig. 5	250	–	100	–	30	–	500	–	ns
$\overline{IRQ}$ Release Time		t_{IR}	Fig. 6	–	1200	–	900	–	700	–	1200	ns
$\overline{RTS}$ Delay Time		t_{RTS}	Fig. 6	–	560	–	480	–	400	–	1000	ns
Rise Time and Fall Time (or 10% of the pulse width if smaller)		t_r, t_f		–	1000	–	500	–	250	–	1000	ns

2. BUS TIMING CHARACTERISTICS

1) READ

Item	Symbol	Test Condition	HD6350		HD63A50		HD63B50		HD6850		HD68A50		Unit
			min	max	min	max	min	max	min	max	min	max	
Enable Cycle Time	t_{cycE}	Fig. 7	1000	–	666	–	500	–	1000	–	666	–	ns
Enable "High" Pulse Width	PW_{EH}	Fig. 7	450	–	280	–	220	–	450	25000	280	25000	ns
Enable "Low" Pulse Width	PW_{EL}	Fig. 7	430	–	280	–	210	–	430	–	280	–	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	t_{AS}	Fig. 7	80	–	60	–	40	–	140	–	140	–	ns
Data Delay Time	t_{DDR}	Fig. 7	–	290	–	180	–	150	–	320	–	220	ns
Data Hold Time	t_H	Fig. 7	20	100	20	100	20	100	10	–	10	–	ns
Address Hold Time	t_{AH}	Fig. 7	10	–	10	–	10	–	10	–	10	–	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	Fig. 7	–	25	–	25	–	20	–	25	–	25	ns

2) WRITE

Item	Symbol	Test Condition	HD6350		HD63A50		HD63B50		HD6850		HD68A50		Unit
			min	max	min	max	min	max	min	max	min	max	
Enable Cycle Time	t_{cycE}	Fig. 8	1000	–	666	–	500	–	1000	–	666	–	ns
Enable "High" Pulse Width	PW_{EH}	Fig. 8	450	–	280	–	220	–	450	25000	280	25000	ns
Enable "Low" Pulse Width	PW_{EL}	Fig. 8	430	–	280	–	210	–	430	–	280	–	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	t_{AS}	Fig. 8	80	–	60	–	40	–	140	–	140	–	ns
Data Setup Time	t_{DSW}	Fig. 8	165	–	80	–	60	–	195	–	80	–	ns
Data Hold Time	t_H	Fig. 8	10	–	10	–	10	–	10	–	10	–	ns
Address Hold Time	t_{AH}	Fig. 8	10	–	10	–	10	–	10	–	10	–	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	Fig. 8	–	25	–	25	–	20	–	25	–	25	ns

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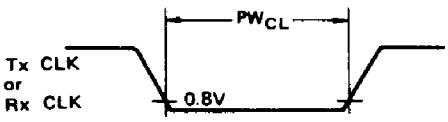


Figure 1 Clock Pulse Width, "Low" State

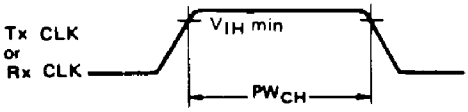


Figure 2 Clock Pulse Width, "High" State

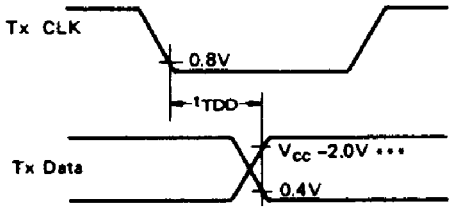


Figure 3 Transmit Data Output Delay

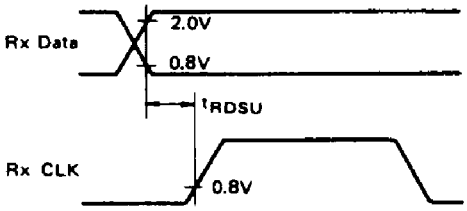


Figure 4 Receive Data Setup Time (÷1 Mode)

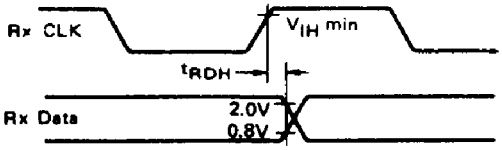
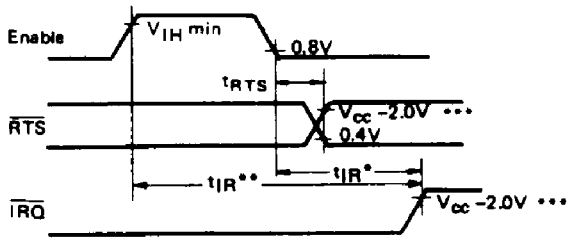


Figure 5 Receive Data Hold Time (÷1 Mode)



* (1) $\overline{IRQ}$ Release Time applied to Rx Data Register read operation.
(2) $\overline{IRQ}$ Release Time applied to Tx Data Register write operation.
(3) $\overline{IRQ}$ Release Time applied to control Register write TIE = 0, RIE = 0 operation.

** $\overline{IRQ}$ Release Time applied to Rx Data Register read operation right after read status register, when $\overline{IRQ}$ is asserted by $\overline{DCD}$ rising edge.

*** 2.4V for HD6850.

(Note) Note that followings take place when $\overline{IRQ}$ is asserted by the detection of transmit data register empty status. $\overline{IRQ}$ is released to "High" asynchronously with E signal when $\overline{CTS}$ goes "High". (Refer to Figure 14)

Figure 6 $\overline{RTS}$ Delay and $\overline{IRQ}$ Release Time

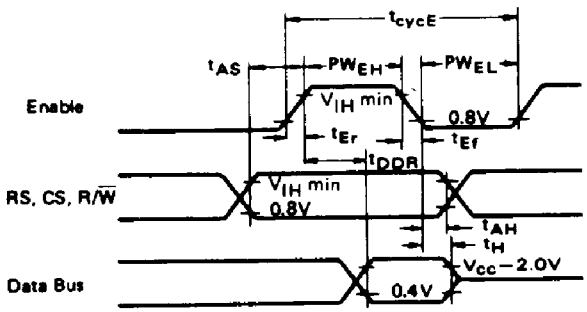


Figure 7 Bus Read Timing Characteristics
(Read information from ACIA)

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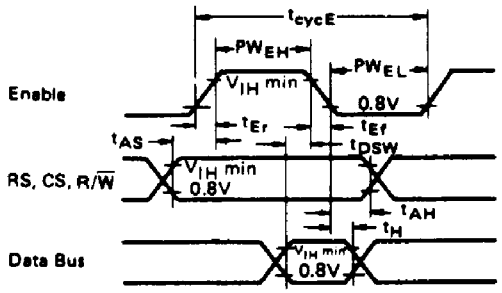
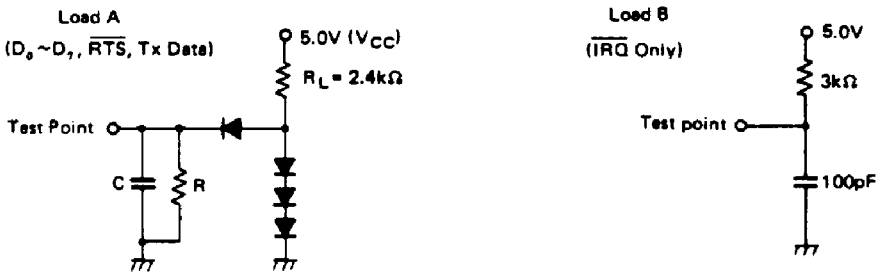


Figure 8 Bus Write Timing Characteristics
(Write information into ACIA)



C = 130pF for D_0~D_7
= 30pF for $\overline{RTS}$ and Tx Data
R* = 10kΩ for D_0 ~ D_7, $\overline{RTS}$ and Tx Data
All diodes are 1S2074Ⓗ or Equivalent.

* HD6850
R = 11kΩ for D_0 ~ D_7
= 24kΩ for RTS and Tx Data.

Figure 9 Bus Timing Test Loads

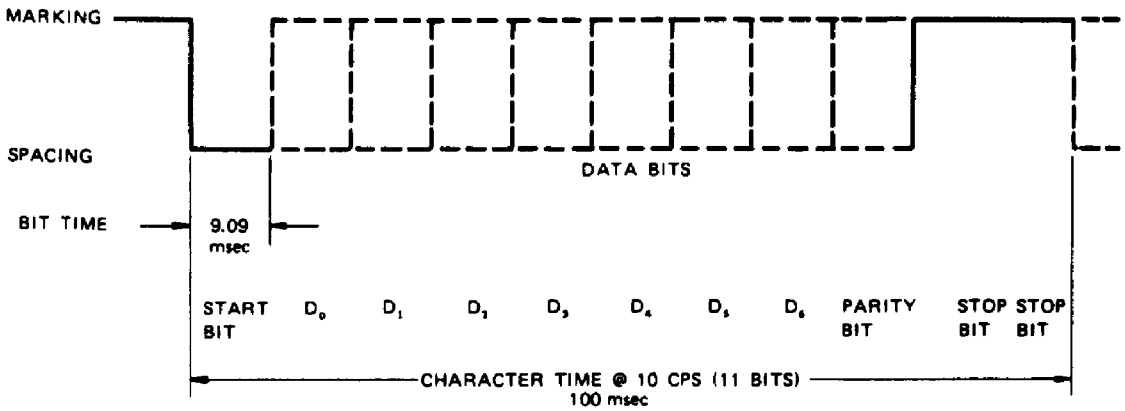
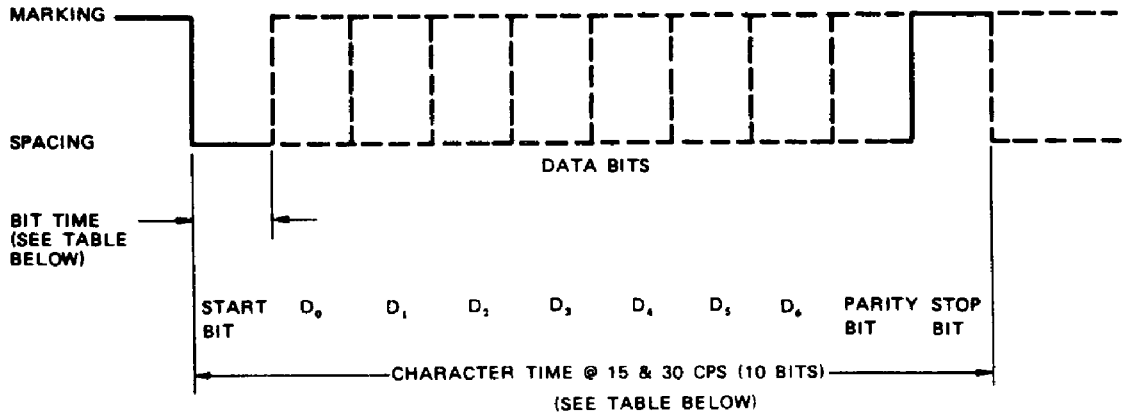


Figure 10 110 Baud Serial ASCII Data Timing

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BAUD RATE	150	300
CHARACTERS/SEC	15	30
BIT TIME (msec)	6.67	3.33
CHARACTER TIME (msec)	66.7	33.3

$$\text{BIT TIME} = \frac{\text{SEC}}{\text{BAUD RATE}}$$

Figure 11 150 & 300 Baud Serial ASCII Data Timing

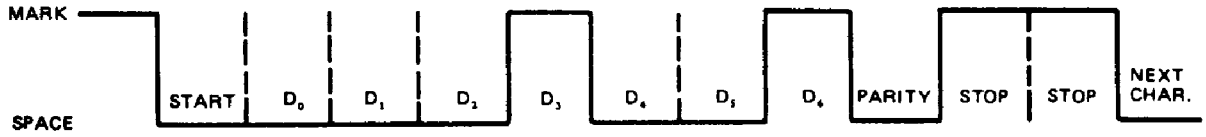


Figure 12 Send a 7 Bit ASCII Char. "H" Even Parity
– 2 Stop Bits H = 48_{16} = 1001000_2

■ DATA OF ACIA

ACIA is an interface adappter which controls transmission and reception of Asynchronous serial data. Some examples of serial data are shown in Figs. 10 ~ 12.

■ INTERNAL STRUCTURE OF ACIA

ACIA provides the following; 8-bit Bi-directional Data Buses (D_0 ~ D_7), Receive Data Input (Rx Data), Transmit Data Output (Tx Data), three Chip Selects (CS_0, CS_1, $\overline{CS_2}$), Register Select Input (RS), Two Control Input (Read/Write: R/$\overline{W}$, Enable: E), Interrupt Request Output($\overline{IRQ}$), Clear-to-Send ($\overline{CTS}$) to control the modem, Request-to-Send ($\overline{RTS}$), Data Carrier Detect($\overline{DCD}$) and Clock Inputs(Tx CLK, Rx CLK) used for synchronization of received and transmitted data. This ACIA also provides four registers; Status Register, Control Register, Receive Register and Transmit Register.

24-pin dual-in-line type package is used for the ACIA. Internal Structure of ACIA is illustrated in Fig. 13.

■ ACIA OPERATION

• Master Reset

ACIA has an internal master reset function controlled by software, since it has no hardware reset pin. Bit 0 and bit 1 of control register should be set to "11" to execute master reset, also bit 5 and bit 6 should be programmed to get predetermined $\overline{RTS}$ output accordingly. To release the master reset, the data other than "11" should be written into bit 0, bit 1 of the control register. When the master reset is released, the control register needs to be programmed to get predetermined options such as clock divider ratios, word length, one or two stop bits, parity(even, old, or none), etc.

It may happen that "Low" level output is provided in $\overline{IRQ}$ pin during the time after power-on till master reset. In the system using ACIA, interrupt mask bit of MPU should be released after the master reset of ACIA. (MPU interrupt should be prohibited until MPU program completes the master reset of ACIA.) Transmit Data Register (TDR) and Receive Data Register (RDR) can not be reset by master reset.

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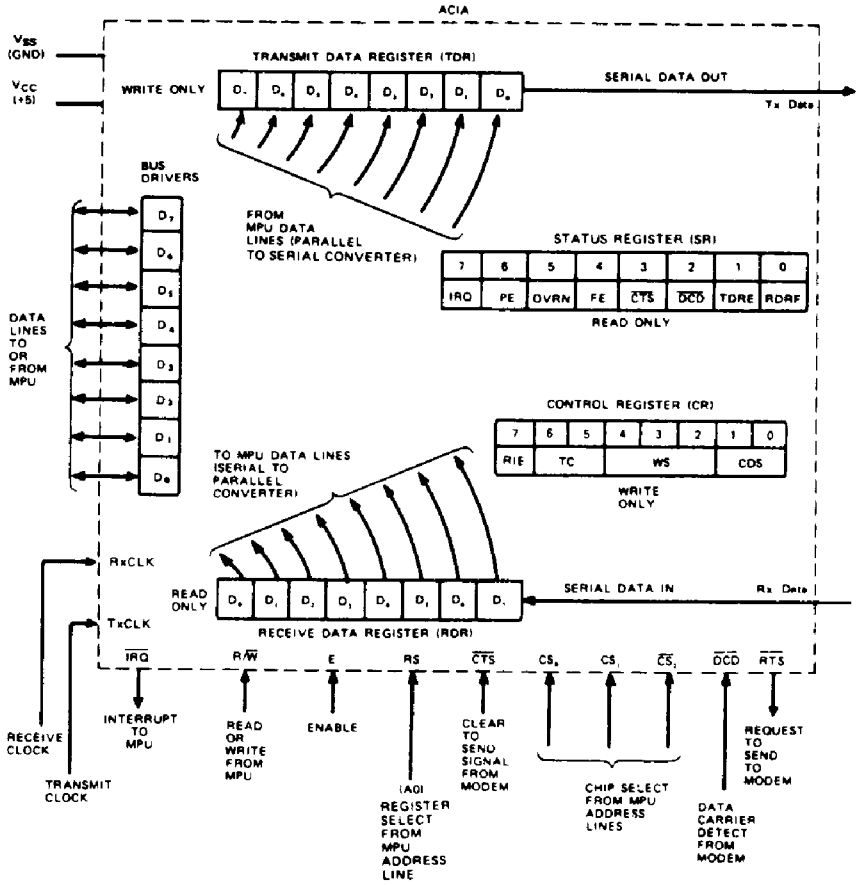


Figure 13 Internal Structure of ACIA

- **Transmit**

A typical transmitting sequence consists of reading the ACIA Status Register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to a Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted (because of double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

- **Receive**

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divide-by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of the leading mark-space transition of the start bit. False start bit delection capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the MPU. When parity has been selected for an 8-bit word (7 bits plus parity), the receiver strip the parity bit (D_7="0") so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read again to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the Shift register. The above sequence continues until all characters have been received.

■ ACIA INTERNAL REGISTERS

The ACIA provides four registers; Transmit Data Register (TDR), Receive Data Register(RDR), Control Register(CR) and Status Register(SR). The content of each of the registers is summarized in Table 1.

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Table 1 Definition of ACIA Register Contents

Buffer Address	RS=1 · R/$\overline{W}$=0 ****	RS=1 · R/$\overline{W}$=1	RS=0 · R/$\overline{W}$=0	RS=0 · R/$\overline{W}$=1
Data Bus	Transmit Data Register	Receiver Data Register	Control Register	Status Register
	(Write Only)	(Read Only)	(Write Only)	(Read Only)
0	Data Bit 0*	Data Bit 0	Counter Divide Select (CR0)	Rx Data Reg. Full (RDRF)
1	Data Bit 1	Data Bit 1	Counter Divide Select (CR1)	Tx Data Reg. Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Select 1 (CR2)	Data Carrier Detect ($\overline{DCD}$)
3	Data Bit 3	Data Bit 3	Word Select 2 (CR3)	Clear to Send ($\overline{CTS}$)
4	Data Bit 4	Data Bit 4	Word Select 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Tx Control 1 (CR5)	Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Tx Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Rx Interrupt Enable (CR7)	Interrupt Request (IRQ)

* Leading bit = LSB = Bit 0
** Data bit will be zero in 7-bit plus parity modes.
*** Data bit is "don't care" in 7-bit plus parity modes.
**** 1 ... "High" level, 0 ... "Low" level

- **Transmit Data Register (TDR)**

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the ACIA has been addressed and RS · R/$\overline{W}$ is selected. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go "0". Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within 2 bit time + several E cycles of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

- **Receive Data Register (RDR)**

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) on the status buffer to go "1" (full). Data may then be read through the bus by addressing the ACIA and R/$\overline{W}$ "High" when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

- **Control Register**

The ACIA Control Register consists of eight bits of write-only buffer that are selected when RS and R/$\overline{W}$ are "Low". This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send ($\overline{RTS}$) peripheral/modem control output.

Counter Divide Select Bits (CR0 and CR1)

The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver section of the ACIA. Additionally, these bits are used to provide a master reset for the ACIA which clears the Status Register (except for external conditions on $\overline{CTS}$ and $\overline{DCD}$) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set "1" to reset the ACIA. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

Table 2 Function of Counter Devide Select Bit

CR1	CR0	Function
0	0	÷1
0	1	÷16
1	0	÷64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4)

The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

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Table 3 Function of Word Select Bit

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6)

Two Transmitter Control bits provide for the control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send ($\overline{RTS}$) output, and the transmission of a Break level (space). The following encoding format is used:

Table 4 Function of Transmitter Control-Bit

CR6	CR5	Function
0	0	$\overline{RTS}$ = "Low", Transmitting Interrupt Disabled.
0	1	$\overline{RTS}$ = "Low", Transmitting Interrupt Enabled.
1	0	$\overline{RTS}$ = "High", Transmitting Interrupt Disabled.
1	1	$\overline{RTS}$ = "Low", Transmits a Break level on the Transmit Data Output. Transmitting Interrupt Disabled.

Receive Interrupt Enable Bit (CR7)

The following interrupts will be enabled by a "1" in bit position 7 of the Control Register (CR7): Receive Data Register Full, Overrun, or a "Low" to "High" transistion on the Data Carrier Detect ($\overline{DCD}$) signal line.

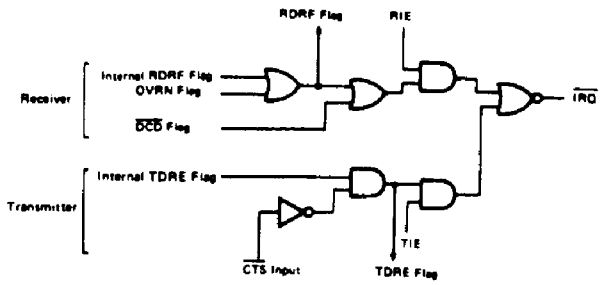


Figure 14 $\overline{IRQ}$ Internal Circuit

- **Status Register**

Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This read-only register is selected when RS is "Low" and R/$\overline{W}$ is "High". Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the ACIA.

Receive Data Register Full (RDRF), Bit 0

RDRF indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. Data Carrier Detect ($\overline{DCD}$) being "High" also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1

The Transmit Data Register Empty bit being set "1" indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The "0" state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect ($\overline{DCD}$), Bit 2

The $\overline{DCD}$ bit will be "1" when the $\overline{DCD}$ input from a modem has gone "High" to indicate that a carrier is not present. This bit going "1" causes an Interrupt Request to be generated when the Receive Interrupt Enable is set. It remains "1" after the $\overline{DCD}$ input is returned "Low" until cleared by first reading the Status Register and then the Data Register or until a master reset occurs. If the $\overline{DCD}$ input remains "High" after read status and read data or master reset has occurred, the interrupt is cleared, the $\overline{DCD}$ status bit remains "1" and will follow the $\overline{DCD}$ input.

Clear-to-Send ($\overline{CTS}$), Bit 3

The $\overline{CTS}$ bit indicates the state of the $\overline{CTS}$ input from a modem. A "Low" $\overline{CTS}$ input indicates that there is a $\overline{CTS}$ from the modem. In the "High" state, the Transmit Data Register Empty bit is inhibited and the $\overline{CTS}$ status bit will be "1". Master reset does not affect the Clear-to-Send Status bit.

Framing Error (FE), Bit 4

FE flag indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the 1st stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The FE flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN), Bit 5

Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register or by a Master Reset.

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Parity Error (PE), Bit 6

The PE flag indicates that the number of "1"s (highs) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request (IRQ), Bit 7

The IRQ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{IRQ}$ output is "Low" the IRQ bit will be "1" to indicate the interrupt or service request status. IRQ is cleared by a read operation to the Receive Data Register or a write operation to the Transmit Data Register. (Refer to Figure 14.)

■ SIGNAL FUNCTIONS

• Interface Signal for MPU

Bi-Directional Data Bus (D_0~D_7)

The bi-directional data bus (D_0~D_7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high impedance (off) state except when the MPU performs an ACIA read operation.

Enable (E)

The Enable signal, E, is a high impedance TTL compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the HMCS6800 ϕ_2 Clock. The ACIA accepts both continuous pulse signal and strobe type signal as Enable input.

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When R/$\overline{W}$ is "High" (MPU Read cycle), ACIA output drivers are turned on and a selected register is read. When it is "Low", the ACIA output drivers are turned off and the MPU writes into a selected register. Therefore, the R/$\overline{W}$ signal is used to select read-only or write-only registers within the ACIA.

Chip Select (CS_0, CS_1, $\overline{CS_2}$)

These three high impedance TTL compatible input lines are used to address the ACIA. The ACIA is selected when CS_0 and CS_1 are "High" and $\overline{CS_2}$ is "Low". Transfers of data to and from the ACIA are then performed under the control of the Enable signal, Read/Write, and Register Select.

Register Select (RS)

The RS line is a high impedance input that is TTL compatible. A "High" level is used to select the Transmit/Receive Data Registers and a "Low" level the Control/Status Registers. The R/$\overline{W}$ signal line is used in conjunction with Register Select to select the read-only or write-only register in each register pair.

Interrupt Request ($\overline{IRQ}$)

$\overline{IRQ}$ is a TTL compatible, open-drain (no internal pullup), active "Low" output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains "Low" as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set.

Clock Inputs

Separate high impedance TTL compatible inputs are provided for clocking of transmitted and received data. Clock frequencies of 1, 16 or 64 times the data rate may be selected.

Transmit Clock (Tx CLK)

The Tx CLK input is used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock.

Receive Clock (Rx CLK)

The Rx CLK input is used for synchronization of received data. (In the ÷ 1 mode, the clock and data must be synchronized externally.) The receiver samples the data on the positive transition of the clock.

• Serial Input/Output Lines

Receive Data (Rx Data)

The Rx Data line is a high impedance TTL compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used. Data rates are in the range of 0 to 500 kbps when external synchronization is utilized.

Transmit Data (Tx Data)

The Tx Data output line transfers serial data to a modem or other peripheral. Data rates in the range of 0 to 500 kbps when external synchronization is utilized.

Modem Control

The ACIA includes several functions that permit limited control of a peripheral or modem. The functions included are $\overline{CTS}$, $\overline{RTS}$ and $\overline{DCD}$.

Clear-to-Send ($\overline{CTS}$)

This high impedance TTL compatible input provides automatic control of the transmitting end of a communications link via the modem $\overline{CTS}$ active "Low" output by inhibiting the Transmit Data Register Empty (TDRE) status bit. (Refer to Figure 15.)

Request-to-Send ($\overline{RTS}$)

The $\overline{RTS}$ output enables the MPU to control a peripheral or modem via the data bus. The $\overline{RTS}$ output corresponds to the state of the Control Register bits CR5 and CR6. When CR6=0 or both CR5 and CR6=1, the $\overline{RTS}$ output is "Low" (the active state). This output can also be used for Data Terminal Ready ($\overline{DTR}$). (Refer to Figure 15.)

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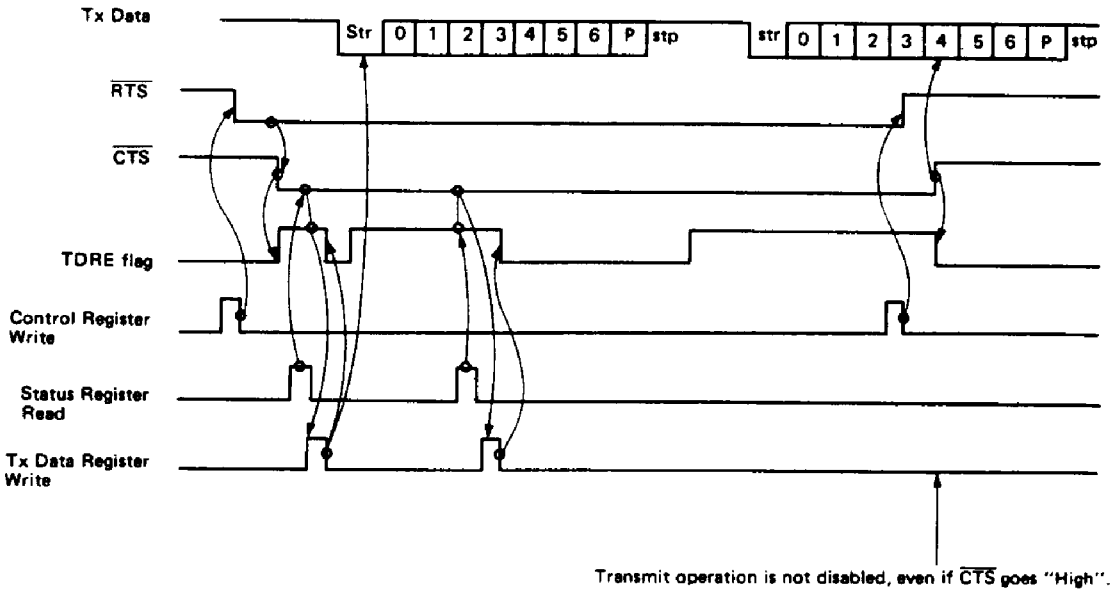


Figure 15 $\overline{RTS}$ and $\overline{CTS}$ Timing Chart (Example of 2 bytes transmission)

Data Carrier Detect ($\overline{DCD}$)

$\overline{DCD}$ is the input signal corresponding to the "carrier detect" signal which shows carrier detect of modem.

$\overline{DCD}$ signal is used to control the receiving operation. When $\overline{DCD}$ input goes "High", ACIA stops all the receiving operation and sets receiving part in reset status. It means that receive shift register stops shifting, error detection circuit and synchro, zation circuit of receive clock are reset. When $\overline{DCD}$ is in "High" level, the receiving part of ACIA is kept in initial status and the operation in the receiving part is prohibited. When $\overline{DCD}$ goes "Low", the receiving part is allowed to receive data. In this case, the following process is needed to reset $\overline{DCD}$ flag and restarts the receive operation. (Refer to Figure 16.)

(1) Return $\overline{DCD}$ input from "High" to "Low".
(2) Read status register. ($\overline{DCD}$ flag = "1")
(3) Read receive data register (Uncertain data will be read.)

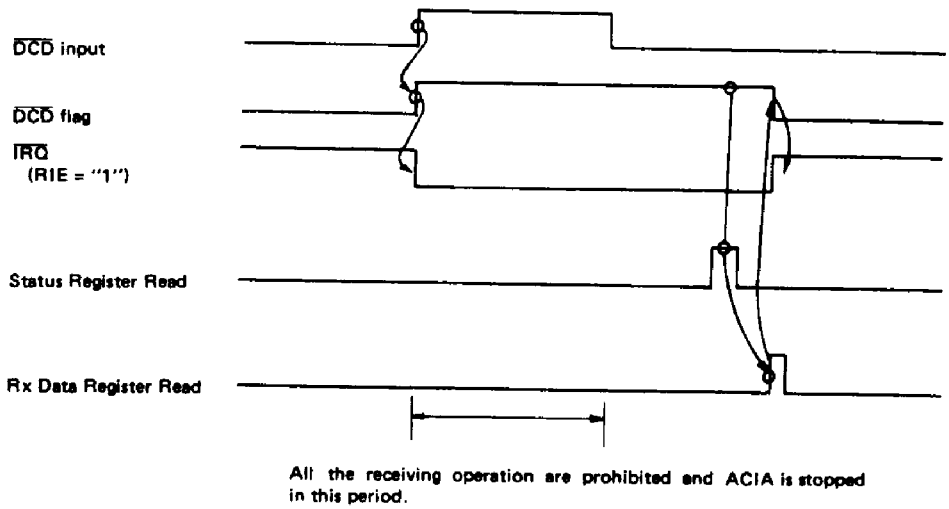


Figure 16 $\overline{DCD}$ Flag Timing Chart

■ **Note for Use** (HD6350 only)

Input Signal, which is not necessary for user's application, should be used fixed to "High" or "Low" level. This is applicable to the following signal pins.
Rx Data, Rx CLK, Tx CLK, $\overline{CTS}$, $\overline{DCD}$

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