BSS138LT1

Preferred Device

Power MOSFET 200 mA, 50 V

N−Channel SOT−23

Typical applications are DC−DC converters, power management in portable and battery−powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

Features

- Pb−Free Packages are Available
- Low Threshold Voltage ($V_{GS(th)}$: 0.5 V−1.5 V) Makes it Ideal for Low Voltage Applications
- Miniature SOT−23 Surface Mount Package Saves Board Space

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	50	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	± 20	Vdc
Drain Current − Continuous @ T_A = 25°C − Pulsed Drain Current ($t_p \le 10$ μs)	 I_D I_{DM}	 200 800	mA
Total Power Dissipation @ T_A = 25°C	P_D	225	mW
Operating and Storage Temperature Range	T_J, T_{stg}	− 55 to 150	°C
Thermal Resistance − Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Maximum Lead Temperature for Soldering Purposes, for 10 seconds	T_L	260	°C

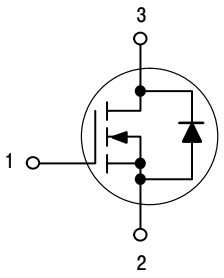
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

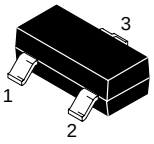
ON Semiconductor®

http://onsemi.com

200 mA, 50 V
$R_{DS(on)}$ = 3.5 Ω

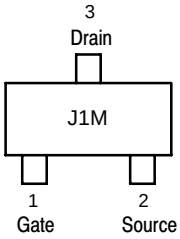
N−Channel





SOT−23
CASE 318
STYLE 21

MARKING DIAGRAM & PIN ASSIGNMENT



J1 = Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
BSS138LT1	SOT−23	3000 Tape & Reel
BSS138LT1G	SOT−23 (Pb−Free)	3000 Tape & Reel
BSS138LT3	SOT−23	10,000 Tape & Reel
BSS138LT3G	SOT−23 (Pb−Free)	10,000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	50	−	−	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	 − −	 − −	 0.1 0.5	μAdc
Gate−Source Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	−	−	±0.1	μAdc
ON CHARACTERISTICS (Note 1)						
Gate−Source Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mAdc)		$V_{GS(th)}$	0.5	−	1.5	Vdc
Static Drain−to−Source On−Resistance (V_{GS} = 2.75 Vdc, I_D < 200 mAdc, T_A = −40°C to +85°C) (V_{GS} = 5.0 Vdc, I_D = 200 mAdc)		$r_{DS(on)}$	 − −	 5.6 −	 10 3.5	Ohms
Forward Transconductance (V_{DS} = 25 Vdc, I_D = 200 mAdc, f = 1.0 kHz)		g_{fs}	100	−	−	mmhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	−	40	50	pF
Output Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	−	12	25	
Transfer Capacitance	(V_{DG} = 25 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	−	3.5	5.0	
SWITCHING CHARACTERISTICS (Note 2)						
Turn−On Delay Time	(V_{DD} = 30 Vdc, I_D = 0.2 Adc,)	$t_{d(on)}$	−	−	20	ns
Turn−Off Delay Time		$t_{d(off)}$	−	−	20	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

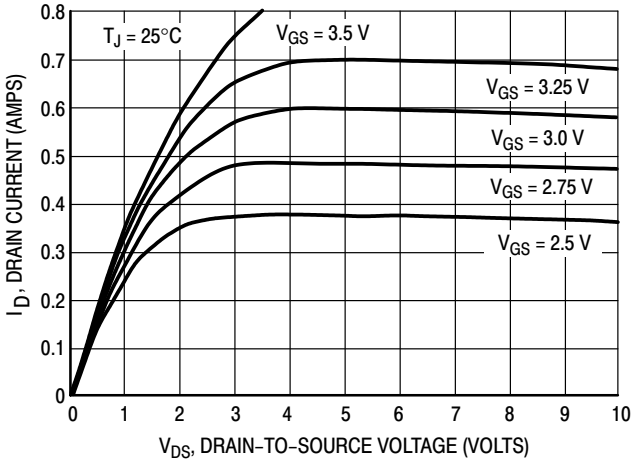


Figure 1. On−Region Characteristics

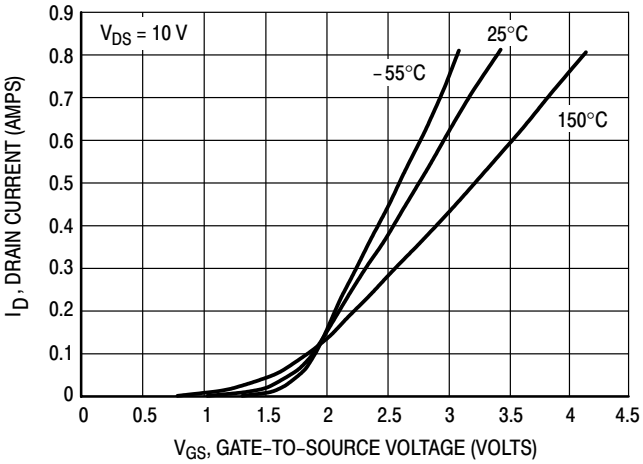


Figure 2. Transfer Characteristics

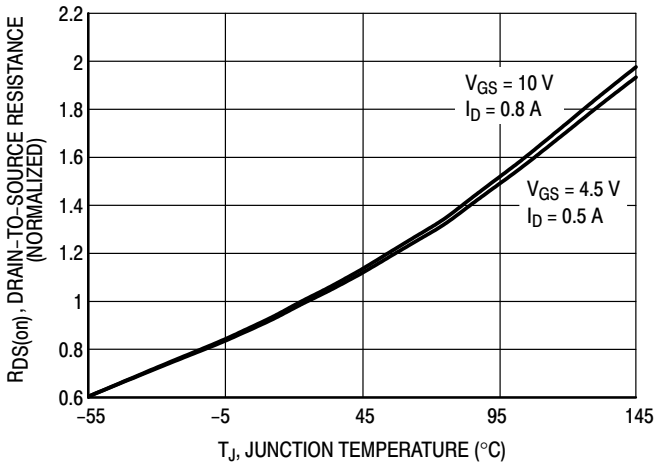


Figure 3. On−Resistance Variation with Temperature

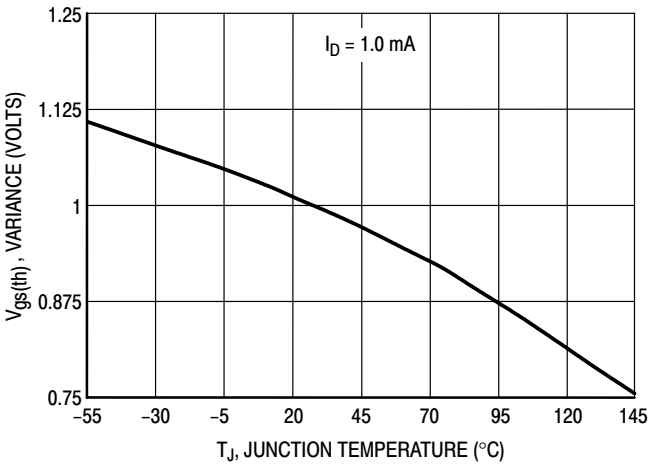


Figure 4. Threshold Voltage Variation with Temperature

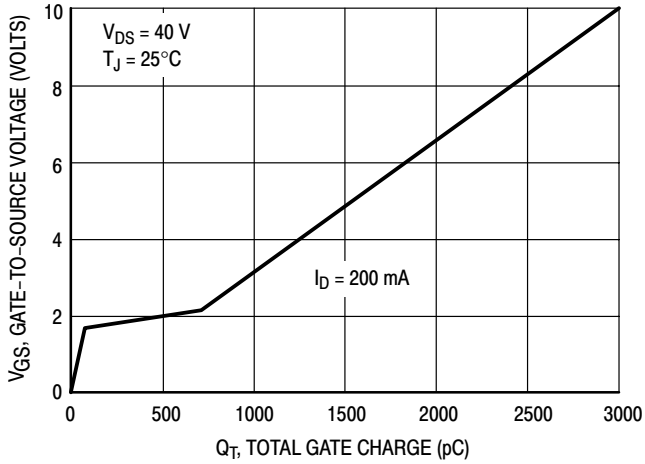


Figure 5. Gate Charge

TYPICAL ELECTRICAL CHARACTERISTICS

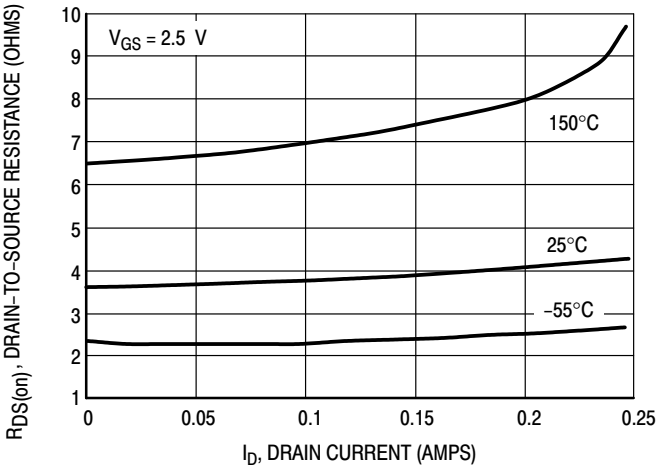


Figure 6. On−Resistance versus Drain Current

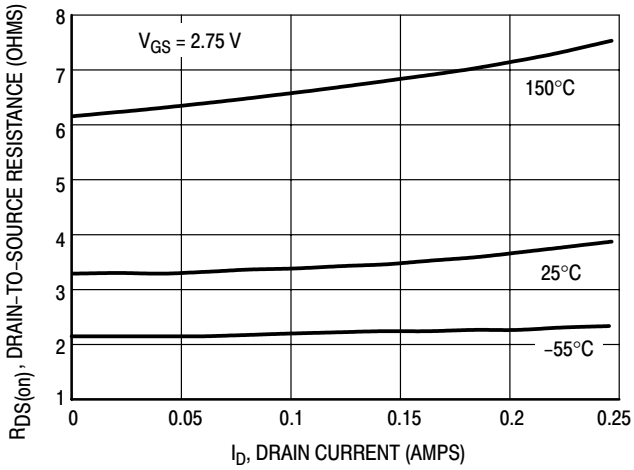


Figure 7. On−Resistance versus Drain Current

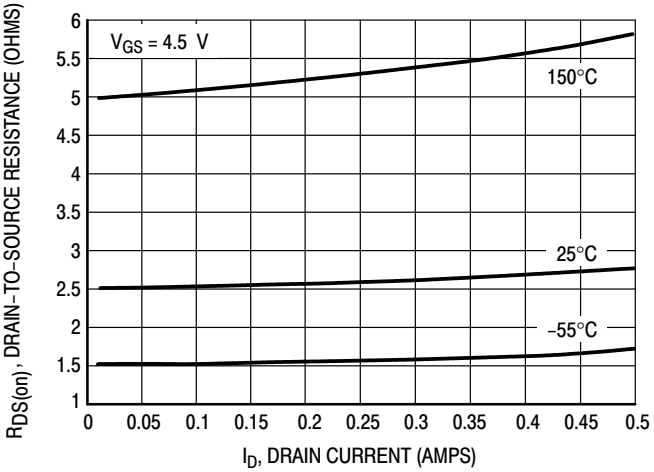


Figure 8. On−Resistance versus Drain Current

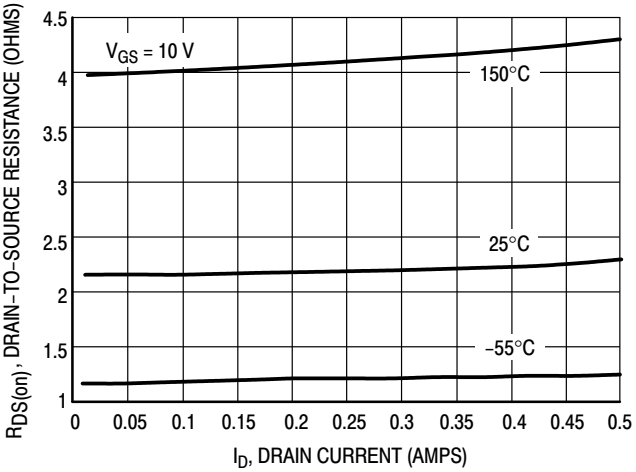


Figure 9. On−Resistance versus Drain Current

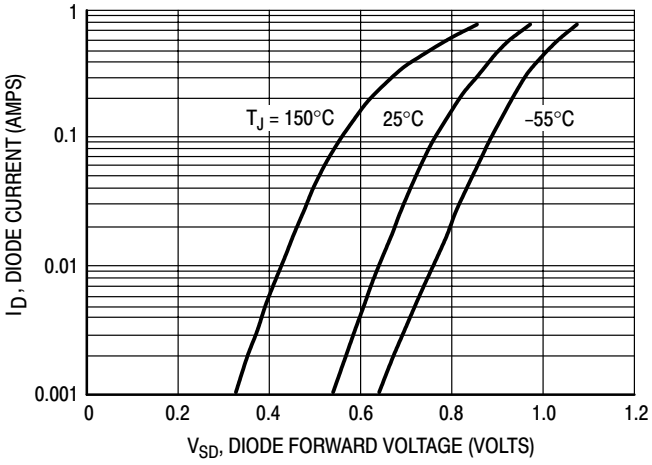


Figure 10. Body Diode Forward Voltage

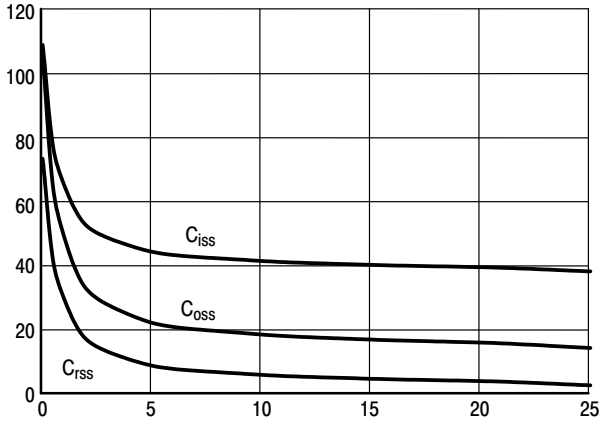
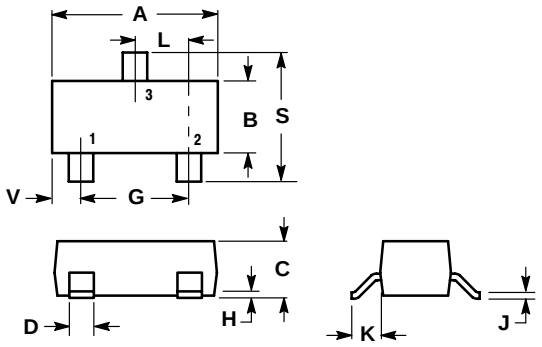


Figure 11. Capacitance

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AH

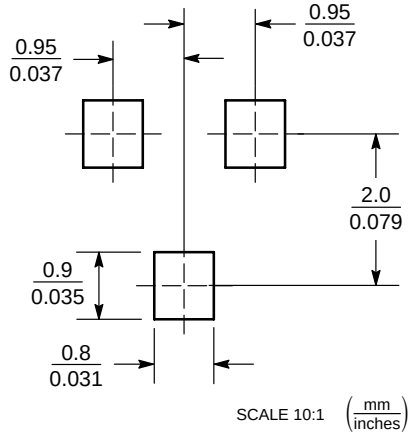


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−03 AND −07 OBSOLETE, NEW STANDARD 318−08.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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