SYA75603A/03B/604A/04B

2/4 Outputs Ultra-Low Additive Jitter PCIe 1/2/3/4/5 Clock Buffer for Automotive

Features

- Two (SYA75603A/03B) and Four (SYA75604A/04B) PCIe 1/2/3/4/5 Compliant Outputs
- Ultra-Low Additive Jitter 10 fs (PCIe Gen5)
- Supports Frequencies of up to 250 MHz
- Transparent for Spread Spectrum
- Supports 1.8V ±10%, 2.5V ±10% and 3.3V ±10% Power Supplies
- Outputs Low Power HCSL with Embedded 85Ω (SYA75603A/04A) and 100Ω (SYA75603B/04B) Termination Resistors
- Individual Glitch Free Output Enable (OExb) Control Pins
- Accepts DC Coupled HCSL Input Signal and AC Coupled PECL, LVDS and CML
- Extended Temperature Range: –40°C to +105°C
- 3 mm x 3 mm VQFN Package

Applications

- ADAS
- PCIe Based SSD drives
- Infotainment System

General Description

The SYA75603A, SYA75603B, SYA75604A, and SYA75604B are industry leading PCIe clock buffers with ultra-low additive jitter:

- 10 fs (PCIe 5.0)
- 20 fs (PCIe 3.0/4.0)
- 52 fs in the 12 kHz to 20 MHz band

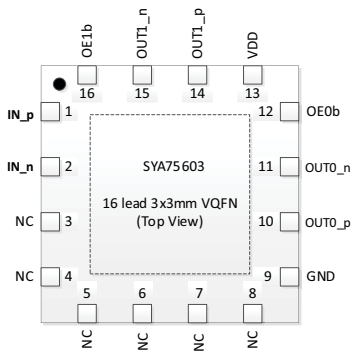
They can be used in all PCIe 1/2/3/4/5 common clock and SRIS applications.

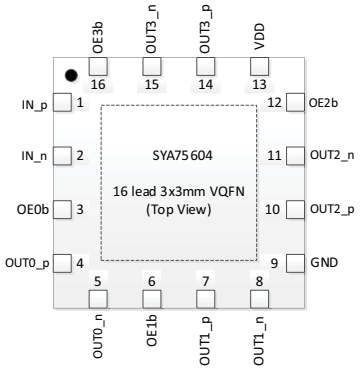
SYA75603A/03B and SYA75604A/04B are two and four output (respectively) PCIe clock buffers with glitch free per-output enable/disable control hardware pins. Both devices are packaged in a 3 mm x 3 mm VQFN.

The SYA75603A/03B/604A/04B have embedded low-dropout regulators (LDO) for superior power noise supply rejection. They support 1.8V, 2.5V, and 3.3V supplies with tolerance of ±10% which exceeds ±9% required by PCIe Card Electro Mechanical Specification.

All parts are Automotive Grade 2 compliant:
–40°C to +105°C

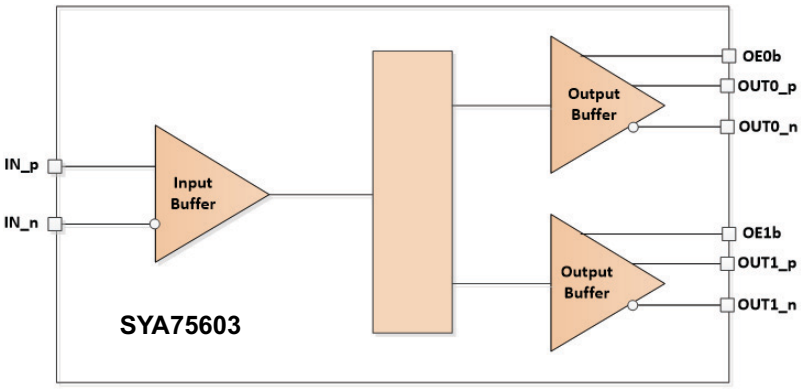
Package Types

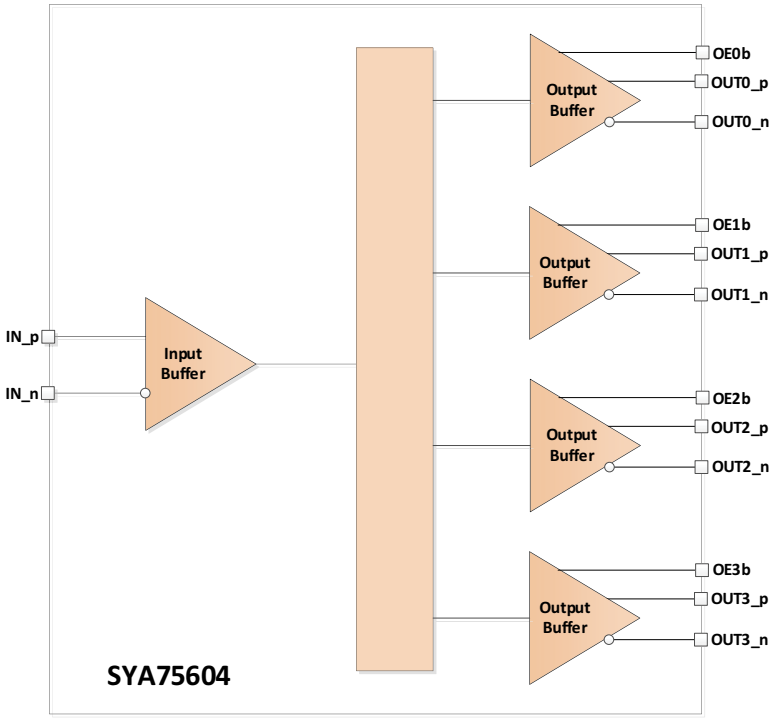




© 2021 Microchip Technology Inc. and its subsidiaries

Functional Block Diagrams





© 2021 Microchip Technology Inc. and its subsidiaries

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD}).....–0.5V to +4.6V
Input Voltage (V_{IN}) .....–0.5V to V_{DD} +0.5V
Input ESD Protection (HBM).....2 kV

Operating Ratings ‡

1.8V Operating Voltage (V_{DD}).....+1.62V to +1.98V
2.5V Operating Voltage (V_{DD}).....+2.25V to +2.75V
3.3V Operating Voltage (V_{DD}).....+2.97V to +3.63V

† Notice: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions may affect device reliability.

‡ Notice: The data sheet limits are not guaranteed if the device is operated beyond the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 3.3V ±10%, 2.5V±10%; 1.8V±10%T_A = –40°C to +105°C, unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Current Consumption						
Core Device Current	I_{DD}	—	9	13		All outputs disabled
Current dissipation per each LP-HCSL output	I_{OUT_HCSL}	—	3.5	3.9	mA	Note 1
Power Supply Noise Rejection Ratio Characteristics						
Power Supply Noise Rejection Ratio	$PSNRR_{HSCL}$	—	70	—	dB	Note 3, 100 mV_{PP}, 100 kHz noise injected to V_{DD}. Clock Frequency 100 MHz, V_{DD} = 3.3V
Input Characteristics						
Input Slew Rate	SR_{IN}	0.6	—	—	V/ns	Note 3
Differential Input High Voltage	V_{IH}	0.15	—	—	V	—
Differential Input Low Voltage	V_{IL}	—	—	–0.15	V	—
Input Voltage Swing	V_{SWING}	0.15	—	—	V_{DIFF}	—
Absolute Crossing Point Voltage	V_{CROSS}	0.25	—	0.55	V	Note 3
Variation of V_{CROSS} Over All Edges	V_{CROSS_DELTA}	—	—	0.14	V	Note 3
Voltage High for Output Enable	V_{IH_OE}	0.7* V_{DD}	—	—	V	—
Voltage Low for Output Enable	V_{IL_OE}	—	—	0.3* V_{DD}	V	—
Input Leakage Current	I_{IL_IN}	–5	—	5	µA	V_{IN} = $V_{IN(MAX)}$, V_{IN} = GND
Input Capacitance	C_{IN}	—	—	5	pF	Note 3
Input Leakage Current for OExb Inputs (Includes Current due to Pull-Down Resistors)	I_{IL_OE}	–5	—	50	µA	V_{IN} = V_{DD}, V_{IN} = GND

© 2021 Microchip Technology Inc. and its subsidiaries

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{DD} = 3.3V ±10%, 2.5V±10%; 1.8V±10%T_A = –40°C to +105°C, unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Single Ended Input Common Mode Voltage (IN_p) (HCSL Common Mode)	V_{SIC}	0.25	—	0.55	V	—
Single Ended Input Voltage Swing for IN_p	V_{SID}	0.3	—	1.45	V	—
Maximum Input Voltage	V_{IN}(MAX)	—	—	1.15	V	—
Minimum Input Voltage	V_{IN}(MIN)	–0.3	—	—	V	—
Input Frequency (Differential)	f_{IN}	0	—	250	MHz	Note 2
Input Frequency (Single Ended)	f_{IN_SE}	0	—	250	MHz	Note 2
Input Duty Cycle	DC	35	—	65	%	Note 3

Note 1: Tested with 100 MHz clock with outputs driving 5” long trace terminated with 2 pF capacitors to ground.

2: Output Enable control pins are synchronous with the input clock and it takes four rising edges before outputs get enabled and five rising edges before outputs get disabled. Hence the minimum input frequency is greater than 0 Hz. Once the outputs are enabled the input clock frequency can be reduced to 0 Hz.

3: Ensured by design and/or characterization, not tested in production.

OUTPUT ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 3.3V ±10%, 2.5V±10%; 1.8V±10%T_A = –40°C to +105°C, C_{LOAD} = 2 pF unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Rising Edge Rate	—	1	2.5	4	V/ns	Note 2, Note 3
Falling Edge Rate	—	1	2.5	4	V/ns	Note 2, Note 3
Differential Output High Voltage	V_{OH}	0.6	—	0.9	V	Note 2
Differential Output Low Voltage	V_{OL}	–0.9	—	–0.6	V	Note 2
Absolute Crossing Voltage	V_{CROSS}	0.25	—	0.55	V	Note 1, Note 4, Note 5, Note 13
Variation of V_{CROSS} Over All Rising Clock Edges	V_{CROSS_DELTA}	—	—	0.14	V	Note 1, Note 4, Note 8, Note 13
Ring Back Voltage Margin	V_{RB}	–0.1	—	0.1	V	Note 2, Note 10, Note 13
Time Before V_{RB} is Allowed	t_{STABLE}	500	—	—	ps	Note 2, Note 10, Note 13
Cycle-to-Cycle Additive Jitter	$t_{CCJITTER}$	—	6.5	8.1	ps	Note 2, Note 13
Absolute Maximum Output Voltage	V_{MAX}	—	—	1.15	V	Note 1, Note 6
Absolute Minimum Output Voltage	V_{MIN}	–0.3	—	—	V	Note 1, Note 7
Output Duty Cycle	V_{DC}	48	50	52	%	When input has 50% duty cycle and V_{IN} ≥ 200 mV, Note 2
Rising to Falling Edge Matching	Rise-Fall Matching	—	—	20	%	Note 1, Note 11
Clock Source DC Impedance (OUTx_p) for parts with 100Ω differential embedded impedance	$Z_{C\text{-}DC_OUT_p}$	40	—	60	Ω	—
Clock Source DC Impedance (OUTx_n) for parts with 100Ω differential embedded impedance	$Z_{C\text{-}DC_OUT_n}$	40	—	60	Ω	—

© 2021 Microchip Technology Inc. and its subsidiaries

OUTPUT ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{DD} = 3.3V ±10%, 2.5V±10%; 1.8V±10%T_A = –40°C to +105°C, C_{LOAD} = 2 pF unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Clock Source DC Impedance (OUTx_p) for parts with 85Ω differential embedded impedance	$Z_{C\text{-}DC_OUT_p}$	34	—	51	Ω	—
Clock Source DC Impedance (OUTx_n) for parts with 85Ω differential embedded impedance	$Z_{C\text{-}DC_OUT_n}$	34	—	51	Ω	—
Output Frequency	F_{MAX}	0	—	250	MHz	—
Output to Output Skew	t_{OOSK}	—	—	30	ps	Note 13
Part to Part Output Skew	t_{POOSK}	—	—	50	ps	Note 13
Input to Output Delay	t_{IOD}	0.9	1.2	1.5	ns	—
Output Enable Time	t_{EN}	—	—	3.5	cycles	Note 12
Output Disable Time	t_{DIS}	—	—	4.5	cycles	Note 12

Note 1: Measurement taken from single ended waveform.

2: Measurement taken from differential waveform.

3: Measured from –150 mV to +150 mV on the differential waveform (derived from OUTx_p to OUTx_n). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 1-5.

4: Measured at crossing point where the instantaneous voltage value of the rising edge of OUTx_p equals the falling edge of OUTx_n. See Figure 1-1.

5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 1-1.

6: Defined as the maximum instantaneous voltage including overshoot. See Figure 1-1.

7: Defined as the minimum instantaneous voltage including undershoot. See Figure 1-1.

8: Defined as the total variation of all crossing voltages of Rising OUTx_p and Falling OUTx_n. This is the maximum allowed variance in V_{CROSS} for any particular system. See Figure 1-2.

9: System board compliance measurements must use the test load card described in Figure 1-7. OUTx_p and OUTx_n are to be measured at the load capacitors C_{LOAD}. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements.

10: T_{STABLE} is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the V_{RB} ±100 mV differential range. See Figure 1-6.

11: Matching applies to rising edge rate for OUTx_p and falling edge rate for OUTx_n. It is measured using a ±75 mV window centered on the median cross point where OUTx_p rising meets OUTx_n falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of OUTx_p should be compared to the Fall Edge Rate of OUTx_n; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 1-3.

12: Output Enable control pins are synchronous with the input clock and it takes four rising edges before outputs get enabled and five rising edges before outputs get disabled. Hence the minimum input frequency is greater than 0 Hz. Once the outputs are enabled the input clock frequency can be reduced to 0 Hz.

13: Ensured by design and/or characterization, not tested in production.

© 2021 Microchip Technology Inc. and its subsidiaries

JITTER AND PHASE NOISE

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Peak-to-Peak Additive Jitter	p-p A_{JRMS}	—	—	4.5	ps	Note 1, Note 2, Note 4
Additive Jitter as per PCIe 1.0 (1.5 MHz to 22 MHz)	$t_{jPCIe_1.0}$	—	0.7	0.8	ps_{RMS}	Note 1, Note 2, Note 4
Additive Jitter as per PCIe 2.0 high band (1.5 MHz to 50 MHz)	$t_{jPCIe_2.0_high}$	—	70	90	fs_{RMS}	Note 1, Note 2, Note 4
Additive Jitter as per PCIe 2.0 low band (10 kHz to 1.5 MHz)	$t_{jPCIe_2.0_low}$	—	14	20	fs_{RMS}	Note 1, Note 2, Note 4
Additive Jitter as per PCIe 2.0 mid band (5 MHz to 16 MHz)	$t_{jPCIe_2.0_mid}$	—	55	74	fs_{RMS}	Note 1, Note 2, Note 4
Additive Jitter as per PCIe 3.0 (PLL_BW = 2 to 5 MHz, CDR = 10 MHz)	$t_{jPCIe_3.0}$	—	18	22	fs_{RMS}	Note 1, Note 2, Note 4
Additive Jitter as per PCIe 4.0 (PLL_BW = 2 to 5 MHz, CDR = 10 MHz)	$t_{jPCIe_4.0}$	—	18	22	fs_{RMS}	Note 1, Note 2, Note 4
Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 to 1.8 MHz, CDR for 32 GT/s CC)	$t_{jPCIe_5.0}$	—	7.5	10	fs_{RMS}	Note 2, Note 3, Note 4
Additive jitter as per Intel QPI 9.6 Gbps	t_{jQPI}	—	35	45	fs_{RMS}	Note 1, Note 2, Note 4
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j_1M_20M}$	—	51	66	fs_{RMS}	Note 1, Note 2, Note 4 (100 MHz clock)
		—	40	54	fs_{RMS}	Note 1, Note 2, Note 4 (133 MHz clock)
Additive RMS jitter in 12 kHz to 20 MHz band	tj_12k_20M	—	52	68	fs_{RMS}	Note 1, Note 2, Note 4 (100 MHz clock)
		—	44	58	fs_{RMS}	Note 1, Note 2, Note 4 (133 MHz clock)
Noise Floor	NF	—	–165	–163	dBc/Hz	Note 1, Note 2, Note 4 (100 MHz clock)
		—	–165	–163	dBc/Hz	Note 1, Note 2, Note 4 (133 MHz clock)

Note 1: Measured into AC test load as per Figure 1-7.

2: Measured from differential crossing point to differential crossing point.

3: Measured with 50Ω termination in instrument without a test load.

4: Ensured by design and/or characterization, not tested in production.

© 2021 Microchip Technology Inc. and its subsidiaries

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	16 Pin VQFN 3 mmx3 mm	Unit	Condition
Temperature Ranges				
Junction to Ambient Thermal Resistance	θ_{JA}	35.7	°C/W	Still air
		30.8		1m/s airflow
		28.6		2.5m/s airflow
Junction to Board Thermal Resistance	θ_{JB}	5	°C/W	—
Junction to Case Thermal Resistance	θ_{JC}	49.5	°C/W	—
Thermal Characterization, Junction to Top of Package	Ψ_{JT}	3	°C/W	Still air

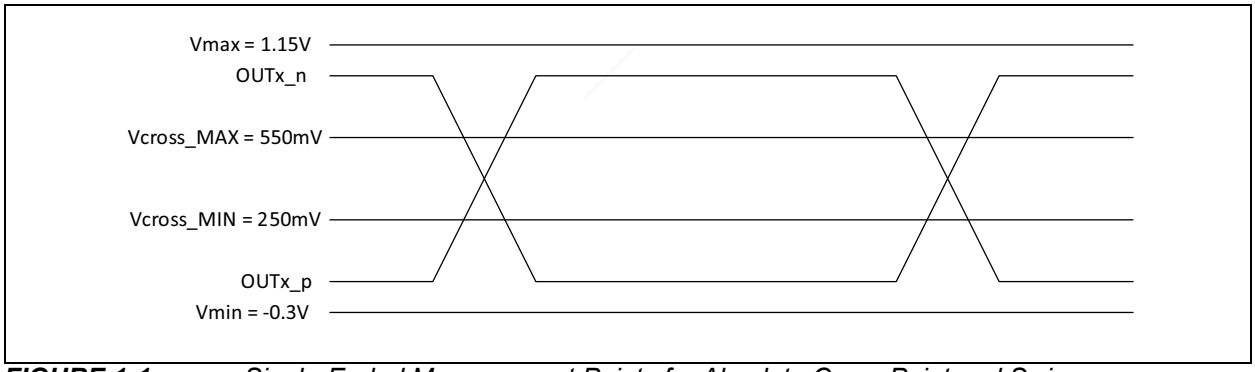


FIGURE 1-1: *Single-Ended Measurement Points for Absolute Cross Point and Swing.*

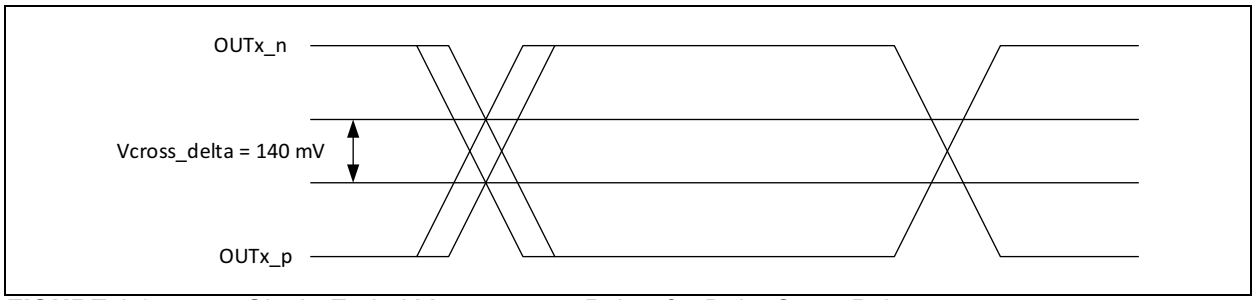


FIGURE 1-2: *Single-Ended Measurement Points for Delta Cross Point.*

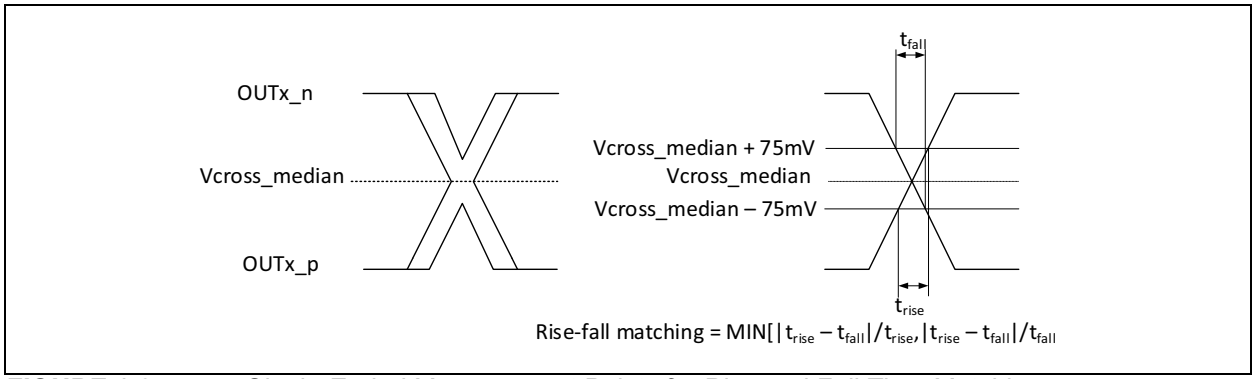


FIGURE 1-3: *Single-Ended Measurement Points for Rise and Fall Time Matching.*

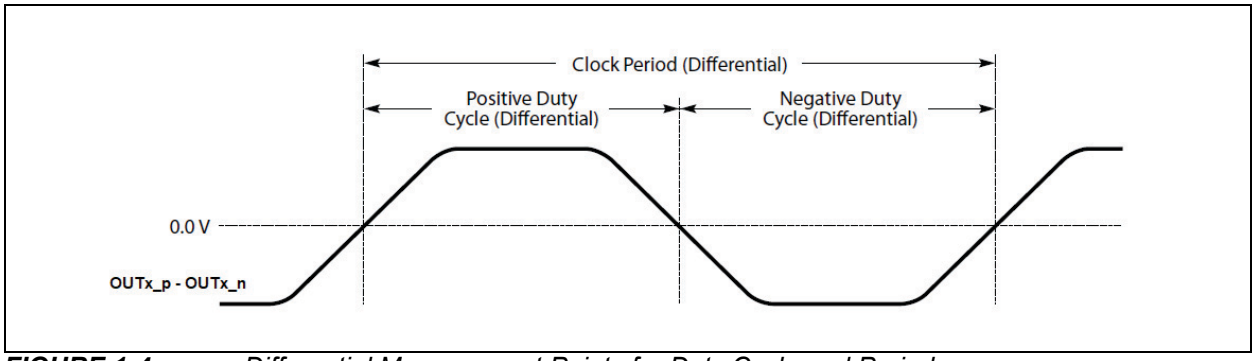


FIGURE 1-4: *Differential Measurement Points for Duty Cycle and Period.*

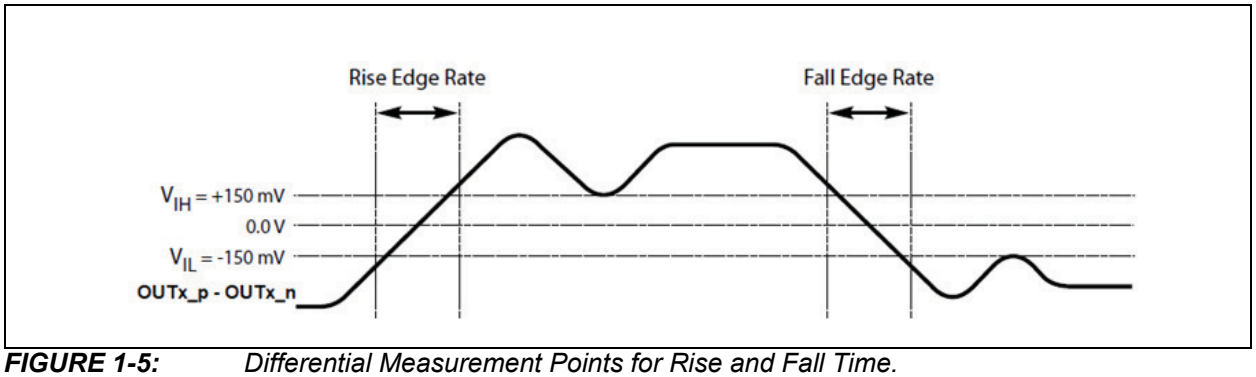


FIGURE 1-5: *Differential Measurement Points for Rise and Fall Time.*

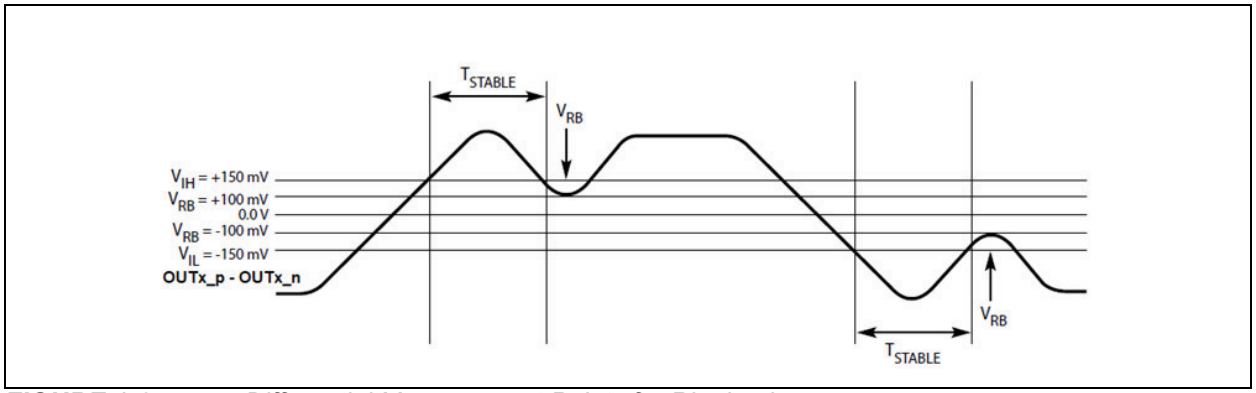


FIGURE 1-6: *Differential Measurement Points for Ringback.*

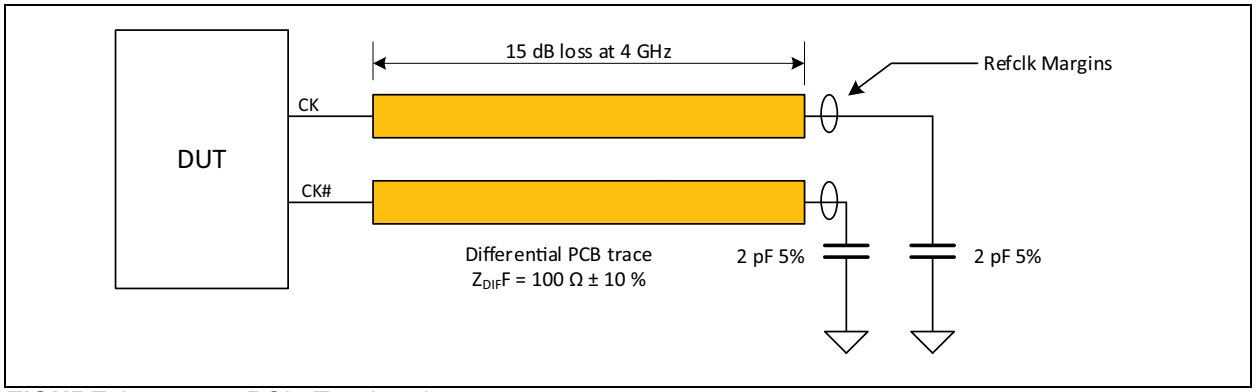


FIGURE 1-7: *PCIe Test Load.*

© 2021 Microchip Technology Inc. and its subsidiaries

2.0 TYPICAL OPERATING CHARACTERISTICS

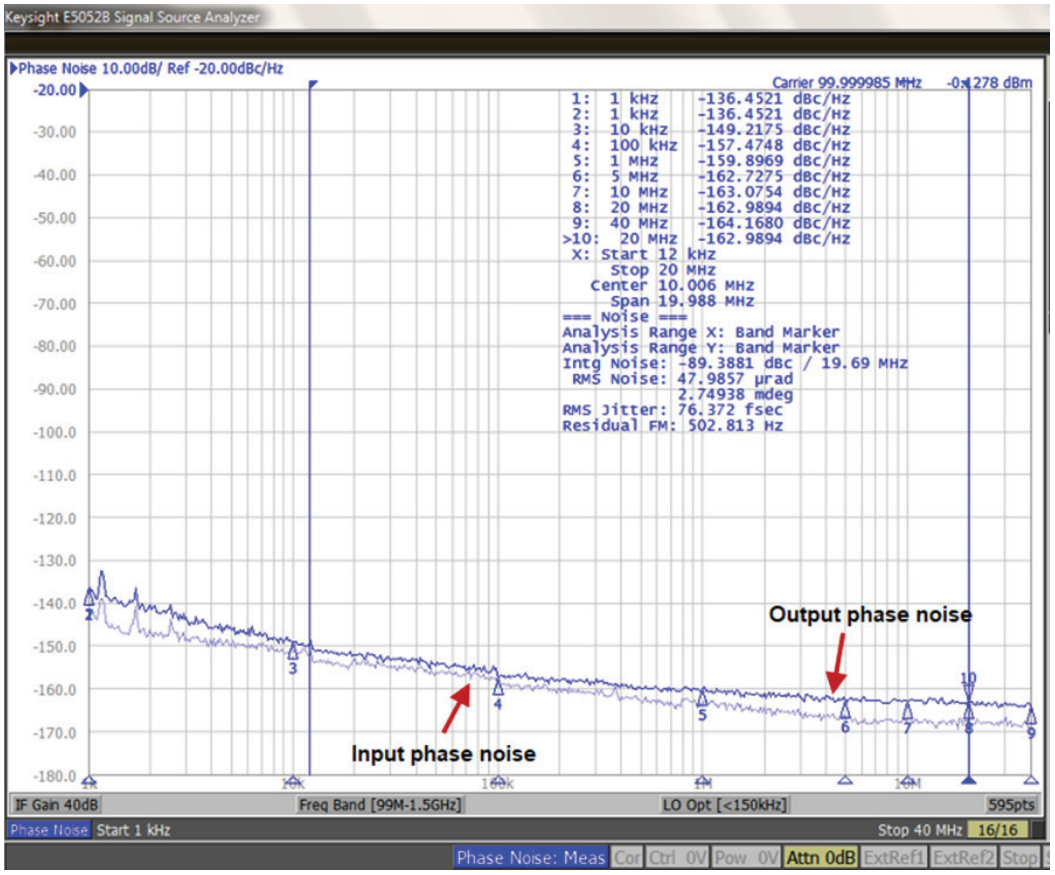


FIGURE 2-1: *Typical Expected Phase Noise.*

3.0 PIN DESCRIPTIONS

All device inputs and outputs are LP-HCSL unless described otherwise. The Type column uses the following symbols:

- I: Input
- IPD: Input with 100 kΩ internal pull-down resistor
- O: Output
- P: Power supply

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: SYA75604A/B AND SYA75603A/B PIN FUNCTION TABLE

Pin Number	Pin Name SYA75604A/B	Pin Name SYA75603A/B	Type	Description
Input Reference				
1	IN_p	IN_p	I	**Differential/Single Ended Input Reference** Input frequency range >0 Hz to 250 MHz **Note 1:** >0 Hz means frequency higher than DC. Output Enable control pins (OExb) need 3.5 clock cycles of the input clock to enable and 4.5 clock to disable the output. This feature ensures glitch free transition of the outputs. **Note 2:** The differential input has hysteresis of 30 mV that prevents outputs from randomly toggling when both p and n inputs are at the same voltage level. For example, when p and n inputs are held low, as in the case when the buffer is driven from an HCSL driver that is disabled.
2	IN_n	IN_n		
Output Clocks				
4	OUT0_p	NC	O	**Ultra-Low Additive Jitter Differential Outputs 0 to 1 (SYA75603A/B) and 0 to 3 (SYA75604A/B)** Output frequency range >0 Hz to 250 MHz NC are no connect pins. They are not bonded to the die but they should be soldered to the board for mechanical reasons.
5	OUT0_n	NC		
7	OUT1_p	NC		
8	OUT1_n	NC		
10	OUT2_p	OUT0_p		
11	OUT2_n	OUT0_n		
14	OUT3_p	OUT1_p		
15	OUT3_n	OUT1_n		
Control Inputs				
3	OE0b	NC	IPD	**Output Enable Control** When OExb is low the output x where x = {0,1} for SYA75603A/B and x = {0,1,2,3} for SYA75604A/B is active. OExb is synchronous and takes 3.5 clock cycles of the input clock to enable and 4.5 clock to disable the output. OExb pins are pulled-down with 100 kΩ resistor NC are no connect pins. They are not bonded to the die but they should be soldered to the board for mechanical reasons.
6	OE1b	NC		
12	OE2b	OE0b		
16	OE3b	OE1b		
Power and Ground				
13	VDD	VDD	P	**Positive Supply Voltage:** Connect to either 3.3V, 2.5V, or 1.8V supply.
9 ePad	GND	GND	P	**Ground:** Connect to ground.

© 2021 Microchip Technology Inc. and its subsidiaries

4.0 FUNCTIONAL DESCRIPTION

The SYA75603A/03B/604A/04B are PCIe clock buffers with ultra-low additive jitter. They can be used in all PCIe 1/2/3/4/5 common clock and SRIS applications.

SYA75603A/03B and SYA75604A/04B are two and four output PCIe clock buffers with glitch free per-output enable/disable control hardware pins. Both devices are packaged in 3 mm x 3 mm VQFN.

They have embedded low-dropout regulators (LDO) for superior power noise supply rejection. They support 1.8V, 2.5V, and 3.3V supplies with tolerance of ±10% which exceeds ±9% required by PCIe Card Electro Mechanical Specification.

4.1 Clock Input

Please refer to the Functional Block Diagrams for how to terminate different signals fed to the input of the device.

Figure 4-1 and Figure 4-2 show how to terminate input of the device in most common cases: Low Power HCSL (LPHCSL), HCSL, and single ended LVCMOS.

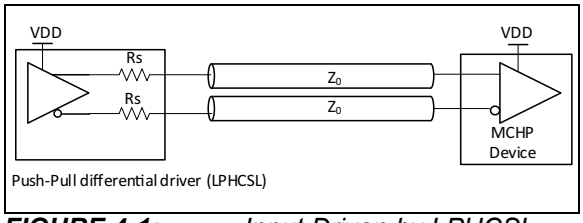


FIGURE 4-1: *Input Driven by LPHCSL Driver.*

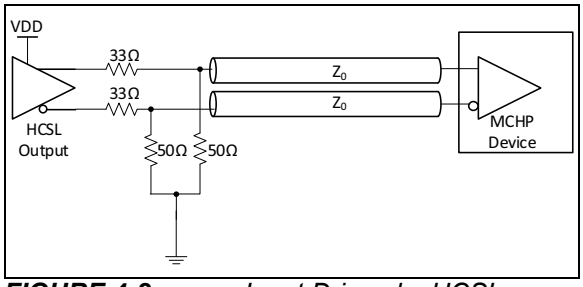
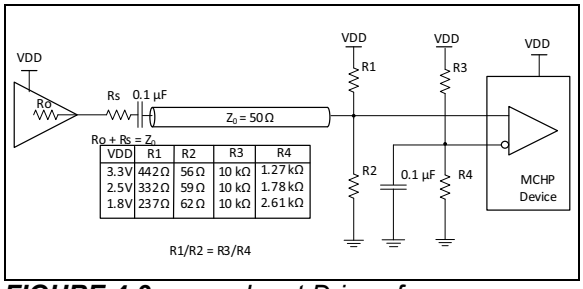


FIGURE 4-2: *Input Driven by HCSL Driver.*

Figure 4-3 shows how to terminate a single ended output such as LVCMOS. This example assumes 50Ω transmission line which is the most common for single ended CMOS signaling. Ideally, resistors R1 and R2 should be 100Ω each and R_O + R_S should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor R_S should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (0.3V). The source resistors of R_S = 270Ω could be used for standard LVCMOS driver. This will provide 516 mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) * (1/(270Ω + 50Ω)) = 5.16 mA.

For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.



VDD	R1	R2	R3	R4
3.3V	442Ω	56Ω	10 kΩ	1.27 kΩ
2.5V	332Ω	59Ω	10 kΩ	1.78 kΩ
1.8V	237Ω	62Ω	10 kΩ	2.61 kΩ

FIGURE 4-3: *Input Driven from a Single-Ended CMOS Output.*

The differential input has hysteresis of 30 mV that prevents outputs from randomly toggling when both p and n inputs are at the same voltage level. For example, when p and n inputs are held low, as in the case when the buffer is driven from an HCSL driver that is disabled.

4.2 Clock Outputs

Differential outputs have embedded termination resistors as shown in Figure 4-4. This provides significant saving relative to traditional current based HCSL outputs which require four resistors per differential output.

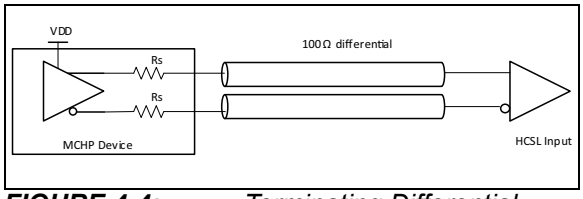


FIGURE 4-4: *Terminating Differential Outputs.*

Embedded termination resistors in SYA75603A/03B/604A/04B are matched for 100Ω differential transmission line.

4.3 Output Enable

Each output of SYA75603A/03B/604A/04B has an active-low Output Enable (OExb) control pin. The Output Enable and Disable function is synchronous with the input clock, which results in glitchless transitions as shown in Figure 4-5 and Figure 4-6. The OExb is sampled on the falling edge of the differential input (or falling edge of IN_p signal). It takes 3.5 clock cycles of the input clock to enable an output and 4.5 clock cycles to disable the output, after the change of OExb is sampled.

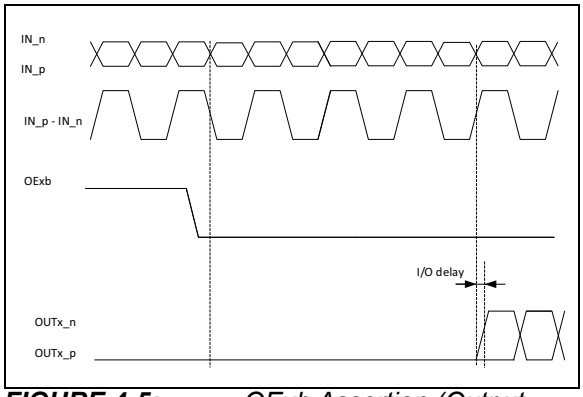


FIGURE 4-5: *OExb Assertion (Output Enable) Timing Diagram.*

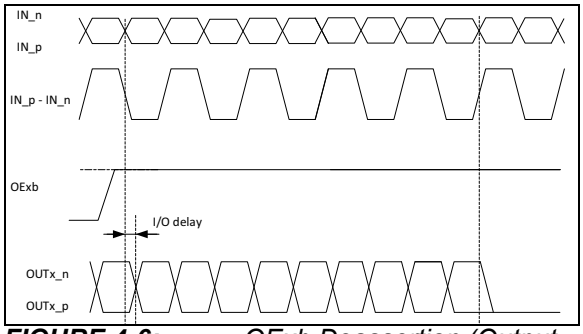


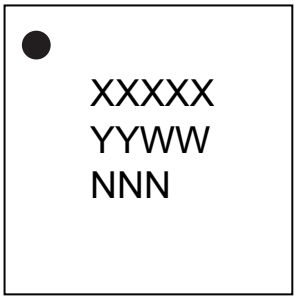
FIGURE 4-6: *OExb Deassertion (Output Disable) Timing Diagram.*

© 2021 Microchip Technology Inc. and its subsidiaries

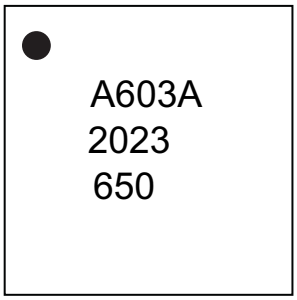
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

16-Lead VQFN*



Example

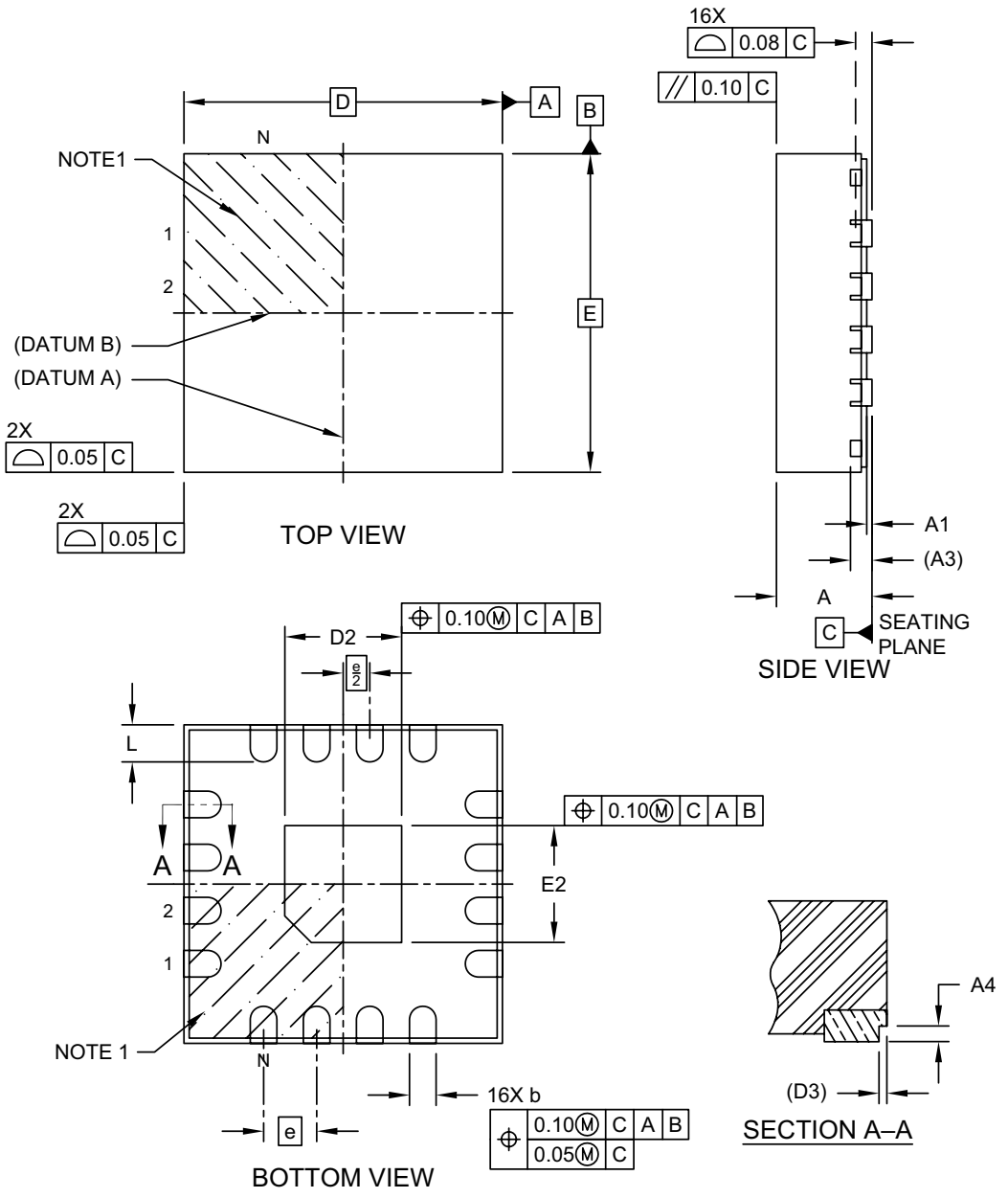


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

16-Lead VQFN 3.0 mm x 3.0 mm Package Outline and Recommended Land Pattern

16-Lead Very Thin Quad Flat, No Lead Package (4MX) - 3x3x0.9 mm Body [VQFN]
With 1.10 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

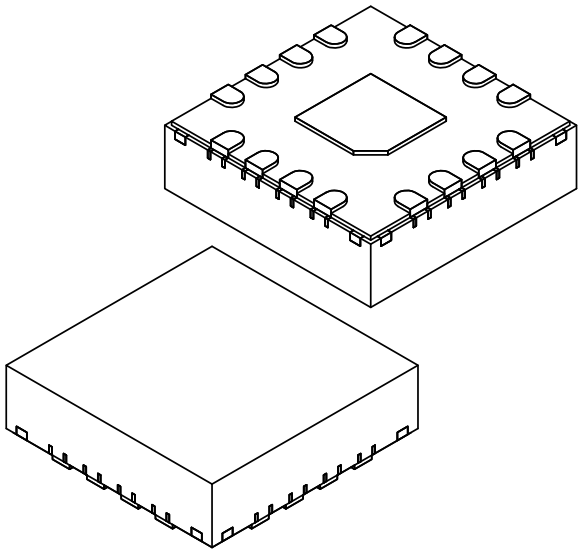


Microchip Technology Drawing C04-508 Rev A Sheet 1 of 2

© 2021 Microchip Technology Inc. and its subsidiaries

16-Lead Very Thin Quad Flat, No Lead Package (4MX) - 3x3x0.9 mm Body [VQFN]
With 1.10 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.00	1.10	1.20
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.00	1.10	1.20
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.25	0.35	0.45
Wettable Flank Step Length	D3		0.05 REF	
Wettable Flank Step Height	A4	0.10	-	0.19

Notes:

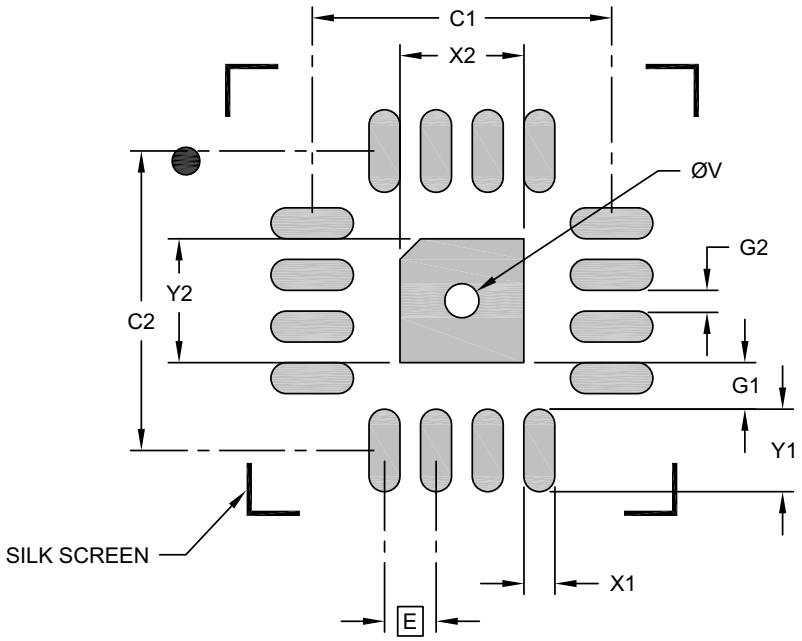
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-508 Rev A Sheet 2 of 2

© 2021 Microchip Technology Inc. and its subsidiaries

16-Lead Very Thin Quad Flat, No Lead Package (4MX) - 3x3x0.9 mm Body [VQFN]
With 1.10 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.20
Optional Center Pad Length	Y2			1.20
Contact Pad Spacing	C1		2.90	
Contact Pad Spacing	C2		2.90	
Contact Pad Width (X16)	X1			0.30
Contact Pad Length (X16)	Y1			0.80
Contact Pad to Center Pad (X16)	G1	0.45		
Contact Pad to Contact Pad (X12)	G2	0.20		
Thermal Via Diameter	V		0.33	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2508 Rev A

© 2021 Microchip Technology Inc. and its subsidiaries

APPENDIX A: REVISION HISTORY

Revision A (October 2021)

- Initial release of SYA75603A/03B/604A/04B as Microchip data sheet DS20006438A.

NOTES:

© 2021 Microchip Technology Inc. and its subsidiaries

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XXX	[-XX]	XXX
Device	Package	Media Type	Automotive Suffix

Device:	SYA75603A: 2 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5 85Ω Clock Buffer for Automotive SYA75603B: 2 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5 100Ω Clock Buffer for Automotive SYA75604A: 4 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5 85Ω Clock Buffer for Automotive SYA75604B: 4 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5 100Ω Clock Buffer for Automotive
Package:	TWL = 16-Lead 3 mm x 3 mm VQFN (Wettable Flank)
Media Type:	<blank> = 120/Tube T/R = 3,300/Reel
Automotive Suffix:	VXX = Automotive Suffix in which “XX” is assigned by Microchip. Standard value “AO” is for standard automotive part.

Examples:

a) SYA75603ATWL-VAO:	2 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5 85Ω Clock Buffer, 16-Lead 3 mm x 3 mm VQFN, 120/Tube, Standard Automotive
b) SYA75604BTWL-VAO:	4 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5 100Ω Clock Buffer, 16-Lead 3 mm x 3 mm VQFN, 120/Tube, Standard Automotive
c) SYA75604ATWL-TRVAO	4 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5 85Ω Clock Buffer, 16-Lead 3 mm x 3 mm VQFN, 3,300/Reel, Standard Automotive

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at https://www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

For information regarding Microchip’s Quality Management Systems, please visit www.microchip.com/quality.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, GridTime, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, NVM Express, NVMe, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, Symmcom, and Trusted Time are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2021, Microchip Technology Incorporated and its subsidiaries.

All Rights Reserved.

ISBN: 978-1-5224-9019-7

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

© 2021 Microchip Technology Inc. and its subsidiaries