F71858AD

Hardware Monitor, KBC with GPIO & ACPI

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F71858AD Datasheet Revision History

Version	Date	Page	Revision History
0.10P	2009/6/19	-	Preliminary Version
0.11P	2009/8/6	-	Add Application Circuit Add Registers & Application Circuits
0.12P	2010/10/5	39	Add TSI/SMBus Address Register – Index 08h

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Table of Content

1. General Description 4
2. Feature List 4
3. Key Specification 6
4. Pin Configuration 7
5. Pin Description 8
   5.1 Power Pin 8
   5.2 LPC Interface 8
   5.3 Keyboard Controller 9
   5.4 ACPI 9
   5.5 H/W Monitor 10
6. Function Description 11
   6.1 Power on Strapping 11
   6.2 Keyboard Controller 11
   6.3 ACPI function 13
   6.4 Hardware monitor 18
   6.5 LED function 27
   6.6 AMD TSI and Intel SST PECI Function 27
   6.7 Watchdog Timer Function 28
7. Register Description 29
   7.1 Global Control Registers 29
   7.2 KBC Registers 32
   7.3 ACPI and PME Registers 34
   7.4 Hardware Monitor Registers (Index port: 0x295; Data port: 0x296) 38
   7.5 GPIO Registers 60
   7.6 WDT Registers 65
8. PCB Layout Guide 67
9. Electrical Characteristics 69
   9.1 Absolute Maximum Ratings 69
   9.2 DC Characteristics 69
   9.3 DC Characteristics Continued 69
   9.4 AC Characteristics 71
10. Ordering Information 75
11. Package Dimensions (48LQFP) 76
12. Application Circuit 77

1. General Description

The F71858AD is hardware KBC integrating the ACPI, temperature sensing and fan control functions specific for the legacy free MB application. The KBC functions include one keyboard and one PS/2 mouse, and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. The controller will assert an interrupt to the system when data are placed in its output buffer.

The F71858AD provides the ACPI control signals as well such as S3 state, resume reset, 12 pins GPIO, WDT, PCI reset outputs or power OK signals. The power LED is programmable and compliant with PC2001.

As to the environment sensing functions, F71858AD provides 2 remote analog dual current temp. sensing inputs and one internal local temperature sensing. One HW_IRQ (alert signal) will be issued while the temperature is over the programmable limit. 4 fan monitoring inputs and 3 fan controlling outputs provide Fintek's patented auto-fan controlling features. Besides, the F71858AD supports AMD TSI and Intel PECI/SST interfaces for next generation CPU temp. sensing technology.

F71858AD is in LPC interface and powered by 3VCC, 3V standby, and battery. The package is in 48 pin LQFP Green Package.

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2. Feature List

- **General Functions**
  - Comply with LPC Spec. 1.1
  - Hardware Keyboard Controller support one PS/2 keyboard and one PS/2 mouse
  - Hardware Gate A20 and Hardware Keyboard Reset
  - Support ACPI 3.0
  - 12 GPIO Pins
  - WDT signal
  - HWM functions (Also support PECI fan control mechanism)

- **KBC**
  - LPC interface support serial interrupt channel 1, 12.
  - Two 16bit Programmable Address fully decoder, default 0x60 and 0x64.
  - Support two PS/2 interface, one for PS/2 mouse and the other for keyboard.

- Keyboard's scan code support set1, set2.
- Programmable compatibility with the 8042.
- Support both interrupt and polling modes.
- Hardware Gate A20 and Hardware Keyboard Reset.

ACPI Functions

- 1 reset input and 5 PCI reset output pins
- 2 programmable power LED
- S3Gate control
- Resume reset
- Power ok signal

Hardware Monitor Functions

- 2 current type accurate (3℃) thermal inputs for CPU thermal diode/2N3906 transistors
- One internal local thermal sensor
- Pin HW_IRQ# (default limit 100°C for CPU temp.)
- Temperature sensing range from -40℃~127℃
- 4 fan speed monitoring inputs
- 3 fan speed auto-control (support 3 wire and 4 wire fans)
- Support PWM and DAC mode control
- Default PWM duty is 40% when system boot up promptly
- Provide Intel PECI/SST interface for temperature sensing
- Provide AMD TSI interface for temperature sensing
- Support 3 channels voltage monitor (VCC3V + VSB3V + VBAT)
- Voltage monitor resolution is 8mV per LSB

GPIO Function

- Total 12 pins GPIO
- GPIO supports interrupt event by PME/SERIRQ

Watch Dog Timer

- Time resolution minute/second by option
- Maximum 256 minutes or 256 seconds
- Output WDT signal via PWOK pin

Package

- 48-pin LQFP

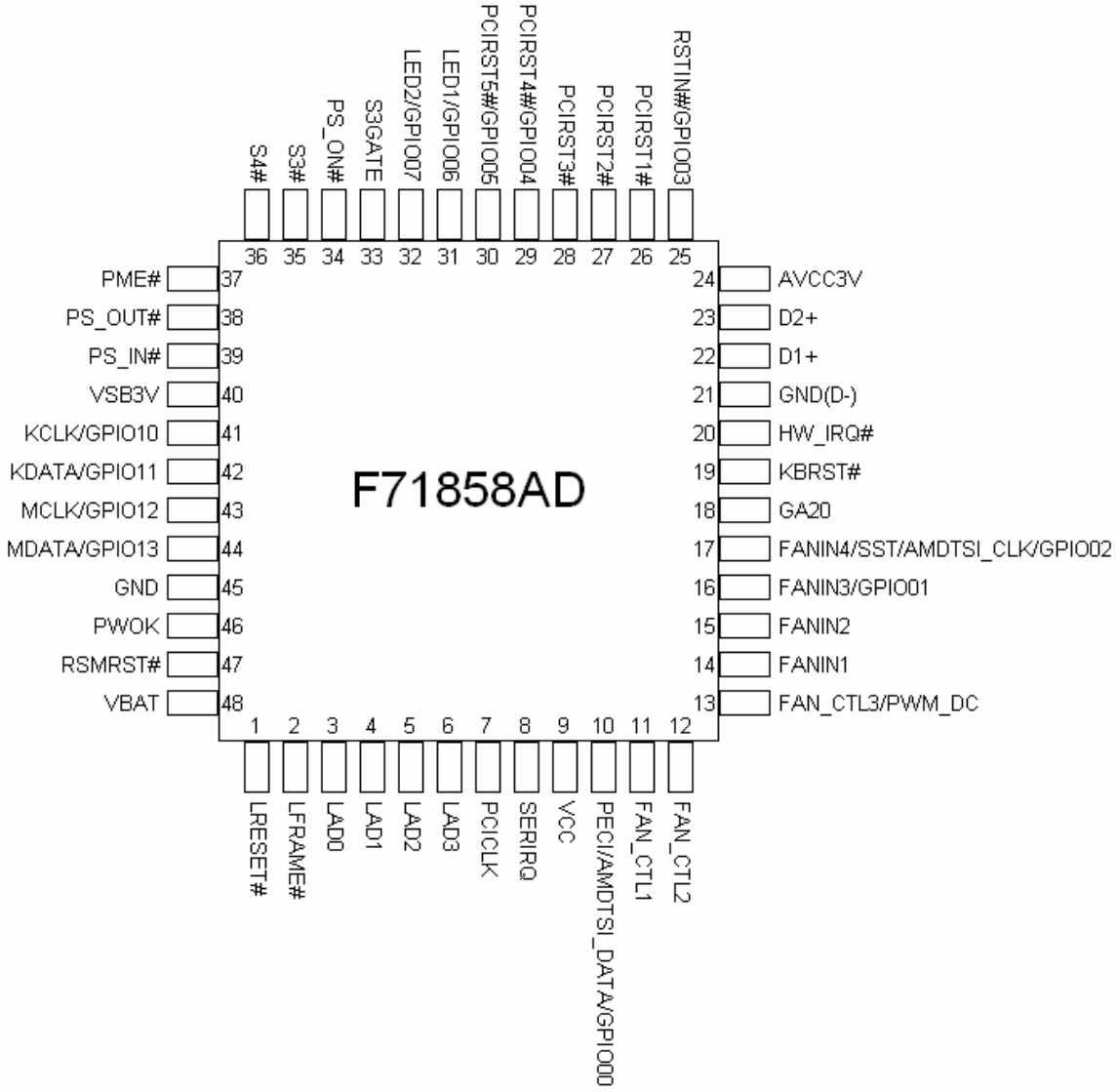
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3. Key Specification

- Supply Voltage 3.0V to 3.6V
- Operating Supply Current 5 mA typ.

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4. Pin Configuration



5. Pin Description

I/O_{12t}	- TTL level bi-directional pin with 12 mA source-sink capability.
$I/OOD_{12st,5v}$	- TTL level bi-directional pin and schmitt trigger, can select to OD or OUT by register, with 12 mA source-sink capability.
$I/OOD_{16st,5v}$	- TTL level bi-directional pin and schmitt trigger, can select to OD or OUT by register, with 16 mA source-sink capability, 5V tolerance.
$OD_{16u,10k}$	- Open-drain output pin with 16 mA sink capability, pull-up 10k ohms.
$OD_{16,5V}$	- Open-drain output pin with 16 mA sink capability, 5V tolerance.
$I/OD_{12st,5v}$	- TTL level bi-directional pin and schmitt trigger, Open-drain output with 12 mA sink capability, 5V tolerance.
$I/OD_{12t,5v}$	-TTL level bi-directional pin, Open-drain output with 12 mA sink capability, 5V tolerance.
O_{16}	-Output pin with 16 mA source-sink capability.
OD_{12}	- Open-drain output pin with 12 mA sink capability
$OD_{12,5v}$	- Open-drain output pin with 12 mA sink capability, 5V tolerance.
$IN_{t,5v}$	- TTL level input pin,5V tolerance.
$IN_{t,5v}$	- TTL level input pin,5V tolerance.
IN_{st}	- TTL level input pin and schmitt trigger.
IN_{t}	- TTL level input pin
$IN_{st,5v}$	- TTL level input pin and schmitt trigger, 5V tolerance.
$I_{Lv}/O_{D8,S1}$	- Bi-directional pin with 8mA source and 1mA sink capability, input level over 0.9v for high and under 0.5v for low .
I_{Lv}/OD_{12}	- Bi-directional pin with 12mA sink capability, input level over 0.9v for high and under 0.5v for low .
I_{Lv}/OOD_{12}	- Bi-directional pin, can select to OD or OUT by register, with 12mA source-sink capability, input level over 0.9v for high and under 0.5v for low .
IN_{Iv}	- Input pin, input level over 0.9v for high and under 0.5v for low .
AOUT	- Output pin(Analog).
AIN	- Input pin(Analog).
P	- Power.

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5.1 Power Pin

Pin No.	Pin Name	Type	Description
9	VCC	P	3V power
21	GND(D-)	P	Ground for temperature sensing usage.
24	AVCC3V	P	3V power for analog (Provide voltage monitor)
40	VSB3V	P	3V stand by power (Provide voltage monitor)
45	GND	P	Ground
48	VBAT	P	Battery power (Provide voltage monitor)

5.2 LPC Interface

Pin No.	Pin Name	Type	PWR	Description
1	LRESET#	$IN_{st,5v}$	VCC	Reset signal. It can connect to PCIRST# signal on the host.
2	LFRAME#	IN_{st}	VCC	Indicates start of a new cycle or termination of a

				broken cycle.
3,4,5,6	LAD[3:0]	I/O_{12t}	VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
7	PCICLK	IN_t	VCC	33MHz PCI clock input.
8	SERIRQ	I/O_{12t}	VCC	Serial IRQ input/Output.

5.3 Keyboard Controller

Pin No.	Pin Name	Type	PWR	Description
18	GA20	$OD_{16,u10k}$	VCC	Gate A20 output. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P21)
19	KBRST#	$OD_{16\text{-}u10k}$	VCC	Keyboard reset. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P20)
41	KCLK	$I/OD_{16st,5V}$	VSB	Keyboard Clock.
	GPIO10	$I/OOD_{16st,5V}$	VSB	General purpose IO
42	KDATA	$I/OD_{16st,5V}$	VSB	Keyboard Data.
	GPIO11	$I/OOD_{16st,5V}$	VSB	General purpose IO
43	MCLK	$I/OD_{16st,5V}$	VSB	PS2 Mouse Clock.
	GPIO12	$I/OOD_{16st,5V}$	VSB	General purpose IO
44	MDATA	$I/OD_{16st,5V}$	VSB	PS2 Mouse Data.
	GPIO13	$I/OOD_{16st,5V}$	VSB	General purpose IO

5.4 ACPI

Pin No.	Pin Name	Type	PWR	Description
25	RSTIN#	$IN_{st,5v}$	VSB	Reset buffer input signal.
	GPIO03	$I/OOD_{12st,5V}$	VSB	General purpose IO
26	PCIRST1#	$OD_{16,5V}$	VSB	Output buffer of RSTIN# and LRESET# for IDE reset.
27,28	PCIRST[2:3]#	O_{16}	VSB	Output buffer of RSTIN# and LRESET#.
29	PCIRST4#	O_{16}	VSB	Output buffer of RSTIN# and LRESET#.
	GPIO04	$I/OOD_{16st,5V}$	VSB	General purpose IO
30	PCIRST5#	$OD_{16,5V}$	VSB	Output buffer of RSTIN# and LRESET# for IDE reset.
	GPIO05	$I/OOD_{16st,5V}$	VSB	General purpose IO
31	LED1	$OD_{16,5V}$	VSB	Power LED for VSB.
	GPIO06	$I/OOD_{16st,5V}$	VSB	General purpose IO
32	LED2	$OD_{16,5V}$	VSB	Power LED for VSB.
	GPIO07	$I/OOD_{16st,5V}$	VSB	General purpose IO
33	S3GATE	$OD_{12,5v}$	VSB	Control dual voltage signal.
34	PS_ON#	$OD_{12,5v}$	VSB	Power supply on-off control output. Connect to ATX power supply PS_ON# signal.
35	S3#	IN_{st}	VSB	S3# Input is Main power on-off switch input.
36	S4#	IN_{st}	VSB	S4# Input is for S3/S4 (S5) state switch input.
38	PS_OUT#	OD_{12}	VSB	Panel Switch Output. This pin is low active and pulse output. It is power on request output#.

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39	PS_IN#	$IN_{st,5v}$	VSB	Main power switch button input.
46	PWOK	$I/OD_{12t,5V}$	VBAT	PWOK function, It is power good signal of VCC, which is delayed 400ms (default and programmable) as VCC arrives at 2.8V. Watchdog signal can be asserted via this pin.
47	RSMRST#	OD_{12}	VBAT	Resume Reset# function, It is power good signal of VSB, which is delayed 66ms as VSB arrives at 2.3V.

5.5 H/W Monitor

Pin No.	Pin Name	Type	PWR	Description
10	PECI	$I_{Lv}/O_{D8,S1}$	VCC	Intel PECI hardware monitor interface.
	AMDTSI_DATA	I_{Lv}/OD_{12}		AMD TSI data interface.
	GPIO00	I_{Lv}/OOD_{12}		General purpose IO
11	FAN_CTL1	$OD_{12,5v}$ AOUT	VCC	Fan 1 control output. This pin provides PWM duty-cycle output or a voltage output. Default PWM duty is 40%.
12	FAN_CTL2	$OD_{12,5v}$ AOUT	VCC	Fan 2 control output. This pin provides PWM duty-cycle output or a voltage output. Default PWM duty is 40%.
13	FAN_CTL3	$OD_{12,5V}$ AOUT	VCC	Fan 3 control output and 3pin fan is recommended to be controlled by this pin but not 4pin fan. This pin provides PWM duty-cycle output or a voltage output.
	PWM_DC	$IN_{t,5v}$	VCC	Power on strapping : Pull high: Fan control method will be in PWM Mode NC: Fan control method will be in DAC Mode
14	FANIN1	$IN_{st,5v}$	VCC	Fan 1 tachometer input.
15	FANIN2	$IN_{st,5v}$	VCC	Fan 2 tachometer input.
16	FANIN3	$IN_{st,5v}$	VCC	Fan 3 speed input. Default PWM duty is 40%.
	GPIO01	$I/OOD_{12st,5V}$	VCC	General purpose IO
17	FANIN4	IN_{Iv}	VCC	Fan 4 speed input.
	SST	$I_{Lv}/O_{D8,S1}$		Intel SST hardware monitor interface.
	AMDTSI_CLK	OD_{12}		Clock output for AMD TSI interface.
	GPIO02	I_{Lv} /OOD_{12}		General purpose IO
20	HW_IRQ#	$OD_{12,5V}$	VCC	Active low output. This pin will be logic low when the temperature exceeds its limit or fan fault event.
22	D1+(CPU)	AOUT AIN	VCC	Thermal diode/transistor temperature sensor input.
23	D2+	AOUT AIN	VCC	Thermal diode/transistor temperature sensor input.
37	PME#	OD_{12}	VSB	Generated PME event. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the S3 state.

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6. Function Description

6.1 Power on Strapping

Pin No.	Symbol	Value	Description
13	PWM_DC	1	Fan control mode: PWM mode. (Default)
		0	Fan control mode: DAC mode.

6.2 Keyboard Controller

The KBC circuit provides the functions included a keyboard and/or a PS/2 mouse, and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. The controller will assert an interrupt to the system when data are placed in its output buffer.

Output Buffer

The output buffer is an 8-bit read-only register at I/O address 60h. The keyboard controller uses the output buffer to send the scan code received from the keyboard and data bytes required by commands to the system.

Input Buffer

The input buffer is an 8-bit write-only register at I/O address 60h or 64h. Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to keyboard through the controller's input buffer only if the input buffer full bit in the status register is “0”.

Status Register

The status register is an 8-bit read-only register at I/O address 64h that holds information about the status of the keyboard controller and interface. It may be read at any time.

BIT	BIT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full

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2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller (KCCB). It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Mouse Output Buffer	0: Muse output buffer empty 1: Mouse output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

Commands

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte</td></tr>
<tr><td>60h</td><td>Write Command Byte
<table>
<tr><th>BIT</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
<tr><td>1</td><td>Enable Mouse Interrupt</td></tr>
<tr><td>2</td><td>System flag</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>4</td><td>Disable Keyboard Interface</td></tr>
<tr><td>5</td><td>Disable Mouse interface</td></tr>
<tr><td>6</td><td>IBM keyboard Translate Mode</td></tr>
<tr><td>7</td><td>Reserve</td></tr>
</table></td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Auxiliary Interface Test
8’h00: indicate Auxiliary interface is ok.
8’h01: indicate Auxiliary clock is low.
8’h02: indicate Auxiliary clock is high
8’h03: indicate Auxiliary data is low
8’h04: indicate Auxiliary data is high</td></tr>
<tr><td>AAh</td><td>Self-test
Returns 055h if self test succeeds</td></tr>
</table>

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ABh	keyboard Interface Test 8'h00: indicate keyboard interface is ok. 8'h01: indicate keyboard clock is low. 8'h02: indicate keyboard clock is high 8'h03: indicate keyboard data is low 8'h04: indicate keyboard data is high
ADh	Disable Keyboard Interface
AEh	Enable Keyboard Interface
C0h	Read Input Port(P1) and send data to the system
C1h	Continuously puts the lower four bits of Port1 into STATUS register
C2h	Continuously puts the upper four bits of Port1 into STATUS register
D0h	Send Port2 value to the system
D1h	Only set/reset GateA20 line based on the system data bit 1
D2h	Send data back to the system as if it came from Keyboard
D3h	Send data back to the system as if it came from Muse
D4h	Output next received byte of data from system to Mouse
FEh	Pulse only RC (the reset line) low for 6μs if Command byte is even

KBC Command Description

PS2 wakeup function

The KBC supports keyboard and mouse wakeup function. When pressing combinational keys as (1) CTRL +ESC (2) CTRL+F1 (3) CTRL+SPACE (4) ANY KEY (5) windows 98 wakeup up key under keyboard wakeup function, KBC will assert PME signal. KBC will also assert PME signal via mouse's (1) BUTTON CLICK or (2) BUTTON CLICK AND MOVEMENT. Those wakeup conditions are controlled by configuration register.

6.3 ACPI function

The Advanced Configuration and Power Interface (ACPI) is a system for controlling the use of power in a computer. It lets computer manufacturer and user to determine the computer's power usage dynamically.

There are three ACPI states that are of primary concern to the system designer and they are designated S0, S3 and S5. S0 is a full-power state; the computer is being actively used in this state. The other two are called sleep states and reflect different power consumption when power-down. S3 is a state that the processor is powered down but the last procedural state is being stored in memory which is still active. S5 is a state that memory is off and the last procedural state of the processor has been stored to the hard disk. Take S3 and S5 as comparison, since memory is fast, the computer can quickly come back to full-power state, the disk is slower than the memory and the computer

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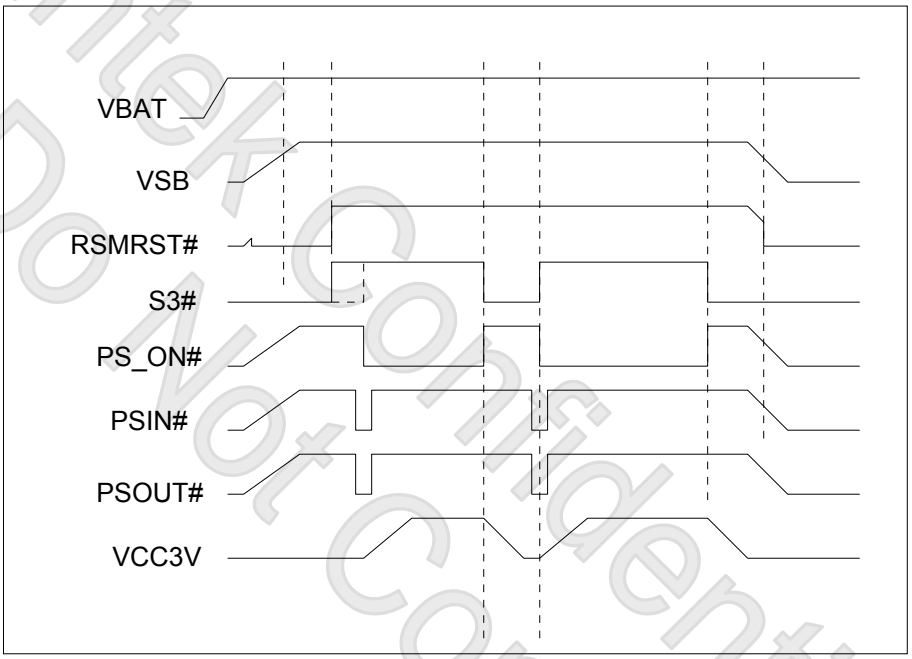
takes longer time to come back to full-power state. However, since the memory is off, S5 draws the minimal power comparing to S0 and S3.

It is anticipated that only the following state transitions may happen:

S0→S3, S0→S5, S5→S0, S3→S0 and S3→S5.

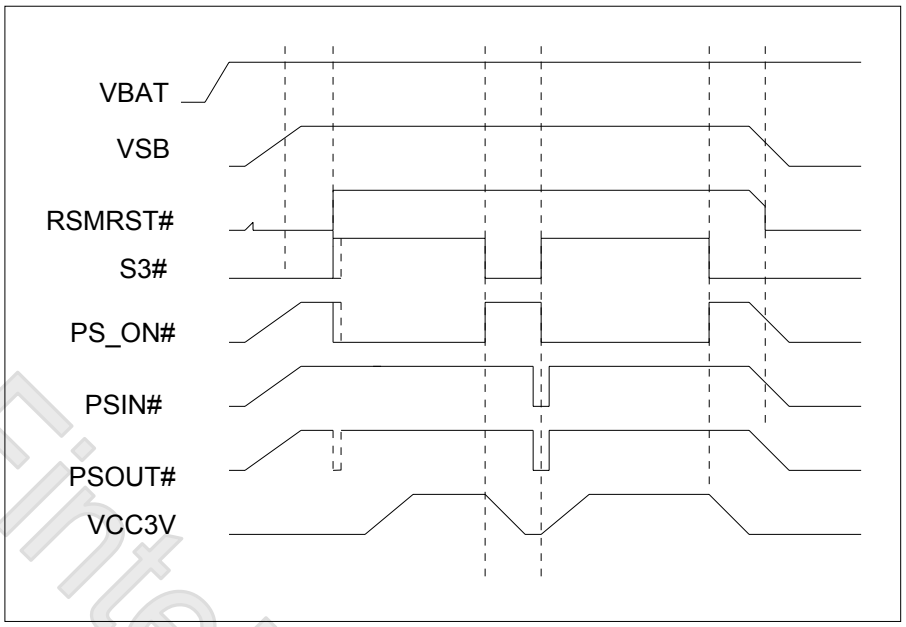
Among them, S3→S5 is illegal transition and won't be allowed by state machine. It is necessary to enter S0 first in order to get to S5 from S3. As for transition S5→S3 will occur only as an immediate state during state transition from S5→S0. It isn't allowed in the normal state transition.

The below diagram described the timing, the always on and always off, keep last state could be set in control register. In keep last state mode, one register will keep the status of before power loss. If it is power on before power loss, it will remain power on when power is resumed, otherwise, if it is power off before power loss, it will remain power off when power is resumed.



ACPI Default Timing Always Off

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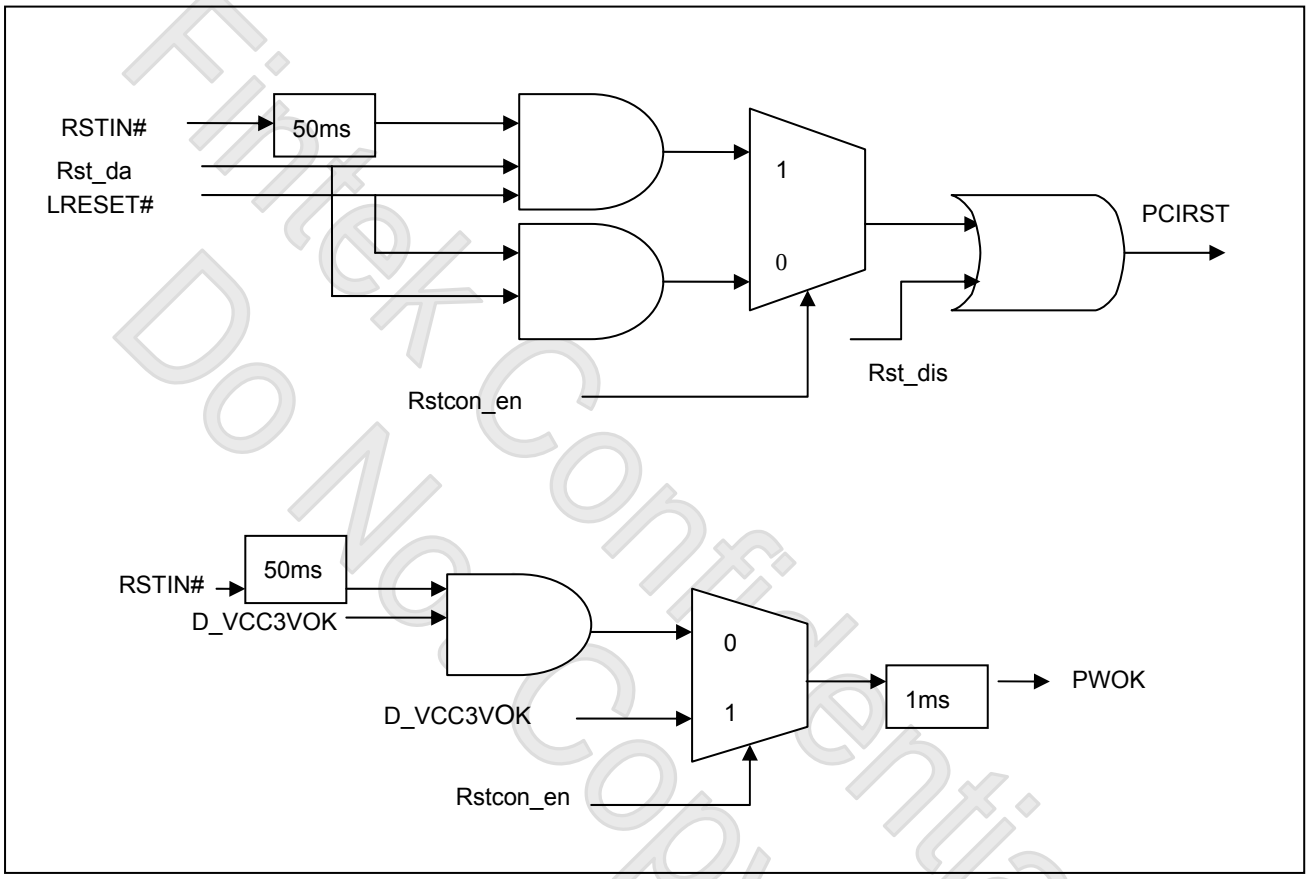
ACPI Default Timing Always On

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PCIRST and PWROK Signals

The F71858AD supports 5 output buffers for 5 reset signals. The result of PCIRST [1:5]# outcome will be affected by conditions as below.

The PWROK signal is affected by RST_IN#/LRESET#/DVCC3VOK.when rstcon_en set 1, POWEROK signal is affected by D_VCC3VOK and when rstcon_en set 0, POWEROK signal is affected by RST_IN#/ LRESET#/D_VCC3VOK.See below for the reference.



PCIRST# and PWROK

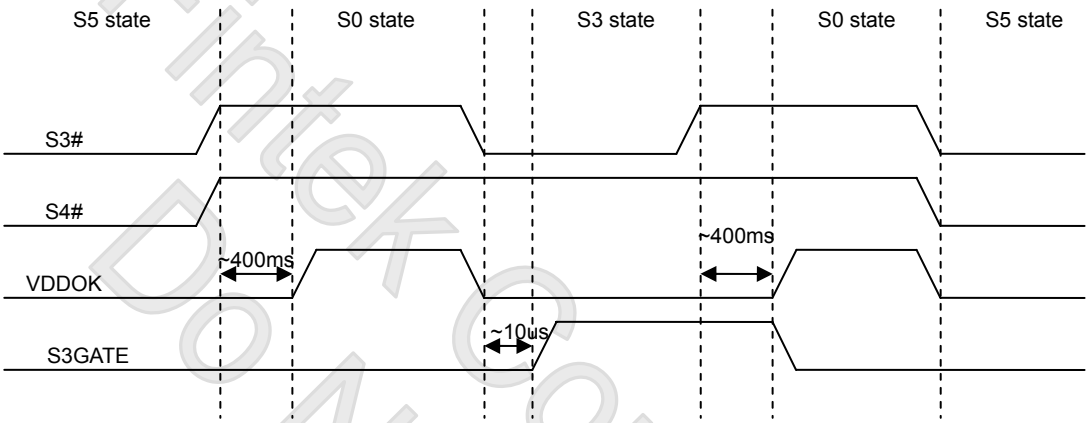
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S3 GATE Signals

The S3GATE signal response S0/S3/S5 state and condition is as below. When system is in S3 state, S3GATE is asserted logic high; the other state is asserted logic low. It is anticipated that only the following state transitions may happen:

S0→S3, S0→S5, S5→S0, S3→S0 and S3→S5.

Among them, S5→S3 is illegal transition and S3GATE signal will be keep logic level.



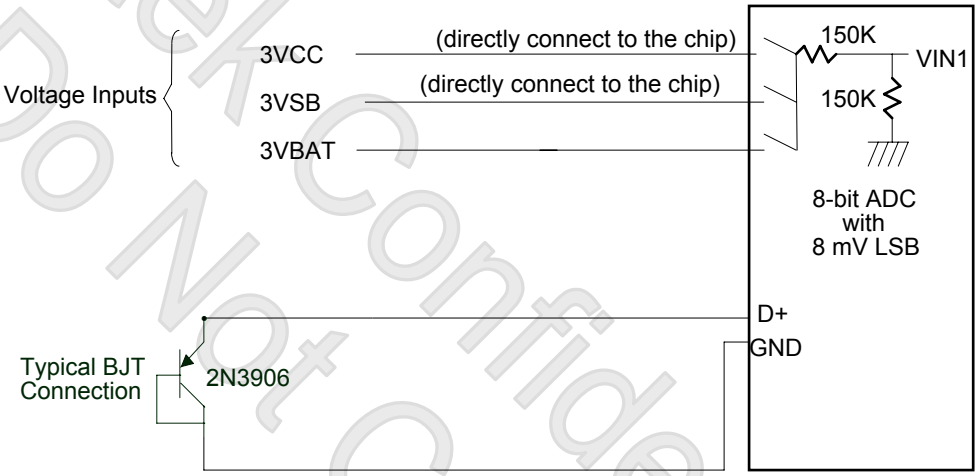
S3GATE Timming

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6.4 Hardware monitor

For the 8-bit ADC has the 8mv LSB, the maximum input voltage of the analog pin is 2.04V. Therefore the voltage under 2.04V (ex:1.5V) can be directly connected to these analog inputs. The voltage higher than 2.04V should be reduced by a factor with external resistors so as to obtain the input range. VCC, VSB 3.3V and VBAT 3V are the exception for it is main power of the F71858AD. Therefore these powers can directly connect to this chip's power pin and need no external resistors. There are two functions in these pins with 3.3V/3V. The first function is to supply internal logic power of the F71858AD and the second function is that this voltage with 3.3V/3V is connected to internal serial resistors to monitor the VCC VSB 3.3V and VBAT voltage. The internal serial resistors are two 150K ohm, so that the internal reduced voltage is half of 3.3V/3V.

F71858AD only support three power voltage monitor but without hardware high low limit protect. So it will not trigger PME event when voltage too high or too low.



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The F71858AD monitors a local and 2 remote temperature sensor. Both can be measured from -40°C to 127°C. The temperature format is as the following table:

Table mode:

Display range is from -40°C to 127°C. The values in high byte registers bit7 is sign bit and the values in high byte registers bit6~bit0 are mean temperature reading value and the unit is 1°C. The value in low bye register bit7~bit5 are temperature reading value and the unit is 0.125°C.

Temperature	Digital Output (High byte)	Digital Output (Low byte)
-40°C	1101 1000	000X XXXX
-1°C	1111 1111	000X XXXX
0°C	0000 0000	000X XXXX

100°C	0110 0100	000X XXXX
127.875°C	0111 1111	111X XXXX
open	1011 1011	000X XXXX
short	1100 1100	000X XXXX

Remote-sensor transistor manufacturers

Manufacturer	Model Number
Panasonic	2SB0709 2N3906
Philips	PMBT3906

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Monitor Temperature from "thermal diode"

Also, if the CPU, GPU or external circuits provide thermal diode for temperature measurement, the F71858AD is capable to these situations. The build-in reference table is for PNP 2N3906 transistor, and each different kind of thermal diode should be matched with specific margin and BJT gain. The transistor is directly connected into temperature pins.

ADC Noise Filtering

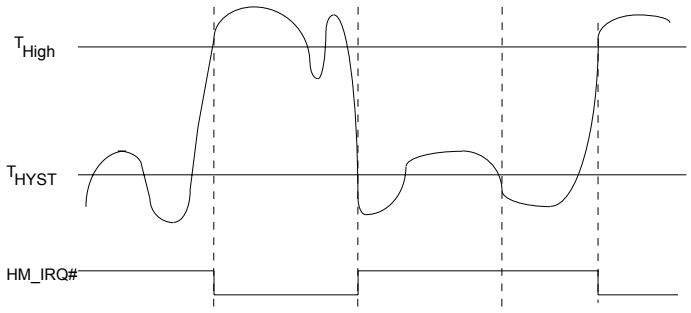
The ADC is integrating type with inherently good noise rejection. Micro-power operation places constraints on high-frequency noise rejection; therefore, careful PCB board layout and suitable external filtering are required for high-accuracy remote measurement in electronically noisy environment. High frequency EMI is best filtered at D+ and D- with an external 2200pF or 3300PF capacitor. Too high capacitance may introduce errors due to the rise time of the switched current source. Nearly all noise sources tested cause the ADC measurement to be higher than the actual temperature, depending on the frequency and amplitude.

Temperature HM_IRQ Signal (HM_IRQ# and PME#)

There are two mode of temperature HM_IRQ function:

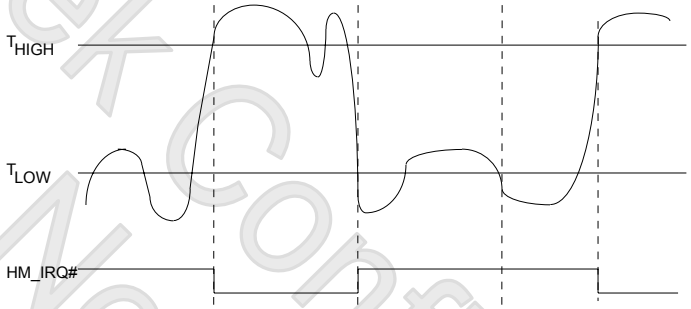
1. Hysteresis mode:

Over temperature event will trigger HM_IRQ# that shown as figure. In hysteresis mode, when monitored temperature exceeds the high temperature threshold value, HM_IRQ# will be asserted until the temperature goes below the hysteresis temperature.



2. High low limit mode: (default):

When in high low limit mode HM_IRQ# for temperature is shown as figure. When monitored temperature exceeds the over-temperature threshold value, HM_IRQ# will be asserted until the temperature goes below the low limit temperature.



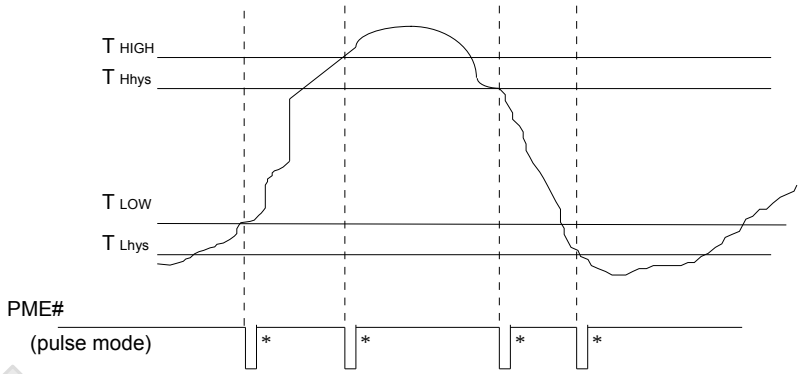
Temperature PME#

There are two mode of temperature PME# function:

1. Hysteresis mode:

PME# interrupt for temperature is shown as figure. Temperature exceeding high limit (low limit) or going below high hysteresis (low hysteresis) will cause an interrupt if the previous interrupt has been reset by writing “1” all the interrupt Status Register.

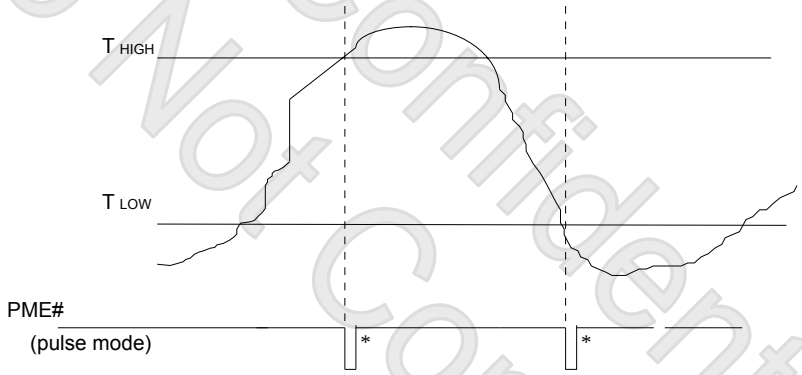
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*Interrupt Reset when Interrupt Status Registers are written 1

2. High low limit mode: (default):

PME# interrupt for temperature is shown as figure. Temperature exceeding high limit or going below low limit will cause an interrupt if the previous interrupt has been reset by writing “1” all the interrupt Status Register.



*Interrupt Reset when Interrupt Status Registers are written 1

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Fan speed count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over 5V. If the input signals from the tachometer outputs are over the 5V, the external trimming circuit should be added to reduce the voltage to obtain the input specification.

Determine the fan counter according to the following equation:

$$\text{Count} = \frac{1.5 \times 10^6}{\text{RPM}}$$

In other words, the fan speed counter has been read from register, the fan speed can be evaluated by the following equation. As for fan, it would be best to use 2 pulses tachometer output per round.

$$\text{RPM} = \frac{1.5 \times 10^6}{\text{Count}}$$

Fan speed control

The F71858AD provides 2 fan speed control methods:

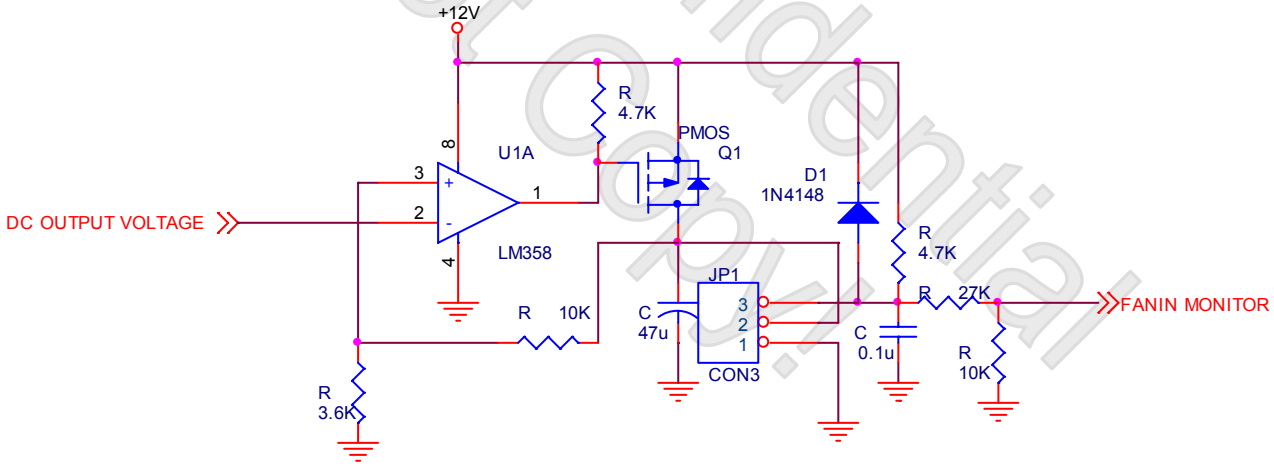
1. DAC FAN CONTROL 2. PWM DUTY CYCLE

DAC Fan Control

The range of DC output is 0~ VCC, controlled by 8-bit register. 1 LSB is about 0.013V (VCC=3.3V). The output DC voltage is amplified by external OP circuit, thus to reach maximum FAN OPERATION VOLTAGE, 12V. The output voltage will be given as followed:

$$\text{Output_voltage (V)} = \text{VCC} \times \frac{\text{Programmed 8bit Register Value}}{256}$$

And the suggested application circuit for DAC fan control would be:

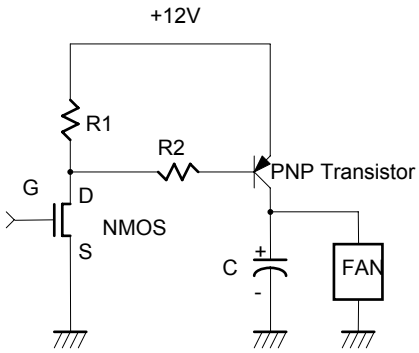


PWM duty Fan Control

The duty cycle of PWM can be programmed by a 8-bit register. The default duty cycle is set to 40%, that is, the default 8-bit registers is set to 66h. The expression of duty can be represented as follows.

$$\text{Duty_cycle(\%)} = \frac{\text{Programmed 8bit Register Value}}{255} \times 100\%$$

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Fan speed control mechanism

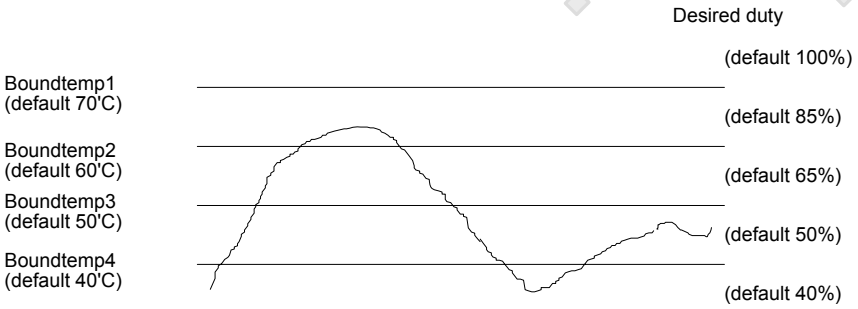
There are some modes to control fan speed and they are 1.Manual mode, 2.Stage auto mode, 3.Linear auto mode. More detail, please refer the description of registers.

Manual mode:

For manual mode, it generally acts as software fan speed control.

Stage auto mode:

At this mode, the F71858AD provides automatic fan speed control related to positive or negative temperature variation of CPU/GPU or the system. The F71858AD can provide four temperature boundaries and five intervals, and each interval has its related fan speed count. All these values should be set by BIOS first. Take below figure as an example. When temperature boundaries are set as 40, 50, 60, and 70°C (each interval differs10°C), the related desired PWM duty for each interval is 100%, 85%, 65%, 50%, and 40%. When the temperature is within 50~60°C, the duty is 65%. Then, the F71858AD will adjust PWMOUT duty-cycle to meet the expected value. It can be said that the fan will be turned on with a specific speed set by BIOS and automatically controlled with the temperature variation. The F71858AD will take charge of all the fan speed control and does not require any software support.

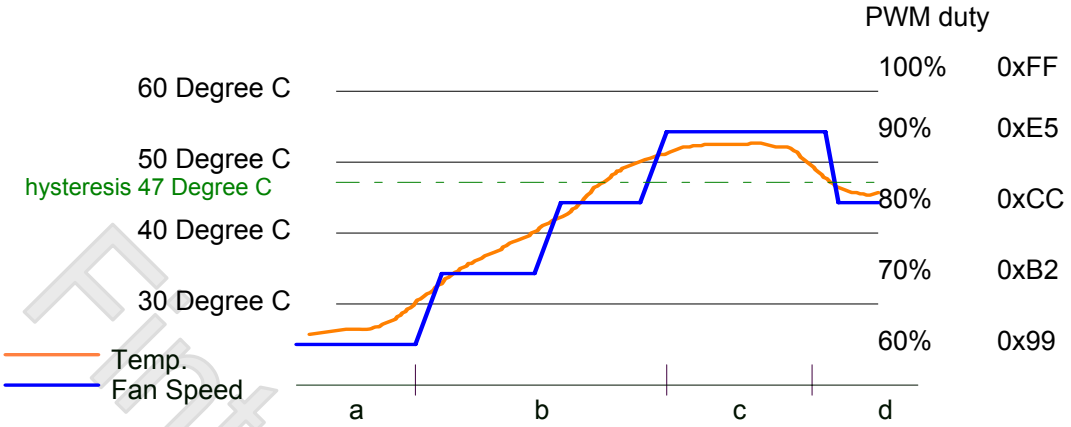


There are two examples as below:

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A. Stage auto mode (PWM Duty)

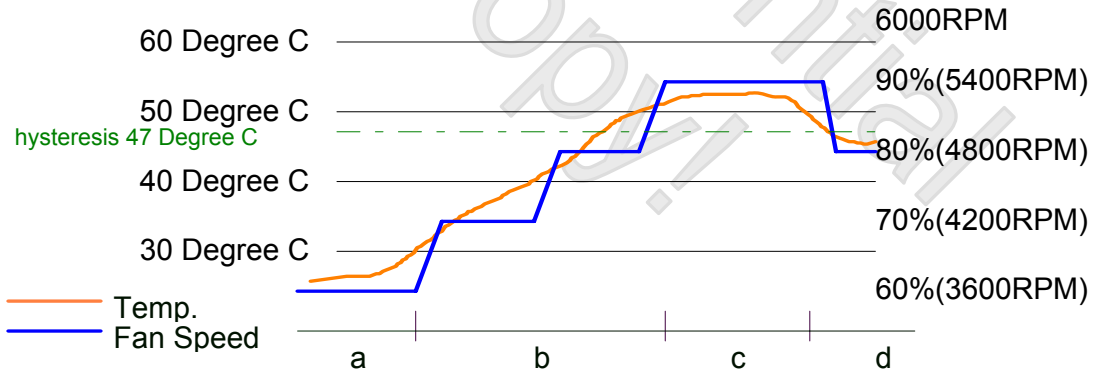
Set temperature as 60°C, 50°C, 40°C, 30°C and Duty as 100%, 90%, 80%, 70%, 60%



a. Once temp. is under 30°C, the lowest fan speed keeps 60% PWM duty
b. Once temp. is over 30°C,40°C,50°C, the fan speed will vary from 60% to 90% PWM duty and increase with temp. level.
c. Once temp. keeps in 55°C, fan speed keeps in 90% PWM duty
d. If set the hysteresis as 3°C (default 4°C), once temp reduces under 47°C, fan speed reduces to 80% PWM duty and stays there.

B. Stage auto mode (RPM%)

Set temperature as 60°C, 50°C, 40°C, 30°C and assume the Full Speed is 6000rpm, set 90% of full speed RPM(5400rpm), 80%(4800rpm), 70%(4200rpm), 60%(3600rpm) of full speed RPM



a. Once temp. is under 30°C, the lowest fan speed keeps 60% of full speed (3600RPM).
b. Once temp. is over 30°C,40°C,50°C, the fan speed will vary from 3600RPM to 5400RPM and increase with temp. level.
c. Once temp. keeps in 55°C, fan speed keeps in 90% of full speed (5400RPM)
d. If set the hysteresis as 3°C (default 4°C), once temp reduces under 47°C, fan speed

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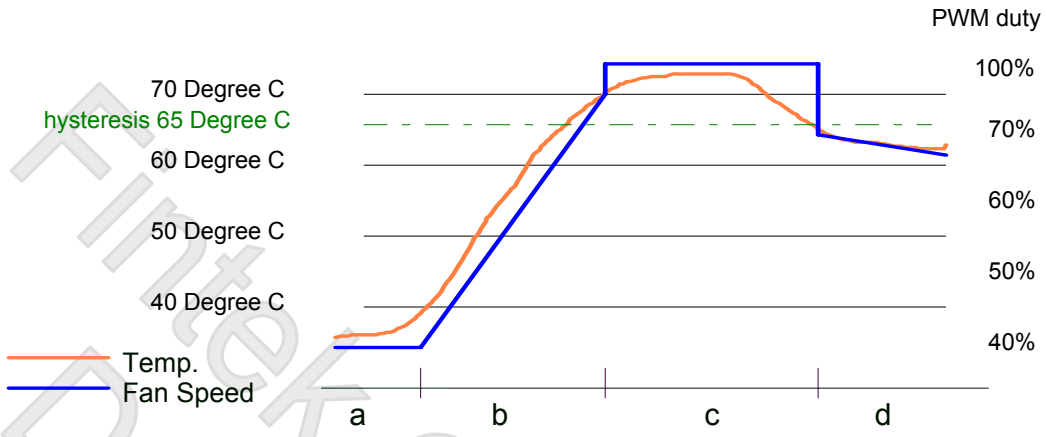
reduces to 4800RPM and stays there.

Linear auto mode:

Otherwise, F71858AD supports linear auto mode. Below two examples are to describe this mode. More detail, please refer the register description.

A. Linear auto mode (PWM Duty)

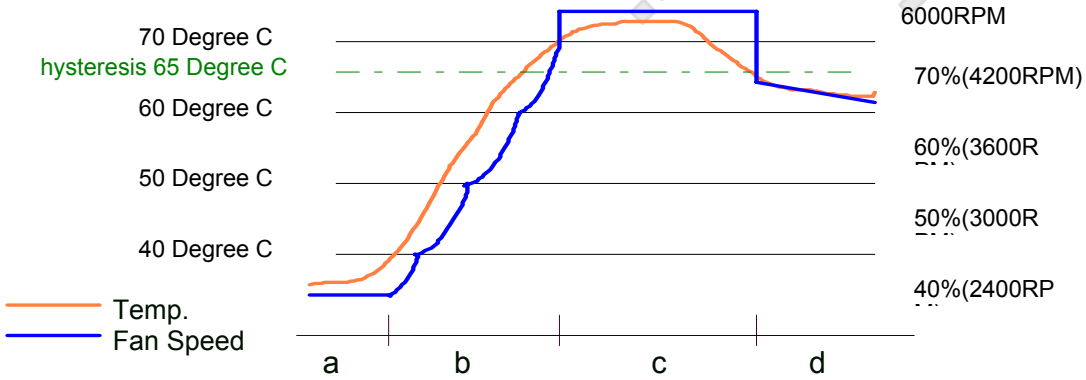
Set temperature as 70°C, 60°C, 50°C, 40°C and Duty as 100%, 70%, 60%, 50%, 40%



a. Once temp. is under 40°C, the lowest fan speed keeps 40% PWM duty
b. Once temp. is over 40°C,50°C,60°C, the fan speed will vary from 40% to 70% PWM duty and linearly increase with temp. variation. The temp.-fan speed monitoring and flash interval is 1sec.
c. Once temp. goes over 70°C, fan speed will directly increase to 100% PWM duty (full speed)
d. If set the hysteresis as 5°C(default is 4°C), once temp reduces under 65°C (not 70°C), fan speed reduces from 100% PWM duty and decrease linearly with temp..

B. Linear auto mode (RPM%)

Set temperature as 70°C, 60°C, 50°C, 40°C and if full speed is 6000RPM, setting 100%, 70%, 60%, 50%, 40% of full speed.



a. Once temp. is under 40°C, the lowest fan speed keeps 40% of full speed (2400RPM)
b. Once temp. is over 40°C,50°C,60°C, the fan speed will vary from 40% to 70% of full

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speed and almost linearly increase with temp. variation. The temp.-fan speed monitoring and flash interval is 1sec.

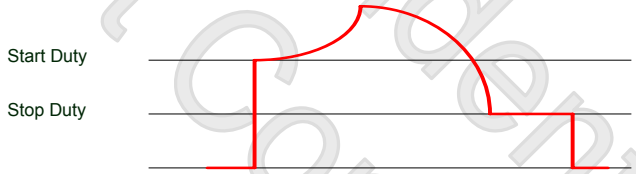
c. Once temp. goes over 70°C, fan speed will directly increase to full speed 6000RPM.
d. If set the hysteresis as 5°C, once temp reduces under 65°C (not 70°C), fan speed reduces from full speed and decrease linearly with temp..

PWMOUT Duty-cycle operating process

In both "Manual RPM" and "Temperature RPM" modes, the F71858AD adjust PWMOUT duty-cycle according to current fan count and expected fan count. It will operate as follows:

(1). When expected count is 0xFFF, PWMOUT duty-cycle will be set to 0x00 to turn off fan.
(2). When expected count is 0x000, PWMOUT duty-cycle will be set to 0xFF to turn on fan with full speed.
(3). If both (1) and (2) are not true,

When PWMOUT duty-cycle decrease to MIN_DUTY(≠ 00h), obviously the duty-cycle will decrease to 00h next, When F71858AD up the fan speed will keep duty-cycle at start duty for 1.2 seconds. After that, the F71858AD starts to compare current fan count and expected count in order to increase or decrease its duty-cycle. This ensures that if there is any glitch during the period, the F71858AD will ignore it.

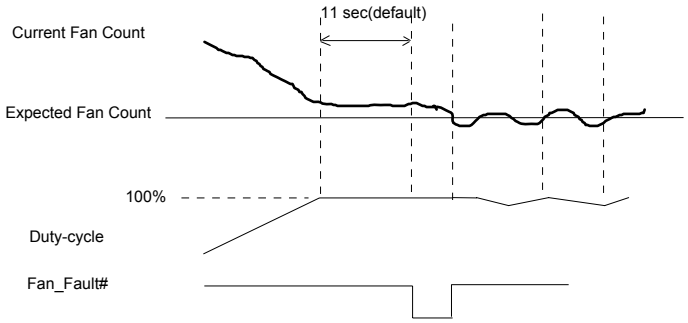


FAN HM_IRQ Signal (HM_IRQ# and PME#)

Fan fault will be asserted when the fan speed doesn't meet the expected fan speed within a programmable period (default is 11 seconds) or when fan stops with respect to PWM duty-cycle which should be able to turn on the fan. There are two conditions may cause the FAN_FAULT# event.

(1). When PWM_Duty reaches 0xFF, the fan speed count can't reach the fan expected count in time.

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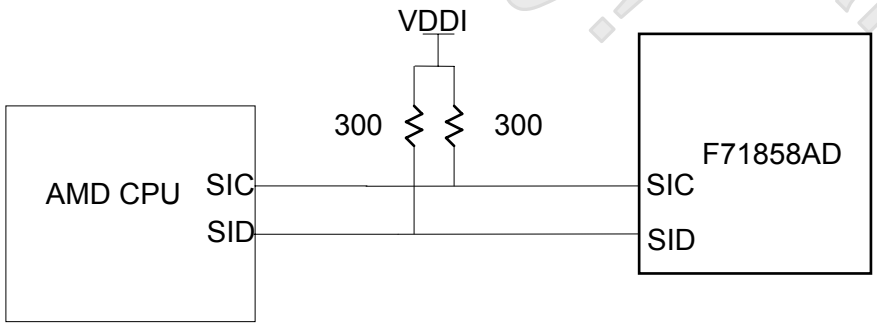
(2). After the period of detecting fan full speed, when PWM_Duty > Min. Duty, and fan count still in 0xFFF.

6.5 LED function

The F71858AD provides two LEDs to indicate system state (S0, S3, and S5) which could be controlled via configuration register. System state could be set as (1) always 0 (2) oscillate 1Hz (3) oscillate 1/2 Hz and (4) always 1. When system is in S0, LED1 is default as 0 and LED2 as 1. When system is in S3, LED1 and LED2 oscillate 1Hz. When system is in S5, LED1 is default as 1 and LED2 as 0.

6.6 AMD TSI and Intel SST PECI Function

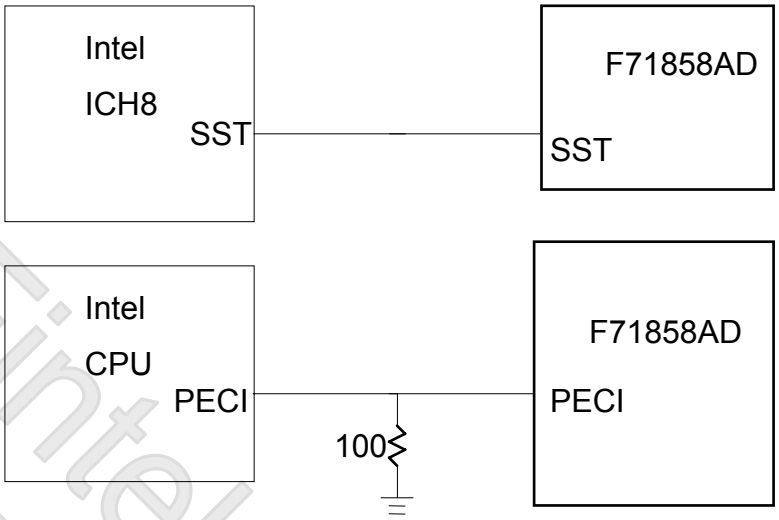
The F71858AD provides Intel SST/PECI/AMD TSI interfaces for new generational CPU temperature sensing. There are SCL and SDA signals for temperature reading from AMD CPU via TSI interface. The SCL signal is for clocking usage, and other is for data transferring. More detail please refer to the register description.



In Intel SST and PECI interfaces, the F71858AD can connect to CPU/SST directly. The F71858AD can read the temperature data from CPU, than the fan control machine of F71858AD can implement the Fan to cool down CPU temperature. As same as PECI, chipset can get information

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from F71858AD including CPU temperature, system temperature (F71858AD provides D+/D- for system temperature sensing), fan speed status by SST. The application circuit is as below. More detail please refer to the register description.



6.7 Watchdog Timer Function

Watch dog timer is provided for system controlling. If time-out can trigger one signal to high/low level/pulse, the signal is depended on register setting.

The time unit has two ways from 1sec or 60sec. In pulse mode, there are four pulse widths can be selected (1ms/25ms/125ms/5sec). Please refer to the device register description for detail.

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7. Register Description

7.1 Global Control Registers

The configuration register is used to control the behavior of the corresponding devices. To configure the register, using the index port to select the index and then writing data port to alter the parameters. The default index port and data port are 0x4E and 0x4F respectively. To enable configuration, the entry key 0x87 must be written to the index port. To disable configuration, write exit key 0x78 twice or key 0xaa once to the index port. Following is an example to enable configuration and disable configuration by using debug.

-o 4e 87
-o 4e 87 (enable configuration)
-o 4e aa (disable configuration)

7.1.1 Software Reset Register — Index 02h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	SOFT_RST	R/W	0	Write 1 to reset the register and device powered by VDD (VCC).

7.1.2 Logic Device Number Register — Index 07h

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Select KBC device configuration registers. 01h: Select PME & ACPI device configuration registers. 02h: Select hardware monitor device configuration registers. 03h: Select GPIO device configuration registers. 04h: Select WDT device configuration registers.

7.1.3 Chip ID Register — Index 20h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID1	R	09h	Chip ID 1 of F71858AD.

7.1.4 Chip ID Register — Index 21h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID2	R	03h	Chip ID2 of F71858AD.

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7.1.5 Vendor ID Register — Index 23h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID1	R	19h	Vendor ID 1 of Fintek devices.

7.1.6 Vendor ID Register — Index 24h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID2	R	34h	Vendor ID 2 of Fintek devices.

7.1.7 Port Select Register — Index 25h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	PORT_4E_EN	R/W	1	The port could be changed by writing this register. 0: Configuration register port is 2E/2F. 1: Configuration register port is 4E/4F. (Default)
3-0	Reserved	-	-	Reserved.

7.1.8 Select KB/MO Wake Up Register — Index 27h (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	DIS_WAKEUP	R/W	0	0: enable KB/MO wakeup function. 1: disable KB/MO wakeup function
6	VSBOK_HYS_DIS	R/W	0	0: Enable VSBOK detect hysteresis. 1: Disable VSBOK detect hysteresys.
5	VSBOK_LVL_SEL	R/W	0	0: VSB3V power good level is 2.8V and not good level is 2.5V. 1: VSB3V power good level is 3.05V and not good level is 2.95V. By VSBOK_HYS_DIS and VSBOK_LVL_SEL, RSMRST# falling edge could be determined: 00: when VSB3V is lower than 2.5V. 01: when VSB3V is lower than 2.95V. 10: when VSB3V is lower than 2.8V. 11: when VSB3V is lower than 3.05V.
4	Reserved	-	0	Reserved.
3	KEY_SEL_ADD	R/W	0	This bit is added to add more wakeup key function.
2	MO_SEL	R/W	0	Select mouse Key to wakeup host 0: click mouse key 1:any mouse key

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<table>
<tr><td>1-0</td><td>KEY_SEL</td><td>R/W</td><td>00</td><td>This registers select the keyboard wake up key. Accompanying with KEY_SEL_ADD, there are eight wakeup keys:
<table>
<tr><th>KEY_SEL_ADD</th><th>KEY_SEL</th><th>Wakeup Key</th></tr>
<tr><td>0</td><td>00</td><td>CTRL + ESC</td></tr>
<tr><td>0</td><td>01</td><td>CTRL + F1</td></tr>
<tr><td>0</td><td>10</td><td>CTRL + USER_WAKEUP_CODE (SPACE)</td></tr>
<tr><td>0</td><td>11</td><td>Any Key</td></tr>
<tr><td>1</td><td>00</td><td>Windows Wakeup</td></tr>
<tr><td>1</td><td>01</td><td>Windows Power</td></tr>
<tr><td>1</td><td>10</td><td>CTRL + Alt + USER_WAKEUP_CODE (SPACE)</td></tr>
<tr><td>1</td><td>11</td><td>USER_WAKEUP_CODE (SPACE)</td></tr>
</table></td></tr>
</table>

7.1.9 Multi-Function Select Register 1 — Index 28h (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO03_EN	R/W	0	RSTIN#/GPIO03 Function Select. 0: Pin function is RSTIN#. 1: Pin function is GPIO03.
5-4	GPIO02_SEL	R/W	0	FANIN4/SST/AMDTSI_CLK/GPIO02 Function Select. 00: Pin function is FANIN4. 01: Pin function is SST. 10: Pin function is AMDTSI_CLK. 11: Pin function is GPIO02.
3	Reserved	-	-	Reserved.
2	GPIO01_EN	R/W	0	FANIN3/GPIO01 Function Select. 0: Pin function is FANIN3. 1: Pin function is GPIO01.
1-0	GPIO00_SEL	R/W	0	PECI/AMDTSI_DAT/GPIO00 Function Select. 00: Pin function is PECI. 01: Reserved. 10: Pin function is AMDTSI_DAT. 11: Pin function is GPIO00.

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7.1.10 Multi-Function Select Register 2 — Index 29h (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	GPIO07_EN	R/W	0	LED2/GPIO07 Function Select. 0: Pin function is LED2. 1: Pin function is GPIO07.
6	GPIO06_EN	R/W	0	LED1/GPIO06 Function Select. 0: Pin function is LED1. 1: Pin function is GPIO06.
5	GPIO05_EN	R/W	0	PCIRST5#/GPIO05 Function Select. 0: Pin function is PCIRST5#. 1: Pin function is GPIO05.
4	GPIO04_EN	R/W	0	PCIRST4#/GPIO04 Function Select. 0: Pin function is PCIRST4#. 1: Pin function is GPIO04.
3-2	Reserved	-	-	Reserved.
1	KB_GP_EN	R/W	0	Keyboard Interface and GPIO Function Select. 0: Pin 41 and 42 are KCLK and KDATA respectively. 1: Pin 41 and 42 are GPIO10 and GPIO11 respectively.
0	MO_GP_EN	R/W	0	Mouse Interface and GPIO Function Select. 0: Pin 43 and 44 are MCLK and MDATA respectively. 1: Pin 43 and 44 are GPIO12 and GPIO13 respectively.

7.2 KBC Registers

7.2.1 Logic Device Number Register

Logic Device Number Register — Index 07H

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Select KBC device configuration registers. 01h: Select PME & ACPI device configuration registers. 02h: Select hardware monitor device configuration registers. 03h: Select GPIO device configuration registers. 04h: Select WDT device configuration registers.

7.2.2 KBC Configuration Registers

KBC Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	KBC_EN	R/W	1	0: disable KBC. 1: enable KBC.

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Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of KBC base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	60h	The LSB of KBC base address.

Keyboard IRQ Channel Enable Register — Index 70h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
0	ENKBCIRQ	R/W	1	Enable the IRQ channel for Keyboard.

Mouse IRQ Channel Enable Register — Index 72h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
0	ENMOCIRQ	R/W	1	Enable the IRQ channel for Mouse.

Auto Swap Register — Index FEh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	AUTO_DET_EN	R/W	0	0: disable auto detect keyboard/mouse swap. 1: enable auto detect keyboard/mouse swap.
6-5	Reserved	-	-	Reserved.
4	KB_MO_SWAP	R/W	0	0: Keyboard/mouse does not swap. 1: Keyboard/mouse swap. This bit is set/clear by hardware if AUTO_DET_EN is set to “1”. Users could also program this bit manually.
3-0	Reserved	-	-	Reserved

User Wakeup Code Register — Index FFh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7-0	USER_WAKEUP_CODE	R/W	29h	This is user define wakeup code. Default is space.

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7.3 ACPI and PME Registers

7.3.1 Logic Device Number Register

Logic Device Number Register — Index 07H

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Select KBC device configuration registers. 01h: Select PME & ACPI device configuration registers. 02h: Select hardware monitor device configuration registers. 03h: Select GPIO device configuration registers. 04h: Select WDT device configuration registers.

7.3.2 ACPI and PME Configuration Registers

Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	PME_EN	R/W	0	0: disable PME. 1: enable PME.

PME Event Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7	WDT_PME_EN	R/W	0	Watchdog Timer PME event enable. 0: disable Watchdog Timer PME event. 1: enable Watchdog Timer PME event.
6	MS_PME_EN	R/W	0	PS/2 mouse PME event enable. 0: disable PS/2 mouse PME event. 1: enable PS/2 mouse PME event.
5	KB_PME_EN	R/W	0	PS/2 keyboard PME event enable. 0: disable PS/2 keyboard PME event. 1: enable PS/2 keyboard PME event.
4	GP_PME_EN	R/W	0	GPIO PME event enable. 0: disable GPIO PME event. 1: enable GPIO PME event.
3-1	Reserved	-	-	Reserved
0	HM_PME_EN	R/W	0	Hardware Monitor PME event enable. 0: disable Hardware Monitor PME event. 1: enable Hardware Monitor PME event.

PME Event Status Register — Index F1h

Bit	Name	R/W	Default	Description
7	WDT_PME_ST	R/WC	-	Watchdog Timer PME event status. 0: Watchdog Timer has no PME event. 1: Watchdog Timer has a PME event to assert. Write 1 to clear to be ready for next PME event.

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6	MS_PME_ST	R/W	0	PS/2 mouse PME event status. 0: PS/2 mouse has no PME event. 1: PS/2 mouse has a PME event to assert. Write 1 to clear to be ready for next PME event.
5	KB_PME_ST	R/W	0	PS/2 keyboard PME event status. 0: PS/2 keyboard has no PME event. 1: PS/2 keyboard has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	GP_PME_ST	R/WC	-	GPIO PME event status. 0: GPIO has no PME event. 1: GPIO has a PME event to assert. Write 1 to clear to be ready for next PME event.
3-1	Reserved	-	-	Reserved
0	HM_PME_ST	R/W	0	Hardware Monitor PME event status. 0: Hardware Monitor has no PME event. 1: Hardware Monitor has a PME event to assert. Write 1 to clear to be ready for next PME event.

ACPI Control Register — Index F4h

Bit	Name	R/W	Default	Description
7	TS3	R/W	0	Set to 1 to enable keyboard or mouse can wakeup from S1 state, It must also set EN_KBCWAKEUP and EN_MOWAKEUP register.
6-5	Reserved	-	-	Reserved.
4	ENKBWAKEUP	R/W	0	0:disable keyboard wakeup signal (PS_OUT#) 1:enable keyboard wakeup signal
3	ENMOWAKEUP	R/W	0	0:disable mouse wakeup signal (PS_OUT#) 1:enable mouse wakeup signal
2-1	PWRCTRL	R/W	11	The ACPI Control the PSON# to 00 : keep last state 10 : Always on 01 : Bypass mode. 11: Always off
0	VSB_PWR_LOSS	R/W	0	When VSB 3V comes, it will set to 1, and write 1 to clear it

ACPI Control Register — Index F5h

Bit	Name	R/W	Default	Description
7	SEL_S3	R/W	0	KBC S3 Signal Select 0: KBC enter S3 state if S3# is low (TS3 is 0) or TS3 is set. 1: KBC enter S3 state if VDD3V below 2.5V.
6	Reserved	-	-	Reserved
5	BYPASS_LRST	R/W	1	0: Enable LRESET# de-bounce circuit (200us) for PCIRST# signal. 1: Disable LRESET# de-bounce circuit (200us) for PCIRST# signal.
4	RSTCON_EN	R/W	0	0: RSTCON# asserts via PWROK. 1: RSTCON# asserts via PCIRST#.
3-2	DELAY	R/W	11	The PWROK delay timing from VCC3VOK by following setting 00 : 100ms 01 : 200ms 10 : 300ms 11 : 400ms

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1	Bypass_db	R/W	0	BYPASS the S3#/S4#/PSIN#/RSTIN# Pins.
0	VINDB_EN	R/W	1	0: Disable RSTCON# 50ms de-bounce circuit. 1: Enable RSTCON# 50ms de-bounce circuit.

ACPI Soft reset Register — Index F6h

Bit	Name	R/W	Default	Description
7	SOFT_RST_ACPI	W	0	Software Reset to ACPI Set to 1 to reset ACPI
6-0	Reserved	-	-	Reserved

ACPI reset enable Register — Index F7h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	PCIRST5_EN	R/W	1	0: Disable PCIRST5# output. 1: Enable PCIRST5# output.
3	PCIRST4_EN	R/W	1	0: Disable PCIRST4# output. 1: Enable PCIRST4# output.
2	PCIRST3_EN	R/W	1	0: Disable PCIRST3# output. 1: Enable PCIRST3# output.
1	PCIRST2_EN	R/W	1	0: Disable PCIRST2# output. 1: Enable PCIRST2# output.
0	PCIRST1_EN	R/W	1	0: Disable PCIRST1# output. 1: Enable PCIRST1# output.

ACPI reset data Register — Index F8h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	PCIRST5_DAT	R/W	0	Write “1” to output PCIRST5# 2ms low pulse.
3	PCIRST4_DAT	R/W	0	Write “1” to output PCIRST4# 2ms low pulse.
2	PCIRST3_DAT	R/W	0	Write “1” to output PCIRST3# 2ms low pulse.
1	PCIRST2_DAT	R/W	0	Write “1” to output PCIRST2# 2ms low pulse.
0	PCIRST1_DAT	R/W	0	Write “1” to output PCIRST1# 2ms low pulse.

LED S0 status Register — Index F9h

Bit	Name	R/W	Default	Description
7	Phase	R/W	0	When bit 7 is the same of the bit 3, LED2 oscillate phase is same with LED1.
6	Reserved	-	-	Reserved
5-4	LED2_S0	R/W	2’b11	Indicate LED2 response when system is in S0 00:LED assert 0 01: oscillate 1Hz 10: oscillate 1/2Hz 11: tri-state
3	Phase	R/W	0	When bit 7 is same with bit 3, LED2 oscillate phase is same with LED1.
2	Reserved	-	-	Reserved

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1-0	LED1_S0	W	2'b00	Indicate LED1 response when system in S0 state 00:LED assert 0 01: oscillate 1Hz 10: oscillate 1/2Hz 11: tri-state

LED S3/S5 status Register — Index FAh

Bit	Name	R/W	Default	Description
7-6	LED2_S5	R/W	2'b00	Indicate LED2 response when system in S5 state 00:LED assert 0 01: oscillate 1Hz 10: oscillate 1/2Hz 11: tri-state
5-4	LED2_S3	R/W	2'b01	Indicate LED2 response when system in S3 state 00:LED assert 0 01: oscillate 1Hz 10: oscillate 1/2Hz 11: tri-state
3-2	LED1_S5	R/W	2'b11	Indicate LED1 response when system in S5 state 00:LED assert 0 01: oscillate 1Hz 10: oscillate 1/2Hz 11: tri-state.
1-0	LED1_S3	W	2'b01	Indicate LED1 response when system in S3 state 00:LED assert 0 01: oscillate 1Hz 10: oscillate 1/2Hz 11: tri-state

PWOK & PS_ON Control Register — Index FBh

Bit	Name	R/W	Default	Description
7	PWOK_DAT	W	1'b0	Write 1 to generate a 250ms low pulse from PWOK.
6-5	Reserved	-	-	Reserved
4	S3_PWOK_EN	R/W	0	0: PWOK doesn't gate with S3#. 1: PWOK gate with S3#.
3-2	PWOK_DELAY	R/W	0	PWOK extra delay. 00: 0ms. 01: 100ms. 10: 200ms. 11: 400ms.
1	WDT_PWOK_EN	R/W	0	0: Disable WDTRST# asserts from PWOK. 1: Enable WDTRST# asserts from PWOK.
0	PSON_DEL_EN	R/W	0	Set "1" to enable delay 4 second to power on.

PCIRST# Level Control Register — Index FCh

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	PCIRST5_GATE	R/W	1	Write 0 to force PCIRST5# low.
3	PCIRST4_GATE	R/W	1	Write 0 to force PCIRST4# low.
2	PCIRST3_GATE	R/W	1	Write 0 to force PCIRST3# low.
1	PCIRST2_GATE	R/W	1	Write 0 to force PCIRST2# low.
0	PCIRST1_GATE	R/W	1	Write 0 to force PCIRST1# low.

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7.4 Hardware Monitor Registers (Index port: 0x295; Data port: 0x296)

***** CR xx = Hardware Monitor Index xx**

7.4.1 Logic Device Number Register

Logic Device Number Register — Index 07H

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Select KBC device configuration registers. 01h: Select PME & ACPI device configuration registers. 02h: Select hardware monitor device configuration registers. 03h: Select GPIO device configuration registers. 04h: Select WDT device configuration registers.

7.4.2 Hardware Monitor Configuration Registers

Hardware Monitor Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	HM_EN	R/W	1	0: disable hardware monitor. 1: enable hardware monitor.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	02h	The MSB of HM base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	95h	The LSB of HM base address.

7.4.3 Hardware Monitor Device Register

Configuration Register — Index 01h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	POWER_DOWN	R/W	0	Hardware monitor function power down.
1	FAN_START	R/W	1	Set one to enable startup of fan monitoring operations; a zero puts the part in standby mode.
0	V_T_START	R/W	1	Set one to enable startup of temperature and voltage monitoring operations; a zero puts the part in standby mode.

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Configuration Register — Index 02h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Return 0.
5-4	HW_IRQ_MODE	R/W	00	00: The HW_IRQ# will be low active level mode. 01: The HW_IRQ# will be low active pulse mode. (160us) 10: The HW_IRQ# will indicate by 1Hz LED function. 11: The HW_IRQ# will indicate by (400/800HZ) BEEP output.
4-0	Reserved	-	-	--

Configuration Register — Index 06h

Bit	Name	R/W	Default	Description
7	NEW_MODE_EN	R/W	0	Set this bit to enable new function mode.
6	Reserved	R	0	Reserved
5-4	Reserved	R/W	0	Reserved
3	OPEN_SHORT_SEL	R/W	0	0: The reading of temperature when open will be 0xBB. The reading of temperature when short will be 0xCC. 1: The reading of temperature when open or short will be 0x80.
2	Reserved	R	0	Reserved
1-0	DIG_RATE_SEL	R/W	0	PECI / AMD TSI will access the external slave device after 00: Diode temperatures convert 1 time. 01: Diode temperatures convert 2 times. 10: Diode temperatures convert 3 times. 11: Diode temperatures convert 4 times.

TSI/SMBUS Address Register — Index 08h

Bit	Name	R/W	Default	Description
7-1	SMBUS_ADDR	R/W	7'h26	When AMD TSI or Intel PCH SMBus is enabled, this byte is used as SMBUS_ADDR. SMBUS_ADDR[7:1] is the slave address sent by the embedded master to fetch the temperature.
0	Reserved	-	-	Reserved

PECI SST AMD TSI Interface Configuration Register — Index 0Ah

Bit	Name	R/W	Default	Description
7-6	Reserved	R/W	0	Reserved.
5	T1_IIR_EN	R/W	0	Set 1 to enable the IIR for AMD TSI/PECI reading.
4	SST_EN	R/W	0	Enable SST Interface.
3-2	PECI_POWER_SEL	R/W	00	00: PECI output high level will be 1.23V 01: PECI output high level will be 1.13V 10: PECI output high level will be 1.00V 11: PECI output high level will be 1.00V
1-0	MEAS_TYPE	R/W	0	Select the CPU temperature measure method 00: External thermal diode. 01: PECI interface. 10: AMD TSI interface. 11: Reserved.

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Dual Single Core select Register — Index 0Bh (MEAS_TYPE ==2'b01)

Bit	Name	R/W	Default	Description
7-4	CPU_SEL	R/W	0	Select the Intel CPU socket number. 0000: no CPU presented. PECI host will use Ping() command to find CPU address. 0001: CPU is in socket 0, i.e. PECI address is 0x30. 0010: CPU is in socket 1, i.e. PECI address is 0x31. 0100: CPU is in socket 2, i.e. PECI address is 0x32. 1000: CPU is in socket 3, i.e. PECI address is 0x33. Others are reserved.
3-2	Reserved	R	0	Reserved
1	TEMPVALUE_SEL	R/W	0	When Dual Core CPU selection. Temperature value measurement method will be selected by this bit. 0: Average dual cores' temperature. 1: Select higher one temperature of these two cores.
0	DUAL_CORE_EN	R/W	0	When PECI interface enable, this will be Dual Single Core select register. 0: Single Core CPU selection 1: Dual Core CPU selection

TCC Activation Temperature Register — Index 0Ch

Bit	Name	R/W	Default	Description
7-0	TCC_TEMP	R/W	0	TCC Activation Temperature. The absolute value of CPU temperature is calculated by the equation if PECI or TSI Interface is enabled: CPU_TEMP = TCC_TEMP + PECI Reading. CPU_TEMP = TCC_TEMP + TSI Reading The range of this register is -128 ~ 127.

SST Address Register — Index 0Dh

Bit	Name	R/W	Default	Description
7-0	SST_ADDR	R/W	8'h4C	Address for SST interface. Programmable.

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CPU Temp. Measure Select Register — Index 0Eh

Bit	Name	R/W	Default	Description
7-4	Reserved	-	0	Reserved.
3	ADD	R/W	0	Temperature scale selection. 1: Temp. Measure = Reading Value + Reading Value* $2^{-Scale[2:0]}$ 0: Temp. Measure = Reading Value - Reading Value* $2^{-Scale[2:0]}$
2-0	SCALE[2:0]	R/W	000	When ADD=1, the Temp. Measure is 000: 1 * Reading Value 001: 3/2 * Reading Value …….. 110: 65/64 * Reading Value 111: 129/128 * Reading Value ---------- When ADD=0, the Temp. Measure is 000: 1 * Reading Value 001: 1/2 * Reading Value …….. 110: 63/64 * Reading Value 111: 127/128 * Reading Value

PECI / AMD TSI Temp. Measure Select Register — Index 0Fh

Bit	Name	R/W	Default	Description
7-4	Reserved	-	0	Reserved.
3	DIG_ADD	R/W	0	Temperature scale selection. 1: Temp. Measure = Reading Value + Reading Value* $2^{-Scale[2:0]}$ 0: Temp. Measure = Reading Value - Reading Value* $2^{-Scale[2:0]}$
2-0	DIG_SCALE[2:0]	R/W	000	When DIG_ADD=1, the Temp. Measure is 000: 1 * Reading Value 001: 3/2 * Reading Value …….. 110: 65/64 * Reading Value 111: 129/128 * Reading Value ---------- When DIG_ADD=0, the Temp. Measure is 000: 1 * Reading Value 001: 1/2 * Reading Value …….. 110: 63/64 * Reading Value 111: 127/128 * Reading Value

*Write CR0E will also write CR0F

Voltage reading and limit— Index 20h- 22h

Address	Attribute	Default	Description
20h	RO	--	VCC3V reading. The unit of reading is 8mV.
21h	RO	--	VSB3V reading. The unit of reading is 8mV.
22h	RO	--	VBAT3V reading. The unit of reading is 8mV.

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Temperature PME# Enable Register — Index 60h

Bit	Name	R/W	Default	Description
7	Reserved	R	0	Reserved
6	EN_T2_HIGH_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt. (CR61 bit6)
5	EN_T1_HIGH_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt. (CR61 bit5)
4	EN_L_HIGH_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt. (CR61 bit4)
3	Reserved	R	0	Reserved
2	EN_ T2_LOW_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt. (CR61 bit2)
1	EN_ T1_LOW_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt. (CR61 bit1)
0	EN_L_LOW_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt. (CR61 bit0)

Temperature Interrupt Status Register — Index 61h

Bit	Name	R/W	Default	Description
7	Reserved	R	0	Reserved
6	T2_HIGH_STS	R/W	0	**H_L_LIMIT_MODE set to 1 (CR69 bit 4) "default"** Set when the TEMP2 (CR74) exceeds the HIGH limit (CR84) or when temperature return from over HIGH to under LOW limit (CR85). Write 1 to clear this bit, write 0 will be ignored. **H_L_LIMIT_MODE set to 0 (CR69 bit 4)** Set when the TEMP2 (CR74) exceeds the HIGH limit (CR84) or when temperature return from over HIGH to under "HIGH limit –hysteresis (CR6D)". Write 1 to clear this bit, write 0 will be ignored.
5	T1_HIGH_STS	R/W	0	**H_L_LIMIT_MODE set to 1 (CR69 bit 4) "default"** Set when the TEMP1 (CR72) exceeds the HIGH limit (CR82) or when temperature return from over HIGH to under LOW limit (CR83). Write 1 to clear this bit, write 0 will be ignored. **H_L_LIMIT_MODE set to 0 (CR69 bit 4)** Set when the TEMP1 (CR72) exceeds the HIGH limit (CR82) or when temperature return from over HIGH to under "HIGH limit –hysteresis (CR6C)". Write 1 to clear this bit, write 0 will be ignored.
4	LOCAL_HIGH_STS	R/W	0	**H_L_LIMIT_MODE set to 1 (CR69 bit 4) "default"** Set when the LOCAL TEMP (CR70) exceeds the HIGH limit (CR80) or when temperature return from over HIGH to under LOW limit (CR81). Write 1 to clear this bit, write 0 will be ignored. **H_L_LIMIT_MODE set to 0 (CR69 bit 4)** Set when the LOCAL TEMP exceeds the HIGH limit (CR80) or when temperature return from over HIGH to under "HIGH limit –hysteresis (CR6C).. Write 1 to clear this bit, write 0 will be ignored.
3	Reserved	R	0	Reserved
2	T2_LOW_STS	R/W	0	**H_L_LIMIT_MODE set to 1 (CR69 bit 4) "default"** This bit always return 0. **H_L_LIMIT_MODE set to 0 (CR69 bit 4)** Set when the TEMP2 exceeds the LOW limit (CR85) or when temperature return from over HIGH to under "LOW limit –hysteresis (CR6D).. Write 1 to clear this bit, write 0 will be ignored.

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1	T1_LOW_STS	R/W	0	**H_L_LIMIT_MODE set to 1 (CR69 bit 4) "default"** This bit always return 0. **H_L_LIMIT_MODE set to 0 (CR69 bit 4)** Set when the TEMP1 exceeds the LOW limit (CR83) or when temperature return from over HIGH to under "LOW limit –hysteresis (CR6C)".. Write 1 to clear this bit, write 0 will be ignored.
0	LOCAL_LOW_STS	R/W	0	**H_L_LIMIT_MODE set to 1 (CR69 bit 4) "default"** This bit always return 0. **H_L_LIMIT_MODE set to 0 (CR69 bit 4)** Set when the LOCAL TEMP exceeds the LOW limit (CR81) or when temperature return from over HIGH to under "LOW limit –hysteresis (CR6C)".. Write 1 to clear this bit, write 0 will be ignored.

Temperature Real Time Status Register — Index 62h

Bit	Name	R/W	Default	Description
7	Reserved	R	0	Reserved
6	T2_HIGH_EXC	R/W	0	**H_L_LIMIT_MODE set to 1 (CR69 bit 4)** Set when the TEMP2 exceeds the HIGH limit (CR84). Clear when the TEMP2 is below the LOW limit (CR85) –hysteresis (CR6D) temperature. **H_L_LIMIT_MODE set to 0 (CR69 bit 4)** Set when the TEMP2 exceeds the HIGH limit (CR84). Clear when the TEMP2 is below the "HIGH limit (CR84) –hysteresis (CR6D)" temperature.
5	T1_HIGH_EXC	R/W	0	**H_L_LIMIT_MODE set to 1 (CR69 bit 4)** Set when the TEMP1 exceeds the HIGH limit (CR82). Clear when the TEMP1 is below the LOW limit (CR83) –hysteresis (CR6C) temperature. **H_L_LIMIT_MODE set to 0 (CR69 bit 4)** Set when the TEMP1 exceeds the HIGH limit (CR82). Clear when the TEMP1 is below the "HIGH limit (CR82)–hysteresis (CR6C)" temperature.
4	LOCAL_HIGH_EXC	R/W	0	**H_L_LIMIT_MODE set to 1 (CR69 bit 4)** Set when the Local TEMP exceeds the HIGH limit (CR80). Clear when the Local TEMP is below the LOW limit (CR81) –hysteresis (CR6C) temperature. **H_L_LIMIT_MODE set to 0 (CR69 bit 4)** Set when the Local TEMP exceeds the HIGH limit (CR80). Clear when the Local TEMP is below the "HIGH limit(CR80)–hysteresis(CR6C)" temperature.
3	Reserved	R	0	Reserved
2	T2_LOW_EXC	R/W	0	**H_L_LIMIT_MODE set to 1 (CR69 bit 4)** This bit always return 0. **H_L_LIMIT_MODE set to 0 (CR69 bit 4)** Set when the TEMP2 exceeds the LOW limit (CR85). Clear when the TEMP2 is below the "LOW limit(CR85) –hysteresis (CR6D)" temperature.
1	T1_LOW_EXC	R/W	0	**H_L_LIMIT_MODE set to 1 (CR69 bit 4)** This bit always return 0. **H_L_LIMIT_MODE set to 0 (CR69 bit 4)** Set when the TEMP1 exceeds the LOW limit (CR83). Clear when the TEMP1 is below the "LOW limit(CR83) –hysteresis (CR6C)" temperature.
0	LOCAL_LOW_EXC	R/W	0	**H_L_LIMIT_MODE set to 1 (CR69 bit 4)** This bit always return 0. **H_L_LIMIT_MODE set to 0 (CR69 bit 4)** Set when the Local TEMP exceeds the LOW limit (CR81). Clear when the Local TEMP is below the "LOW limit (CR81)–hysteresis (CR6C)" temperature.

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CPU Exceeds Limit Temperature Select Register — Index 64h

Bit	Name	R/W	Default	Description
7-5	Reserved	R	-	Reserved
4	CPU_TEMP_SEL	R/W	0	The diode T1 or PECI or AMD TSI temperature is used to compare with T1_HIGH_LIMIT/T1_LOW_LIMIT according to the conditions show below. It is selected by "NEW_MODE_EN" in CR06 [7] and CPU_TEMP_SEL. When {NEW_MODE_EN, CPU_TEMP_SEL} is : 0x: Select diode T1/PECI/AMD TSI base on "MEAS_TYPE" in CR0A [1:0]. 10: Diode T1 is selected 11: Select PECI or AMD TSI base on "MEAS_TYPE" in CR0A [1:0].
3-0	Reserved	-	-	Reserved

HW_IRQ# Output Enable Register 1 — Index 66h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	EN_T2_ HW_IRQ	R/W	0	When T2_HIGH_EXC (CR65 bit6) is active and this bit is Enabled. Then pin HW_IRQ# will be active and user can select HW_IRQ mode from CR 02.
1	EN_T1_ HW_IRQ	R/W	1	When T1_HIGH_EXC (CR65 bit5) is active and this bit is Enabled. Then pin HW_IRQ# will be active and user can select HW_IRQ mode from CR02.
0	EN_LOCAL_HW_IRQ	R/W	0	When LOCAL_HIGH_EXC (CR65 bit4) is active and this bit is Enabled. Then pin HW_IRQ # will be active and user can select HW_IRQ mode from CR02.

Temperature PME# mode and Table Select Register -- Index 69h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	H_L_LIMIT_MODE	R/W	1	**If H_L_LIMIT_MODE set to 1** TEMP exceeds will be set when over HIGH limit. And clear when the TEMP below the LOW limit –hysteresis temperature. **Else if H_L_LIMIT_MODE set to 0** TEMP exceeds will be set when over HIGH/LOW limit. And clear when the TEMP below the "HIGH/LOW limit–hysteresis" temperature.
3-0	Reserved	-	-	Reserved

LOCAL and TEMP1 Limit Hysteresis Select Register -- Index 6Ch

Bit	Name	R/W	Default	Description
7-4	TEMP1_HYS	R/W	0h	TEMP1 will exceeds when over limit until under then "limit - TEMP1_HYS (hysteresis)"
3-0	LOCAL_HYS	R/W	0h	L TEMP will exceeds when over limit until under then "limit – L TEMP_HYS (hysteresis)"

TEMP2 and TEMP3 Limit Hysteresis Select Register -- Index 6Dh

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved
3-0	TEMP2_HYS	R/W	0h	TEMP2 will exceeds when over limit until under then "limit – TEMP2_HYS (hysteresis)"

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DIODE OPEN Status Register -- Index 6Fh

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved
3	T_DIG_OPEN	RO	0h	Open status of PECI or TSI Interface when one of them is enabled.
2	T2_DIODE_OPEN	RO	0h	External diode 2 is open or short
1	T1_DIODE_OPEN	RO	0h	External diode 1 is open or short
0	T0_DIODE_OPEN	RO	0h	Internal diode 0 is open or short

Temperature Register — Index 70h- 8Fh

Address	Attribute	Default	Description
70h	RO	--	Local temperature [10:3] reading. The unit of reading is 1°C.At the moment of reading this register. Bit10 is the sign bit of the local temperature. Maximum display is 127'C, minimum display is -40'C
71h	RO	--	CR71 bit7-bit5 are the Local temperature reading value [2:0]. The unit of reading is 0.125°C.
72h	RO	--	Temperature 1 [10:3] reading. The unit of reading is 1°C.At the moment of reading this register. Bit10 is the sign bit of the temperature 1. Maximum display is 127'C, minimum display is -40'C (When NEW_MODE_EN is set to 1, this byte will always be Diode T1 reading)
73h	RO	--	CR73 bit7-bit5 are the temperature 1 reading value [2:0]. The unit of reading is 0.125°C (When NEW_MODE_EN is set to 1, this byte will always be Diode T1 reading).
74h	RO	--	Temperature 2 [10:3] reading. The unit of reading is 1°C.At the moment of reading this register. Bit10 is the sign bit of the temperature 2. Maximum display is 127'C, minimum display is -40'C
75h	RO	--	CR75 bit7-bit5 are the temperature 2 reading value[2:0]. The unit of reading is 0.125°C.
76-79h	RO	FFh	Reserved
7Ah	RO	--	PECI or TSI temperature reading
7B~7F	RO	FFh	Reserved
80h	R/W	46h	Local Temperature sensor HIGH limit. The unit is 1°C.
81h	R/W	3Ch	Local Temperature sensor LOW limit. The unit is 1°C.
82h	R/W	64h	Temperature sensor 1 HIGH limit. The unit is 1°C.
83h	R/W	55h	Temperature sensor 1 LOW limit. The unit is 1°C.
84h	R/W	64h	Temperature sensor 2 HIGH limit. The unit is 1°C.
85h	R/W	55h	Temperature sensor 2 LOW limit. The unit is 1°C.
86~8Dh	RO	FFH	Reserved

Temperature Filter Select Register -- Index 8Eh

Bit	Name	R/W	Default	Description
7-6	DIG-QUEUR	R/W	1h	The queue time for second filter to quickly update values. 00: 8 times. 01: 16 times. (default). 10: 24 times. 11: 32 times.

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5-4	IIR-QUEUR2	R/W	1h	The queue time for second filter to quickly update values. 00: 8 times. 01: 16 times. (default). 10: 24 times. 11: 32 times.
3-2	IIR-QUEUR1	R/W	1h	The queue time for second filter to quickly update values. 00: 8 times. 01: 16 times. (default). 10: 24 times. 11: 32 times.
1-0	IIR-QUEUR-LOCAL	R/W	1h	The queue time for second filter to quickly update values. 00: 8 times. 01: 16 times. (default). 10: 24 times. 11: 32 times.

FAN PME# Enable Register — Index 90h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	EN_FAN3_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt. (CR91 bit2)
1	EN_FAN2_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt. (CR91 bit1)
0	EN_FAN1_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt. (CR91 bit0)

FAN Interrupt Status Register — Index 91h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	FAN3_STS	R/W	--	This bit is set when the fan3 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
1	FAN2_STS	R/W	--	This bit is set when the fan2 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
0	FAN1_STS	R/W	--	This bit is set when the fan1 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.

FAN Real Time Status Register — Index 92h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	FAN3_EXC	RO	--	This bit set to high mean that fan3 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.
1	FAN2_EXC	RO	--	This bit set to high mean that fan2 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.
0	FAN1_EXC	RO	--	This bit set to high mean that fan1 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.

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FAN FAULT# Enable Register — Index 93h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	FULL_WITH_T2_EN	R/W	0	Set one will enable FAN to force full speed when T2 over high limit.
5	FULL_WITH_T1_EN	R/W	0	Set one will enable FAN to force full speed when T1 over high limit.
4	FULL_WITH_T0_EN	R/W	0	Set one will enable FAN to force full speed when T0 (Local Temperature) over high limit.
3	Reserved	RO	0	Reserved
2	EN_FAN3_ HW_IRQ	R/W	0	When FAN3_EXC (CR92 bit2) is active and this bit is Enabled. The pin HW_IRQ # will be active and user can select HW_IRQ mode from CR02.
1	EN_FAN2_ HW_IRQ	R/W	0	When FAN2_EXC (CR92 bit1) is active and this bit is Enabled. The pin HW_IRQ # will be active and user can select HW_IRQ mode from CR02.
0	EN_FAN1_ HW_IRQ	R/W	0	When FAN1_EXC (CR92 bit0) is active and this bit is Enabled. The pin HW_IRQ # will be active and user can select HW_IRQ mode from CR02.

Fan Type Select Register -- Index 94h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved
5-4	FAN3_TYPE	R/W	1Sb	00: Output PWM mode (push pull) to control fans. 01: Use DAC mode application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Use DAC mode application circuit to control fan speed by fan's power terminal. **Bit 0 default value is trapping by pin FAN3_CTRL. If pull up 10K the bit0 default value is 0, else if without pull up resister bit0 default value will be 1(for DAC mode)**
3-2	FAN2_TYPE	R/W	1Sb	00: Output PWM mode (push pull) to control fans. 01: Use DAC mode application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Use DAC mode application circuit to control fan speed by fan's power terminal. **Bit 0 default value is trapping by pin FAN3_CTRL. If pull up 10K the bit0 default value is 0, else if without pull up resister bit0 default value will be 1(for DAC mode)**
1-0	FAN1_TYPE	R/W	1Sb	00: Output PWM mode (push pull) to control fans. 01: Use DAC mode application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Use DAC mode application circuit to control fan speed by fan's power terminal. **Bit 0 default value is trapping by pin FAN3_CTRL. If pull up 10K the bit0 default value is 0, else if without pull up resister bit0 default value will be 1(for DAC mode)**

"S" mean default by trapping.

Fan mode Select Register -- Index 96h

Bit	Name	R/W	Default	Description
7-6	Reserved	RO	0h	Reserved for fan 4

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5-4	FAN3_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that define in 0xC6-0xCE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** that defined in 0xC6-0xCE. 10: Manual mode fan control, user can write expect **RPM** count to 0xC2-0xC3, and F71858AD will auto control duty cycle (PWM fan type) or voltage (DAC mode type) to control fan speed. 11: Manual mode fan control, user can write expect Duty to 0xC3, and F71858A will auto control duty cycle (PWM fan type) or voltage (DAC mode type) to control fan speed.
3-2	FAN2_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that define in 0xB6-0xBE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** (voltage) that defined in 0xB6-0xBE. 10: Manual mode fan control, user can write expect **RPM** count to 0xB2-0xB3, and F71858AD will auto control duty cycle (PWM fan type) or voltage (DAC mode type) to control fan speed. 11: Manual mode fan control, user can write expect Duty to 0xB3, and F71858A will auto control duty cycle (PWM fan type) or voltage (DAC mode type) to control fan speed.
1-0	FAN1_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that define in 0xA6-0xAE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** that defined in 0xA6-0xAE. 10: Manual mode fan control, user can write expect **RPM** count to 0xA2-0xA3, and F71858AD will auto control duty cycle (PWM fan type) or voltage (DAC mode type) to control fan speed. 11: Manual mode fan control, user can write expect Duty to 0xA3, and F71858A will auto control duty cycle (PWM fan type) or voltage (DAC mode type) to control fan speed.

Auto Fan1 and Fan2 Boundary Hystersis Select Register -- Index 98h

Bit	Name	R/W	Default	Description
7-4	FAN2_HYS	R/W	4h	Boundary hysteresis. (0~15^{o}C) Segment will change when the temperature over the boundary temperature and below the (Boundary temperature– hysteresis).
3-0	FAN1_HYS	R/W	4h	Boundary hysteresis. (0~15^{o}C) Segment will change when the temperature over the boundary temperature and below the (Boundary temperature – hysteresis).

Auto Fan3 Boundary Hystersis Select Register -- Index 99h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved
3-0	FAN3_HYS	R/W	2h	Boundary hysteresis. (0~15^{o}C) Segment will change when the temperature over the boundary temperature and below the (Boundary temperature– hysteresis).

Fan1~Fan3 Duty Change Rate Select Register -- Index 9Bh (FAN_PROG_SEL = 0 or NEW_MODE_EN = 0)

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved

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5-4	FAN3_RATE_SEL	R/W	1h	Fan3 duty update rate: 00: 2.5Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
3-2	FAN2_RATE_SEL	R/W	1h	Fan2 duty update rate: 00: 2.5Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_RATE_SEL	R/W	1h	Fan1 duty update rate: 00: 2.5Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

Fan1~Fan3 Duty Change Rate Select Register -- Index 9Bh (FAN_PROG_SEL = 1 or NEW_MODE_EN = 0)

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved
5-4	FAN3_DN_RATE_SEL	R/W	1h	Fan3 duty update rate when duty is decreasing: 00: 2.5Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
3-2	FAN2_DN_RATE_SEL	R/W	1h	Fan2 duty update rate when duty is decreasing: 00: 2.5Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_DN_RATE_SEL	R/W	1h	Fan1 duty update rate when duty is decreasing: 00: 2.5Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

FAN1 and FAN2 START UP DUTY-CYCLE/VOLTAGE — Index 9Ch

Bit	Name	R/W	Default	Description
7-4	FAN2_MIN_DUTY	R/W	5h	When fan start, the FAN_CTRL2 will increase duty-cycle from 0 to this (value x 8) directly. And if fan speed is down, the FAN_CTRL 2 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).
3-0	FAN1_MIN_DUTY	R/W	5h	When fan start, the FAN_CTRL 1 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 1 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

FAN3 START UP DUTY-CYCLE/VOLTAGE — Index 9Dh

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved
3-0	FAN3_MIN_DUTY	R/W	5h	When fan start, the FAN_CTRL 3 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 3 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

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FAN POWER-ON LOADED DUTY-CYCLE/VOLTAGE — Index 9Eh

Bit	Name	R/W	Default	Description
7-0	PWRON_DEF_DUTY	R/W	66h	When Power-On, this duty will be directly loaded to FAN1~FAN3 for controlling fan. (Default duty is 40%)

Fan Fault Time Register -- Index 9Fh

Bit	Name	R/W	Default	Description
7	FAN_PROG_SEL	R/W	0	Select FAN_UP_RATE or FAN_DN_RATE to be programmed if "NEW_MODE_EN" in CR06 [7] is 1.
6-4	Reserved	--	--	Reserved
3-0	F_FAULT_TIME	R/W	Ah	This register determines the time of fan fault. The condition to cause fan fault event is: When PWM_Duty reaches FFh, if the fan speed count can't reach the fan expect count in time. The unit of this register is 1 second. The default value is 11 seconds. (Set to 0 , means 1 seconds. ; Set to 1, means 2 seconds. Set to 2, means 3 seconds. ….) Another condition to cause fan fault event is fan stop and the PWM duty is greater than the minimum duty programmed by the register index 97-98h.

Fan1 Index A0h- AFh

Address	Attribute	Default	Description
A0h	RO	8'h0f	FAN1 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A1h	RO	8'hff	FAN1 count reading (LSB).
A2h	R/W	8'h00	**RPM mode(CR96 bit0=0):** FAN1 expect speed count value (MSB), in auto fan mode (CR96 bit1➔0) this register is auto updated by hardware. **Duty mode(CR96 bit0=1):** This byte is reserved byte.
A3h	R/W	8'h01	**RPM mode(CR96 bit0=0):** FAN1 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. **Duty mode(CR96 bit0=1):** The Value programming in this byte is duty value. In auto fan mode(CR96 bit1➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
A4h	R/W	8'h03	FAN1 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A5h	R/W	8'hff	FAN1 full speed count reading (LSB).

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FAN1 BOUNDARY 1 TEMPERATURE – Index A6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TEMP1	R/W	46h ($70^{o}C$)	The 1st BOUNDARY temperature for FAN1. (Bit7 is sign bit of this boundary temperature. When NEW_MODE_EN is not set to 1, only BOUND1TEMP1[6:0] can be used as 1st BOUNDARY temperature) When FAN1 temperature is **exceed** this boundary, FAN1 expect value will load from segment **1** register (index AAh). When FAN1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load from segment **2** register (index ABh). When NEW_MODE_EN at CR06[7] is set to 1, F71858AD will support negative temperature for boundary temperatures. Bit 7 of boundary temperatures will be sign bit.

FAN1 BOUNDARY 2 TEMPERATURE – Index A7h

Bit	Name	R/W	Default	Description
7-0	BOUND2TEMP1	R/W	3C ($60^{o}C$)	The 2nd BOUNDARY temperature for FAN1. (Bit7 is sign bit of this boundary temperature. When NEW_MODE_EN is not set to 1, only BOUND2TEMP1[6:0] can be used as 2nd BOUNDARY temperature) When FAN1 temperature is **exceed** this boundary, FAN1 expect value will load from segment **2** register (index ABh). When FAN1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load from segment **3** register (index ACh). When NEW_MODE_EN at CR06[7] is set to 1, F71858AD will support negative temperature for boundary temperatures. Bit 7 of boundary temperatures will be sign bit.

FAN1 BOUNDARY 3 TEMPERATURE – Index A8h

Bit	Name	R/W	Default	Description
7-0	BOUND3TEMP1	R/W	32h ($50^{o}C$)	The 3rdBOUNDARY temperature for FAN1. (Bit7 is sign bit of this boundary temperature. When NEW_MODE_EN is not set to 1, only BOUND3TEMP1[6:0] can be used as 3rd BOUNDARY temperature) When FAN1 temperature is **exceed** this boundary, FAN1 expect value will load from segment **3** register (index ACh). When FAN1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load from segment **4** register (index ADh). When NEW_MODE_EN at CR06[7] is set to 1, F71858AD will support negative temperature for boundary temperatures. Bit 7 of boundary temperatures will be sign bit.

FAN1 BOUNDARY 4 TEMPERATURE – Index A9h

Bit	Name	R/W	Default	Description
7-0	BOUND4TEMP1	R/W	28h ($40^{o}C$)	The 4th BOUNDARY temperature for FAN1. (Bit7 is sign bit of this boundary temperature. When NEW_MODE_EN is not set to 1, only BOUND4TEMP1[6:0] can be used as 4th BOUNDARY temperature) When FAN1 temperature is **exceed** this boundary, FAN1 expect value will load from segment **4** register (index ADh). When FAN1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load from segment **5** register (index AEh). When NEW_MODE_EN at CR06[7] is set to 1, F71858AD will support negative temperature for boundary temperatures. Bit 7 of boundary temperatures will be sign bit.

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FAN1 SEGMENT 1 SPEED COUNT – Index AAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED1	R/W	FFh (100%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: $Expect\ speed = \left(\frac{32}{32+value}\right) \times Full\ speee$ 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 2 SPEED COUNT – Index ABh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED1	R/W	D9h (85%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 3 SPEED COUNT – Index ACh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED1	R/W	A6h (65%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 4 SPEED COUNT – Index ADh

Bit	Name	R/W	Default	Description
7-0	SEC4SPEED1	R/W	80h (50%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 5 SPEED COUNT – Index AEh

Bit	Name	R/W	Default	Description
7-0	SEC5SPEED1	R/W	66h (40%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

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FAN1 Temperature Mapping Select – Index AFh

Bit	Name	R/W	Default	Description
7	FAN1_LD_BEFORE_EN	R/W	0	Set 1 that fan speed will keep current temp. status before system re-boot up.
6	FAN1_NO_STOP	R/W	0	Set 1 that FAN1 will not stop but keep at FAN1_MIN_DUTY x 4.
5	FAN1_UP_T_EN	R/W	0	Set 1 to force FAN1 to the highest speed if any temperature over its high limit.
4	FAN1_INTERPOLATION_EN	R/W	0	Set 1 will enable the interpolation of the fan expect table. (Auto Linear Mode)
3	FAN1_JUMP_HIGH_EN	R/W	1	Set 1 that FAN1 speed will jump to FAN1 SEGMENT 1 SPEED when temperature over T1 Boundary 1. Set 0 that FAN1 speed will raise up to FAN1 SEGMENT 1 SPEED by slop value(CR9B) when temperature over T1 Boundary 1.
2	FAN1_JUMP_LOW_EN	R/W	1	Set 1 that FAN1 speed will jump to FAN1 SEGMENT 2 SPEED when temperature under FAN1 Boundary Hystersis. Set 0 that FAN1 speed will decrease to FAN1 SEGMENT 2 SPEED by slop value(CR9B) when temperature under FAN1 Boundary Hystersis.
1-0	FAN1_TEMP_SEL	R/W	1	0: fan1 follows local temperature 0. 1: fan1 follows temperature 1. 2: fan1 follows temperature 2. 3: fan1 follows PECI or TSI temperature. (when NEW_MODE_EN at CR06[7] is set to 1)

Fan2 Index B0h- BFh

Address	Attribute	Default	Description
B0h	RO	8'h0f	FAN2 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B1h	RO	8'hff	FAN2 count reading (LSB).
B2h	R/W	8'h00	**RPM mode(CR96 bit2=0):** FAN2 expect speed count value (MSB), in auto fan mode (CR96 bit3➔0) this register is auto updated by hardware. **Duty mode(CR96 bit2=1):** This byte is reserved byte.
B3h	R/W	8'h01	**RPM mode(CR96 bit2=0):** FAN2 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. **Duty mode(CR96 bit2=1):** The Value programming in this byte is duty value. In auto fan mode (CR96 bit3➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
B4h	R/W	8'h03	FAN2 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B5h	R/W	8'hff	FAN2 full speed count reading (LSB).

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FAN2 BOUNDARY 1 TEMPERATURE – Index B6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TEMP2	R/W	46h ($70^{o}C$)	The 1st BOUNDARY temperature for FAN2. (Bit7 is sign bit of this boundary temperature. When NEW_MODE_EN is not set to 1, only BOUND1TEMP2[6:0] can be used as 1st BOUNDARY temperature) When FAN2 temperature is **exceed** this boundary, FAN2 expect value will load from segment **1** register (index BAh). When FAN2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load from segment **2** register (index BBh). When NEW_MODE_EN at CR06[7] is set to 1, F71858AD will support negative temperature for boundary temperatures. Bit 7 of boundary temperatures will be sign bit.

FAN2 BOUNDARY 2 TEMPERATURE – Index B7h

Bit	Name	R/W	Default	Description
7-0	BOUND2TEMP2	R/W	3C ($60^{o}C$)	The 2ndBOUNDARY temperature for FAN2. (Bit7 is sign bit of this boundary temperature. When NEW_MODE_EN is not set to 1, only BOUND2TEMP2[6:0] can be used as 2nd BOUNDARY temperature) When FAN2 temperature is **exceed** this boundary, FAN2 expect value will load from segment **2** register (index BBh). When FAN2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load from segment **3** register (index BCh). When NEW_MODE_EN at CR06[7] is set to 1, F71858AD will support negative temperature for boundary temperatures. Bit 7 of boundary temperatures will be sign bit.

FAN2 BOUNDARY 3 TEMPERATURE – Index B8h

Bit	Name	R/W	Default	Description
7-0	BOUND3TEMP2	R/W	32h ($50^{o}C$)	The 3rd BOUNDARY temperature for FAN2. (Bit7 is sign bit of this boundary temperature. When NEW_MODE_EN is not set to 1, only BOUND3TEMP2[6:0] can be used as 3rd BOUNDARY temperature) When FAN2 temperature is **exceed** this boundary, FAN2 expect value will load from segment **3** register (index BCh). When FAN2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load from segment **4** register (index BDh). When NEW_MODE_EN at CR06[7] is set to 1, F71858AD will support negative temperature for boundary temperatures. Bit 7 of boundary temperatures will be sign bit.

FAN2 BOUNDARY 4 TEMPERATURE – Index B9h

Bit	Name	R/W	Default	Description
7-0	BOUND4TEMP2	R/W	28h ($40^{o}C$)	The 4th BOUNDARY temperature for FAN2. (Bit7 is sign bit of this boundary temperature. When NEW_MODE_EN is not set to 1, only BOUND4TEMP2[6:0] can be used as 4th BOUNDARY temperature) When FAN2 temperature is **exceed** this boundary, FAN2 expect value will load from segment **4** register (index BDh). When FAN2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load from segment **5** register (index BEh). When NEW_MODE_EN at CR06[7] is set to 1, F71858AD will support negative temperature for boundary temperatures. Bit 7 of boundary temperatures will be sign bit.

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FAN2 SEGMENT 1 SPEED COUNT – Index BAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED2	R/W	FFh (100%)	The meaning of this register is depending on the FAN_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. $\text{Expect speed} = \left(\frac{32}{32 + \text{value}}\right) \times \text{Full speeed}$ 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 2 SPEED COUNT – Index BBh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED2	R/W	D9h (85%)	The meaning of this register is depending on the FAN_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 3 SPEED COUNT – Index BCh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED2	R/W	A6h (65%)	The meaning of this register is depending on the FAN_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 4 SPEED COUNT – Index BDh

Bit	Name	R/W	Default	Description
7-0	SEC4SPEED2	R/W	80h (50%)	The meaning of this register is depending on the FAN_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 5 SPEED COUNT – Index BEh

Bit	Name	R/W	Default	Description
7-0	SEC5SPEED2	R/W	66h (40%)	The meaning of this register is depending on the FAN_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

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FAN2 Temperature Mapping Select – Index BFh

Bit	Name	R/W	Default	Description
7	FAN2_LD_BEFORE_EN	R/W	0	Set 1 that fan speed will keep current temp. status before system re-boot up.
6	FAN2_NO_STOP	R/W	0	Set 1 that FAN2 will not stop but keep at FAN2_MIN_DUTY x 4.
5	FAN2_UP_T_EN	R/W	0	Set 1 to force FAN2 to the highest speed if any temperature over its high limit.
4	FAN2_INTERPOLATION_EN	R/W	0	Set 1 will enable the interpolation of the fan expect table. (Auto Linear Mode)
3	FAN2_JUMP_HIGH_EN	R/W	1	Set 1 that FAN2 speed will jump to Fan2 SEGMENT 1 SPEED when temperature over T2 Boundary 1. Set 0 that FAN2 speed will raise up to Fan2 SEGMENT 1 SPEED by slope value (CR9B) when temperature over T2 Boundary 1.
2	FAN2_JUMP_LOW_EN	R/W	1	Set 1 that FAN2 speed will jump to Fan2 SEGMENT 2 SPEED when temperature under FAN2 Boundary Hystersis. Set 0 that FAN2 speed will decrease to Fan2 SEGMENT 2 SPEED by slope value (CR9B) when temperature under FAN2 Boundary Hystersis.
1-0	FAN2_TEMP_SEL	R/W	2	0: fan2 follows local temperature 0. 1: fan2 follows temperature 1. 2: fan2 follows temperature 2. 3: fan2 follows PECI or TSI temperature. (when NEW_MODE_EN at CR06[7] is set to 1)

Fan3 Index C0h- CFh

Address	Attribute	Default	Description
C0h	RO	8'h0F	FAN3 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C1h	RO	8'hff	FAN3 count reading (LSB).
C2h	R/W	8'h00	**RPM mode(CR96 bit4=0):** FAN3 expect speed count value (MSB), in auto fan mode (CR96 bit5➔0) this register is auto updated by hardware. **Duty mode(CR96 bit4=1):** This byte is reserved byte.
C3h	R/W	8'h01	**RPM mode(CR96 bit4=0):** FAN3 expect speed count value (LSB) or expect PWM duty , in auto fan mode this register is auto updated by hardware and read only. **Duty mode(CR96 bit4=1):** The Value programming in this byte is duty value. In auto fan mode (CR96 bit5➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
C4h	R/W	8'h03	FAN3 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C5h	R/W	8'hff	FAN3 full speed count reading (LSB).

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FAN3 BOUNDARY 1 TEMPERATURE – Index C6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TEMP3	R/W	46h ($70^{o}C$)	The 1st BOUNDARY temperature for FAN3. (Bit7 is sign bit of this boundary temperature. When NEW_MODE_EN is not set to 1, only BOUND1TEMP3[6:0] can be used as 1st BOUNDARY temperature) When FAN3 temperature is **exceed** this boundary, FAN3 expect value will load from segment **1** register (index CAh). When FAN3 temperature is **below** this boundary – hysteresis, FAN3 expect value will load from segment **2** register (index CBh). When NEW_MODE_EN at CR06[7] is set to 1, F71858AD will support negative temperature for boundary temperatures. Bit 7 of boundary temperatures will be sign bit.

FAN3 BOUNDARY 2 TEMPERATURE – Index C7h

Bit	Name	R/W	Default	Description
7-0	BOUND2TEMP3	R/W	3C ($60^{o}C$)	The 2nd BOUNDARY temperature forFAN3. (Bit7 is sign bit of this boundary temperature. When NEW_MODE_EN is not set to 1, only BOUND2TEMP3[6:0] can be used as 2nd BOUNDARY temperature) When FAN3 temperature is **exceed** this boundary, FAN3 expect value will load from segment **2** register (index CBh). When FAN3 temperature is **below** this boundary – hysteresis, FAN3 expect value will load from segment **3** register (index CCh). When NEW_MODE_EN at CR06[7] is set to 1, F71858AD will support negative temperature for boundary temperatures. Bit 7 of boundary temperatures will be sign bit.

FAN3 BOUNDARY 3 TEMPERATURE – Index C8h

Bit	Name	R/W	Default	Description
7-0	BOUND3TEMP3	R/W	32h ($50^{o}C$)	The 3rd BOUNDARY temperature for FAN3. (Bit7 is sign bit of this boundary temperature. When NEW_MODE_EN is not set to 1, only BOUND3TEMP3[6:0] can be used as 3rd BOUNDARY temperature) When FAN3 temperature is **exceed** this boundary, FAN3 expect value will load from segment **3** register (index CCh). When FAN3 temperature is **below** this boundary – hysteresis, FAN3 expect value will load from segment **4** register (index CDh). When NEW_MODE_EN at CR06[7] is set to 1, F71858AD will support negative temperature for boundary temperatures. Bit 7 of boundary temperatures will be sign bit.

FAN3 BOUNDARY 4 TEMPERATURE – Index C9h

Bit	Name	R/W	Default	Description
7-0	BOUND4TEMP3	R/W	28h ($40^{o}C$)	The 4th BOUNDARY temperature for FAN3. (Bit7 is sign bit of this boundary temperature. When NEW_MODE_EN is not set to 1, only BOUND4TEMP3[6:0] can be used as 4th BOUNDARY temperature) When FAN3 temperature is **exceed** this boundary, FAN3 expect value will load from segment **4** register (index CDh). When FAN3 temperature is **below** this boundary – hysteresis, FAN3 expect value will load from segment **5** register (index CEh). When NEW_MODE_EN at CR06[7] is set to 1, F71858AD will support negative temperature for boundary temperatures. Bit 7 of boundary temperatures will be sign bit.

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FAN3 SEGMENT 1 SPEED COUNT – Index CAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED3	R/W	FFh (100%)	The meaning of this register is depending on the FAN_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. $\text{Expect speed} = \left(\frac{32}{32 + \text{value}}\right) \times \text{Full speeed}$ 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 2 SPEED COUNT – Index CBh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED3	R/W	D9h (85%)	The meaning of this register is depending on the FAN_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 3 SPEED COUNT – Index CCh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED3	R/W	A6h (65%)	The meaning of this register is depending on the FAN_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 4 SPEED COUNT – Index CDh

Bit	Name	R/W	Default	Description
7-0	SEC4SPEED3	R/W	80h (50%)	The meaning of this register is depending on the FAN_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 5 SPEED COUNT – Index CEh

Bit	Name	R/W	Default	Description
7-0	SEC5SPEED3	R/W	66h (40%)	The meaning of this register is depending on the FAN_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

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FAN3 Temperature Mapping Select – Index CFh

Bit	Name	R/W	Default	Description
7	FAN3_LD_BEFORE_EN	R/W	0	Set 1 that fan speed will keep current temp. status before system re-boot up.
6	FAN3_NO_STOP	R/W	0	Set 1 that FAN3 will not stop but keep at FAN3_MIN_DUTY x 4.
5	FAN3_UP_T_EN	R/W	0	Set 1 to force FAN3 to the highest speed if any temperature over its high limit.
4	FAN3_INTERPOLATION_EN	R/W	0	Set 1 will enable the interpolation of the fan expect table. (Auto Linear Mode)
3	FAN3_JUMP_HIGH_EN	R/W	1	Set 1 that FAN3 speed will jump to Fan3 SEGMENT 1 SPEED when temperature over T0 Boundary 1. Set 0 that FAN3 speed will raise up to Fan3 SEGMENT 1 SPEED by slop value (CR9B) when temperature over T0 Boundary 1.
2	FAN3_JUMP_LOW_EN	R/W	1	Set 1 that FAN3 speed will jump to Fan3 SEGMENT 2 SPEED when temperature under FAN3 Boundary Hystersis. Set 0 that FAN3 speed will decrease to Fan3 SEGMENT 2 SPEED by slop value (CR9B) when temperature under FAN3 Boundary Hystersis.
1-0	FAN3_TEMP_SEL	R/W	0	0: fan3 follows local temperature 0. 1: fan3 follows temperature 1. 2: fan3 follows temperature 2. 3: fan3 follows PECI or TSI temperature. (when NEW_MODE_EN at CR06[7] is set to 1)

Fan4 Index D0h- D1h

Address	Attribute	Default	Description
D0h	RO	8'h0F	FAN4 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
D1h	RO	8'hff	FAN4 count reading (LSB).

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7.5 GPIO Registers

7.5.1 Logic Device Number Register

Logic Device Number Register — Index 07H

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Select KBC device configuration registers. 01h: Select PME & ACPI device configuration registers. 02h: Select hardware monitor device configuration registers. 03h: Select GPIO device configuration registers. 04h: Select WDT device configuration registers.

7.5.2 GPIO Configuration Registers

GPIRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELGPIRQ	R/W	0h	Select the IRQ channel for GPIO interrupt.

GPIO0 Output Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7	GPIO07_OE	R/W	0	0: GPIO07 is in input mode. 1: GPIO07 is in output mode.
6	GPIO06_OE	R/W	0	0: GPIO06 is in input mode. 1: GPIO06 is in output mode.
5	GPIO05_OE	R/W	0	0: GPIO05 is in input mode. 1: GPIO05 is in output mode.
4	GPIO04_OE	R/W	0	0: GPIO04 is in input mode. 1: GPIO04 is in output mode.
3	GPIO03_OE	R/W	0	0: GPIO03 is in input mode. 1: GPIO03 is in output mode.
2	GPIO02_OE	R/W	0	0: GPIO02 is in input mode. 1: GPIO02 is in output mode. This bit is reset by LRESET#.
1	GPIO01_OE	R/W	0	0: GPIO01 is in input mode. 1: GPIO01 is in output mode. This bit is reset by LRESET#.
0	GPIO00_OE	R/W	0	0: GPIO00 is in input mode. 1: GPIO00 is in output mode. This bit is reset by LRESET#.

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GPIO0 Output Data Register — Index F1h

Bit	Name	R/W	Default	Description
7	GPIO07_VAL	R/W	1	0: GPIO07 outputs 0 when in output mode. 1: GPIO07 outputs1 when in output mode.
6	GPIO06_VAL	R/W	1	0: GPIO06 outputs 0 when in output mode. 1: GPIO06 outputs1 when in output mode.
5	GPIO05_VAL	R/W	1	0: GPIO05 outputs 0 when in output mode. 1: GPIO05 outputs 1 when in output mode.
4	GPIO04_VAL	R/W	1	0: GPIO04 outputs 0 when in output mode. 1: GPIO04 outputs 1 when in output mode.
3	GPIO03_VAL	R/W	1	0: GPIO03 outputs 0 when in output mode. 1: GPIO03 outputs 1 when in output mode.
2	GPIO02_VAL	R/W	1	0: GPIO02 outputs 0 when in output mode. 1: GPIO02 outputs 1 when in output mode. This bit is reset by LRESET#.
1	GPIO01_VAL	R/W	1	0: GPIO01 outputs 0 when in output mode. 1: GPIO01 outputs 1 when in output mode. This bit is reset by LRESET#.
0	GPIO00_VAL	R/W	1	0: GPIO00 outputs 0 when in output mode. 1: GPIO00 outputs 1 when in output mode. This bit is reset by LRESET#.

GPIO0 Pin Status Register — Index F2h

Bit	Name	R/W	Default	Description
7	GPIO07_IN	R	-	The pin status of LED2/GPIO07.
6	GPIO06_IN	R	-	The pin status of LED1/GPIO06.
5	GPIO05_IN	R	-	The pin status of PCIRST5#/GPIO05.
4	GPIO04_IN	R	-	The pin status of PCIRST4#/GPIO04.
3	GPIO03_IN	R	-	The pin status of RSTIN#/GPIO03.
2	GPIO02_IN	R	-	The pin status of FANIN4/SST/AMDTSI_CLK/GPIO02.
1	GPIO01_IN	R	-	The pin status of FANIN3/GPIO01.
0	GPIO00_IN	R	-	The pin status of PECI/AMDTSI_DATA/GPIO00.

GPIO0 Drive Enable Register — Index F3h

Bit	Name	R/W	Default	Description
7	GPIO07_DRV_EN	R/W	0	0: GPIO07 is open drain in output mode. 1: GPIO07 is push pull in output mode.
6	GPIO06_DRV_EN	R/W	0	0: GPIO06 is open drain in output mode. 1: GPIO06 is push pull in output mode.
5	GPIO05_DRV_EN	R/W	0	0: GPIO05 is open drain in output mode. 1: GPIO05 is push pull in output mode.
4	GPIO04_DRV_EN	R/W	0	0: GPIO04 is open drain in output mode. 1: GPIO04 is push pull in output mode.
3	GPIO03_DRV_EN	R/W	0	0: GPIO03 is open drain in output mode. 1: GPIO03 is push pull in output mode.

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2	GPIO02_DRV_EN	R/W	0	0: GPIO02 is open drain in output mode. 1: GPIO02 is push pull in output mode. This bit is reset by LRESET#.
1	GPIO01_DRV_EN	R/W	0	0: GPIO01 is open drain in output mode. 1: GPIO01 is push pull in output mode. This bit is reset by LRESET#.
0	GPIO00_DRV_EN	R/W	0	0: GPIO00 is open drain in output mode. 1: GPIO00 is push pull in output mode. This bit is reset by LRESET#.

GPIO0 PME Enable Register — Index F4h

Bit	Name	R/W	Default	Description
7	GPIO07_PME_EN	R/W	0	0: Disable GPIO07 PME. 1: Enable GPIO07 PME when GPIO07_PME_ST is set.
6	GPIO06_PME_EN	R/W	0	0: Disable GPIO06 PME. 1: Enable GPIO06 PME when GPIO06_PME_ST is set.
5	GPIO05_PME_EN	R/W	0	0: Disable GPIO05 PME. 1: Enable GPIO05 PME when GPIO05_PME_ST is set.
4	GPIO04_PME_EN	R/W	0	0: Disable GPIO04 PME. 1: Enable GPIO04 PME when GPIO04_PME_ST is set.
3	GPIO03_PME_EN	R/W	0	0: Disable GPIO03 PME. 1: Enable GPIO03 PME when GPIO03_PME_ST is set.
2	GPIO02_PME_EN	R/W	0	0: Disable GPIO02 PME. 1: Enable GPIO02 PME when GPIO02_PME_ST is set. This bit is reset by LRESET#.
1	GPIO01_PME_EN	R/W	0	0: Disable GPIO01 PME. 1: Enable GPIO01 PME when GPIO01_PME_ST is set. This bit is reset by LRESET#.
0	GPIO00_PME_EN	R/W	0	0: Disable GPIO00 PME. 1: Enable GPIO00 PME when GPIO00_PME_ST is set. This bit is reset by LRESET#.

GPIO0 PME Detect Select Register — Index F5h

Bit	Name	R/W	Default	Description
7	GPIO07_DET_SEL	R/W	0	0: Rising edge will trigger a PME event. 1: Falling edge will trigger a PME event.
6	GPIO06_DET_SEL	R/W	0	0: Rising edge will trigger a PME event. 1: Falling edge will trigger a PME event.
5	GPIO05_DET_SEL	R/W	0	0: Rising edge will trigger a PME event. 1: Falling edge will trigger a PME event.
4	GPIO04_DET_SEL	R/W	0	0: Rising edge will trigger a PME event. 1: Falling edge will trigger a PME event.
3	GPIO03_DET_SEL	R/W	0	0: Rising edge will trigger a PME event. 1: Falling edge will trigger a PME event.
2	GPIO02_DET_SEL	R/W	0	0: Rising edge will trigger a PME event. 1: Falling edge will trigger a PME event. This bit is reset by LRESET#.

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1	GPIO01_DET_SEL	R/W	0	0: Rising edge will trigger a PME event. 1: Falling edge will trigger a PME event. This bit is reset by LRESET#.
0	GPIO00_DET_SEL	R/W	0	0: Rising edge will trigger a PME event. 1: Falling edge will trigger a PME event. This bit is reset by LRESET#.

GPIO0 PME Status Register — Index F6h

Bit	Name	R/W	Default	Description
7	GPIO07_PME_ST	R/WC	0	0: No GPIO07 PME event. 1: A GPIO07 PME event is trigger, write "1" to clear.
6	GPIO06_PME_ST	R/WC	0	0: No GPIO07 PME event. 1: A GPIO07 PME event is trigger, write "1" to clear.
5	GPIO05_PME_ST	R/WC	0	0: No GPIO07 PME event. 1: A GPIO07 PME event is trigger, write "1" to clear.
4	GPIO04_PME_ST	R/WC	0	0: No GPIO07 PME event. 1: A GPIO07 PME event is trigger, write "1" to clear.
3	GPIO03_PME_ST	R/WC	0	0: No GPIO07 PME event. 1: A GPIO07 PME event is trigger, write "1" to clear.
2	GPIO02_PME_ST	R/WC	0	0: No GPIO07 PME event. 1: A GPIO07 PME event is trigger, write "1" to clear. This bit is reset by LRESET#.
1	GPIO01_PME_ST	R/WC	0	0: No GPIO07 PME event. 1: A GPIO07 PME event is trigger, write "1" to clear. This bit is reset by LRESET#.
0	GPIO00_PME_ST	R/WC	0	0: No GPIO07 PME event. 1: A GPIO07 PME event is trigger, write "1" to clear. This bit is reset by LRESET#.

GPIO1 Output Enable Register — Index E0h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3	GPIO13_OE	R/W	0	0: GPIO13 is in input mode. 1: GPIO13 is in output mode.
2	GPIO12_OE	R/W	0	0: GPIO12 is in input mode. 1: GPIO12 is in output mode.
1	GPIO11_OE	R/W	0	0: GPIO11 is in input mode. 1: GPIO11 is in output mode.
0	GPIO10_OE	R/W	0	0: GPIO10 is in input mode. 1: GPIO10 is in output mode.

GPIO1 Output Data Register — Index E1h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3	GPIO13_VAL	R/W	1	0: GPIO13 outputs 0 when in output mode. 1: GPIO13 outputs 1 when in output mode.

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2	GPIO12_VAL	R/W	1	0: GPIO12 outputs 0 when in output mode. 1: GPIO12 outputs 1 when in output mode.
1	GPIO11_VAL	R/W	1	0: GPIO11 outputs 0 when in output mode. 1: GPIO11 outputs 1 when in output mode.
0	GPIO10_VAL	R/W	1	0: GPIO10 outputs 0 when in output mode. 1: GPIO10 outputs 1 when in output mode.

GPIO1 Pin Status Register — Index E2h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3	GPIO13_IN	R	-	The pin status of MDATA/GPIO13.
2	GPIO12_IN	R	-	The pin status of MCLK/GPIO12.
1	GPIO11_IN	R	-	The pin status of KDATA/GPIO11.
0	GPIO10_IN	R	-	The pin status of KCLK/GPIO10.

GPIO1 Drive Enable Register — Index E3h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3	GPIO13_DRV_EN	R/W	0	0: GPIO13 is open drain in output mode. 1: GPIO13 is push pull in output mode.
2	GPIO12_DRV_EN	R/W	0	0: GPIO12 is open drain in output mode. 1: GPIO12 is push pull in output mode.
1	GPIO11_DRV_EN	R/W	0	0: GPIO11 is open drain in output mode. 1: GPIO11 is push pull in output mode.
0	GPIO10_DRV_EN	R/W	0	0: GPIO10 is open drain in output mode. 1: GPIO10 is push pull in output mode.

GPIO1 PME Enable Register — Index E4h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3	GPIO13_PME_EN	R/W	0	0: Disable GPIO13 PME. 1: Enable GPIO13 PME when GPIO13_PME_ST is set.
2	GPIO12_PME_EN	R/W	0	0: Disable GPIO12 PME. 1: Enable GPIO12 PME when GPIO12_PME_ST is set.
1	GPIO11_PME_EN	R/W	0	0: Disable GPIO11 PME. 1: Enable GPIO11 PME when GPIO11_PME_ST is set.
0	GPIO10_PME_EN	R/W	0	0: Disable GPIO10 PME. 1: Enable GPIO10 PME when GPIO10_PME_ST is set.

GPIO1 PME Detect Select Register — Index E5h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3	GPIO13_DET_SEL	R/W	0	0: Rising edge will trigger a PME event. 1: Falling edge will trigger a PME event.

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2	GPIO12_DET_SEL	R/W	0	0: Rising edge will trigger a PME event. 1: Falling edge will trigger a PME event.
1	GPIO11_DET_SEL	R/W	0	0: Rising edge will trigger a PME event. 1: Falling edge will trigger a PME event.
0	GPIO10_DET_SEL	R/W	0	0: Rising edge will trigger a PME event. 1: Falling edge will trigger a PME event.

GPIO1 PME Status Register — Index E6h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3	GPIO13_PME_ST	R/WC	0	0: No GPIO17 PME event. 1: A GPIO17 PME event is trigger, write “1” to clear.
2	GPIO12_PME_ST	R/WC	0	0: No GPIO17 PME event. 1: A GPIO17 PME event is trigger, write “1” to clear.
1	GPIO11_PME_ST	R/WC	0	0: No GPIO17 PME event. 1: A GPIO17 PME event is trigger, write “1” to clear.
0	GPIO10_PME_ST	R/WC	0	0: No GPIO17 PME event. 1: A GPIO17 PME event is trigger, write “1” to clear.

7.6 WDT Registers

7.6.1 Logic Device Number Register

Logic Device Number Register — Index 07H

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Select KBC device configuration registers. 01h: Select PME & ACPI device configuration registers. 02h: Select hardware monitor device configuration registers. 03h: Select GPIO device configuration registers. 04h: Select WDT device configuration registers.

7.6.2 Watchdog Configuration Registers

WDT Device Base Address Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	0	Reserved
0	WDT_EN	R/W	0	0: disable WDT base address. 1: enable WDT base address.

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Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of WDT base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	00h	The LSB of WDT base address.

Watchdog Control Configuration Register 1 — offset + 05h

Bit	Name	R/W	Default	Description
7	Reserved	R	0	Reserved
6	WDTMOUT_STS	R/W	0	If watchdog timeout event occurs, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	R/W	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	0	Select output mode (0: level, 1: pulse) of RSTOUT# by setting this bit.
3	WD_UNIT	R/W	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	0	Select output polarity of WDTRST# (1: high active, 0: low active) by setting this bit.
1-0	WD_PSWIDTH	R/W	0	Select output pulse width of WDTRST# 00: 1 ms 01: 25 ms 10: 125 ms 11: 5 sec

Watchdog Timer Configuration Register 2 — offset + 06h

Bit	Name	R/W	Default	Description
7-0	WD_TIME	R/W	0	Time of watchdog timer

Watchdog PME Enable Configuration Register 2 — offset + 07h

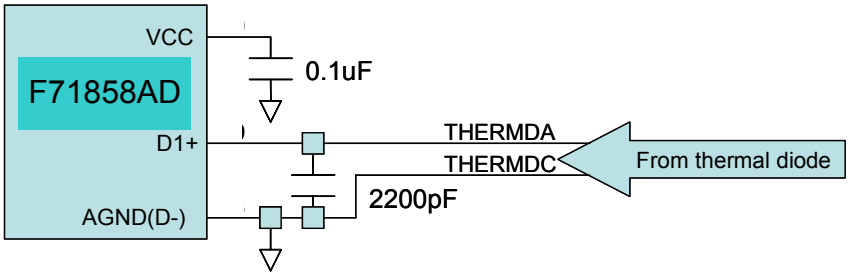
Bit	Name	R/W	Default	Description
7	WDT_PME	R	--	The PME Real Time Status. This bit will set when WDT_PME_EN is set and the watchdog timer is 1 unit before time out (or time out).
6	WDT_PME_EN	R/W	0	0: Disable Watchdog PME. 1: enable Watchdog PME.
5	WDT_PME_ST	R/WC	-	0: No PME event is trigger. 1: A PME event is trigger, write “1” to clear.
4	WDOUT_EN	R/W	0	0: disable Watchdog time out output via PWOK. 1: enable Watchdog time out output via PWOK.
3-0	Reserved	--	--	Reserved.

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8. PCB Layout Guide

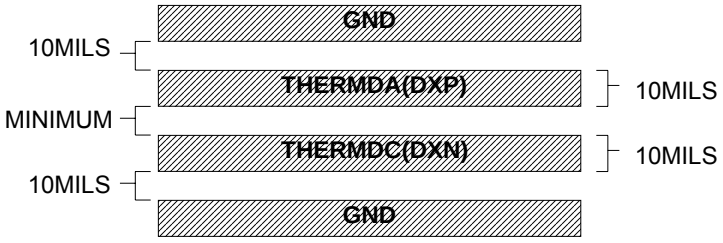
F71858AD adopts **Current Mode** measure method to detect the temperature. This method will not be affected by the different process of CPU via using current mode technology. This technology measures mini-voltage from the remote sensor so a good PCB layout must be needed for noise minimizing. The noises often come from circuit trace which is a track from remote sensor (CPU side) to detect circuit input (F71858AD side). The signal on this track will be inducted mini-noises when it passes through a high electromagnetic area. Those effects will result in the mini-noises and show in the detected side. It will be reported a wrong data which you want to measure. Please pay attention and follow up the check list below in order to get an actual and real temperature inside the chip.

1. The D1+/D2+ and AGND (D-) tracks **Must Not** pass through/by PWM POWER-MOS. Keep as far as possible from POWER MOS.
2. Place a 0.1μF bypass capacitor close to the V_{CC} pin. Place an external 2200pF input filter capacitors across D+, D- and close to the F71858AD. Near the pin AGND (D-) **Must Be** placed a through hole into the GND Plane before connect to the external 2200pF capacitor.



3. Place the F71858AD as close as practical to the remote sensor diode. In noisy environments, such as a computer main-board, the distance can be 4 to 8 inches. (typ). This length can be increased if the worst noise sources are avoided. Noise sources generally include clock generators, CRTs, memory buses and PCI/ISA bus etc.
4. Separated route the D1+, D2+ with AGND (D-) tracks close together and in parallel after adding external 2200pF capacitor. For more reliable, it had better with grounded guard tracks on each side. Provide a ground plane under the tracks if possible. Do not route D+ & D- lines next to the deflection coil of the CRT. And also don't route the trace across fast digital signals which can easily induce bigger error.

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5. Use wide tracks to minimize inductance and reduce noise pickup. 10 mil track minimum width and spacing is recommended.
6. Try to minimize the number of component/solder joints, called through hole, which can cause thermocouple effects. Where through holes are used, make sure that they are in both the D+ and D- path and at the same temperature. Thermocouple effects should not be a major problem as 1℃ corresponds to about 200μV. It means that a copper-solder thermocouple exhibits 3μV/℃, and takes about 200μV of the voltage error at D+ & D- to cause a 1℃ measurement error. Adding a few thermocouples causes a negligible error.
7. If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. It will work up to around 6 to 12 feet.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance will affect the measurement accuracy. When using long cables, the filter capacitor should be reduced or removed. Cable resistance can also induce errors. For example: 1 Ω series resistance introduces about 0.5℃ error.

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9. Electrical Characteristics

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.0	V
Input Voltage	-0.5 to VCC+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

9.2 DC Characteristics

(Ta = 0° C to 70° C, VCC = 3.3V ± 10% , VSS = 0V)

PARAMETER	RATING	
Operating Voltage	3.0 to 3.6	VCC/VSB
Operating Voltage	2.4 to 3.6	VBAT
Standby Current	500uA (Typ.)	VSB

9.3 DC Characteristics Continued

(Ta = 0° C to 70° C, VCC = 3.3V ± 10%, VSS = 0V)

PARAMETER	SYM.	MIN	TYP	MAX.	UNIT	CONDITIONS
I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability(3.3V)						
Input Low Voltage	VIL	-0.5		0.8	V	
Input High Voltage	VIH	2.0		VCC+ 0.3	V	
Output Low Current	IOL		12		mA	0.4V
Output High Current	IOH		12		mA	2.4V
Input High Leakage	ILIH	-1		1	μA	
Input Low Leakage	ILIL	-1		1	μA	
$I/OOD_{16st,5V}$ - TTL level bi-directional pin with 16 mA source-sink capability(3.3V), 5 tolerance						
Input Low Voltage	VIL	-0.5		0.8	V	
Input High Voltage	VIH	2.0		VCC+ 0.3	V	
Output Low Current	IOL		16		mA	0.4V
Output High Current	IOH		16		mA	2.4V
Input High Leakage	ILIH	-1		1	μA	
Input Low Leakage	ILIL	-1		1	μA	
$I/OOD_{12st,5v-}$ TTL level bi-directional pin with 12 mA source-sink capability(3.3V), 5 tolerance						
Input Low Voltage	VIL	-0.5		0.8	V	
Input High Voltage	VIH	2.0		VCC+ 0.3	V	

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Output Low Current	IOL		12		mA	0.4V
Output High Current	IOH		12		mA	2.4V
Input High Leakage	ILIH	-1		1	μA	
Input Low Leakage	ILIL	-1		1	μA	
OD_{12} – Open-drain output pin with12mA source-sink capability(3.3V)						
Output Low Current	IOL		12		mA	0.4V
$OD_{12,5v}$ – Open-drain output pin with12mA source-sink capability(3.3V), 5 tolerance						
Output Low Current	IOL		12		mA	0.4V
$OD_{16,5v}$ – Open-drain output pin with16mA source capability(3.3V), 5v tolerance						
Output Low Current	IOL		16		mA	0.4V
$OD_{16,u10k}$ – Open-drain output pin with16mA source capability(3.3V), 10k pull high to 3.3v						
Output Low Current	IOL		16		mA	0.4V
O_{16} – Output pin with16mA source-sink capability(3.3V)						
Output Low Current	IOL		16		mA	0.4V
Output High Current	IOH		16		mA	2.4V
$I_{LV}/O_{D8,S1}$ – Low level bi-directional pin with 8mA source and 1mA sink capability						
Input Low Voltage	VIL			0.5	V	
Input High Voltage	VIH	0.9			V	
Output Low Current	IOL		1		mA	
Output High Current	IOH		8		mA	0.75*Vtt
Input High Leakage	ILIH	-1		1	μA	
Input Low Leakage	ILIL	-1		1	μA	
I_{LV}/OD_{12} – Low level bi-directional pin with 12mA(3.3v)sink capability						
Input Low Voltage	VIL			0.5	V	
Input High Voltage	VIH	0.9			V	
Output Low Current	IOL		12		mA	
Input High Leakage	ILIH	-1		1	μA	
Input Low Leakage	ILIL	-1		1	μA	
I_{LV}/OOD_{12} – Low level bi-directional pin with 12mA source-sink(3.3v)capability						
Input Low Voltage	VIL			0.5	V	
Input High Voltage	VIH	0.9			V	
Output Low Current	IOL		12		mA	
Output High Current	IOH		12		mA	
Input High Leakage	ILIH	-1		1	μA	
Input Low Leakage	ILIL	-1		1	μA	
IN_{LV} – Low level input pin						
Input Low Threshold Voltage				0.5	V	
Input Hign Threshold Voltage	0.9				V	
Input High Leakage				+1	μA	
Input Low Leakage	-1				μA	
IN_{st} – TTL level input pin and schmitt trigger						
Input Low Threshold Voltage				0.8	V	
Input Hign Threshold Voltage	2.0				V	
Hysteresis		0.5			V	
Input High Leakage				+1	μA	
Input Low Leakage	-1				μA	
$IN_{st,5v}$ – TTL level input pin and schmitt trigger, 5 tolerance						
Input Low Threshold Voltage				0.8	V	
Input Hign Threshold Voltage	2.0				V	
Hysteresis		0.5			V	
Input High Leakage				+1	μA	
Input Low Leakage	-1				μA	
IN_t – TTL level input pin						

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Input Low Threshold Voltage				0.8	V	
Input Hign Threshold Voltage	2.0				V	
Input High Leakage				+1	μA	
Input Low Leakage	-1				μA	
$IN_{t,5v}$ – TTL level input pin, 5 tolerance						
Input Low Threshold Voltage				0.8	V	
Input Hign Threshold Voltage	2.0				V	
Input High Leakage				+1	μA	
Input Low Leakage	-1				μA	

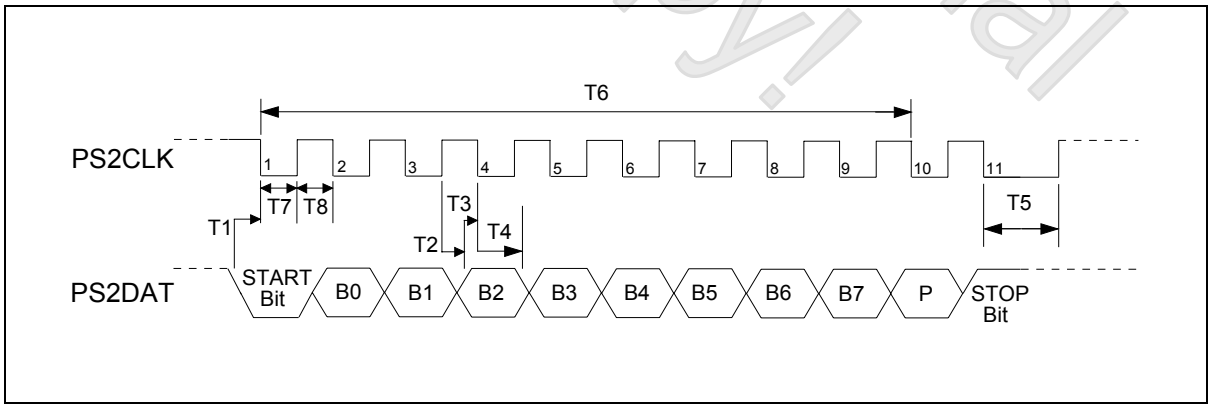
9.4 AC Characteristics

9.4.1 PS/2 Interface

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Duration of start of receive	5	25	μS
T2	Data valid after falling edge of PS2CLK	5	T8 - 5	μS
T3	PS2DAT setup time to falling edge of PS2CLK	1		μS
T4	PS2DAT hold time from falling edge of PS2CLK	5	95	μS
T5	Duration of inhibit PS/2 device	>0		μS
T6	Duration of Data Frame		2	mS
T7	Duration of PS2CLK inactive	30	50	μS
T8	Duration of PS2CLK active	30	50	μS
T9	Duration of PS/2 device inhibit	100	300	μS
T10	Duration of start of transmit		15	mS
T11	Data valid after falling edge of PS2CLK		4	μS
T12	PS2DAT setup time to rising edge of PS2CLK	1		μS
T13	PS2DAT hold time from rising edge of PS2CLK	5	95	μS

PS/2 interface timing table

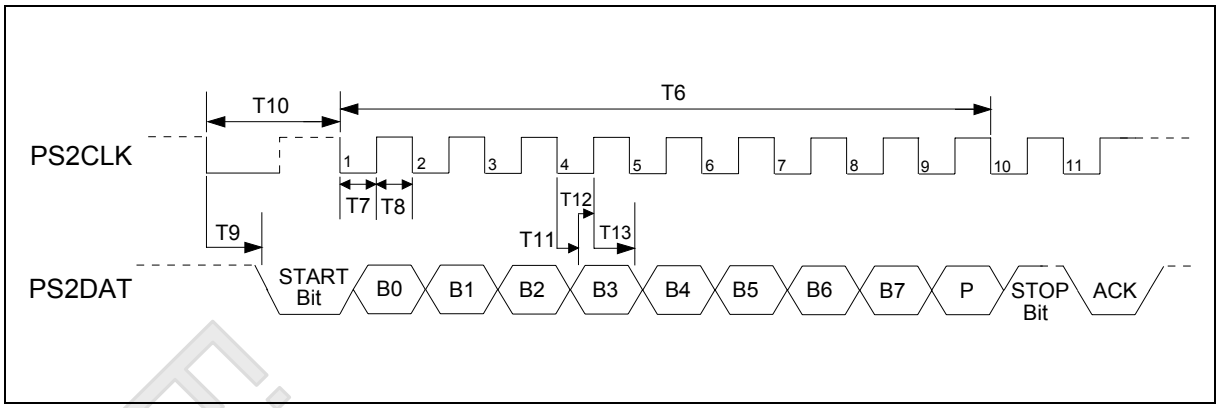
Data Received from PS/2 Device



Host received from PS/2 interface timing diagram

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Data Sent to PS/2 Device



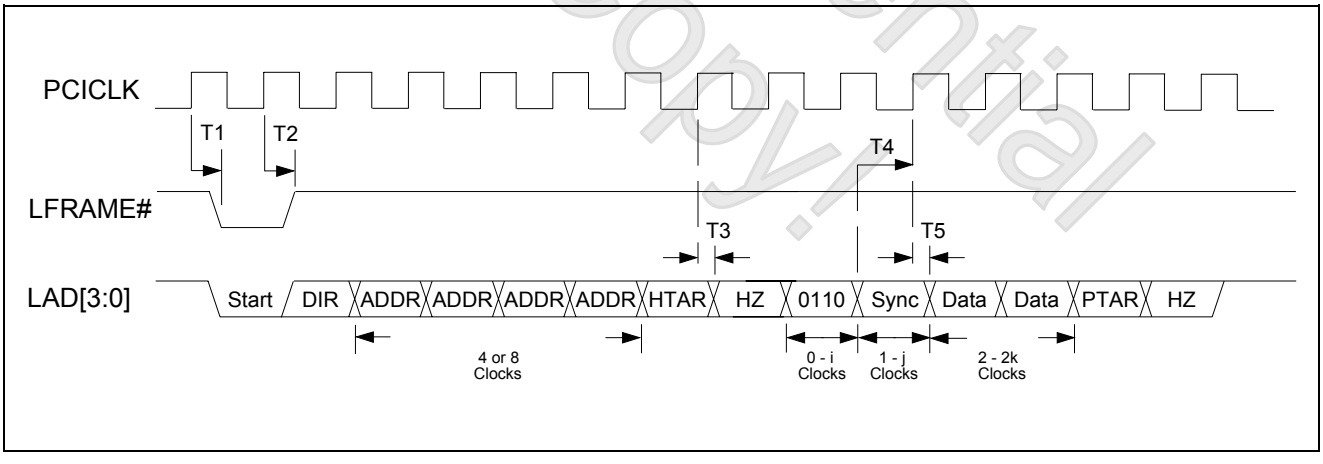
Host Send to PS/2 device timing diagram

9.4.2 LPC Interface

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	LFRAME# drive low after rising edge of PCICLK	2	12	nS
T2	LFRAME# drive high after rising edge of PCICLK	2	12	nS
T3	LDA[3:0] floating after rising edge of PCICLK		28	nS
T4	LDA[3:0] setup time to rising edge of PCICLK	7		nS
T5	LDA[3:0] hold time from rising edge of PCICLK	0		nS
T6	Period of PCICLK	27	33	nS
T7	Duration of PCICLK low	12		nS
T8	Duration of PCICLK high	12		nS

LPC interface timing table

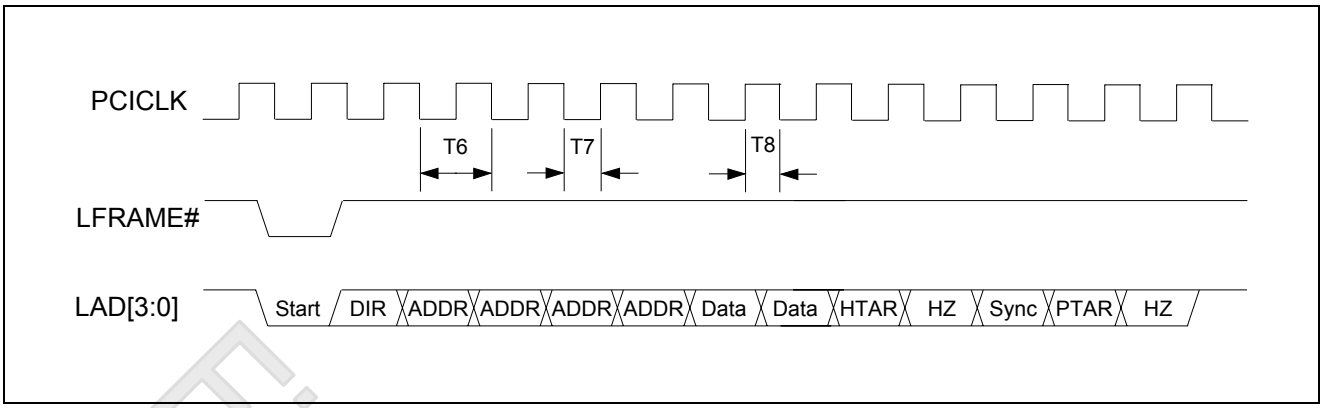
Typical Timing for Host Read



Host read timing diagram

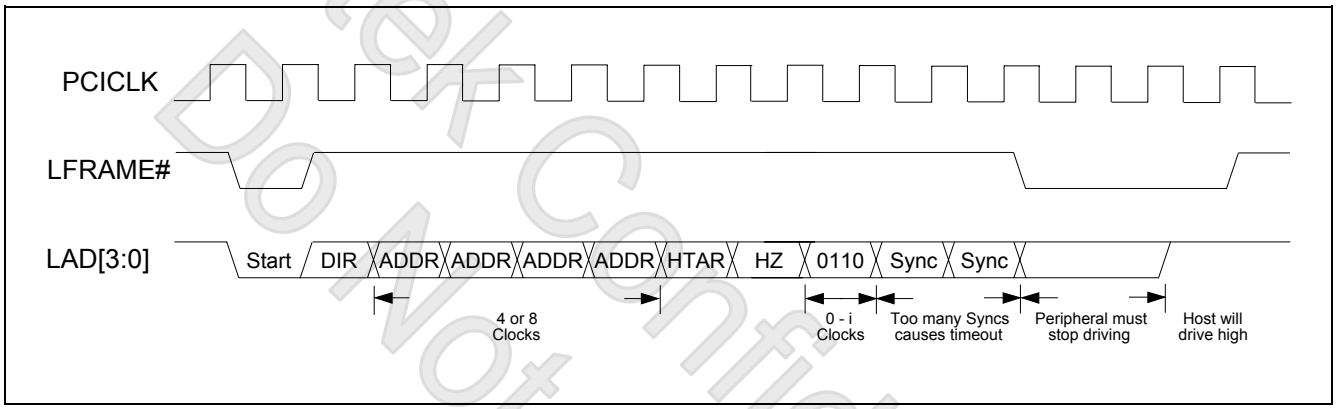
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Typical Timing for Host Write



Host write timing diagram

Timing for Aboart Mechanism



Host abort timing diagram

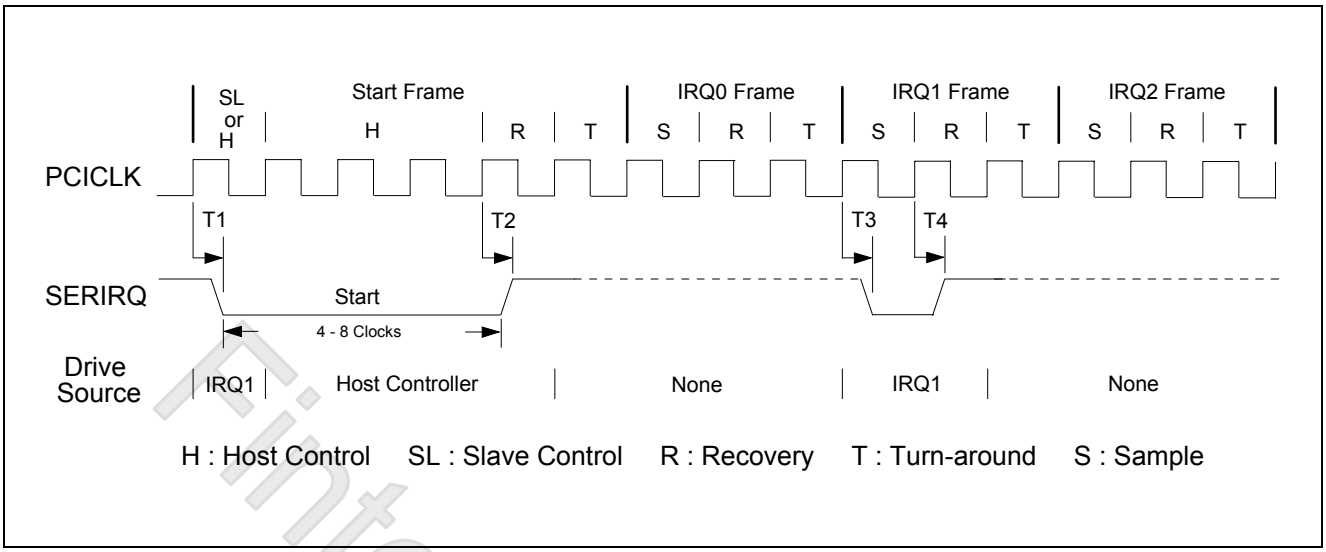
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9.4.3 Serialized IRQ Interface

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Host drive SERIRQ low after rising edge of PCICLK	2	12	nS
T2	Host drive SERIRQ high after rising edge of PCICLK	2	12	nS
T3	Slave drive SERIRQ low after rising edge of PCICLK	2	12	nS
T4	Slave drive SERIRQ high after rising edge of PCICLK	2	12	nS
T5	Period of PCICLK	27	33	nS
T6	Duration of PCICLK low	12		nS
T7	Duration of PCICLK high	12		nS

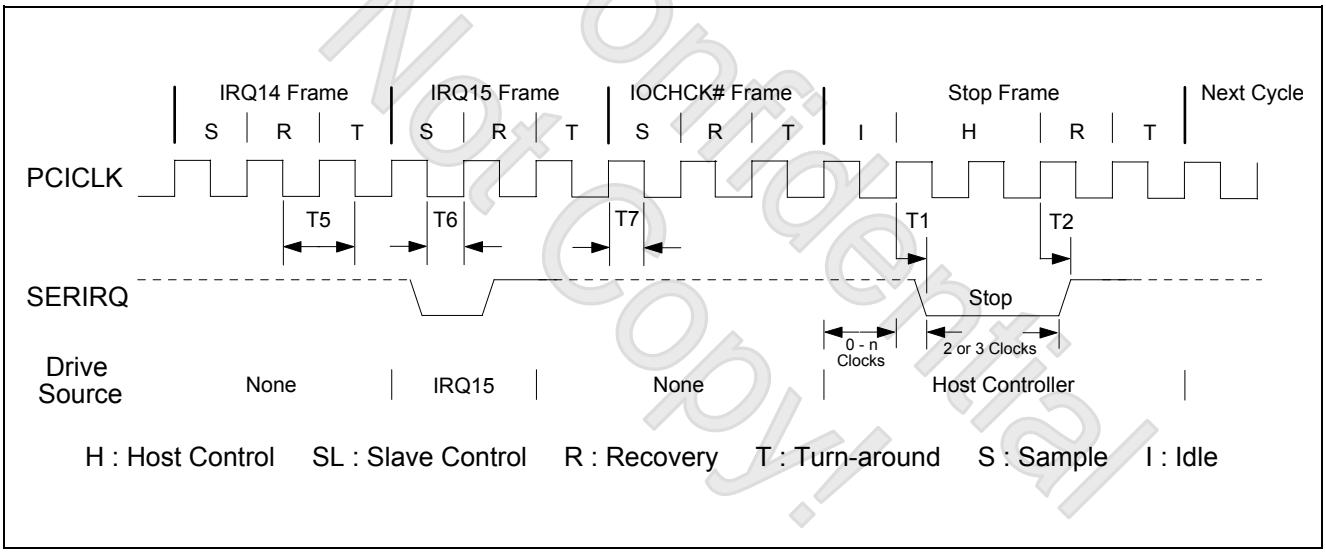
SIRQ interface timing table

Start Frame Timing



SIRQ start frame timing diagram

Stop Frame Timing

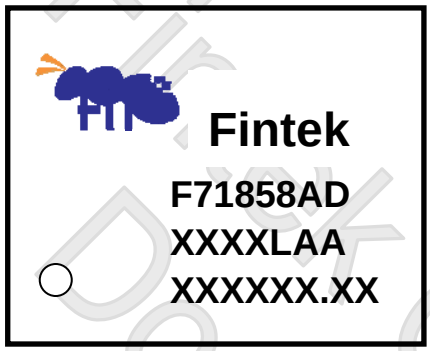


SIRQ stop frame timing diagram

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10.Ordering Information

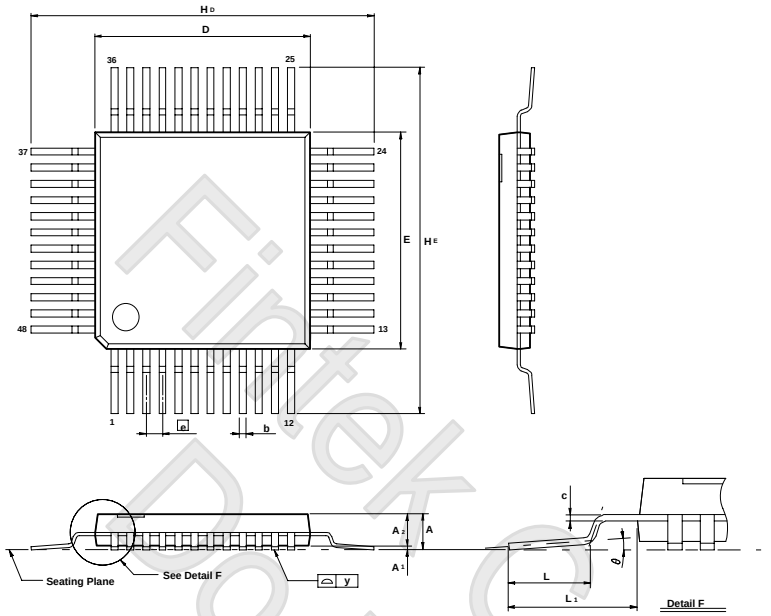
Part Number	Package Type	Production Flow
F71858AD	48-LQFP (Green Package)	Commercial, 0°C to +70°C



Version Identification:
EX: For LAA version

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11.Package Dimensions (48LQFP)



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A				---	---	1.60
A_1				0.05	---	0.15
A_2				1.35	1.40	1.45
b				0.17	0.20	0.27
c				0.09	---	0.20
D					7.00	
E					7.00	
e					0.50	
H_D					9.00	
H_E					9.00	
L				0.45	0.60	0.75
L_1					1.00	
y				---	0.08	---
θ				0	3.5°	7

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

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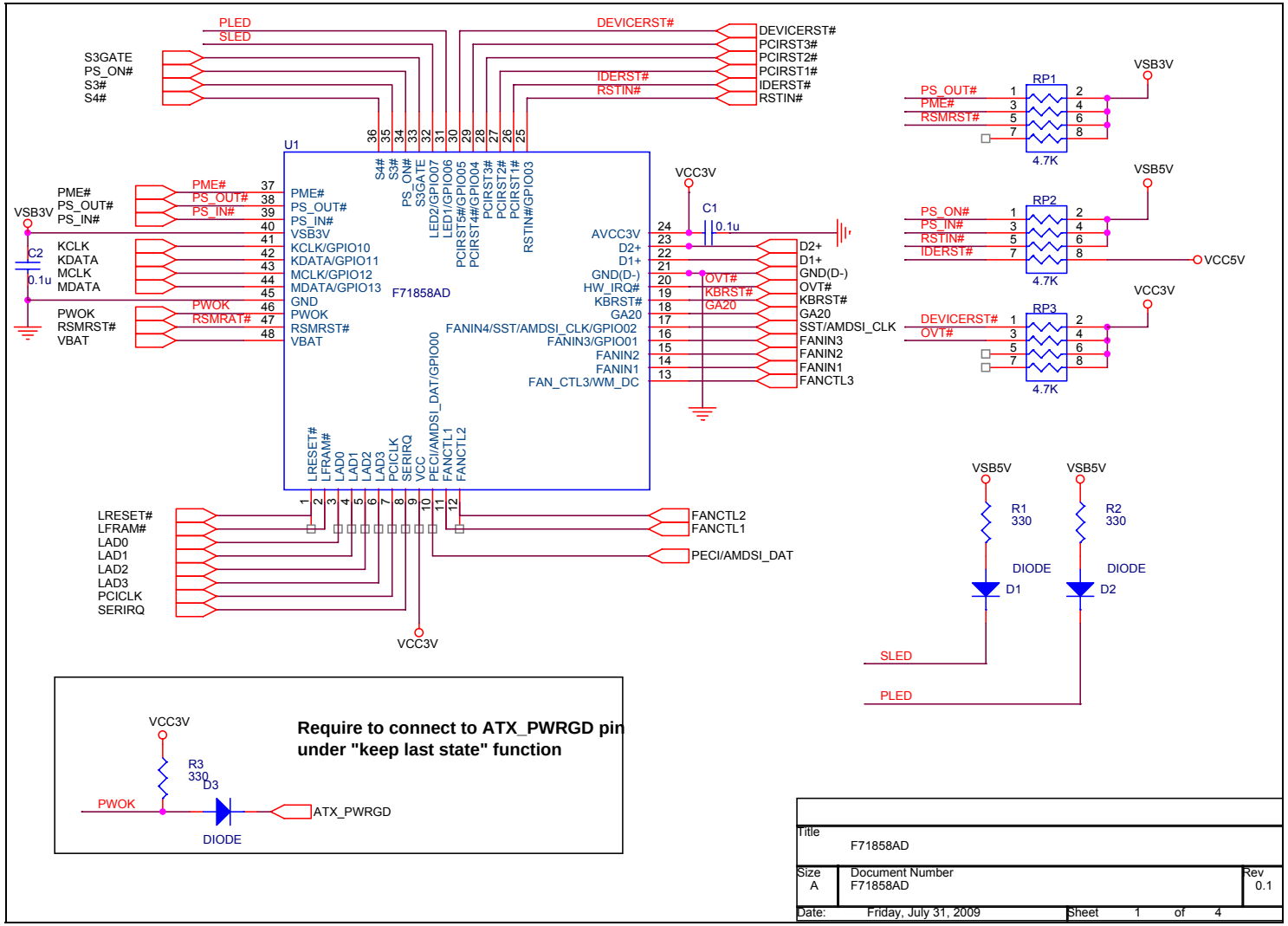
Feature Integration Technology Inc.

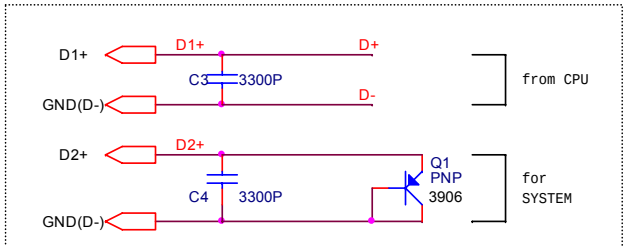
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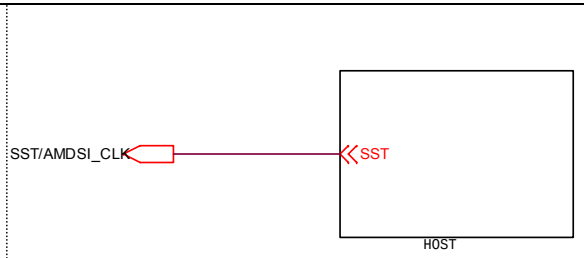
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12.Application Circuit

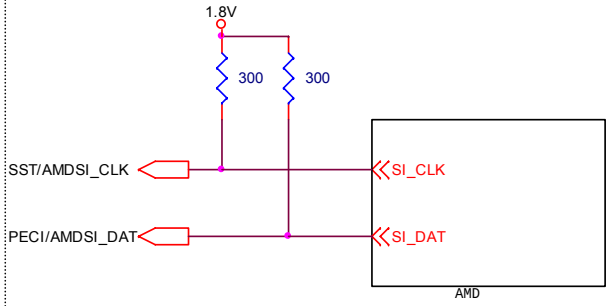




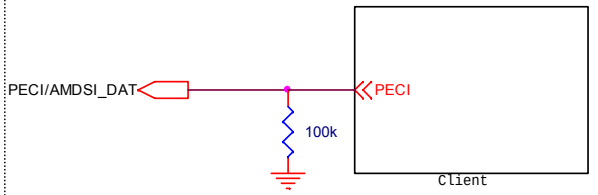
DIODE SENSING CIRCUIT



SST

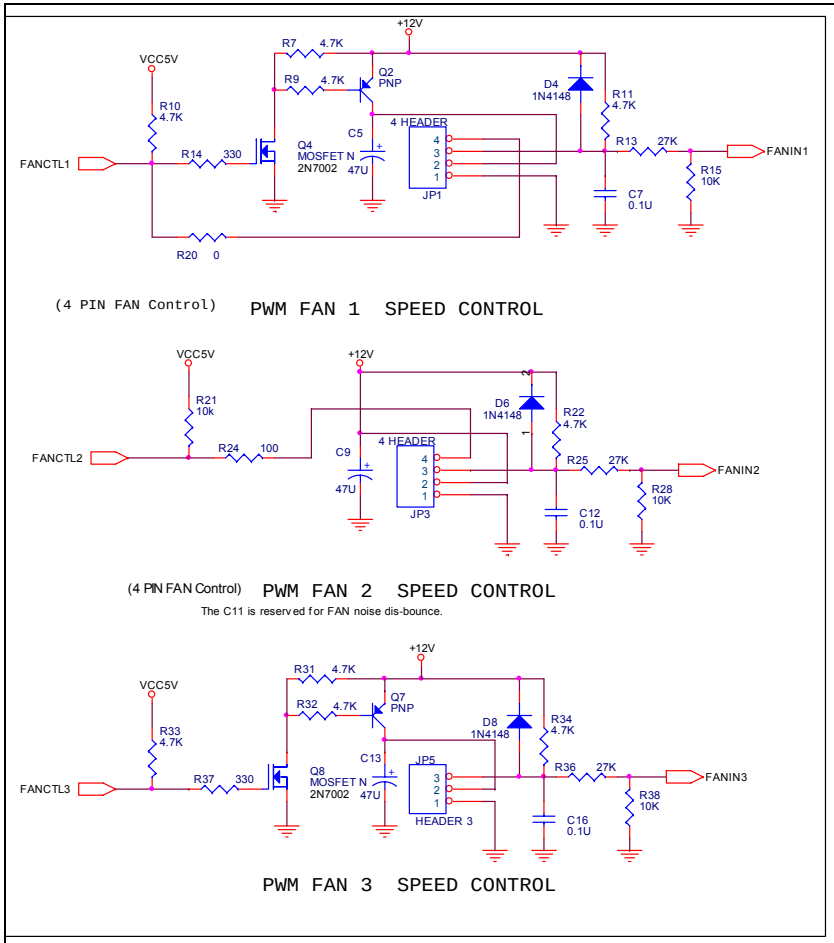


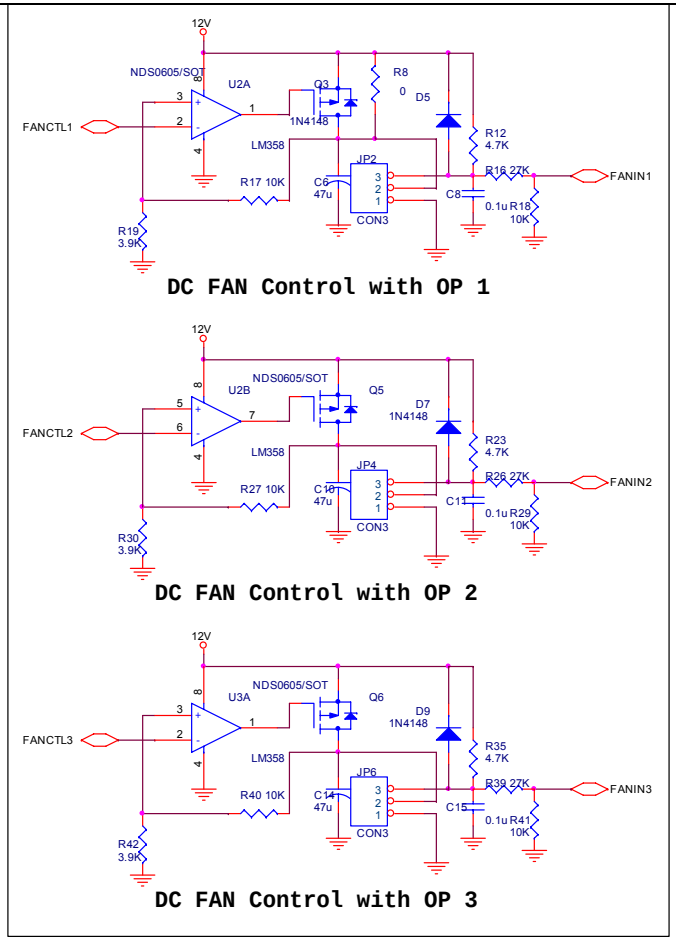
AMDSI



PECI

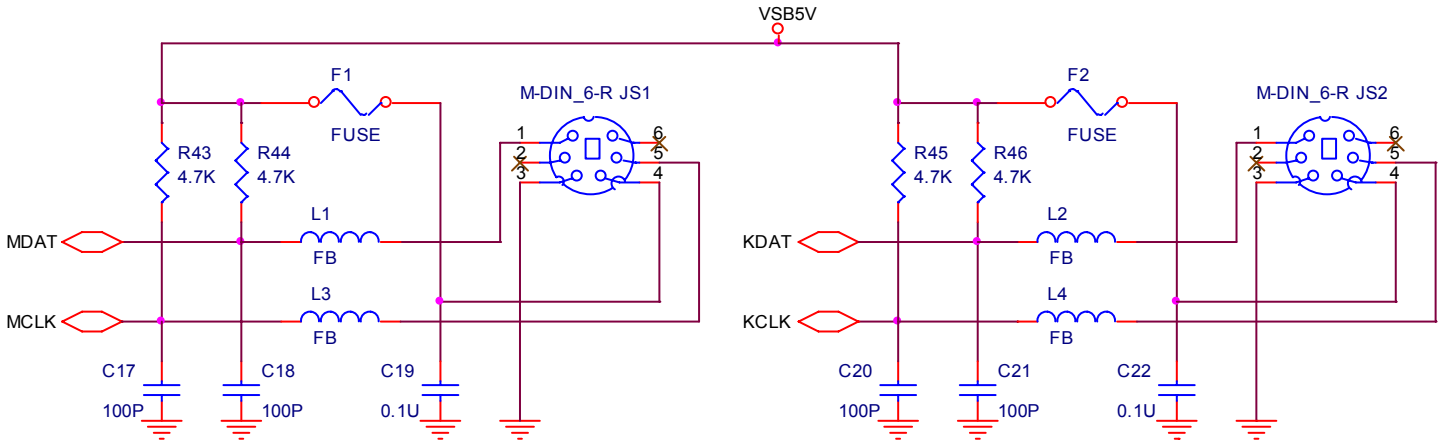
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Date: Friday, July 31, 2009	Sheet 2 of 4	





FAN CONTROL FOR PWM OR DC

Title	FAN circuit	
Size B	Document Number F71858AD	Rev 0.1
Date: Friday, July 31, 2009	Sheet 3 of 4	



PS2 MOUSE INTERFACE **PS2 KEYBOARD INTERFACE**

Title	KBC		
Size A	Document Number F71858AD		Rev 0.1
Date: Friday, July 31, 2009		Sheet 4 of 4	