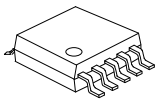
3A DDR BUS TERMINATION REGULATOR



MSOP-10

■ DESCRIPTION

The **UR5517** is a linear regulator which provides up to 3 Amp bi-directional sourcing and sinking capability for DDR1/2/3 SDRAM bus terminator applications. It only requires 20uF of ceramic output capacitance by a integrated operational amplifier which provides fast load transient response.

The **UR5517** also includes two control pins, S3 & S5. If S3 were set in low level, VTT will be turned off and left Hi-Z(sleep-state mode).If setting S5 were set in low level, both VTT and VTTREF will be turned off and discharged to ground(soft-off mode).

■ FEATURES

* Input Voltage Range::3~5.5V
* VLDOIN Voltage Range:1.2V~3.6V
* DDR1/2/3 Termination Voltage Applications
* Sourcing and Sinking Current up to 3A
* ±20mV Accuracy for VTT and VTTREF
* 10mA Buffered Reference(VTTREF)
* Supports High-Z in S3(STR) and Soft-off in S5(Shutdown)
* Integrated Divider Tracks 1/2 VDDQSNS for Both VTT&VTTREF
* Built-In Soft-Start
* Current Limiting Protection
* Thermal Shutdown Protection

■ ORDERING INFORMATION

Ordering Number	Package	Packing
UR5517G-SM2-R	MSOP-10	Tape Reel

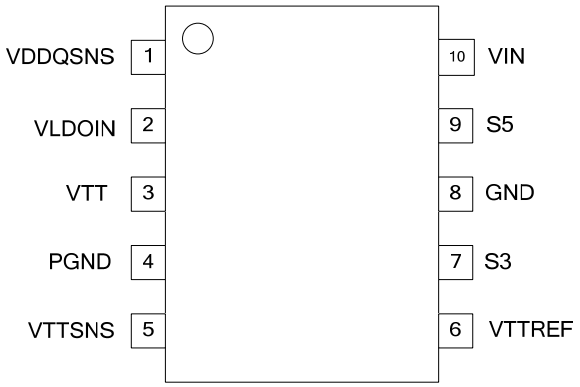
UR5517G-SM2 -R

(1)Packing Type
(2)Package Type
(3)Halogen Free

(1) R: Tape Reel
(2) SM2: MSOP-10
(3) G: Halogen Free

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■ PIN CONFIGURATIONS

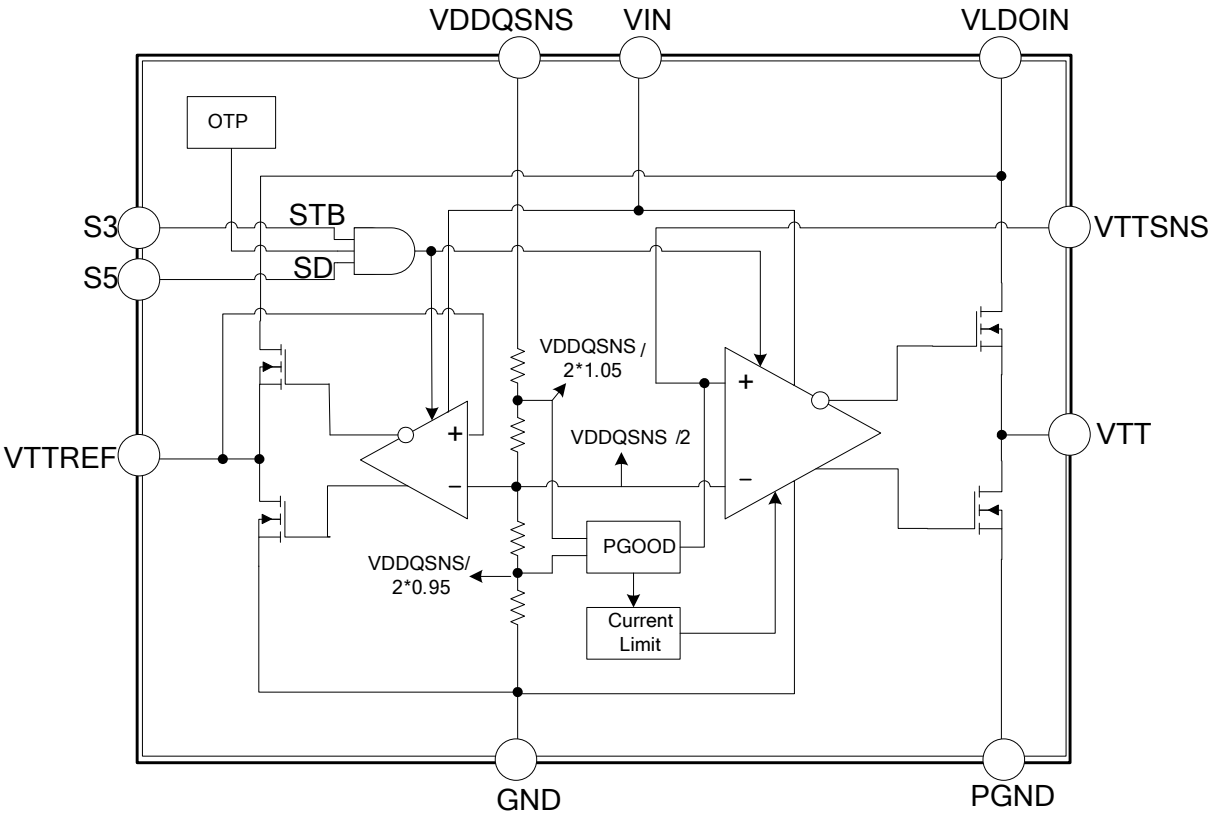


■ PIN DESCRIPTION(Note)

PIN NAME	PIN TYPE	PIN DESCRIPTION
VDDQSNS	I	VDDQ sense input
VLDOIN	I	Power supply for the VTT & VTTREF output stage
VTT	O	Output voltage for connection to termination resistors, equal to VDDQSNS/2
PGND	O	Power ground output for the VTT output
VTTSNS	I	Voltage sense input for the VTT. Connect to plus terminal of the output capacitor
VTTREF	O	Buffered output that is a reference output, equal to VDDQSNS/2
S3	I	Active low suspend to RAM mode control pin, VTT is turned off and left Hi-Z
GND	I	Ground
S5	I	Active low shutdown control pin, both VTT&VTTREF are turned off and discharged to ground
VIN	I	Analog input pin

Note：Recommend connecting the Thermal Pad to the GND for the excellent power dissipation.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage(VIN,VLDOIN,VDDQSNS,S3,S5)		-0.3~6	V
Power Ground Output for the VTT Output	P_{GND}	-0.3~0.3	V
Output Voltage(VTT,VTTREF)	VTT,V_{TTREF}	-0.3~VLDOIN+0.3	V
Junction Temperature	T_J	160	℃
Storage Temperature	T_{STG}	-55 ~ +160	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (Note1, 2)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	3		5.5	V
STR and Shutdown Voltage	S3,S5	-0.1		5.5	V
VDDQ Sense Input	V_{DDQSNS}	1.3		3.6	V
Power Supply for the VTT and VTTREF Output Stage	V_{LDOIN}	1.2		3.6	V
Power Ground Output for the VTT Output	P_{GND}	-0.1		0.1	V
Operating Temperature	T_A	-40		85	℃

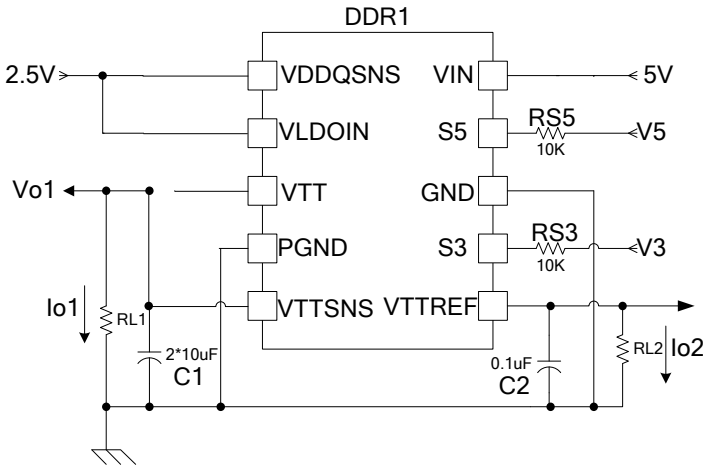
Note: 1. All voltage values are with respect to the network ground terminal unless otherwise noted.
2. Please always keep VLDOIN,VTTSNS,VDDQSNS,S3,S5 lower than VIN on operation.

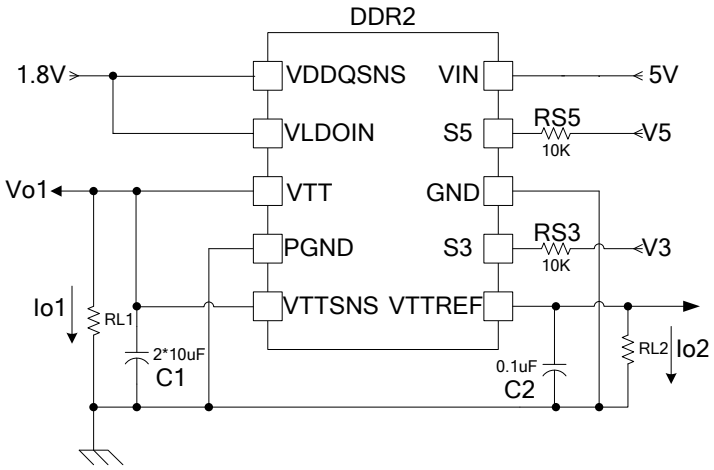
■ ELECTRICAL CHARACTERISTICS

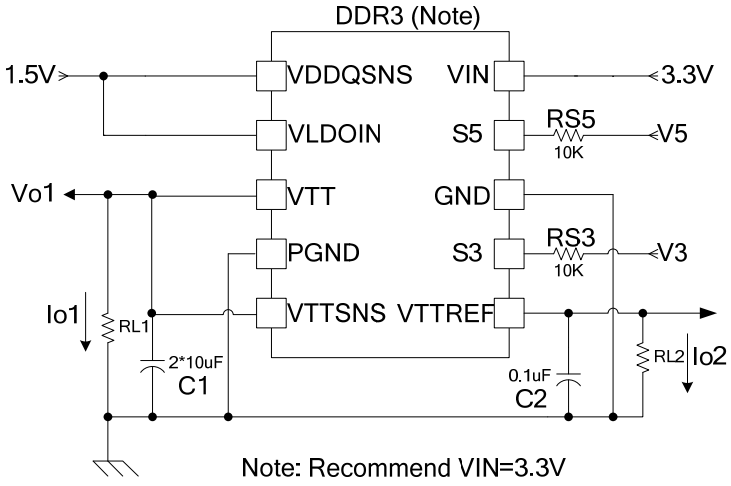
(V_{IN}=5V,VLDOIN=VDDQSNS=2.5V, T_A=25℃.Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current of VIN	I_{VIN}	S5=Hi,S3=Hi, no load(Normal)	0.5	0.8	2	mA
	I_{VINSTB}	S5=Hi,S3=Lo, no load(Standby)		110	200	uA
	I_{VINSDN}	S5=Lo,S3=Lo, no load(Shutdown)			1	uA
Current of VLDOIN	I_{VLDOIN}	S5=Hi,S3=Hi, no load(Normal)		0.03	2	mA
	$I_{VLDOINSTB}$	S5=Hi,S3=Lo, no load(Standby)		0.1	10	uA
	$I_{VLDOINSDN}$	S5=Lo,S3=Lo, no load(Shutdown)		0.1	1	uA
Input Impedance of VDDQSNS	$Z_{VDDQSNS}$	S5=Hi,S3=Hi		200		kΩ
Input Current of VTTSNS	I_{VTTSNS}	S5=Hi,S3=Hi		0.3	1	uA
Output Voltage of VTT	VTT	DDR1(VLDOIN=VDDQSNS=2.5V)		1.25		V
		DDR2(VLDOIN=VDDQSNS=1.8V)		0.9		
		DDR3(VLDOIN=VDDQSNS=1.5V)		0.75		
Load Regulation of VTT (VTTREF-VTT)	VosVTT	I_{VTT} =0	-20		20	mV
		$\lvert I_{VTT} \rvert$ <1.5A	-30		30	
		$\lvert I_{VTT} \rvert$ <3A	-40		40	
Source Current Limit of VTT	$I_{VTTOCLSRC}$	VTT=VDDQSNS/2*0.95,PGOOD=HI	3	4		A
		VTT=0	1.5	2		
Sink Current Limit of VTT	$I_{VTTOCLSNK}$	VTT=VDDQSNS/2*1.05,PGOOD=HI	3	4		A
		VTT=VDDQSNS	1.5	2		
Leakage Current of VTT	I_{VTTLK}	S5=Hi,S3=Lo		0.01		uA
Discharge Current of VTT	I_{VTTDIS}	S5=Lo, VDDQSNS=0V,VTT=0.5V	10	20		mA
Output Voltage of VTTREF	V_{TTREF}	DDR1(VLDOIN=VDDQSNS=2.5V)		1.25		V
		DDR2(VLDOIN=VDDQSNS=1.8V)		0.9		
		DDR3(VLDOIN=VDDQSNS=1.5V)		0.75		
Load Regulation of VTTREF	ΔV_{TTREF}	$\lvert I_{VTTREF} \rvert$ <10mA	-20		20	mV
High Level Input Voltage	V_{IH}	S3 & S5 pin	1.6			V
Low Level Input Voltage	V_{IL}	S3 & S5 pin			1	
Logic Input Leakage Current	I_{ILEAK}	S3 & S5 pin	-1		1	uA
Thermal Shutdown Temperature	T_{SD}	VIN=3V~5.5V		160		℃
Thermal Shutdown Hysteresis	ΔT_{SD}	VIN=3V~5.5V		20		

■ TYPICAL APPLICATIONS CIRCUIT







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